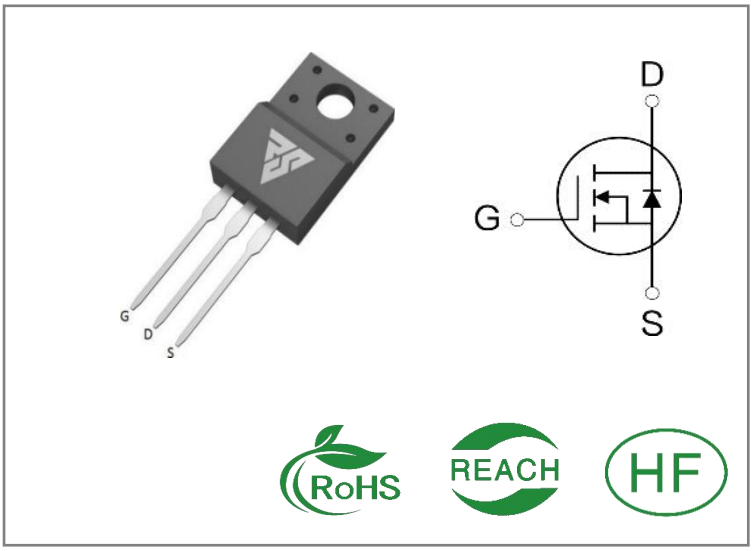
ID	R_{DS}(ON)(Typ)	VDSS
13A	0.39Ω	500V



Applications:
- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

Features:
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS13N50F	T0-220F	RS13N50F	Tube	50 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS13N50F	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current TC=25℃	13	A
IDM	Pulsed Drain Current (Note*1)	52	
PD	Power Dissipation	49	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L = 10mH, VDD = 50V, RG = 25 Ω	352	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature
Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS13N50F	Units	Test Conditions
RθJC	Junction-to-Case	2.55	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	500	--	--	V	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=500V,VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V ,VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	0.39	0.46	Ω	VGS=10V,ID=6.5A
VGS(TH)	Gate Threshold Voltage	3	--	4	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	43.2	--	nS	VDS=250V ID=13A RG=25Ω
trise	Rise Time	--	24.8	--		
td(OFF)	Turn- OFF Delay Time	--	131.8	--		
tfall	Fall Time	--	42.6	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1569	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	171	--		
Crss	Reverse Transfer Capacitance	--	5	--		
Qg	Total Gate Charge	--	30.9	--	nC	VDS=400V ID=13A VGS=10V
Qgs	Gate- to- Source Charge	--	7.8	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	10.6	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	13	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	52	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=6.5A,VGS=0V
trr	Reverse Recovery Time	--	307	--	nS	VGS=0V IS=13A,di/dt=100 A/μs
Qrr	Reverse Recovery Charge	--	3.5	--	μC	

Notes:

* 1. Repetitive rating,pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature Curve

Figure 1. Output Characteristics (T_J = 25ºC)

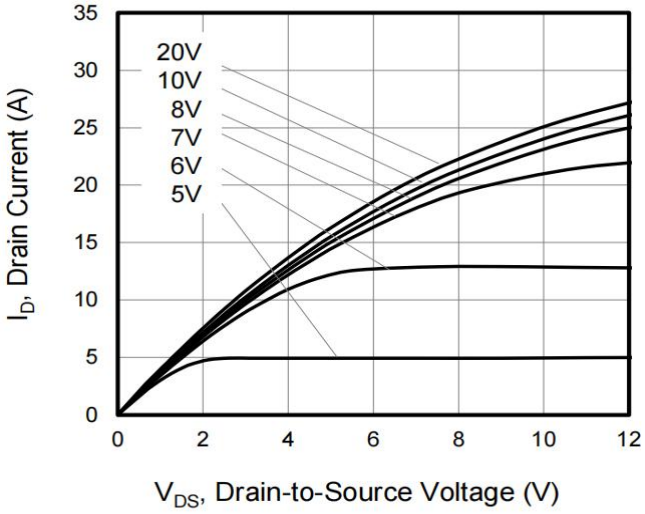


Figure 2. Body Diode Forward Voltage

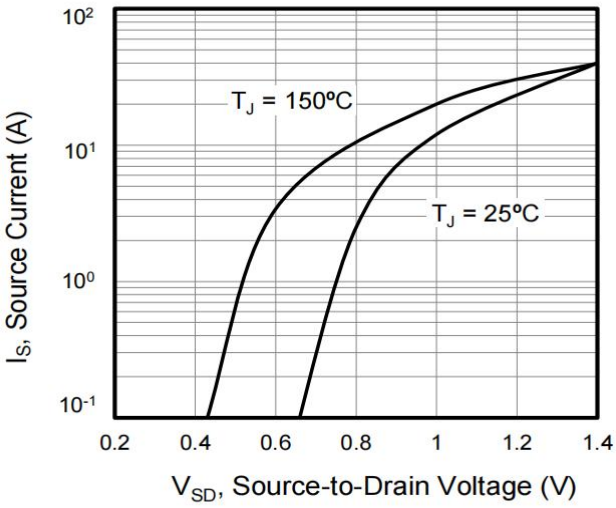


Figure 3. Drain Current vs. Temperature

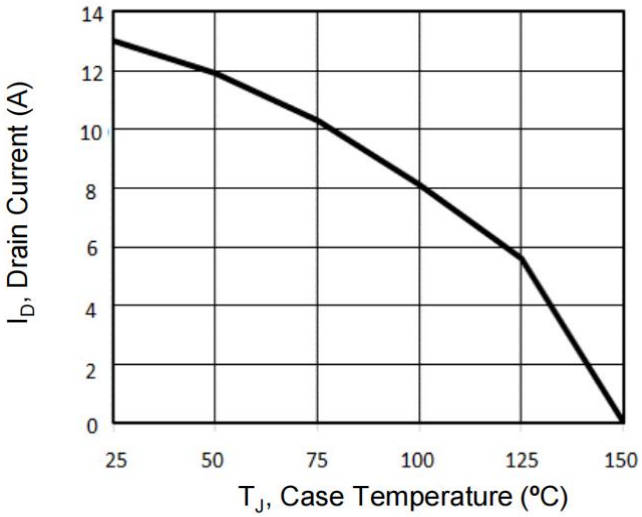


Figure 4. BV_{DSS} Variation vs. Temperature

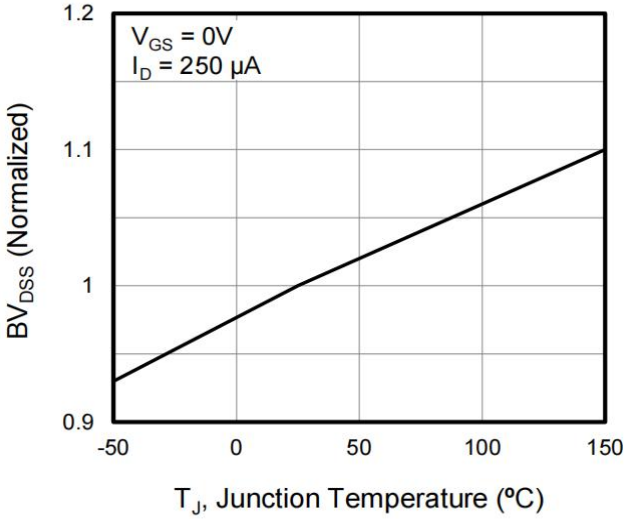


Figure 5. Transfer Characteristics

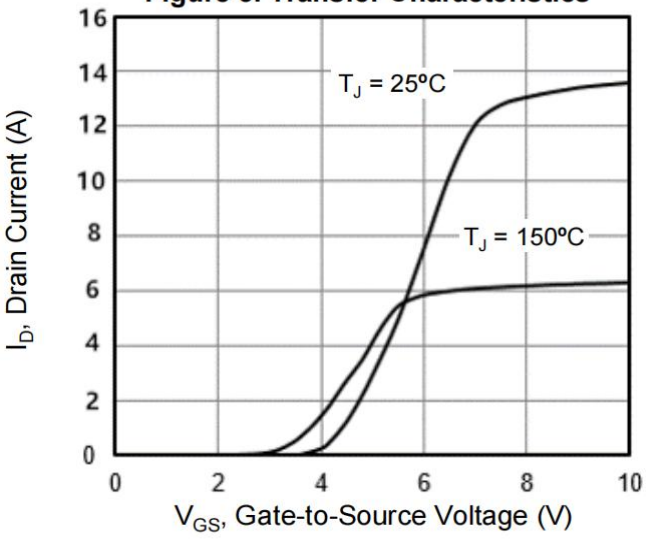


Figure 6. On-Resistance vs. Temperature

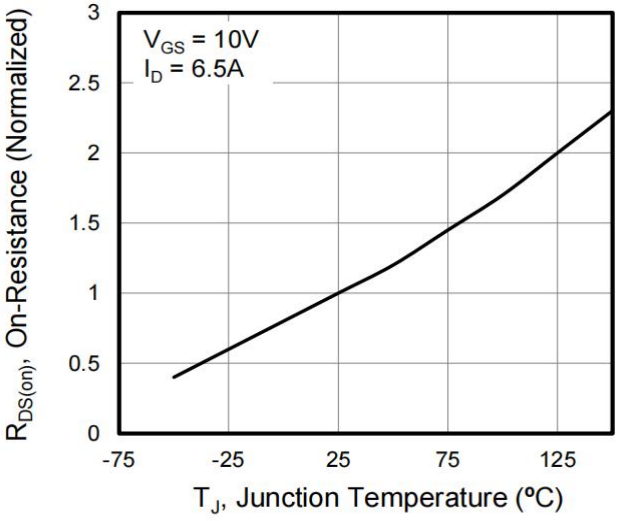


Figure 7. Capacitance

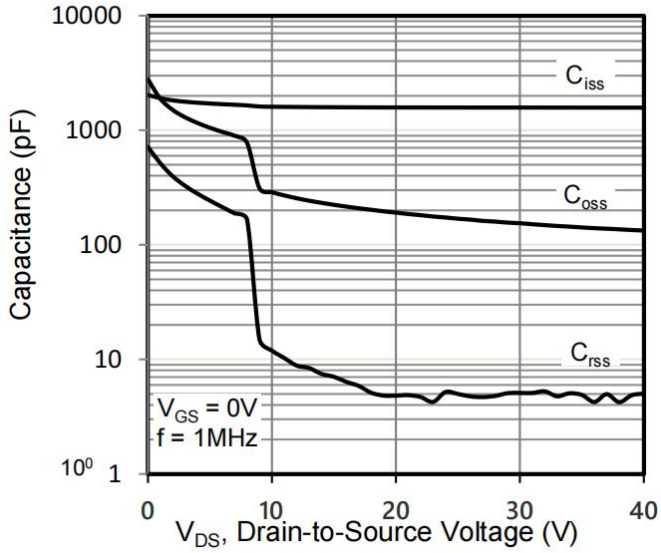


Figure 8. Gate Charge

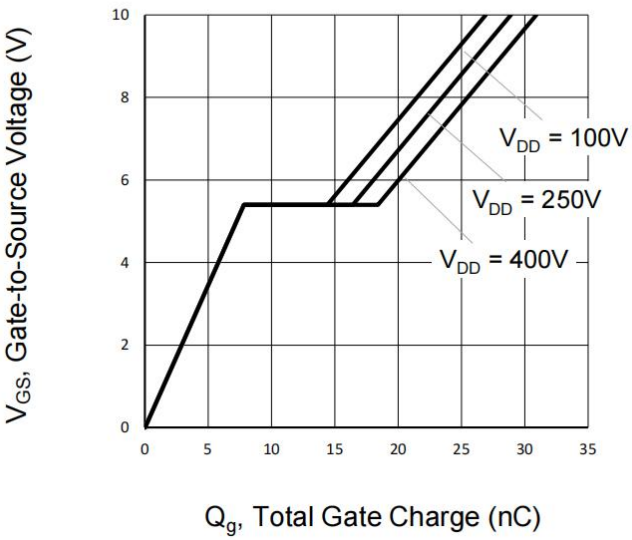
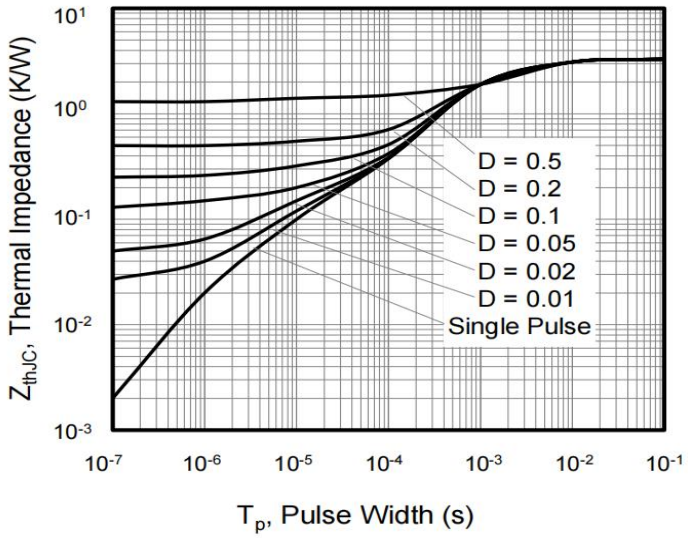


Figure 9. Transient Thermal Impedance



Test Circuits and Waveforms

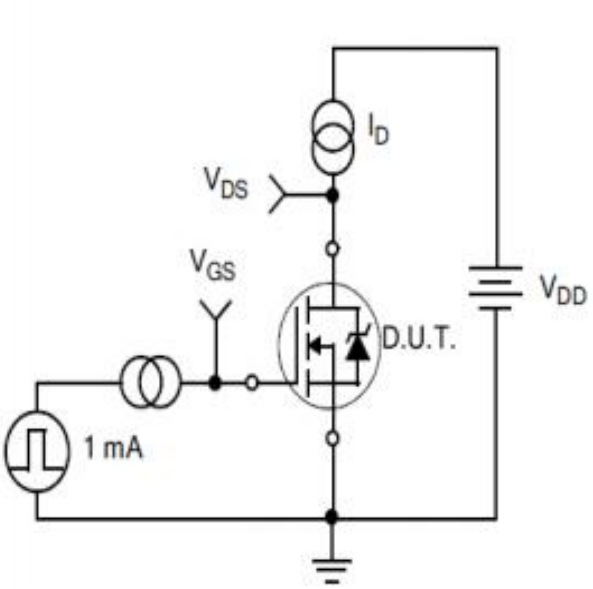


Figure10.
Gate Charge Test Circuit

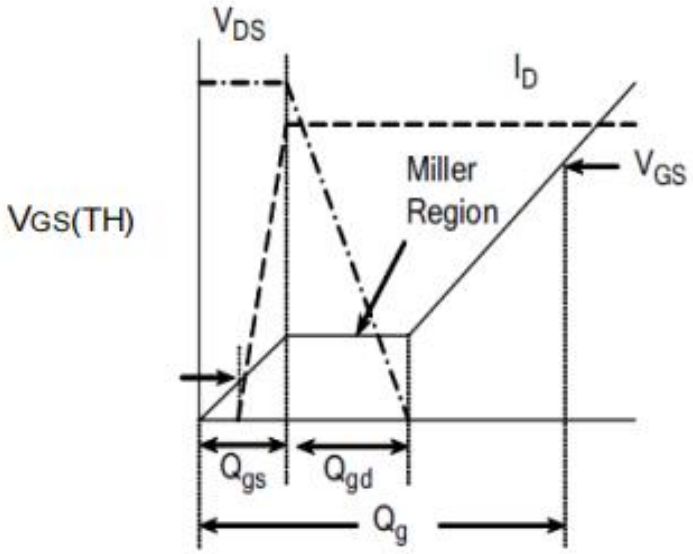


Figure11.
Gate Charge Waveform

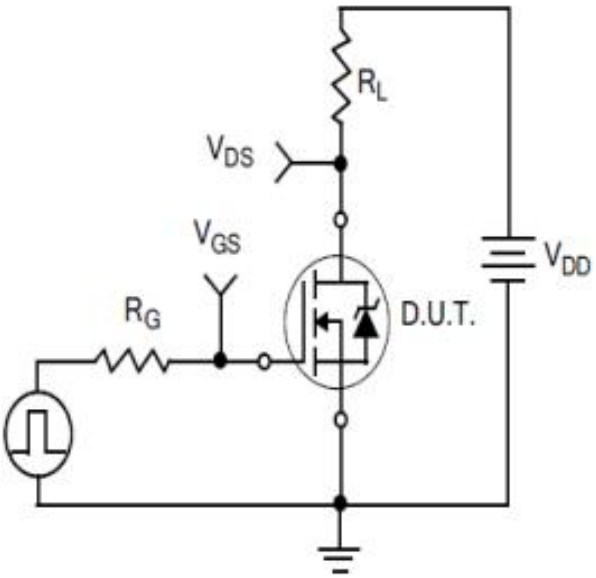


Figure12.
Resistive Switching Test Circuit

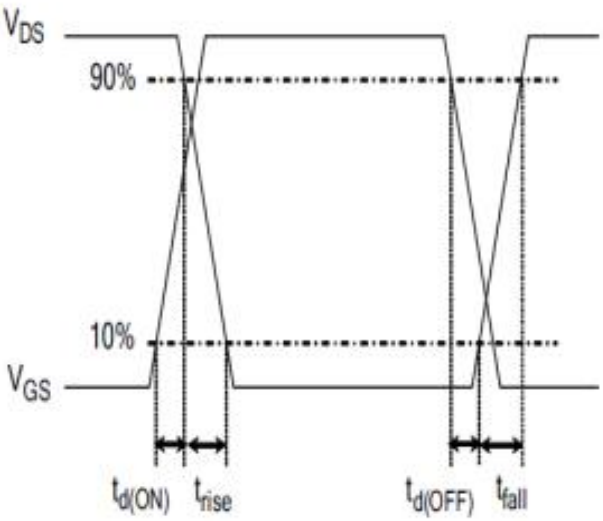


Figure13.
Resistive Switching Waveforms

Test Circuits and Waveforms

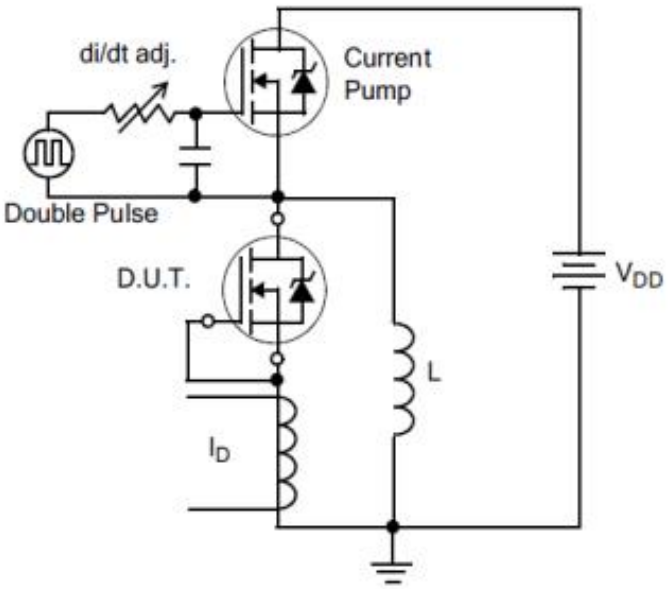


Figure14.Diode Reverse Recovery Test Circuit

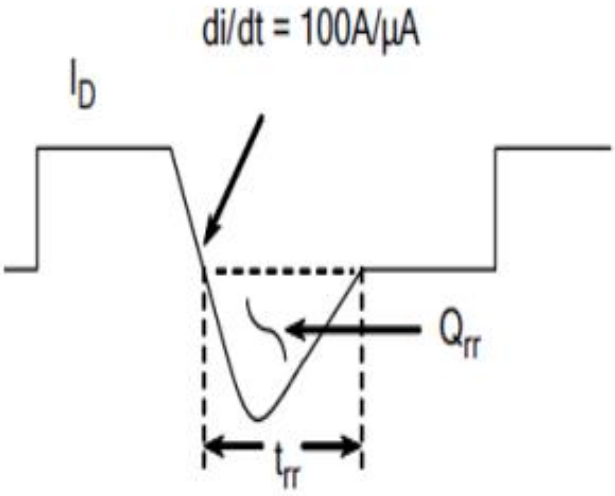


Figure15.Diode Reverse Recovery Waveform

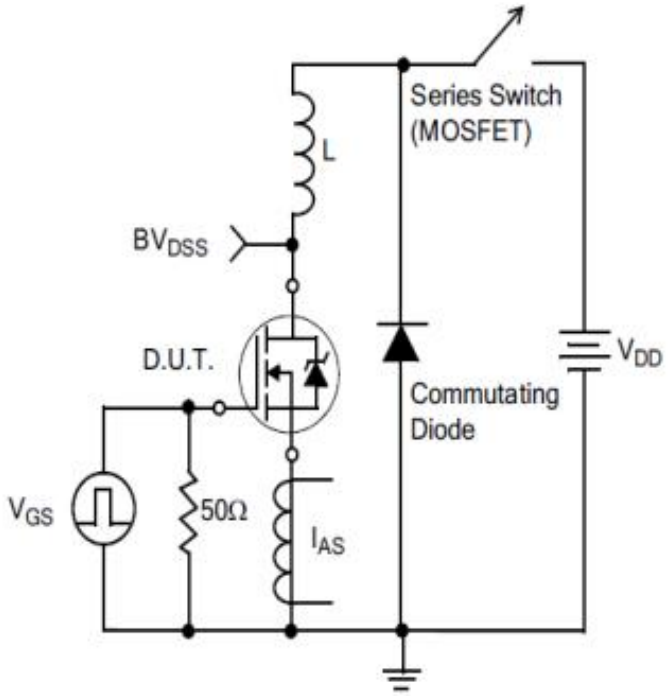
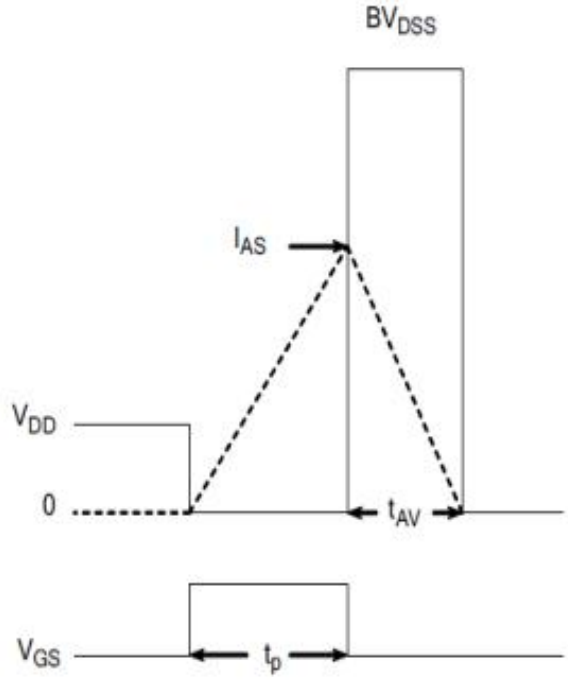


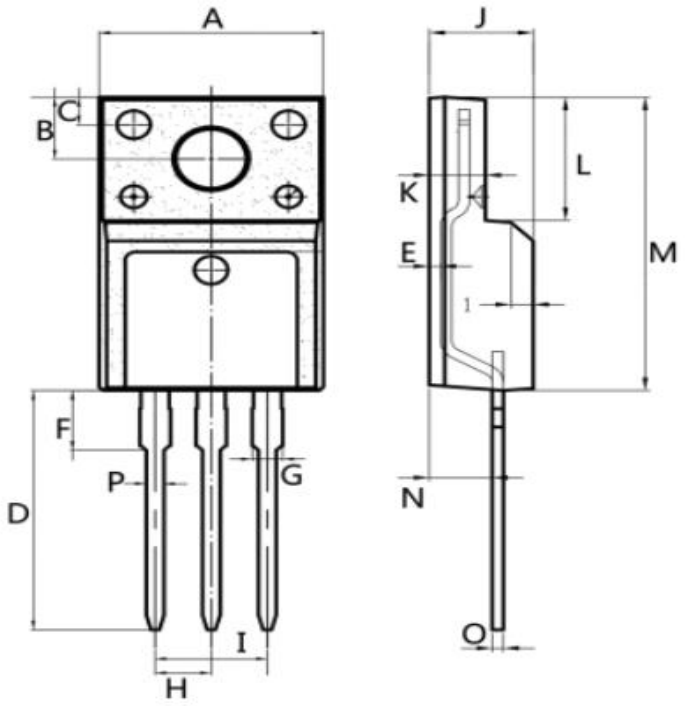
Figure16.Unclamped Inductive Switching Test Circuit



$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure17.Unclamped Inductive Switching Waveforms

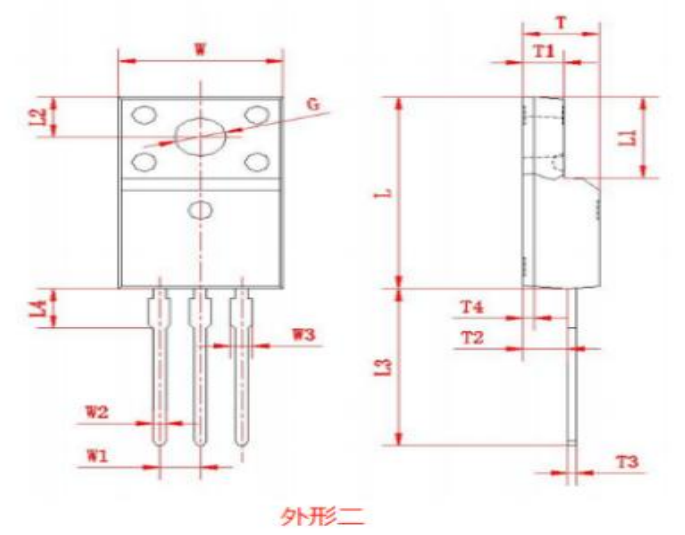
Package outline drawing(TO-220F Unit: mm)



外形一

Dim.	Min.	Max.
A	9.95	10.36
A1	4.5	5.0
B	2.95	3.25
C	1.25	1.45
D	12.60	13.60
E	0.40	0.60
F	2.8	3.5
G	1.30	1.45
H	(2.54)	
I	(5.08)	
J	4.60	4.75
K	2.45	2.65
L	6.5	6.8
M	15.4	16.0
N	2.25	3.05
O	0.45	0.55
P	0.70	0.90

All Dimensions in millimeter



外形二

Dim.	Min.	Max.
W	9.95	10.36
W1	(2.54)	
W2	0.70	0.90
W3	1.25	1.47
L	15.67	16.07
L1	6.48	6.88
L2	3.2	3.4
L3	12.6	13.6
L4	(3.23)	
T	4.50	4.90
T1	2.34	2.74
T2	2.25	2.95
T3	0.45	0.60
T4	(0.70)	
G	3.08	3.28

All Dimensions in millimeter

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