



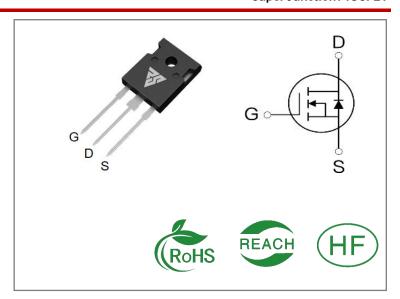
ID	R <sub>DS</sub> (ON)(Typ)	VDSS
100A	20mΩ	600V

### **Applications:**

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- AC-DC Switching Power Supply

### **Features:**

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability
- Fast Recovery Time



**Ordering Information** 

Part Number	Package	Marking	Packing	Qty.
RSF60R026W	T0-247-3	RSF60R026W	Tube	30 PCS

## Absolute Maximun Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RSF60R026W	Units
VDSS	Drain-to-Source Voltage	600	V
ID	Continuous Drain Current TC=25℃	100	
ID	Continuous Drain Current TC=100°C	63.3	A
IDM	Pulsed Drain Current (Note*1)	300	
PD	Power Dissipation	694	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy	3000	mJ
dv/dt	MOSFET dv/ dt ruggedness VDS = 0400V	50	V/ns
dv/dt	Reverse diode dv/dt VDS = 0400V, Tj = $25^{\circ}$ C, ISD $\leq$ ID	15	V/ns
TI TDI/C	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	$\mathbb{C}$
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

<sup>\*</sup> Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.



## **Thermal Resistance**

Symbol	Parameter	RSF60R026W	Units	Test Conditions
RθJC	Junction-to-Case	0.18	°C/W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 °C
RθJA	Junction-to- Ambient	33		1 cubic foot chamber,free air.

## **OFF Characteristics** TJ= 25 °C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	600			V	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current			10	μΑ	VDS=600V,VGS=0 V
1000	Gate- to- Source Forward Leakage			100		VGS=30V ,VDS=0V
IGSS	Gate- to- Source Reverse Leakage			-100	nA	VGS=-30V ,VDS=0 V

## ON Characteristics TJ=25 °C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On- Resistance(Note*2)		20	26	mΩ	VGS=10V,ID=40A
VGS(TH)	Gate Threshold Voltage	3.2	4	4.5	V	VGS=VDS,ID=1mA

## Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time		56			
trise	Rise Time		57			VDS=400V
td(OFF)	Turn- OFF Delay Time		117		nS	ID=40A RG=2Ω
tfall	Fall Time		5.8			



**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		9317			VGS=0V
Coss	Output Capacitance		372		pF	VDS=50V
Crss	Reverse Transfer Capacitance		7.6			f=1.0MHz
Qg	Total Gate Charge		192			VDS=480V
Qgs	Gate- to- Source Charge		60		nC	ID=50A
Qgd	Gate-to-Drain(" Miller") Charge		77			VGS=10V

### **Source-Drain Diode Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current			100	Α	Integral pn- diode
ISM	Maximum Pulsed Current			300	Α	in MOSFET
VSD	Diode Forward Voltage			1.2	V	IS=50A,VGS=0V
trr	Reverse Recovery Time		209		nS	VR=300V
Qrr	Reverse Recovery Charge		2.2		μC	IS=50A,di/dt=100A /μs

#### Notes

<sup>\* 1.</sup> Repetitive rating, pulse width limited by maximum junction temperature.

<sup>\* 2.</sup> Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 1%



## **Typical Feature Curve**

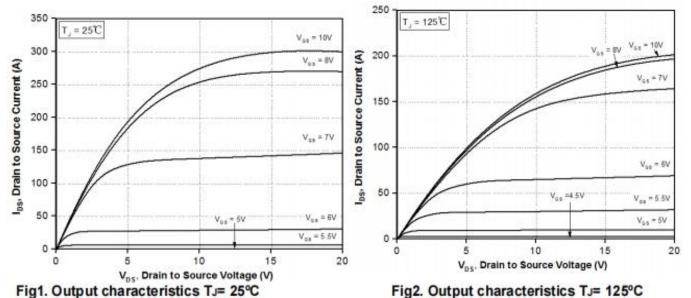
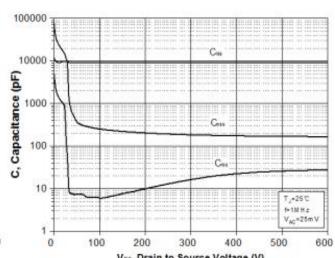


Fig1. Output characteristics T<sub>J</sub>= 25℃



V<sub>DE</sub> = 120V.J<sub>D</sub> = 50A V<sub>DS</sub> = 300V,J<sub>D</sub> = 50A V<sub>DB</sub> = 480V,J<sub>D</sub> = 50A V<sub>GS</sub>, Gate to Source Voltage(V) 2 0 40 120 160 200 Q<sub>G</sub>, Total Gate Charge (nC)

Fig3. Gate charge characteristics

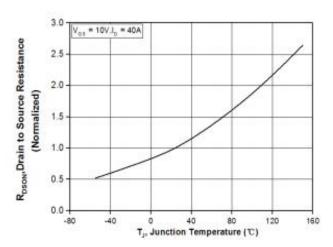


Fig 5. RDS(ON) vs junction temperature

Vos. Drain to Source Voltage (V) Fig 4. Capacitance Characteristics

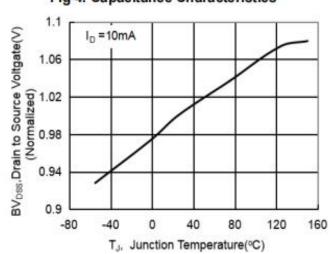


Fig 6. BVpss vs junction temperature



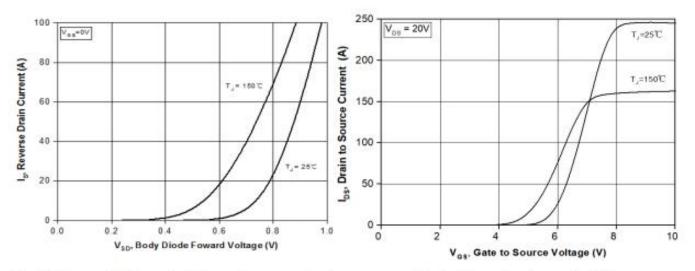
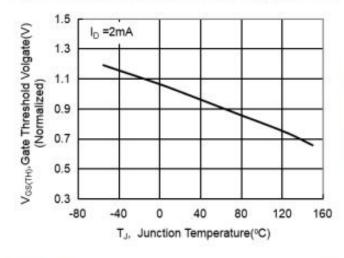


Fig 7 . Forward characteristics of reverse diode

Fig 8. Transfer characteristics



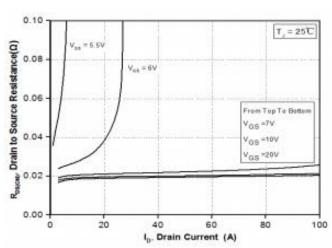


Fig 9. VGS(TH) vs junction temperature

Fig 10. Drain-source on-state resistance T<sub>J</sub>= 25°C

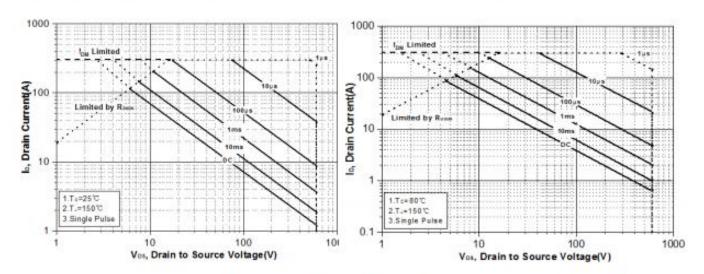


Fig 11. Safe operating area(TO-247) Tc= 25°C

Fig 12. Safe operating area(TO-247) Tc= 80°C



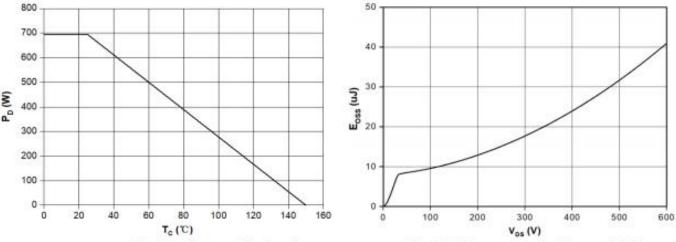


Fig 13. Power dissipation

Fig 14 . Eoss vs Drain-Source Voltage

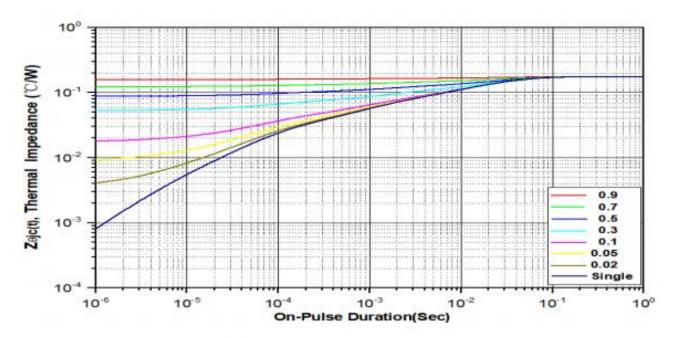


Fig 15. Transient thermal impedance



### **Test Circuits and Waveforms**

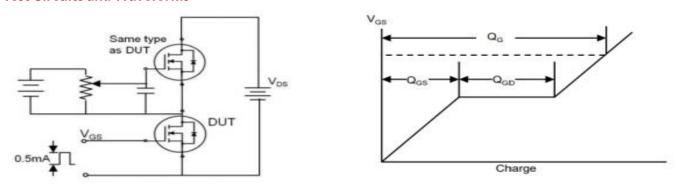


Fig 16. Gate charge test circuit & waveform

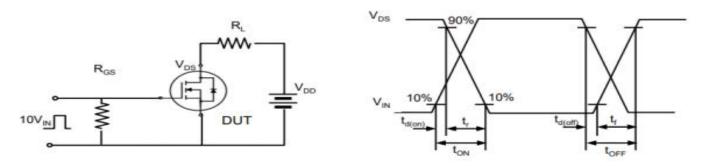


Fig 17. Switching time test circuit & waveform

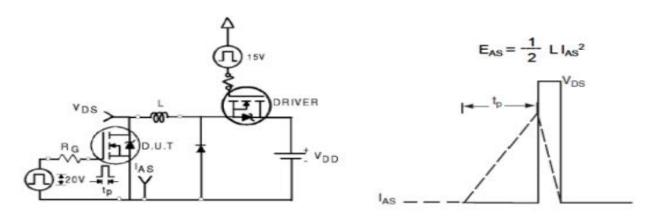


Fig 18. Unclamped Inductive switching test circuit & waveform

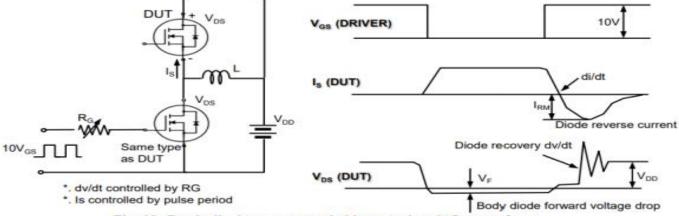
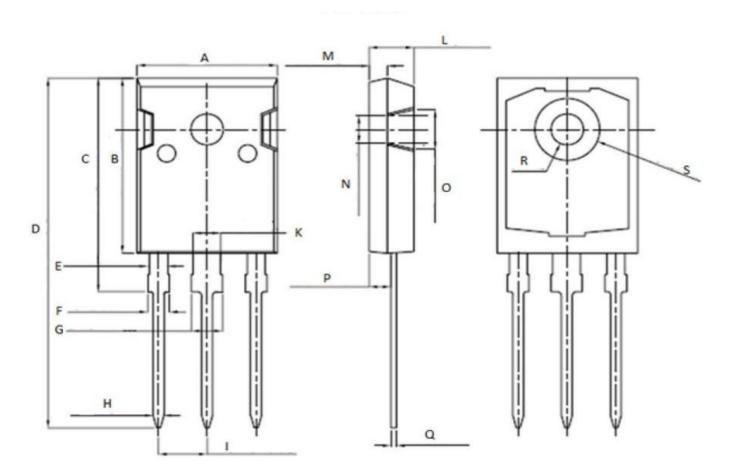


Fig 19. Peak diode recovery dv/dt test circuit & waveform



## Package outline drawing(TO-247-3 Unit: mm)



	Unit: mm	
Symbol	Min.	Max.
Α	15. 95	16. 25
В	20.85	21. 25
С	20.95	21. 35
D	40.5	40.9
E	1.9	2. 1
F	2. 1	2. 25
G	3. 1	3. 25
Н	1.1	1.3
	5. 40	5. 50

	Unit: mm	
Symbol	Min.	Max.
K	2.90	3. 10
L	4.90	5. 30
M	1.90	2.10
N	4.50	4. 70
0	5.40	5. 60
P	2. 29	2.49
Q	0.51	0.71
R	ф3.5	ф 3. 7
S	ф7.1	ф 7. 3



#### **Disclaimers:**

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information in current and complete. All products are sold subject to Reasunos's terms and conditions supplied at the time of orderacknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the speciffications at the time of sale. Testing, reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr- actual agreement, testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using Reasunos's components. To minimize risk, customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license eith- er expressed or implied under its patent rights, nor the rights of others. Reproduction of inform- ation in Reasunos's data sheets or data books is permissible only if reproduction is without modification oralteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all exp- ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such statements.

#### **Life Support Policy:**

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.

As used herein:

- 1. Life support devices or systems are devices or systems which: a.are intended for surgical implant into the human body, b.support or sustain life,
- c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.
- 2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

# 单击下面可查看定价,库存,交付和生命周期等信息

>>REASUNOS(瑞森)