

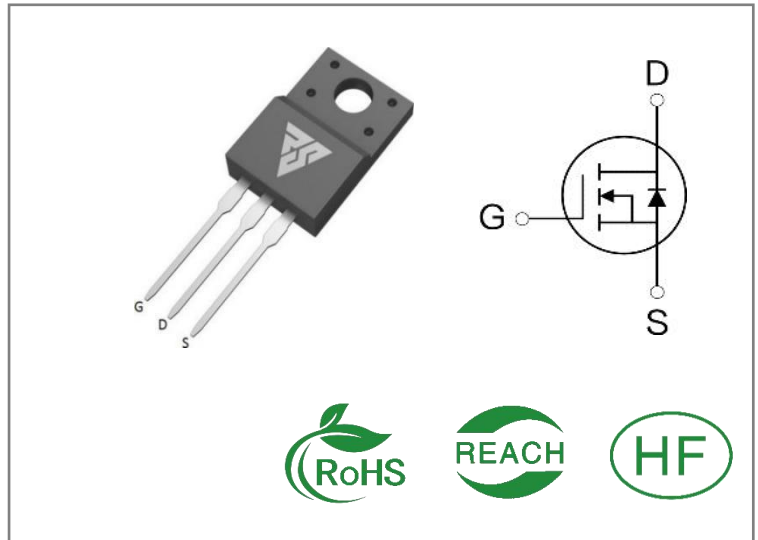
ID	R <sub>DS(ON)</sub> (Typ)	VDSS
13A	0.52Ω	650V

**Applications:**

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

**Features:**

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability


**Ordering Information**

Part Number	Package	Marking	Packing	Qty.
RS13N65F	T0-220F	RS13N65F	Tube	50 PCS

**Absolute Maximum Ratings** Tc= 25°C unless otherwise specified

Symbol	Parameter	RS13N65F	Units
VDSS	Drain-to-Source Voltage	650	V
ID	Continuous Drain Current TC=25°C	13	A
IDM	Pulsed Drain Current (Note*1)	52	
PD	Power Dissipation	45	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy L = 10mH, VDD = 50V, RG = 25 Ω	387	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

\* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

**Thermal Resistance**

Symbol	Parameter	RS13N65F	Units	Test Conditions
R $\theta$ JC	Junction-to-Case	1.75	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 $^{\circ}\text{C}$
R $\theta$ JA	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.

**OFF Characteristics** T<sub>J</sub>= 25 $^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	650	--	--	V	VGS=0V, ID=250 $\mu\text{A}$
IDSS	Drain- to- Source Leakage Current	--	--	1	$\mu\text{A}$	VDS=650V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=30V , VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-30V , VDS=0V

**ON Characteristics** T<sub>J</sub>=25 $^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	0.52	0.65	$\Omega$	VGS=10V, ID=6.5A
VGS(TH)	Gate Threshold Voltage	3	--	4	V	VGS=VDS, ID=250 $\mu\text{A}$

**Resistive Switching Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	49	--	nS	VDS=325V ID=13A RG=25 $\Omega$
trise	Rise Time	--	38	--		
td(OFF)	Turn- OFF Delay Time	--	245	--		
tfall	Fall Time	--	114	--		

**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1779	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	183	--		
Crss	Reverse Transfer Capacitance	--	25	--		
Qg	Total Gate Charge	--	62	--	nC	VDS=520V ID=13A VGS=10V
Qgs	Gate- to- Source Charge	--	9	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	32	--		

**Source- Drain Diode Characteristics**

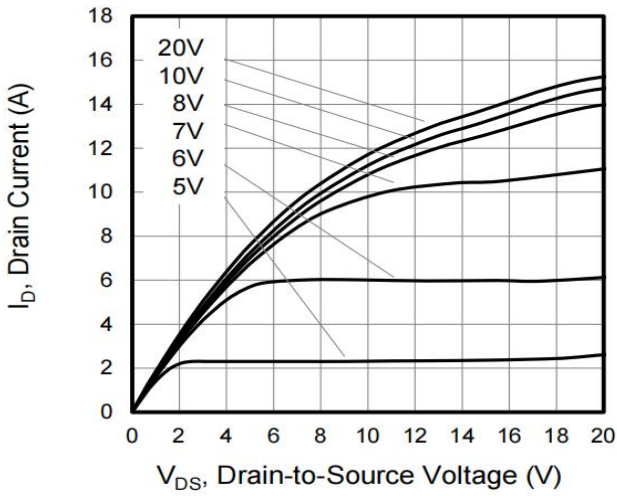
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	13	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	52	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=6.5A,VGS=0V
trr	Reverse Recovery Time	--	582	--	nS	VGS=0V IS=13A,di/dt=100 A/μs
Qrr	Reverse Recovery Charge	--	3.5	--	μC	

**Notes:**

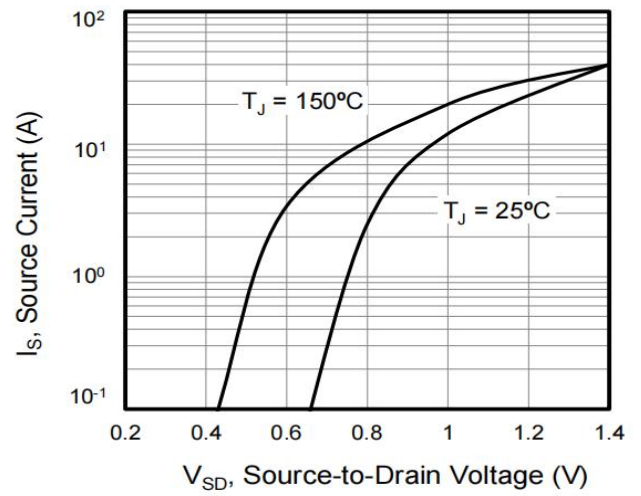
- \* 1. Repetitive rating, pulse width limited by maximum junction temperature.
- \* 2. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 1\%$

**Typical Feature Curve**

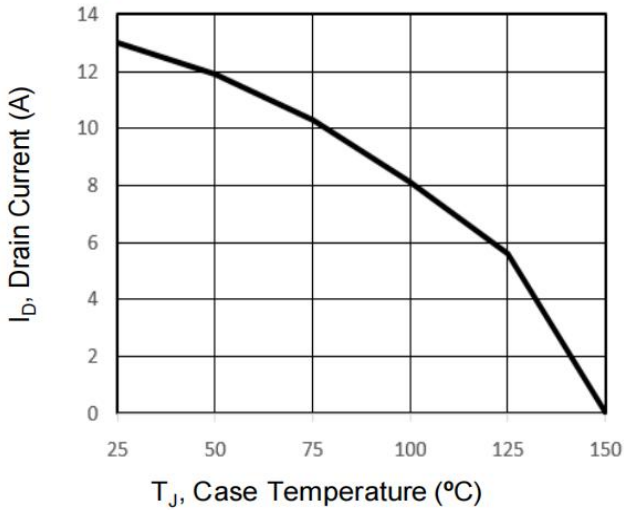
**Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )**



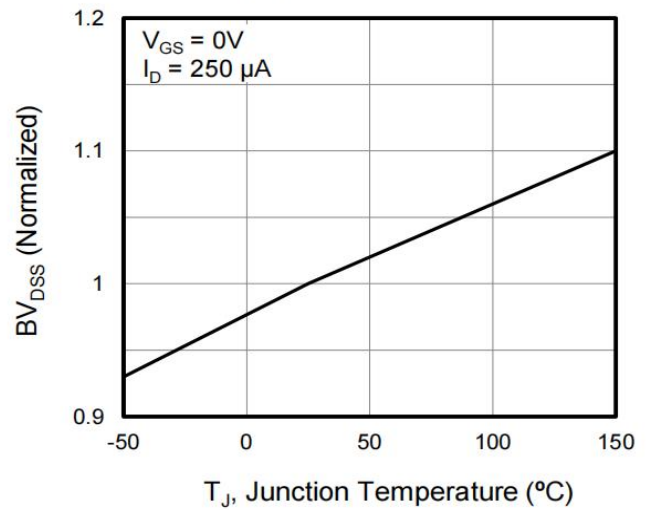
**Figure 2. Body Diode Forward Voltage**



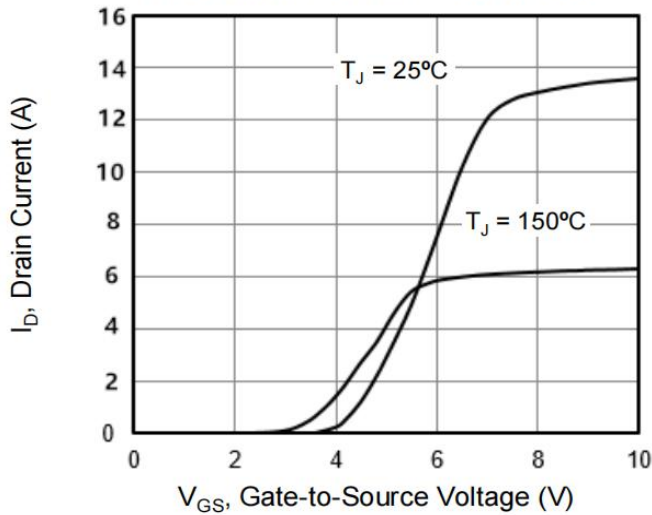
**Figure 3. Drain Current vs. Temperature**



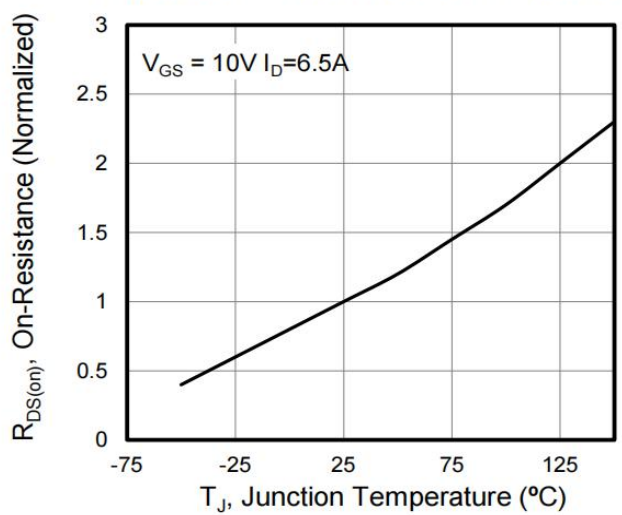
**Figure 4.  $BV_{DSS}$  Variation vs. Temperature**



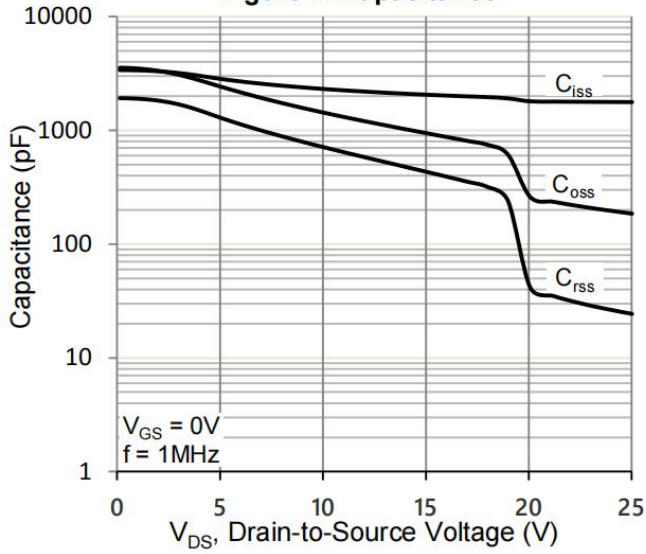
**Figure 5. Transfer Characteristics**



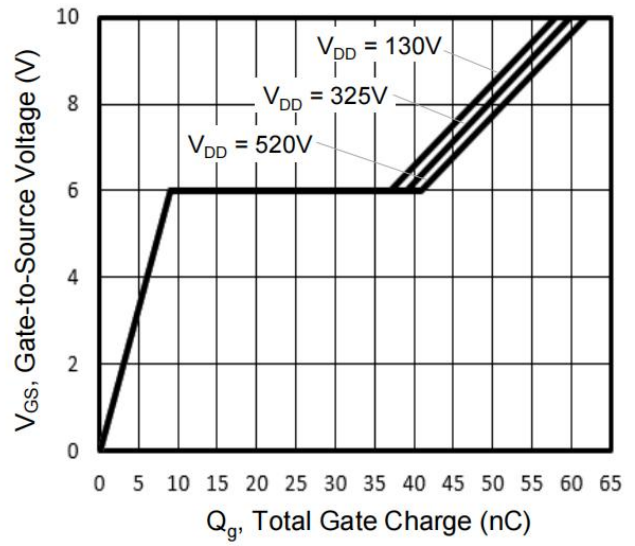
**Figure 6. On-Resistance vs. Temperature**



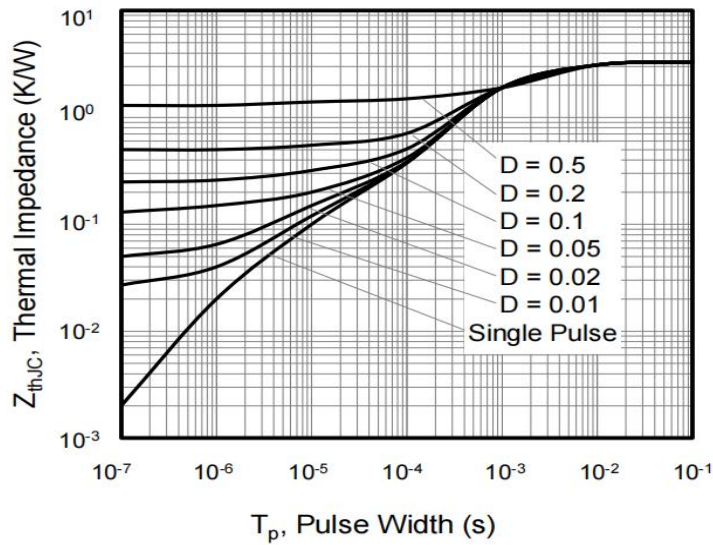
**Figure 7. Capacitance**



**Figure 8. Gate Charge**



**Figure 9. Transient Thermal Impedance**



**Test Circuits and Waveforms**

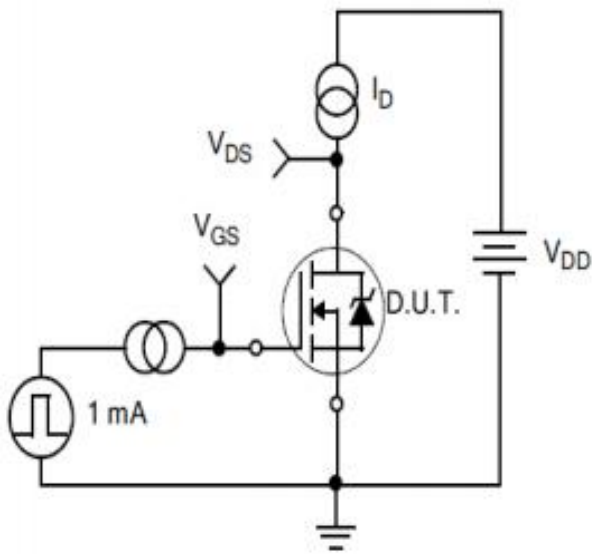


Figure 10.  
Gate Charge Test Circuit

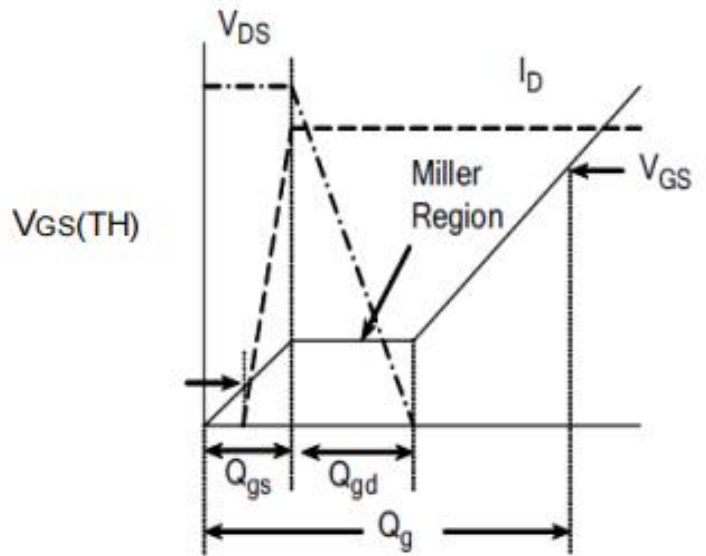


Figure 11.  
Gate Charge Waveform

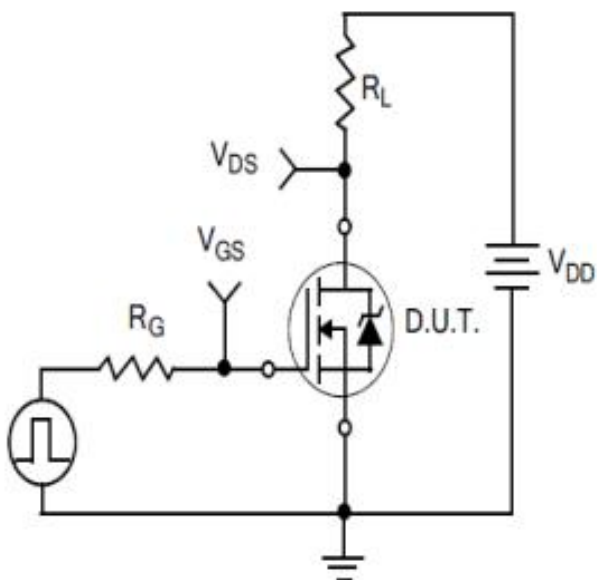


Figure 12.  
Resistive Switching Test Circuit

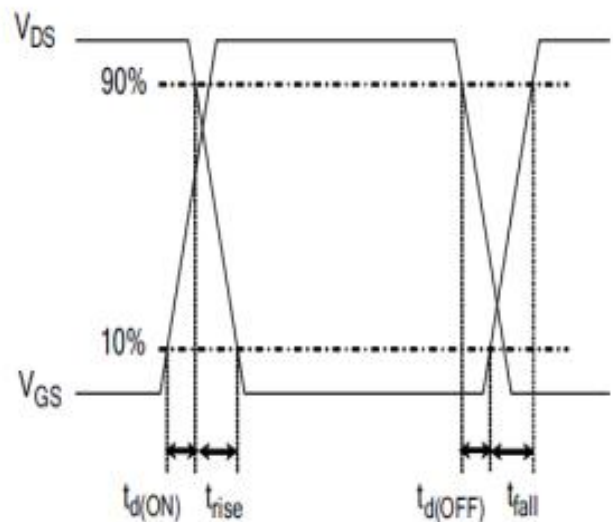


Figure 13.  
Resistive Switching Waveforms



**Test Circuits and Waveforms**

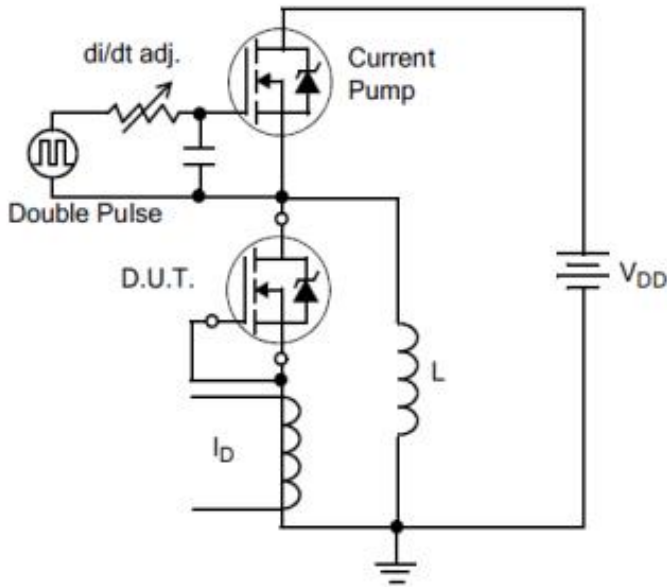


Figure 14. Diode Reverse Recovery Test Circuit

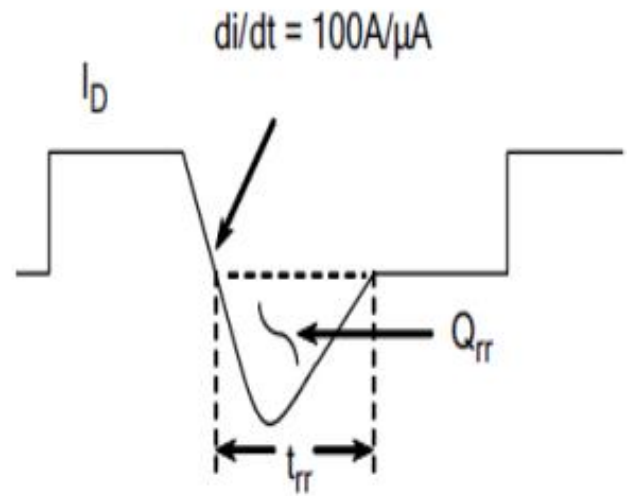


Figure 15. Diode Reverse Recovery Waveform

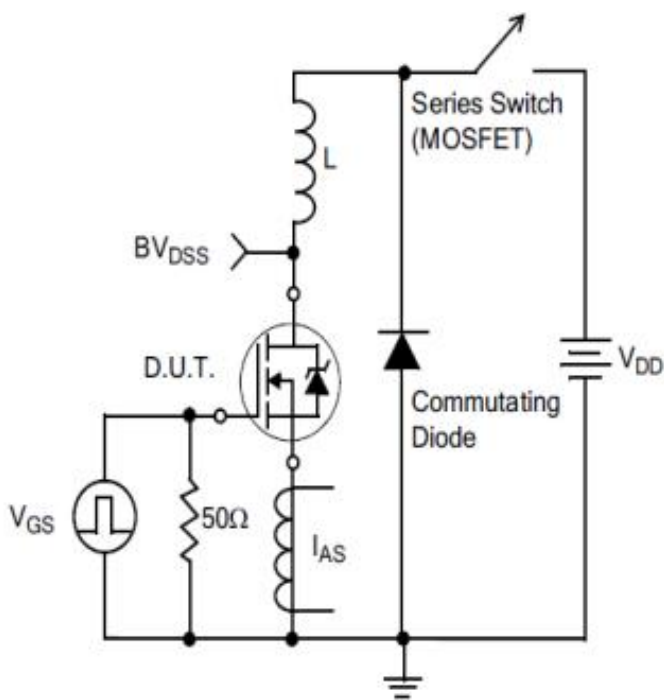
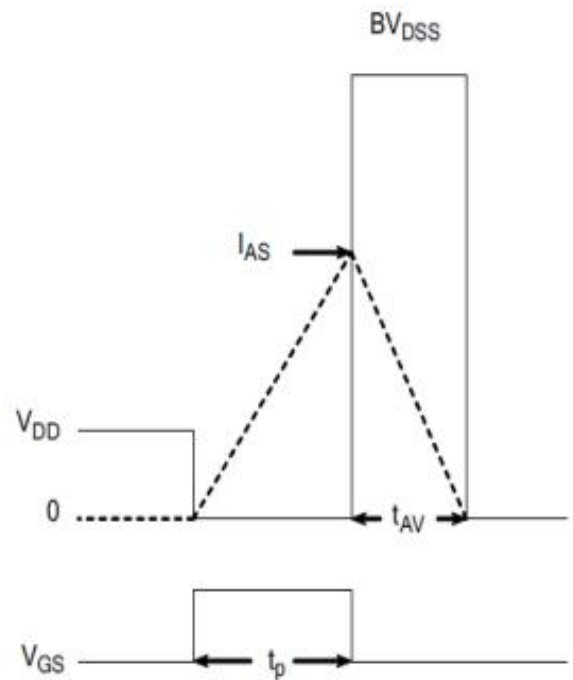


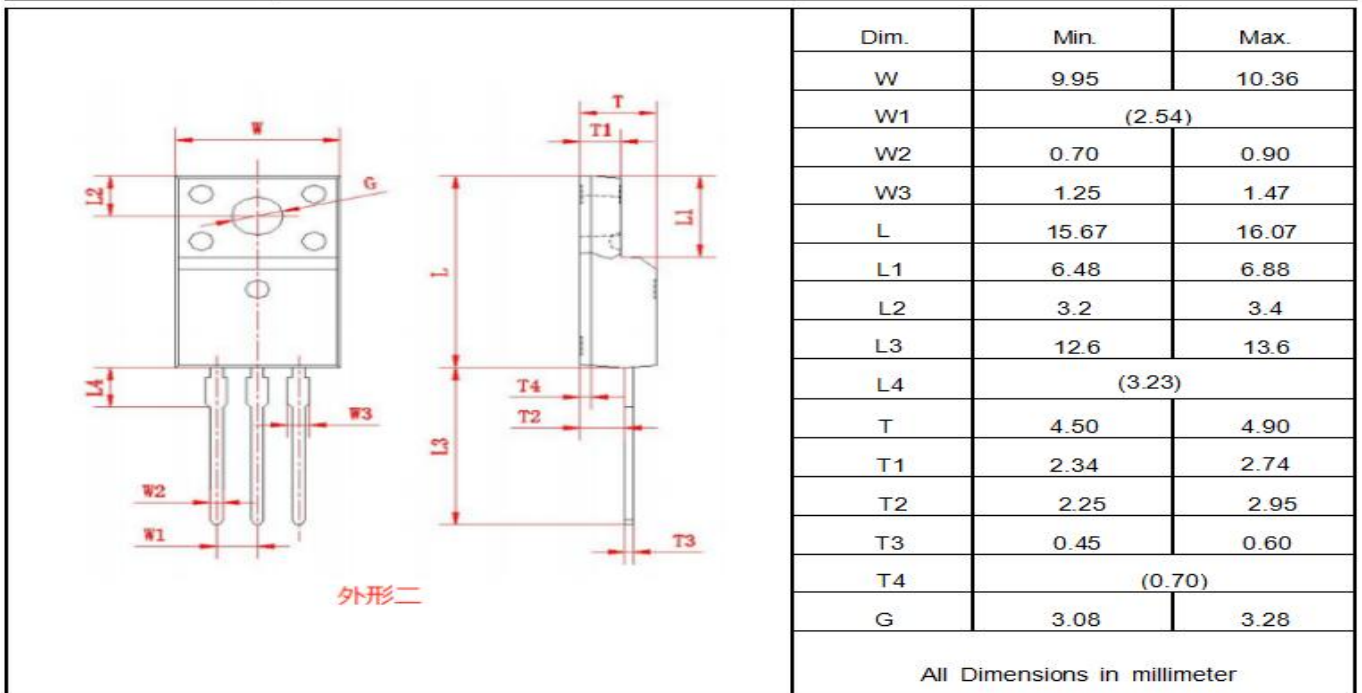
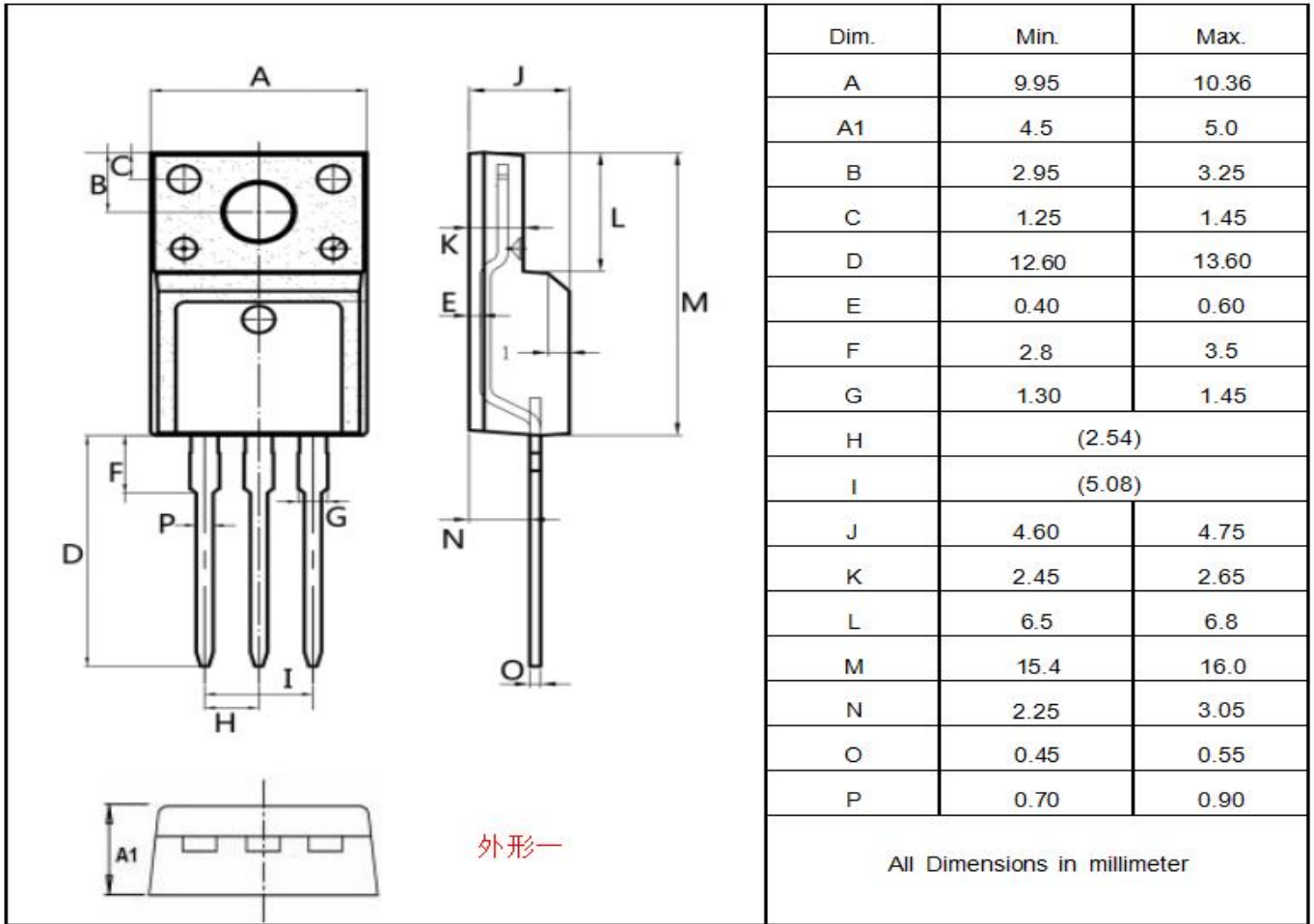
Figure 16. Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure 17. Unclamped Inductive Switching Waveforms

Package outline drawing(TO-220F Unit: mm )





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