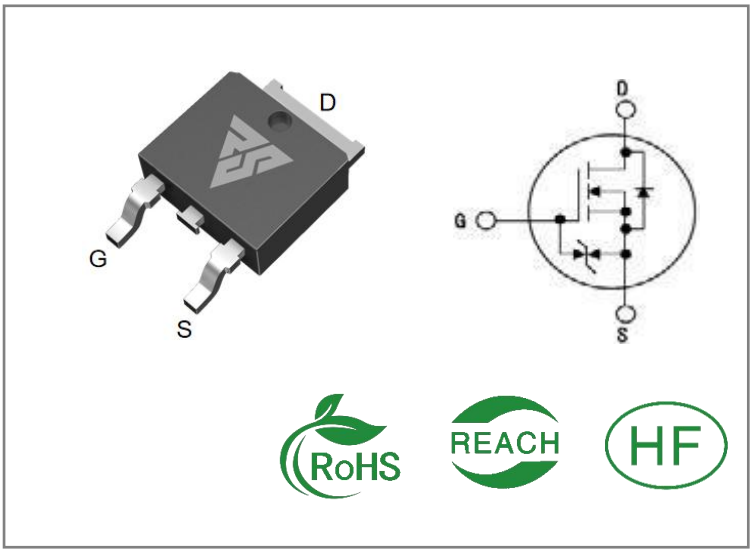
ID	R_{DS}(ON)(Typ)	VDSS
7.6A	480mΩ	650V



Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- AC-DC Switching Power Supply

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability
- Built-in ESD Diode

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RSE65R550D	T0-252	RSE65R550D	Tape&reel	2500 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RSE65R550D	Units
VDSS	Drain-to-Source Voltage	650	V
ID	Continuous Drain Current TC=25℃	7.6	A
ID	Continuous Drain Current TC=100℃	4.8	
IDM	Pulsed Drain Current (Note*1)	23	
PD	Power Dissipation	70	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy IAS=1.45A,VDD = 50V, RG = 25 Ω，TC=25℃	91	mJ
dv/dt	MOSFET dv/ dt ruggedness VDS = 0...400V	50	V/ns
dv/dt	Reverse diode dv/dt VDS = 0...400V, Tj = 25℃, ISD≤ID	15	V/ns
VESD(G-S)	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000	V
TL TPKG	Maximum Temperature for Soldering	300	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RSE65R550D	Units	Test Conditions
RθJC	Junction-to-Case	1.79	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	650	--	--	V	VGS=0V,ID=1mA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=650V,VGS=0 V
IGSS	Gate- to- Source Forward Leakage	--	--	1	μA	VGS=20V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-1		VGS=-20V ,VDS=0 V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	480	550	mΩ	VGS=10V,ID=2.4A
VGS(TH)	Gate Threshold Voltage	2	--	4	V	VGS=VDS,ID=260μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	25	--	nS	VDS=325V ID=3.3A RG=25Ω
trise	Rise Time	--	19	--		
td(OFF)	Turn- OFF Delay Time	--	87	--		
tfall	Fall Time	--	18	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	680	--	pF	VGS=0V VDS=400V f=1.0MHz
Coss	Output Capacitance	--	19	--		
Crss	Reverse Transfer Capacitance	--	2.9	--		
Qg	Total Gate Charge	--	16	--	nC	VDS=520V ID=3.3A VGS=10V
Qgs	Gate- to- Source Charge	--	3.1	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	5.2	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	7.6	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	23	A	
VSD	Diode Forward Voltage	--	--	1.3	V	IS=3.3A,VGS=0V
trr	Reverse Recovery Time	--	250	--	nS	VR=400V IS=3.3A,di/dt=100 A/μs
Qrr	Reverse Recovery Charge	--	1.9	--	μC	

Notes:

* 1. Repetitive rating; pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

Typical Feature Curve

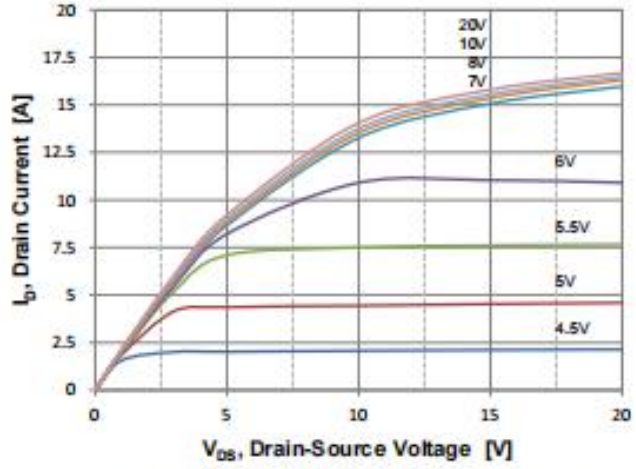


Figure 1. On Region Characteristics

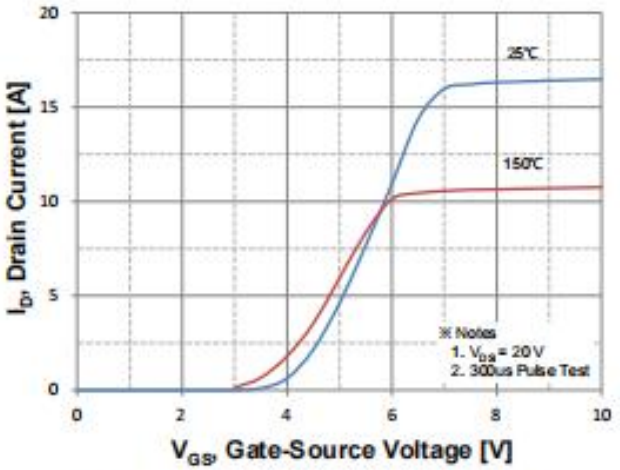


Figure 2. Transfer Characteristics

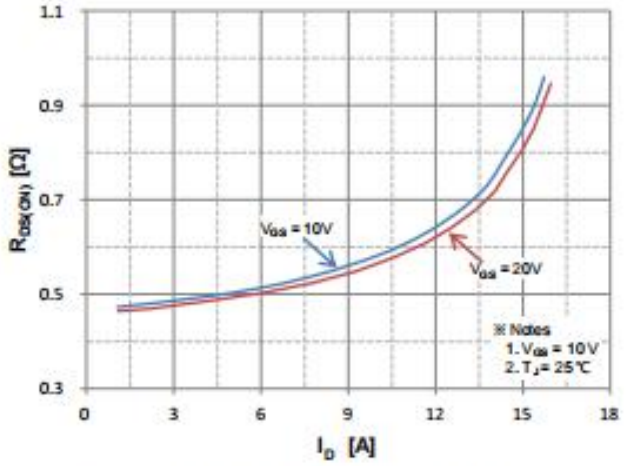


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

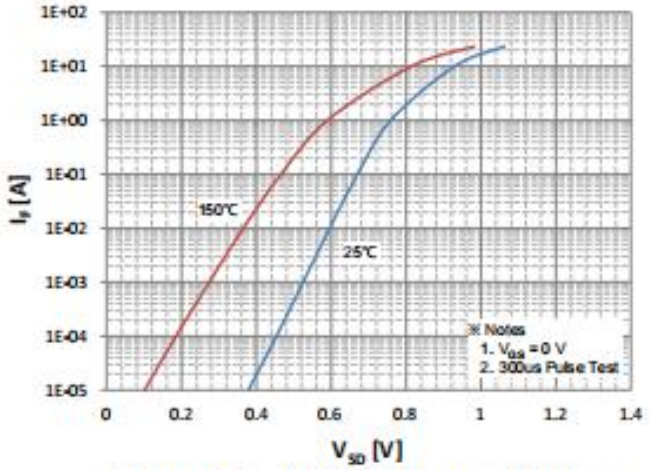


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

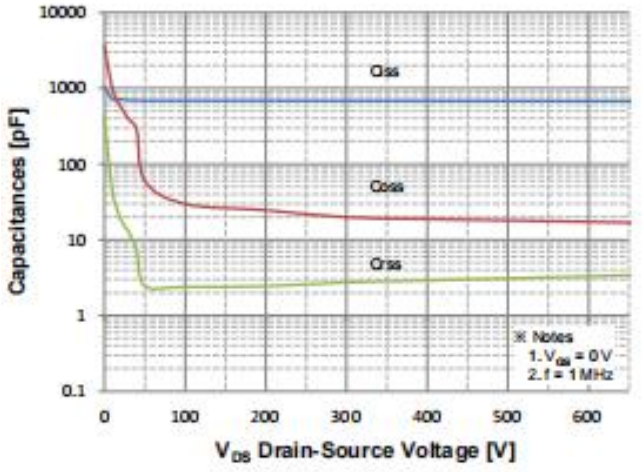


Figure 5. Capacitance Characteristics

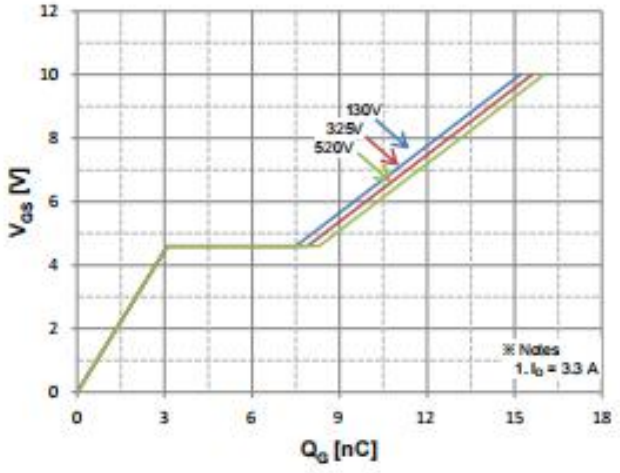


Figure 6. Gate Charge Characteristics

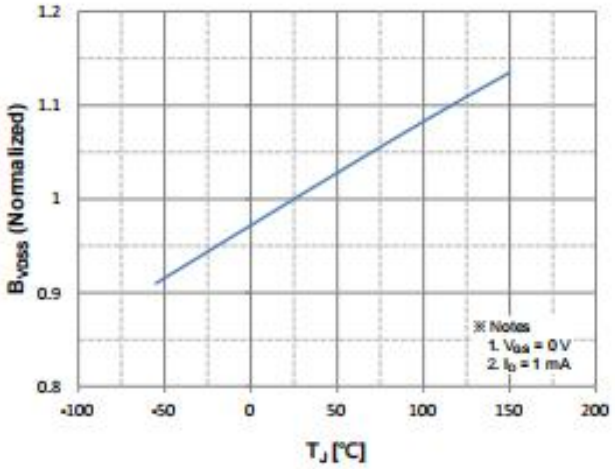


Figure 7. Breakdown Voltage Variation vs. Temperature

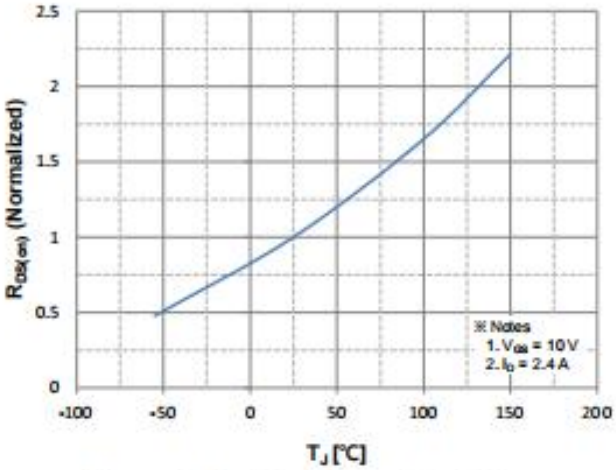


Figure 8. On-Resistance Variation vs. Temperature

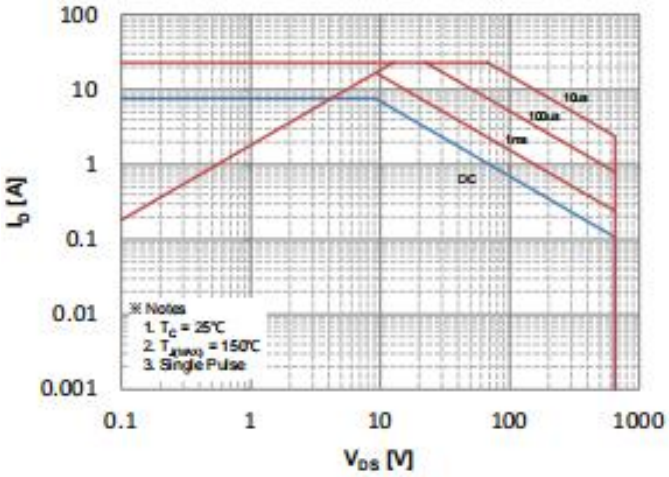


Figure 9. Maximum Safe Operating Area

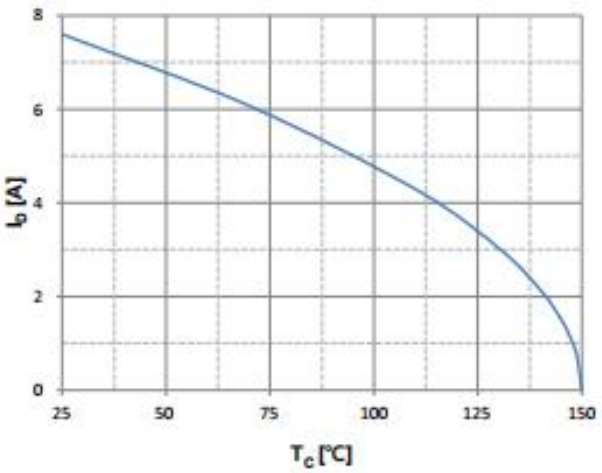


Figure 10. Maximum Drain Current vs. Case Temperature

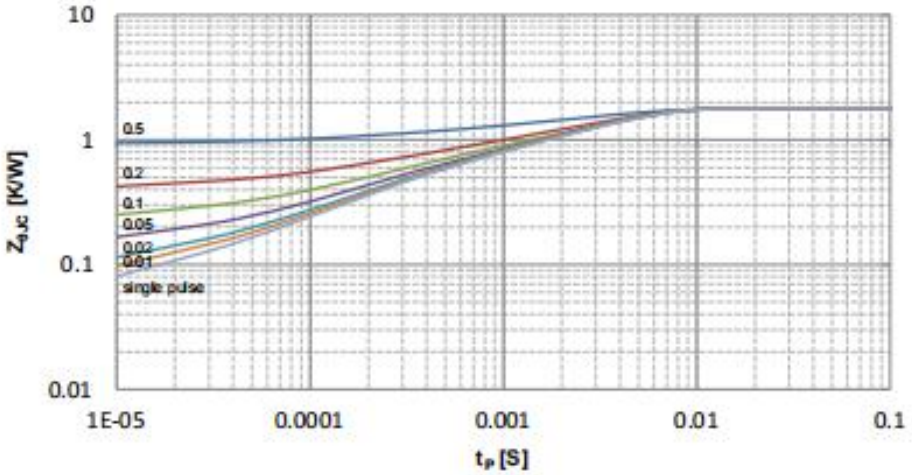


Figure 11. Transient Thermal Response Curve

Test Circuits and Waveforms

Fig 12. Gate Charge Test Circuit & Waveform

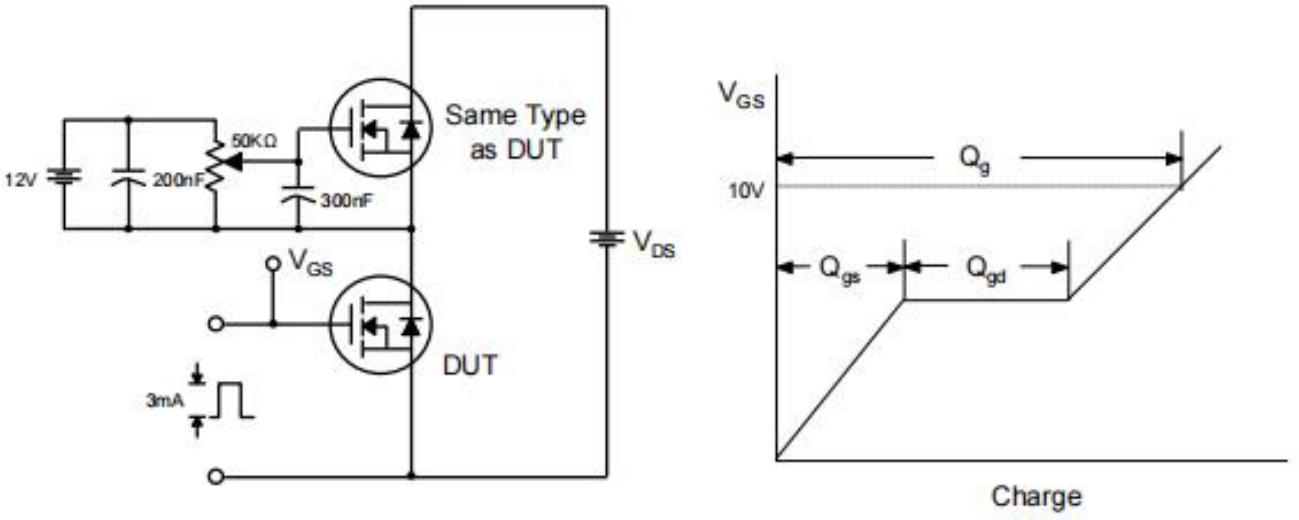


Fig 13. Resistive Switching Test Circuit & Waveforms

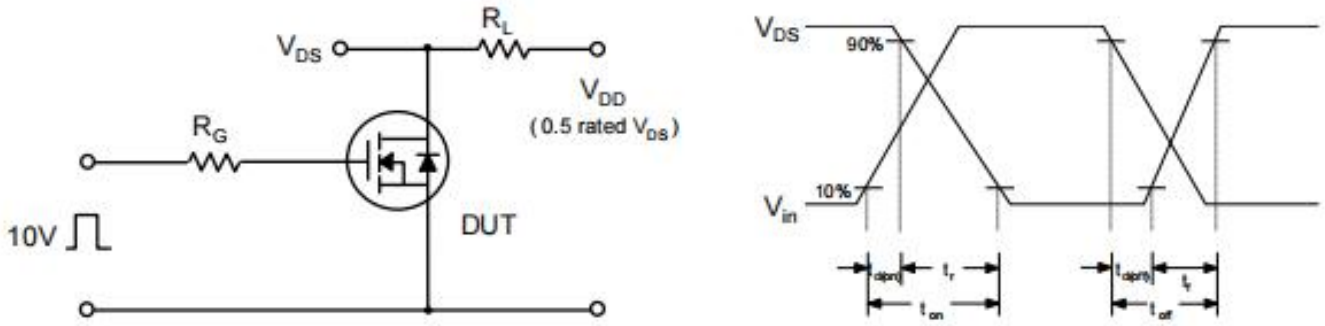
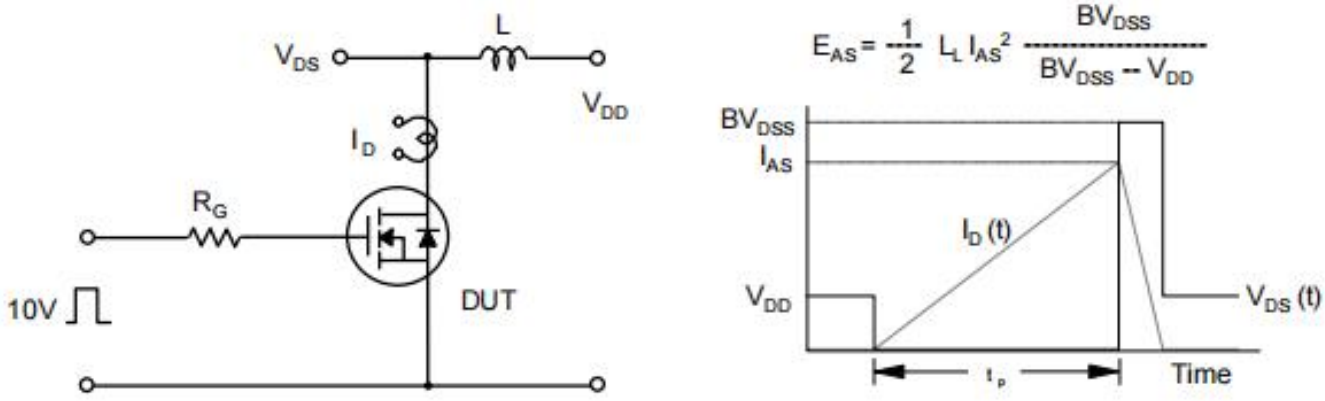
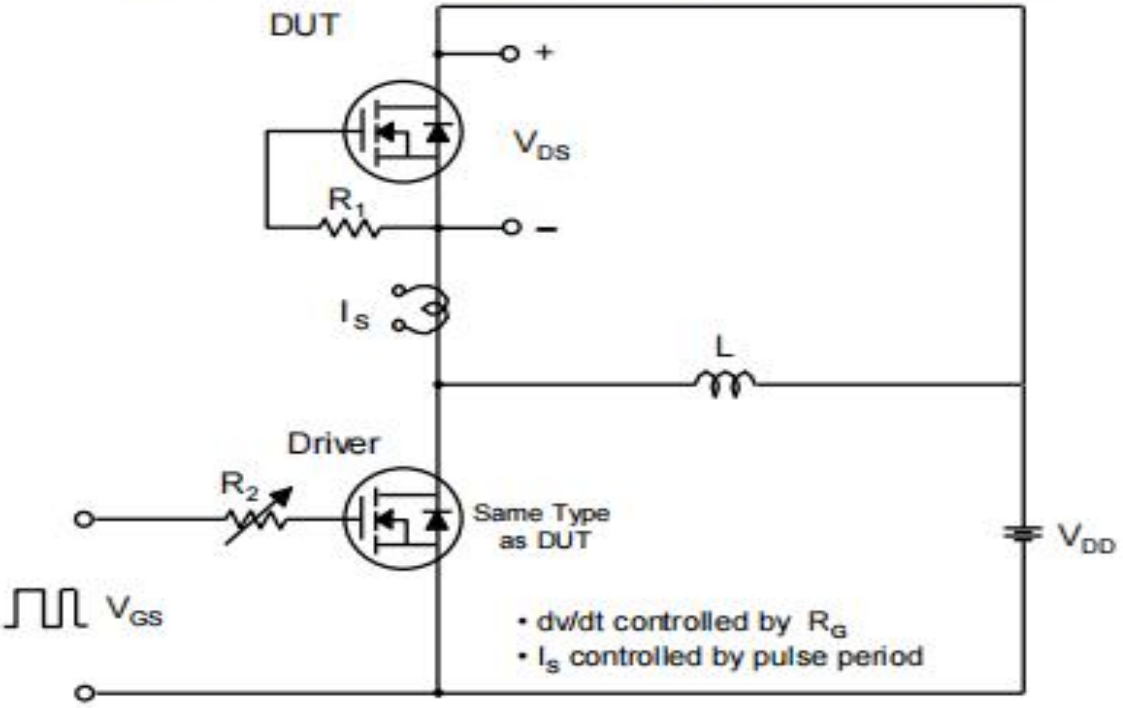


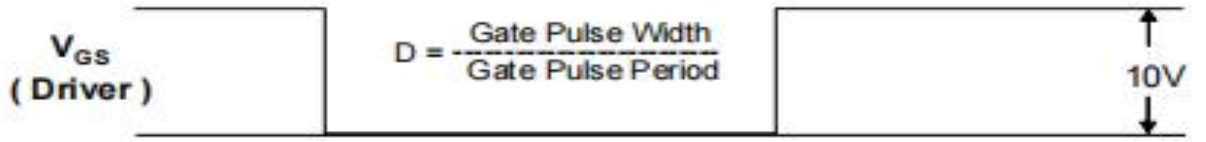
Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

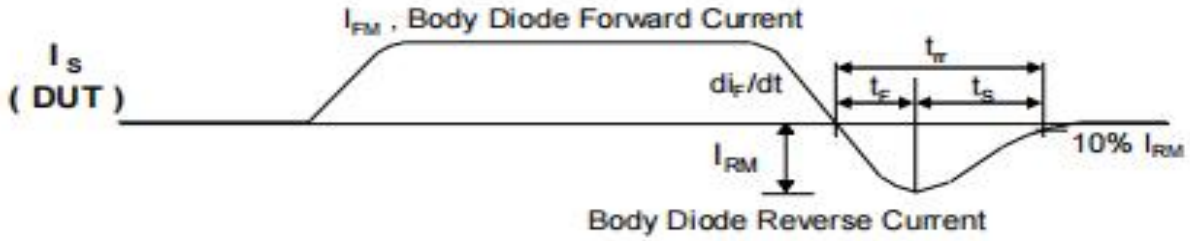


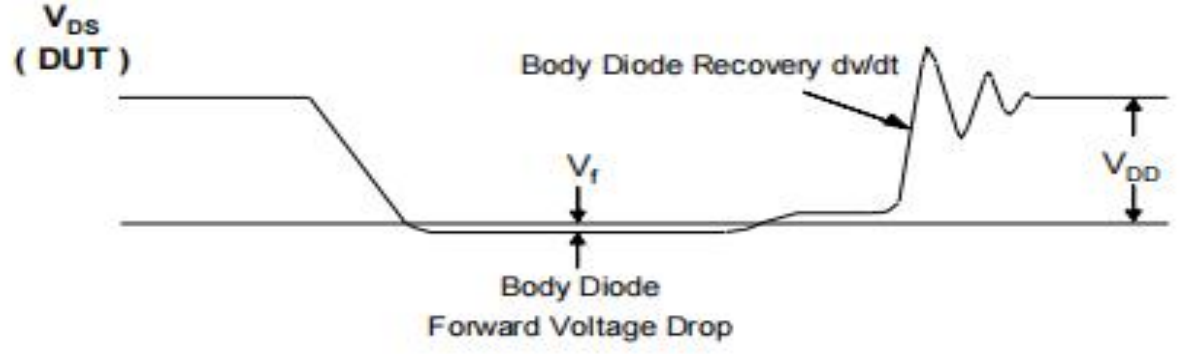
Test Circuits and Waveforms

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

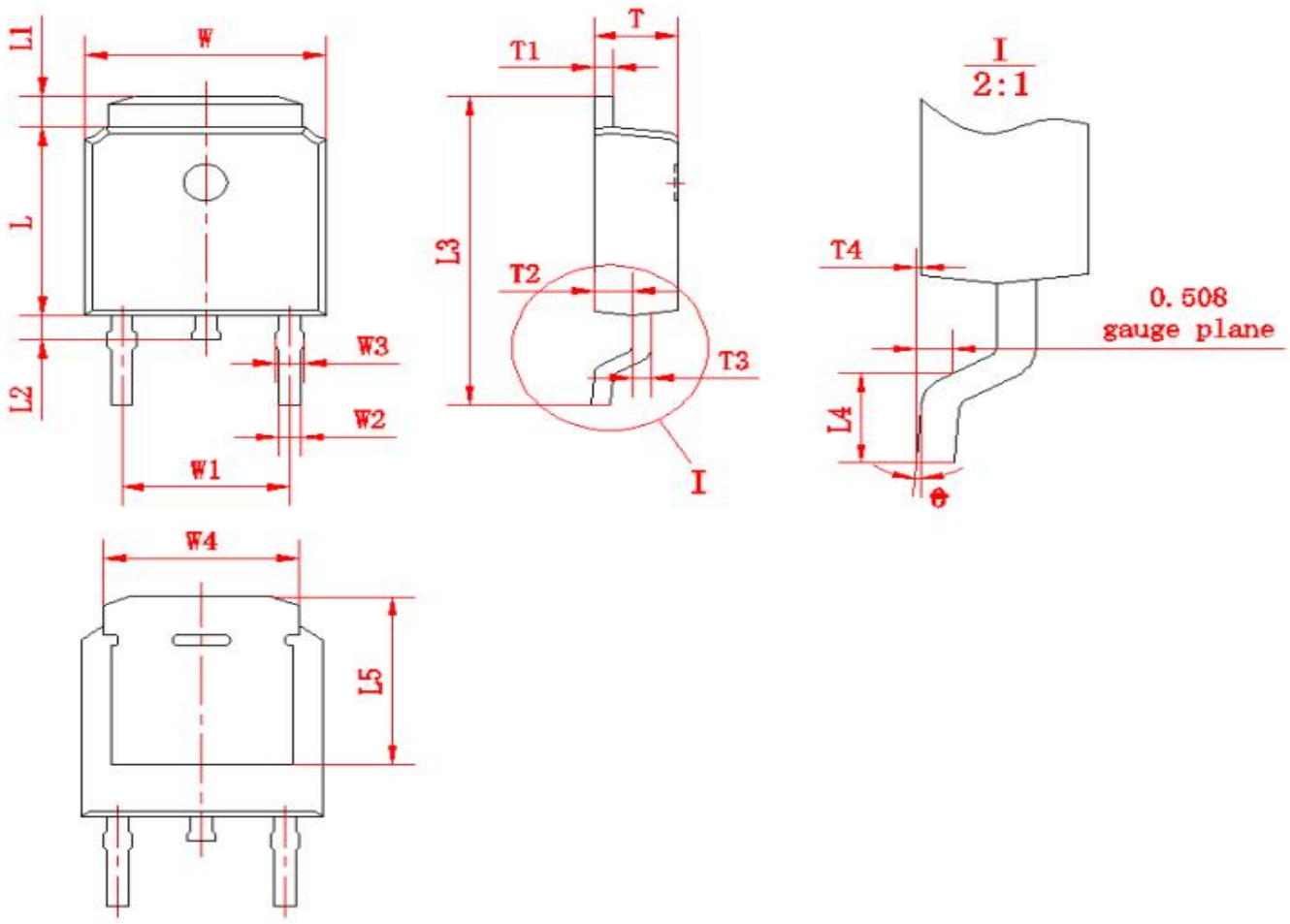








Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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