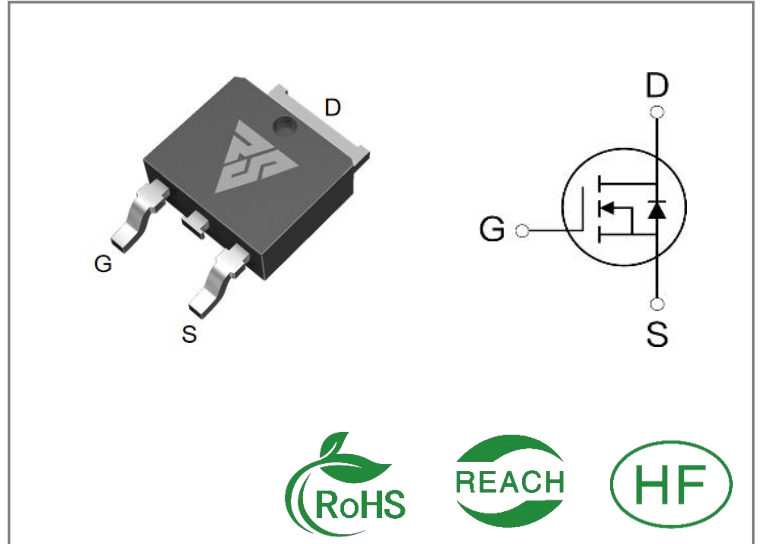


ID	R _{DS(ON)} (Typ)	VDSS
30A	22mΩ	60V


Applications:

- Load Switch
- PWM Applications
- Power Management

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS60N30D	T0-252	RS60N30D	Tape&reel	2500 PCS

Absolute Maximum Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RS60N30D	Units
VDSS	Drain-to-Source Voltage	60	V
ID	Continuous Drain Current TC=25°C	30	A
ID	Continuous Drain Current TC=100°C	14	
IDM	Pulsed Drain Current	60	
PD	Power Dissipation	45	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy L = 0.5mH, VDD = 30V, VG = 10V, Tj = 25°C	72	mJ
TL TPKG	Maximum Temperature for Soldering	300	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.
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Thermal Resistance

Symbol	Parameter	RS60N30D	Units	Test Conditions
R θ JC	Junction-to-Case	3.3	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 °C
R θ JA	Junction-to-Ambient	60		1 cubic foot chamber, free air.

OFF Characteristics T_J= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	60	--	--	V	VGS=0V, ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=60V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V , VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V , VDS=0 V

ON Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	22	35	mΩ	VGS=10V, ID=20A
		--	26	40	mΩ	VGS=4.5V, ID=10A
VGS(TH)	Gate Threshold Voltage	1.2	1.5	2.5	V	VGS=VDS, ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	5	--	nS	VDS=30V ID=2A RG=3Ω VGS=10V
trise	Rise Time	--	2.6	--		
td(OFF)	Turn- OFF Delay Time	--	16	--		
tfall	Fall Time	--	2.3	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	500	--	pF	VGS= 0V VDS=30V f=1.0MHz
Coss	Output Capacitance	--	60	--		
Crss	Reverse Transfer Capacitance	--	25	--		
Qg	Total Gate Charge	--	47	--	nC	VDS= 30V ID=4.5A VGS=10V
Qgs	Gate- to- Source Charge	--	6	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	14	--		

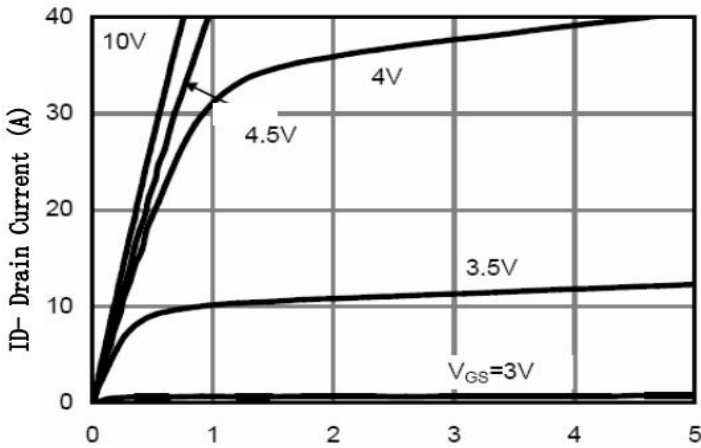
Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	30	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	60	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=20A,VGS=0V
trr	Reverse Recovery Time	--	35	--	nS	VGS=0V IS=20A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	53	--	nC	

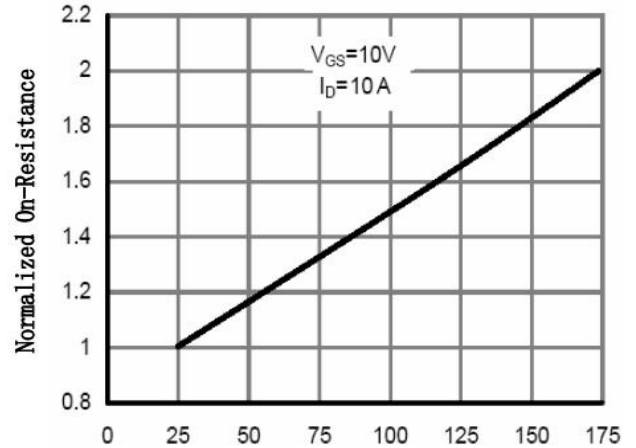
Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$

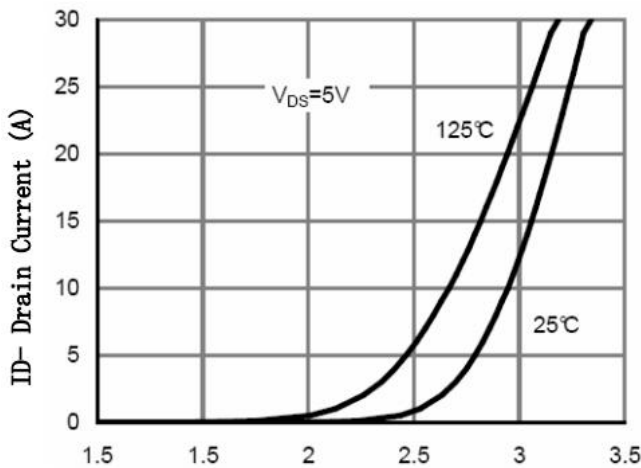
Typical Feature Curve



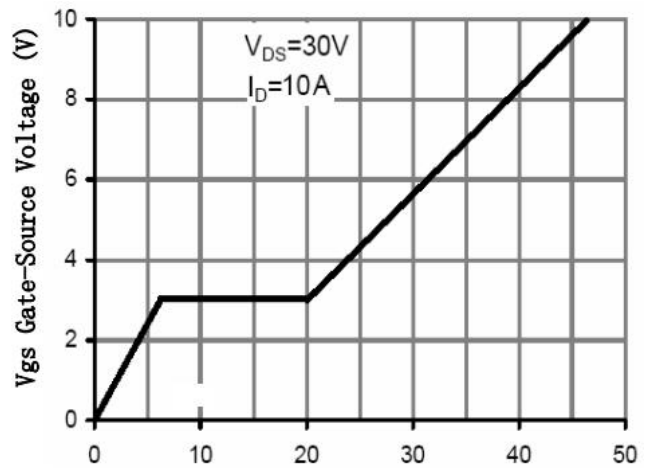
Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



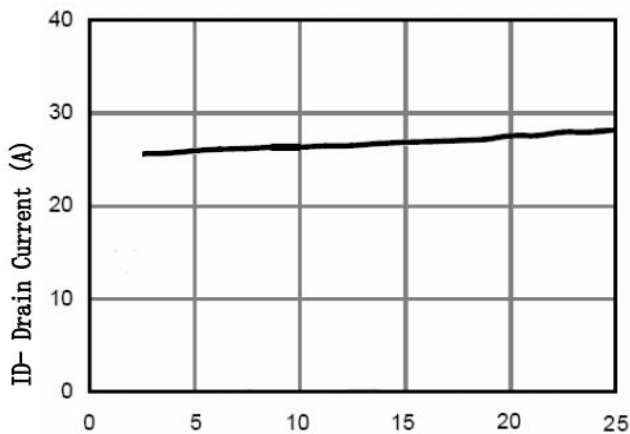
TJ-Junction Temperature (°C)
Figure 2 Rdson-Junction Temperature



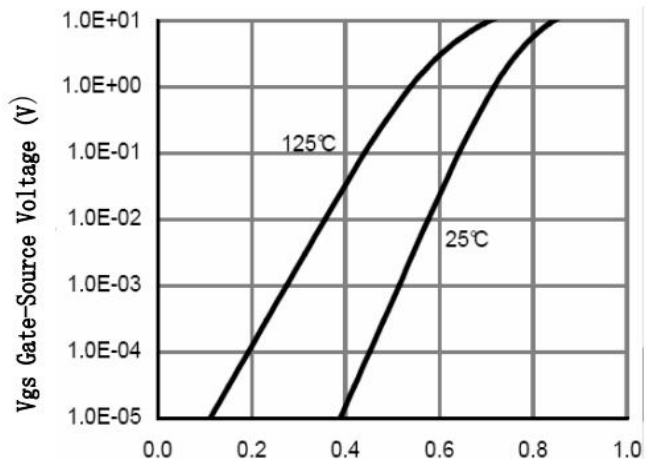
ID- Drain Current (A)
Figure 3 Rdson- Drain Current



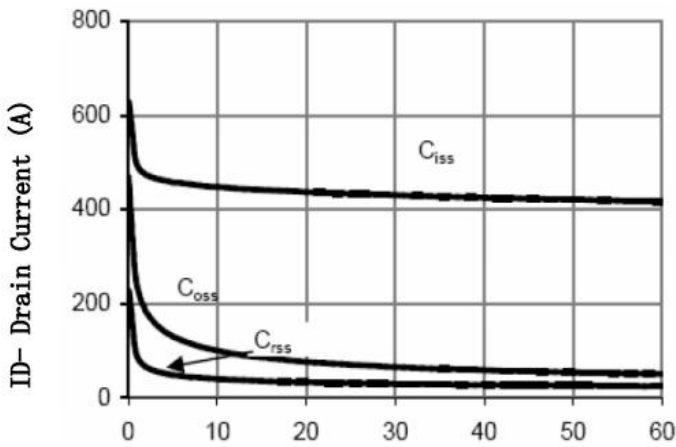
Vsd Source-Drain Voltage (V)
Figure 4 Source- Drain Diode Forward



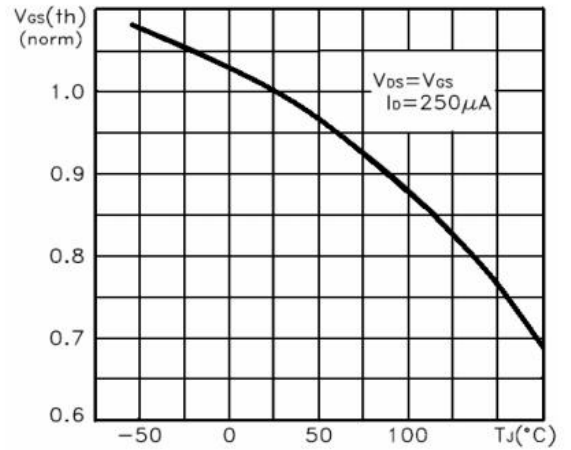
ID- Drain Current (A)
Figure 5 Rdson- Drain Current



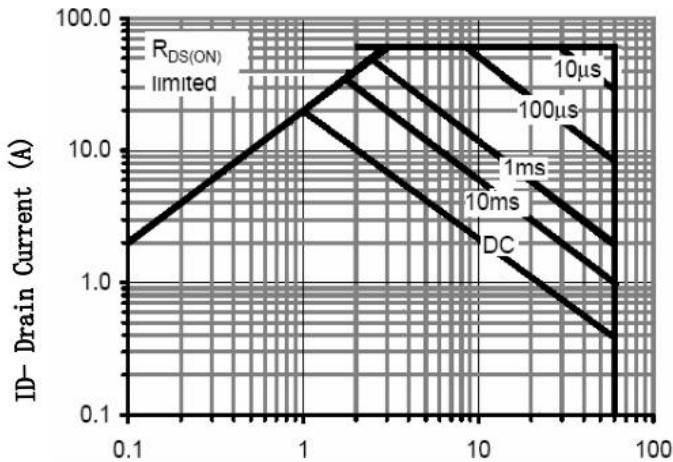
Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



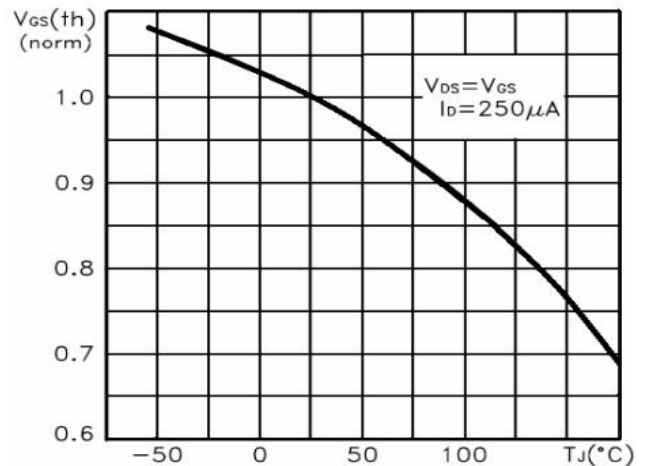
Vds Drain-Source Voltage (V)
Figure 7 Safe Operation Area



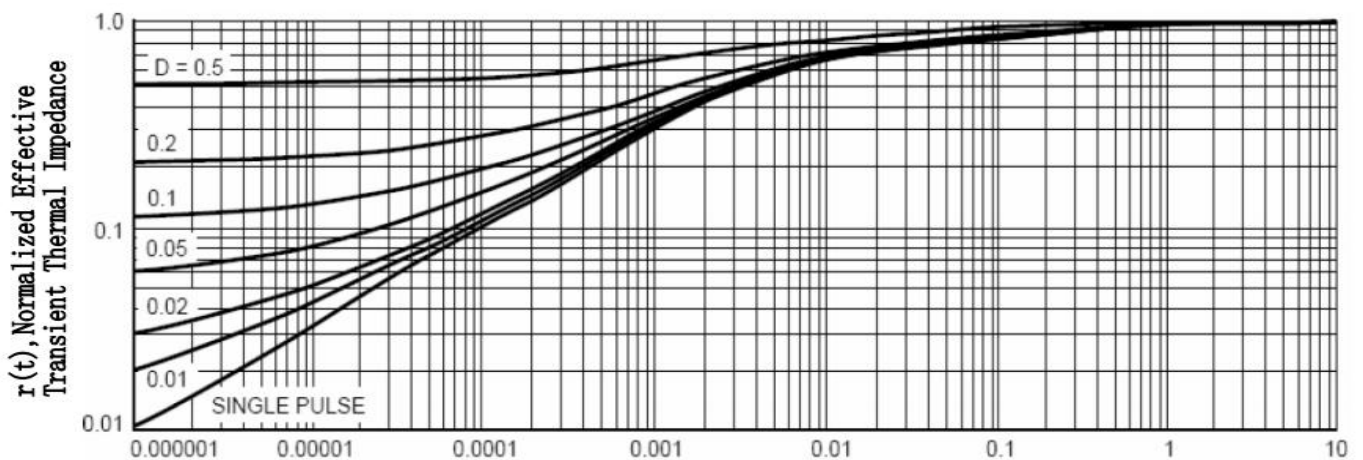
TJ-Junction Temperature(°C)
Figure 8 VGS(th) vs Junction Temperature



Vds Drain-Source Voltage (V)
Figure 9 Safe Operation Area



TJ-Junction Temperature(°C)
Figure 10 VGS(th) vs Junction Temperature



Square Wave Pulse Duration (sec)
Figure 11 Normalized Maximum Transient Thermal Impedance

Test circuits and Waveforms

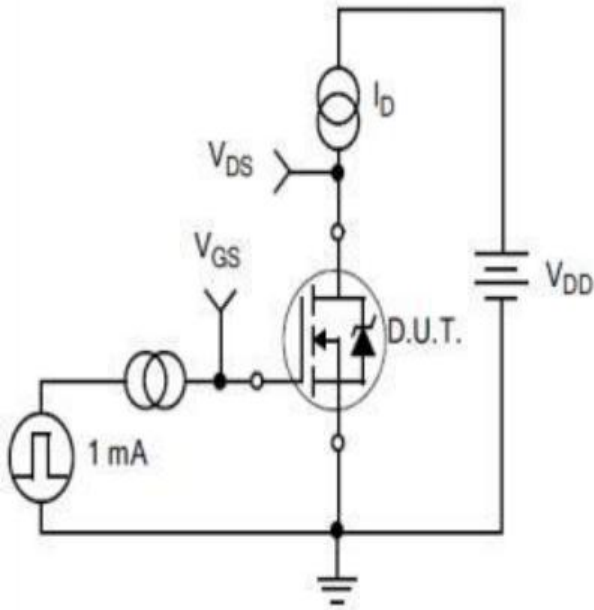


Figure A.
Gate Charge Test Circuit

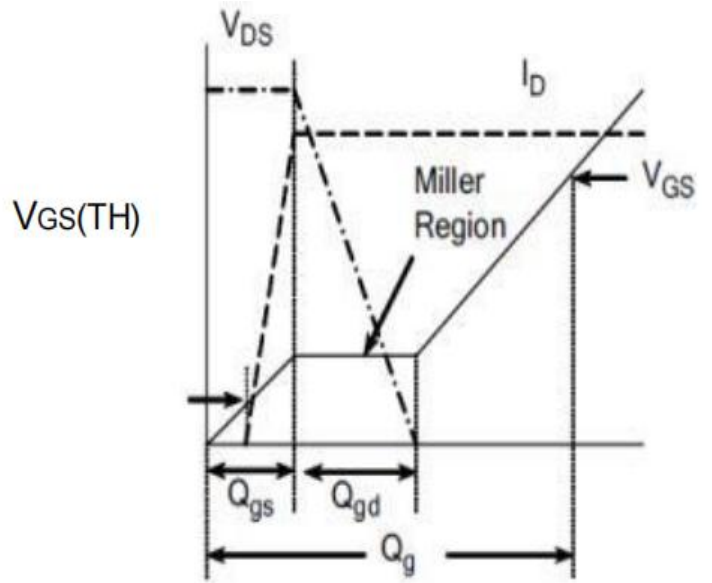


Figure B.
Gate Charge Waveform

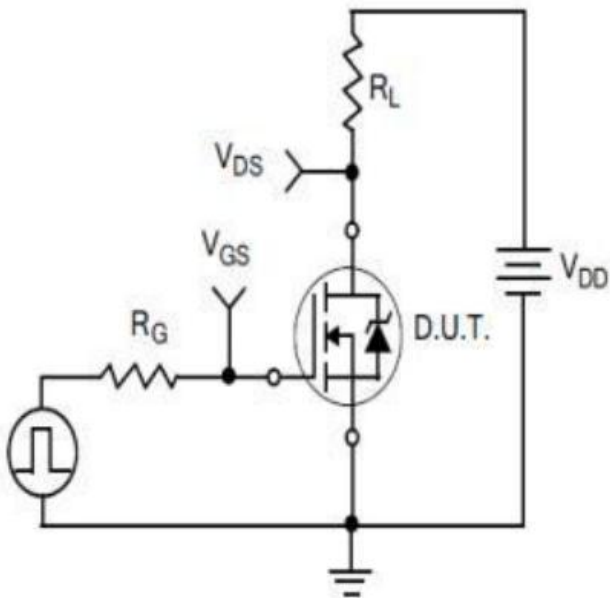


Figure C.
Resistive Switching Test Circuit

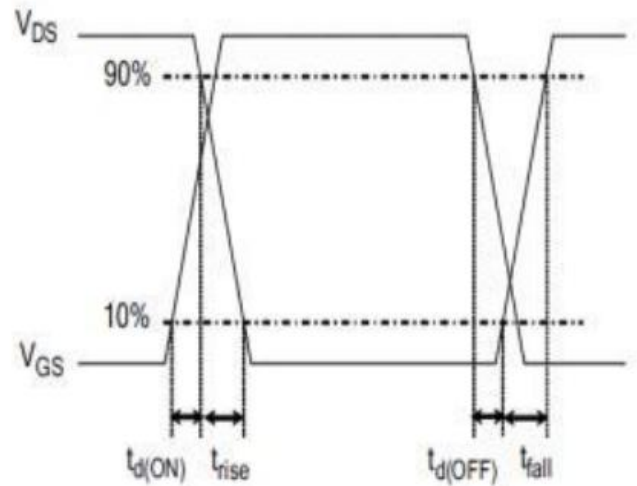


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

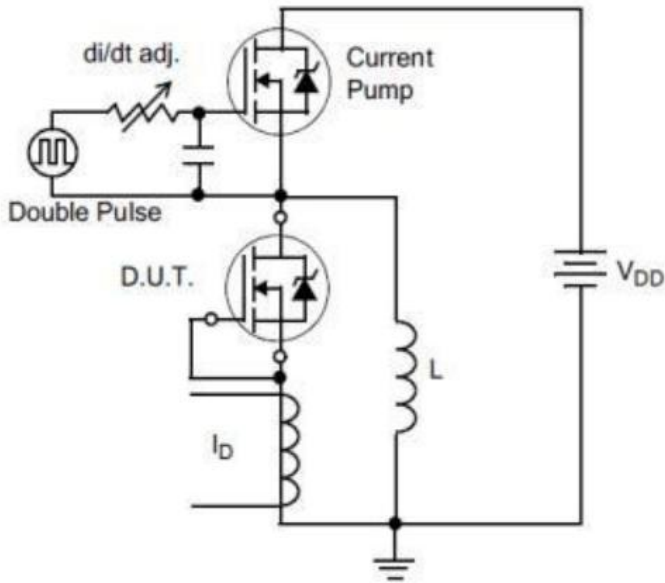


Figure E. Diode Reverse Recovery Test Circuit

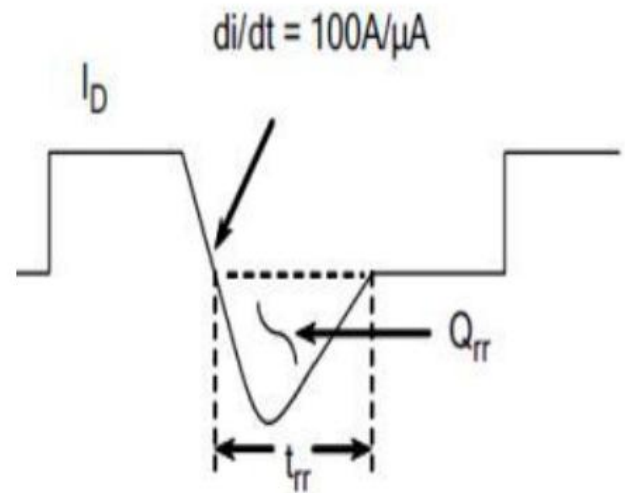


Figure F. Diode Reverse Recovery Waveform

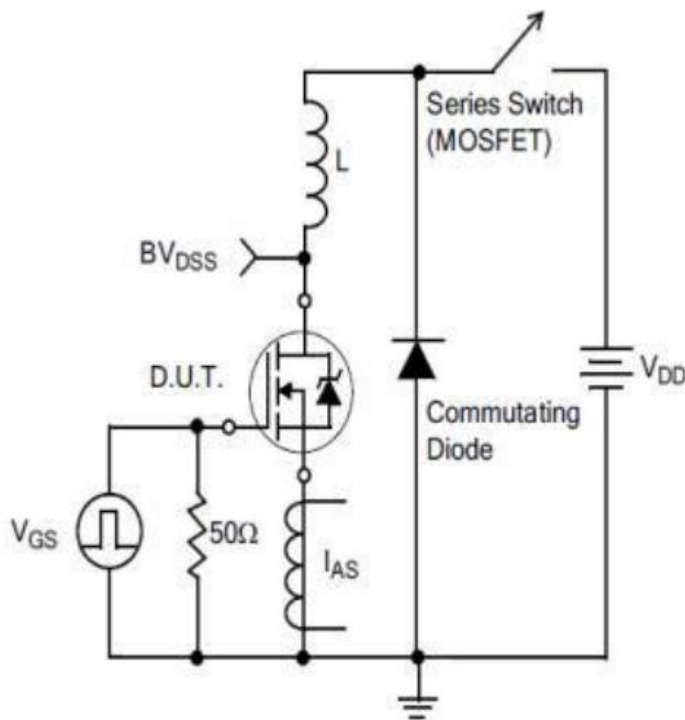
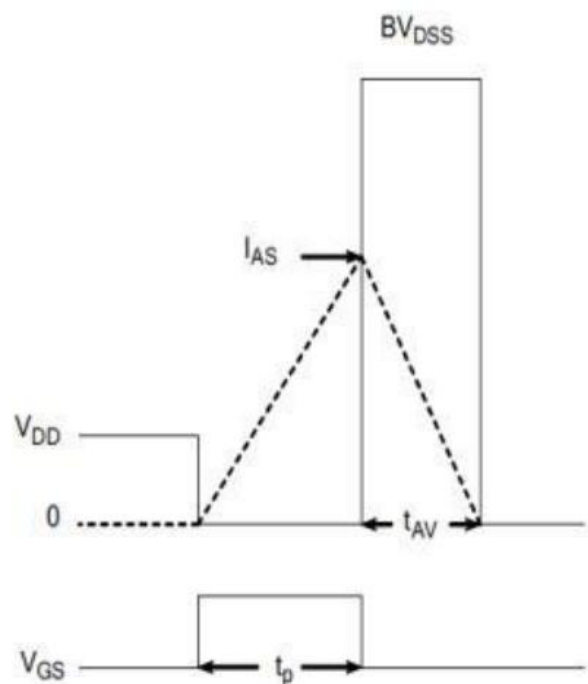


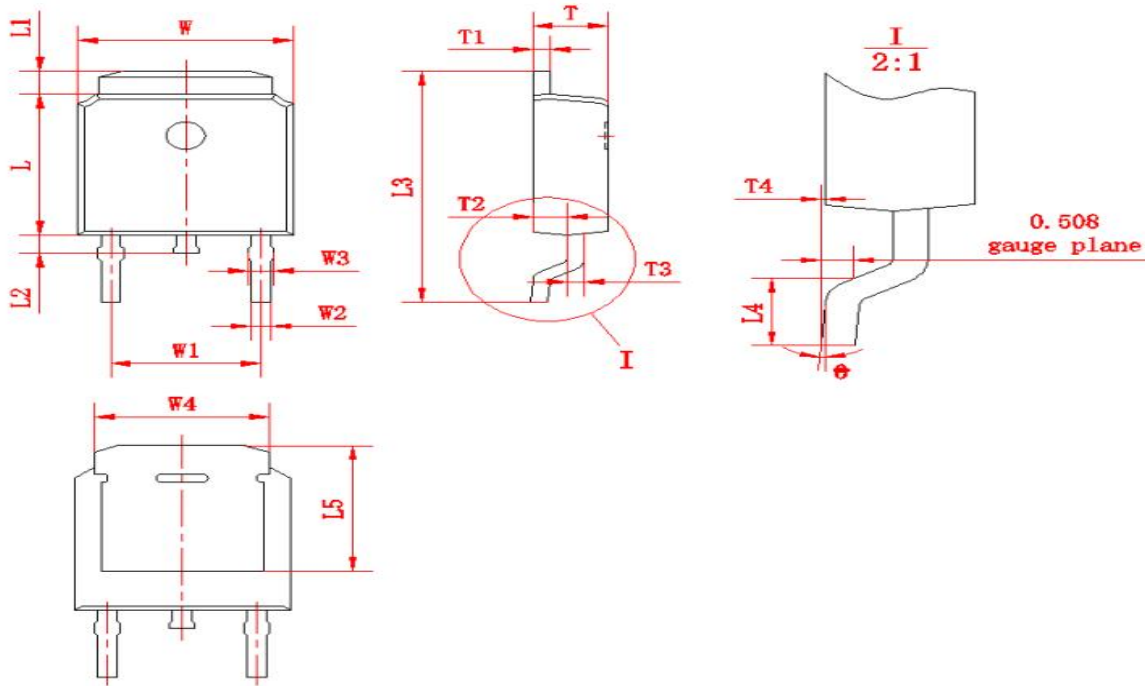
Figure G. Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure H. Unclamped Inductive Switching Waveforms

Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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