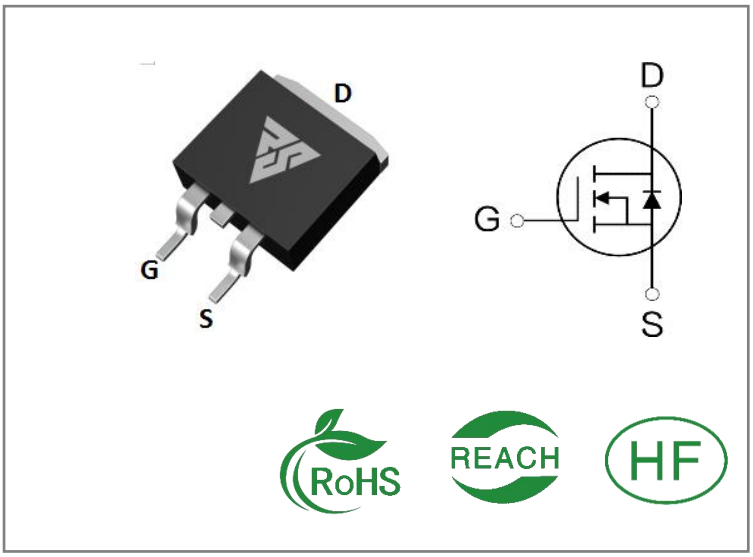
ID	R_{DS}(ON)(Typ)	VDSS
190A	2.2mΩ	100V



Applications:
- Load Switch
- PWM Applications
- Power Managment

Features:
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS100N190S	T0-263	RS100N190S	Tape&reel	800 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS100N190S	Units
VDSS	Drain-to-Source Voltage	100	V
ID	Continuous Drain Current TC=25℃	190	A
ID	Continuous Drain Current TC=100℃	122	
IDM	Pulsed Drain Current	760	
PD	Power Dissipation	272	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH,IS = 42A, RG = 25Ω, Tj = 25℃	418	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature
Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS100N190S	Units	Test Conditions
RθJC	Junction-to-Case	0.46	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	55		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	100	--	--	V	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=80V,VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V ,VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	2.2	2.8	mΩ	VGS=10V,ID=30A
VGS(TH)	Gate Threshold Voltage	2.0	--	4.0	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	33	--	nS	VDS=50V ID=50A RG=3Ω VGS=10V
trise	Rise Time	--	28	--		
td(OFF)	Turn- OFF Delay Time	--	102	--		
tfall	Fall Time	--	36	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	13183	--	pF	VGS= 0V VDS=40V f=1MHz
Coss	Output Capacitance	--	3674	--		
Crss	Reverse Transfer Capacitance	--	2746	--		
Qg	Total Gate Charge	--	112	--	nC	VDS= 50V ID=50A VGS=10V
Qgs	Gate- to- Source Charge	--	31	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	26	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	190	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	760	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=20A,VGS=0V
trr	Reverse Recovery Time	--	89	--	nS	VGS=0V IS=20A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	178	--	nC	

Notes:

* 1. Repetitive rating,pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature Curve

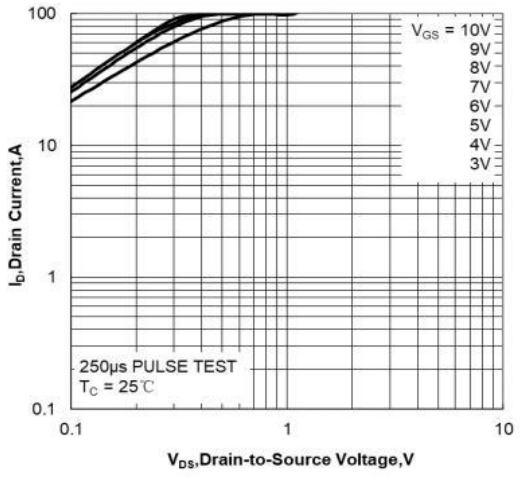


Figure 1. Output Characteristics

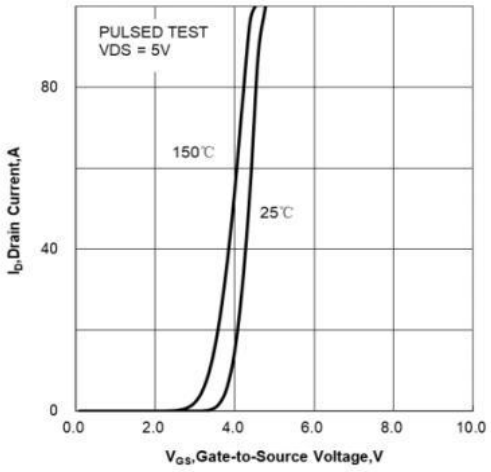


Figure 2. Transfer Characteristics

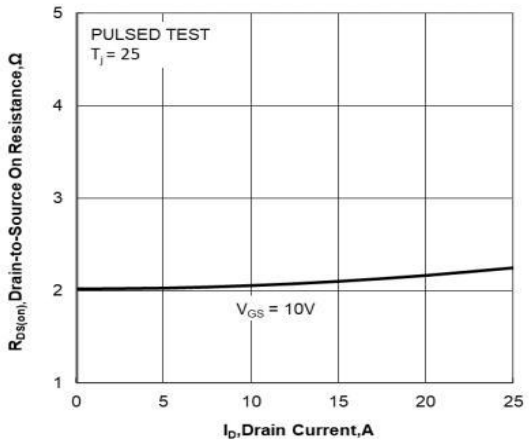


Figure 3. Drain-to-Source On Resistance vs Drain Current

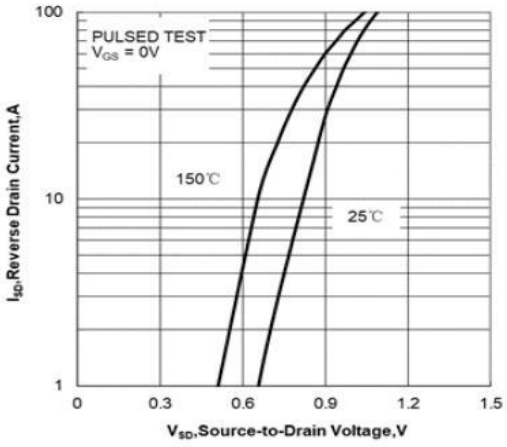


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

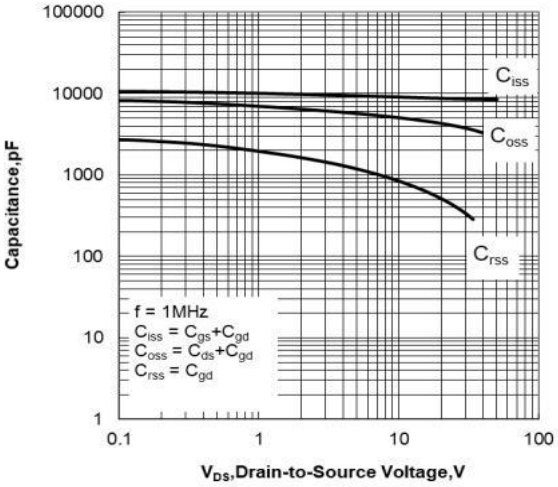


Figure 5. Capacitance Characteristics

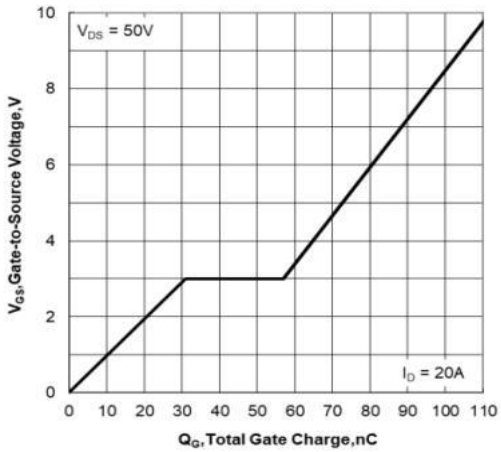


Figure 6. Gate Charge Characteristics

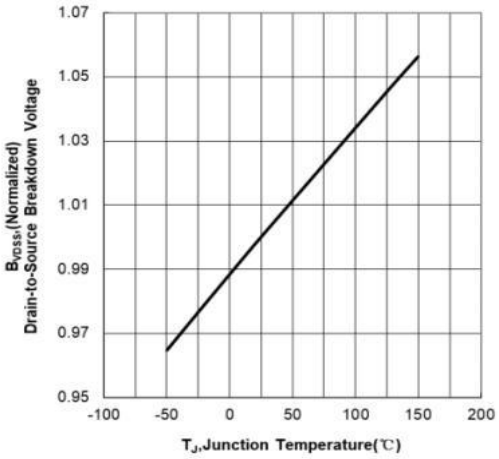


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

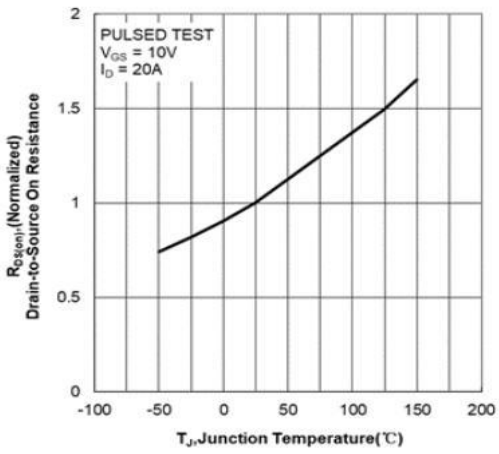


Figure 8. Normalized On Resistance vs Junction Temperature

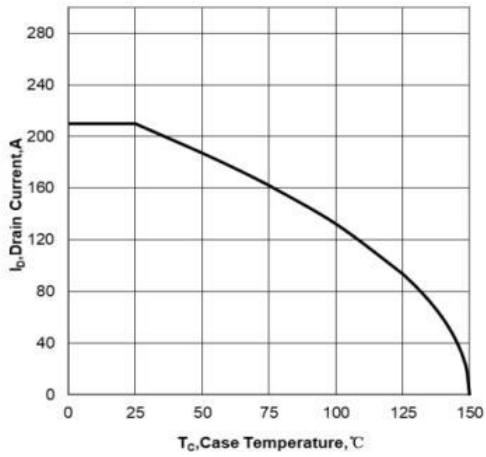


Figure 9. Maximum Continuous Drain Current vs Case Temperature

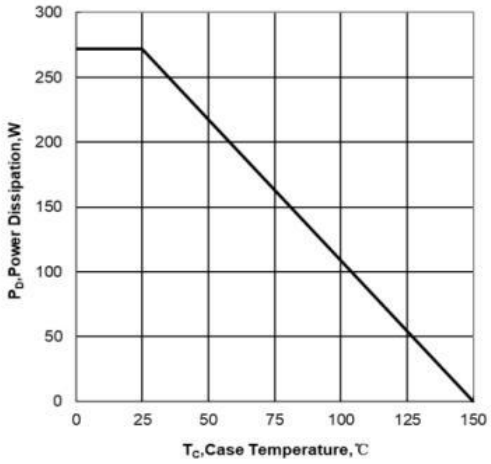


Figure 10. Maximum Power Dissipation vs Case Temperature

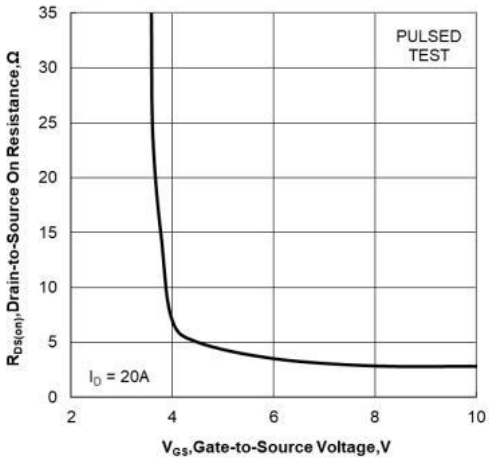


Figure11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

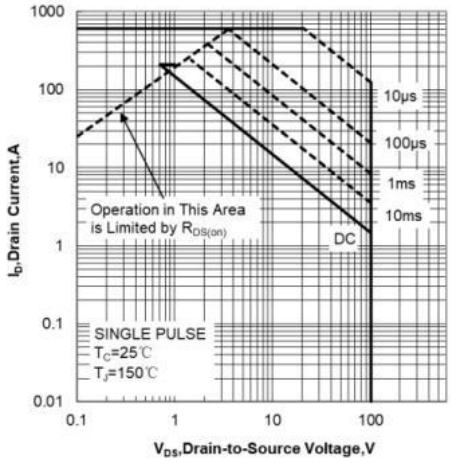


Figure 12. Maximum Safe Operating Area

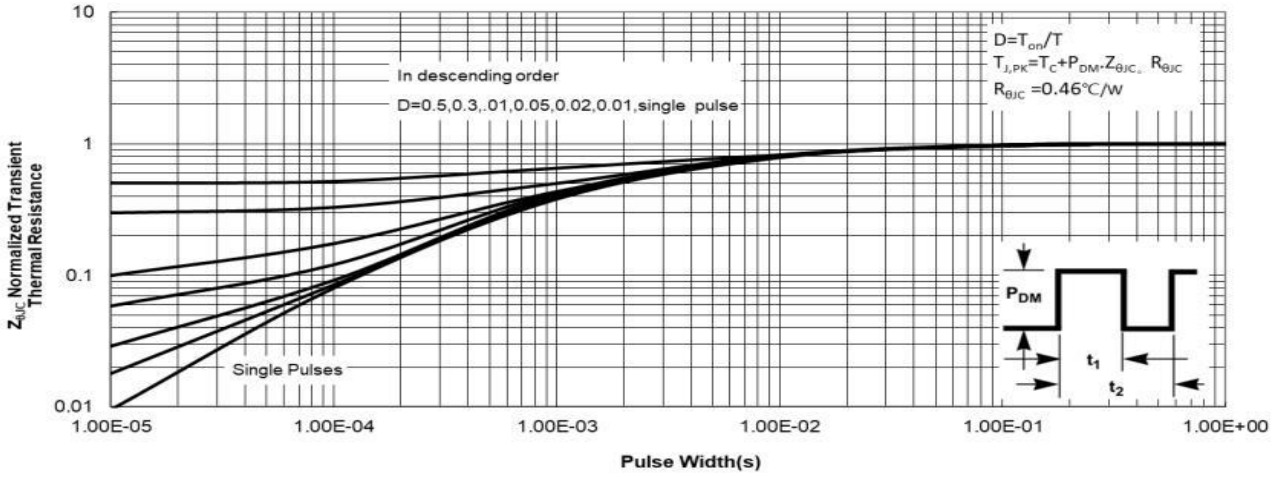


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test ircuits and Waveforms

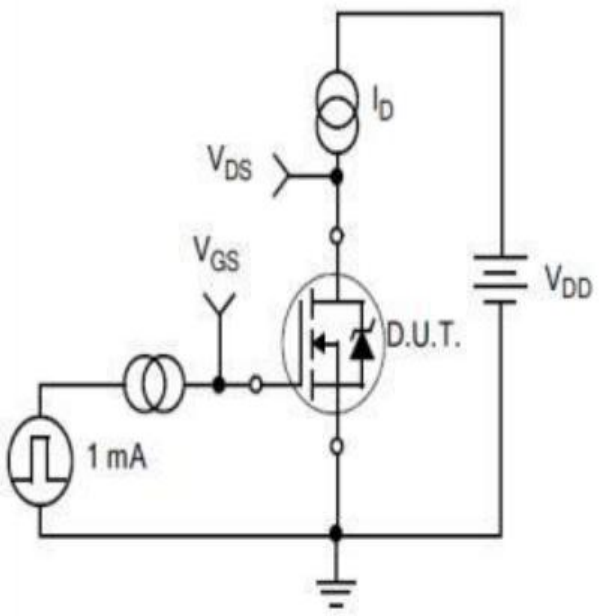


Figure A.
Gate Charge Test Circuit

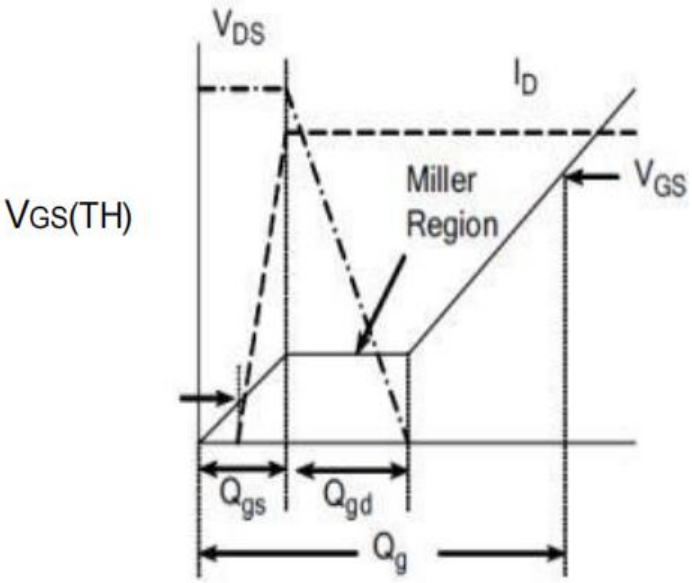


Figure B.
Gate Charge Waveform

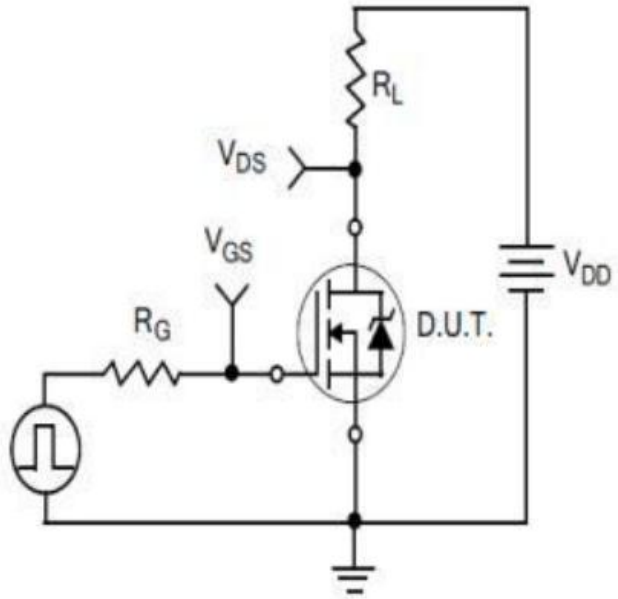


Figure C.
Resistive Switching Test Circuit

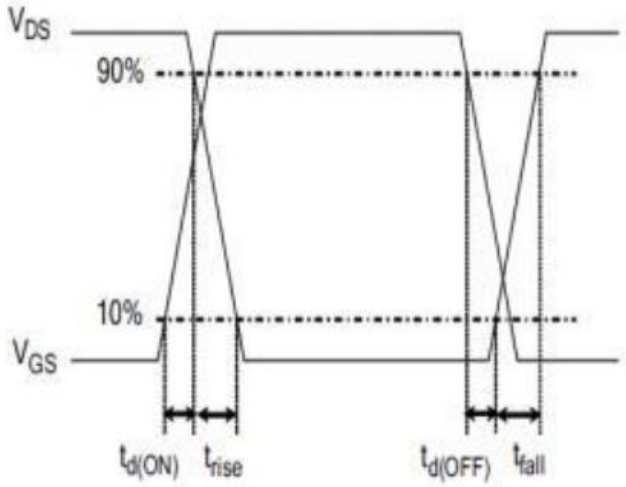


Figure D.
Resistive Switching Waveforms

Test ircuits and Waveforms

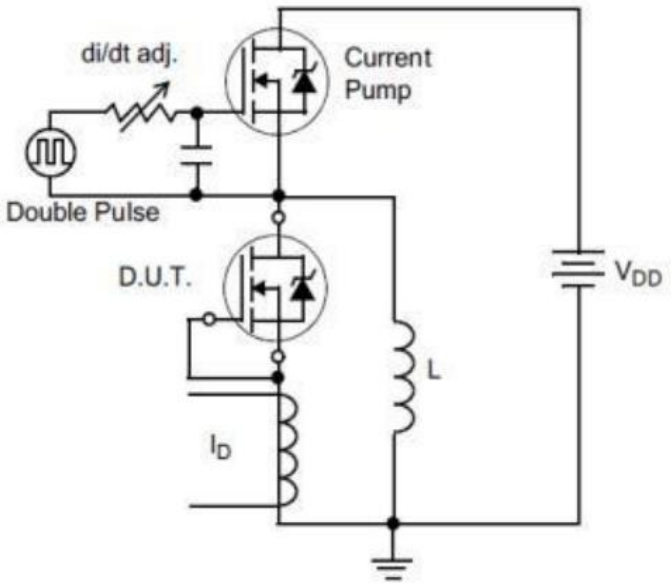


Figure E.Diode Reverse Recovery Test Circuit

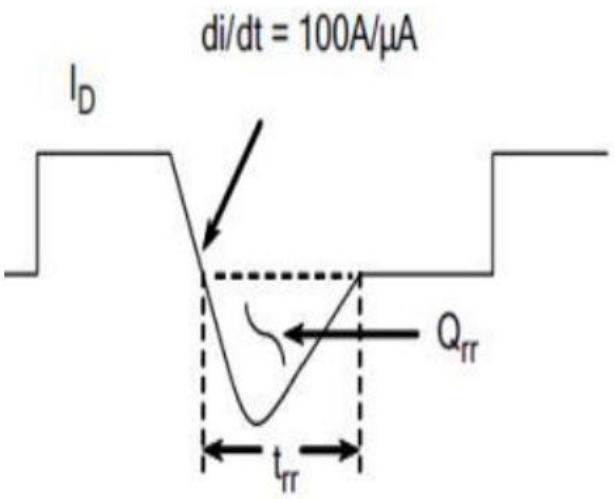


Figure F.Diode Reverse Recovery Waveform

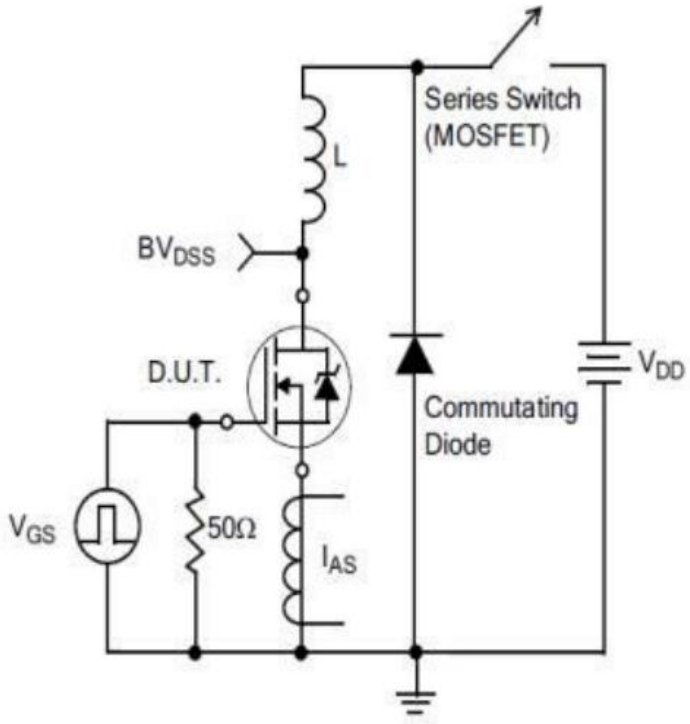
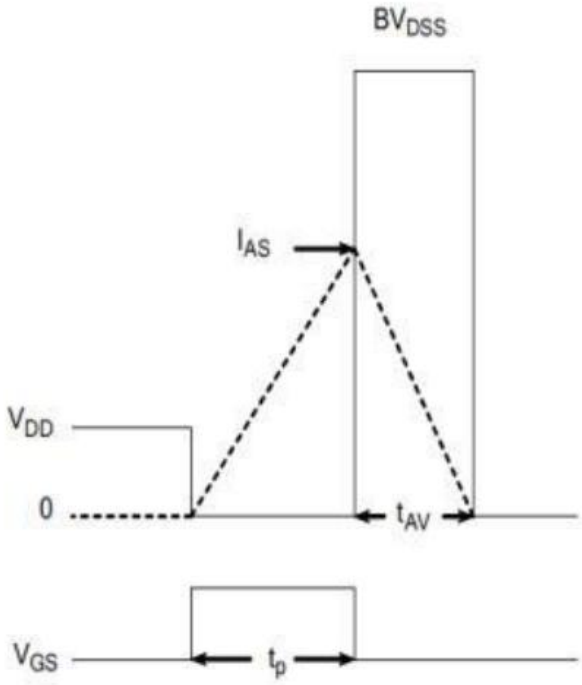


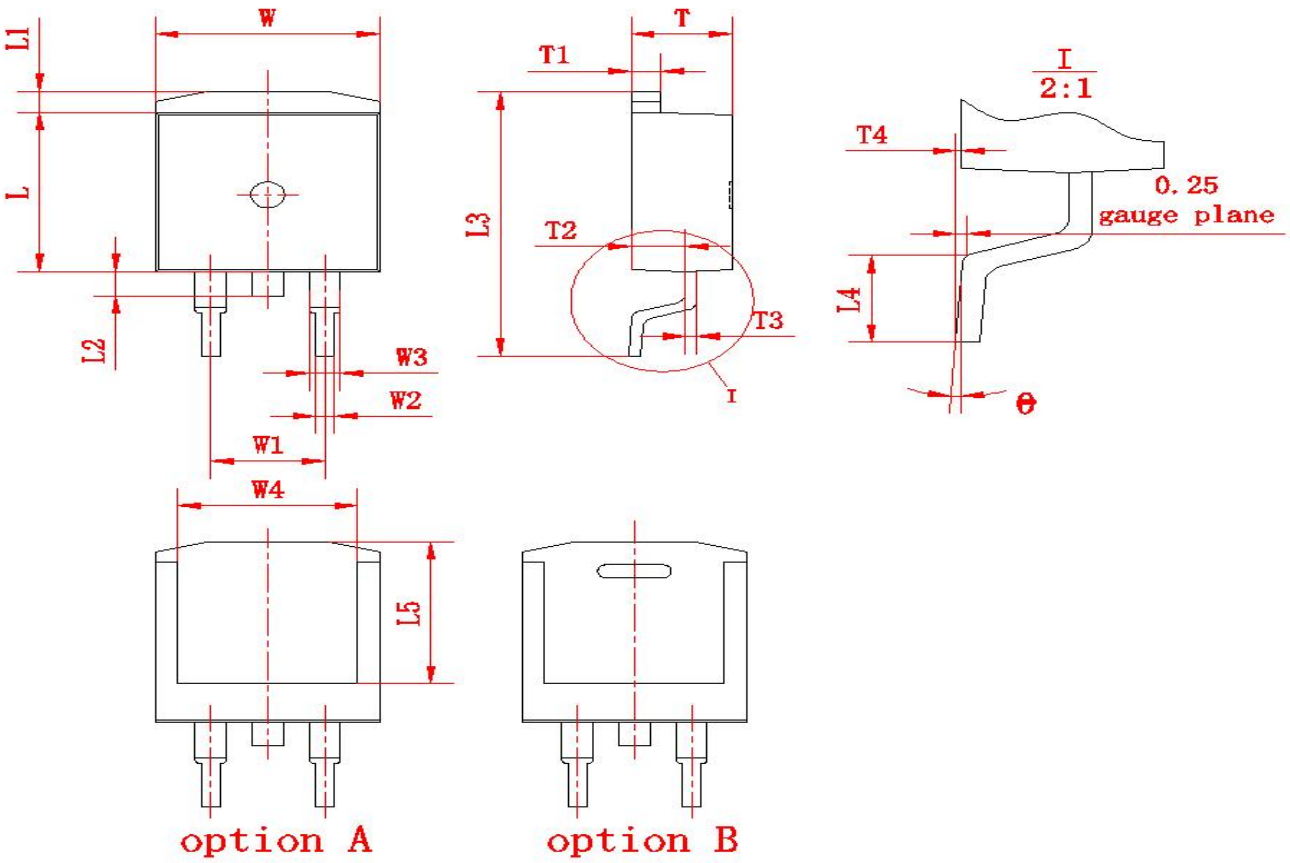
Figure G.Unclamped Inductive Switching Test Circuit



$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure H.Unclamped Inductive Switching Waveforms

Package outline drawing(TO-263 Unit: mm)



（单位：mm）

符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	9.80	10.20	L1	1.00	1.40	T1	1.20	1.40
W1	(5.08)		L2	1.20	1.60	T2	2.20	2.60
W2	0.70	0.95	L3	15.00	15.60	T3	0.45	0.65
W3	1.17	1.62	L4	2.20	2.80	T4	0	0.25
W4	(8.0)		L5	(8.2)		θ	0°	8°
L	9.00	9.40	T	4.30	4.70			

Disclaimers:

Reasunos Semiconductor Technology Co.Ltd (Reasunos) reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of orderacknowledgement.

Reasunos Semiconductor Technology Co.Ltd warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr- actual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology Co.Ltd does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology Co.Ltd does not warrant or convey any license eith- er expressed or implied under its patent rights,nor the rights of others.Reproduction of inform- ation in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology Co.Ltd for that product or service voids all exp- ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology Co.Ltd is not responsi- ble or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology Co.Ltd's Products are not authorized for use as cri- tical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology Co.Ltd.
As used herein:
1. Life support devices or systems are devices or systems which: a.are intended for surgical implant into the human body, b.support or sustain life,
c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.

单击下面可查看定价，库存，交付和生命周期等信息

>>REASUNOS(瑞森)