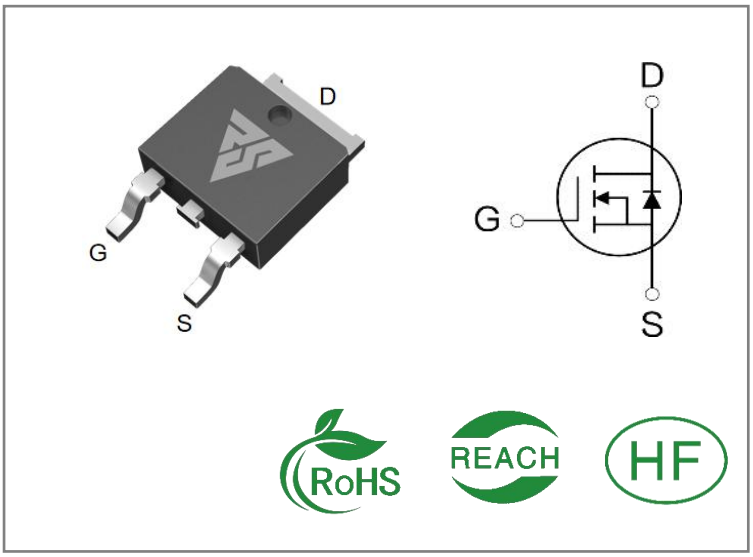
ID	R_{DS}(ON)(Typ)	VDSS
150A	3.0mΩ	30V



Applications:
- Load Switch
- PWM Applications
- Power Managment

Features:
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS30N150D	T0-252	RS30N150D	Tape&reel	2500 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS30N150D	Units
VDSS	Drain-to-Source Voltage	30	V
ID	Continuous Drain Current TC=25℃	150	A
ID	Continuous Drain Current TC=100℃	100	
IDM	Pulsed Drain Current	500	
PD	Power Dissipation	120	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH,VDD = 55V, RG = 25Ω, Tj = 25℃	350	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature
Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS30N150D	Units	Test Conditions
RθJC	Junction-to-Case	1.04	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	20		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	30	--	--	V	VGS=0V,ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=30V,VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V ,VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V ,VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	3.0	4.0	mΩ	VGS=10V,ID=30A
		--	4.0	6.0	mΩ	VGS=4.5V,ID=20A
VGS(TH)	Gate Threshold Voltage	1.0	--	2.0	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	11	--	nS	VDS=20V ID=20A RG=3Ω VGS=10V
trise	Rise Time	--	10	--		
td(OFF)	Turn- OFF Delay Time	--	35	--		
tfall	Fall Time	--	9	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	4000	--	pF	VGS= 0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	450	--		
Crss	Reverse Transfer Capacitance	--	430	--		
Qg	Total Gate Charge	--	75	--	nC	VDS= 15V ID=20A VGS=10V
Qgs	Gate- to- Source Charge	--	9	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	18	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	150	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	500	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=20A,VGS=0V
trr	Reverse Recovery Time	--	26	--	nS	VGS=0V IS=20A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	34	--	nC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature Curve

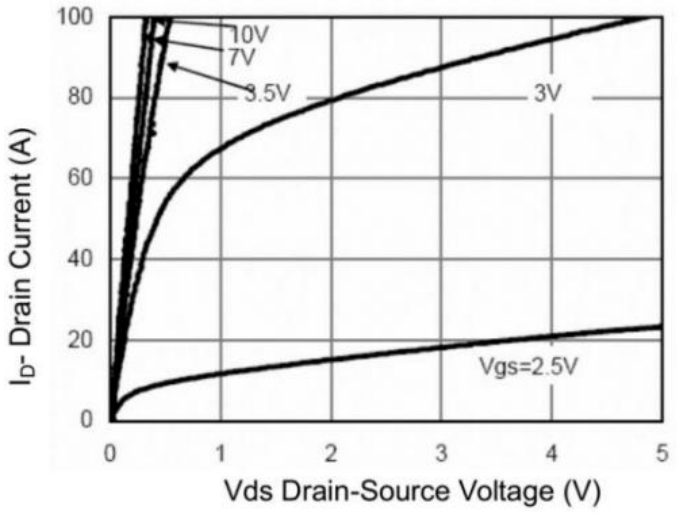


Figure 1 Output Characteristics

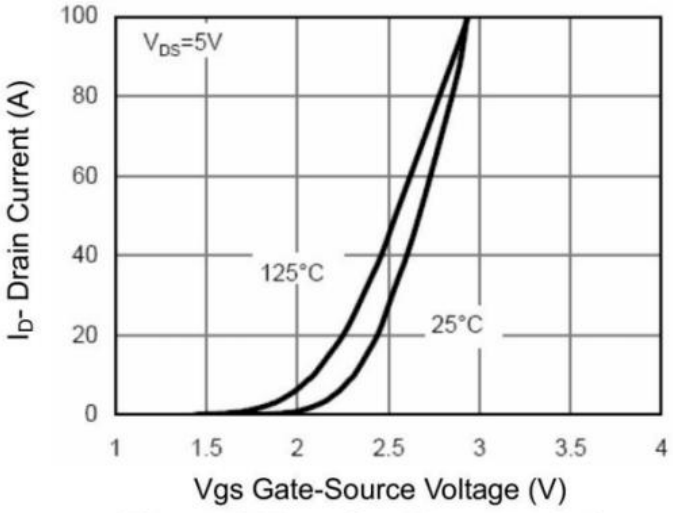


Figure 2 Transfer Characteristics

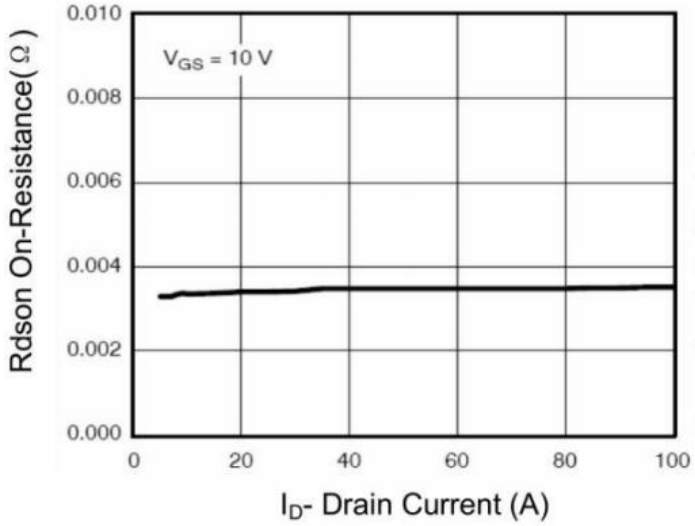


Figure 3 Rdson- Drain Current

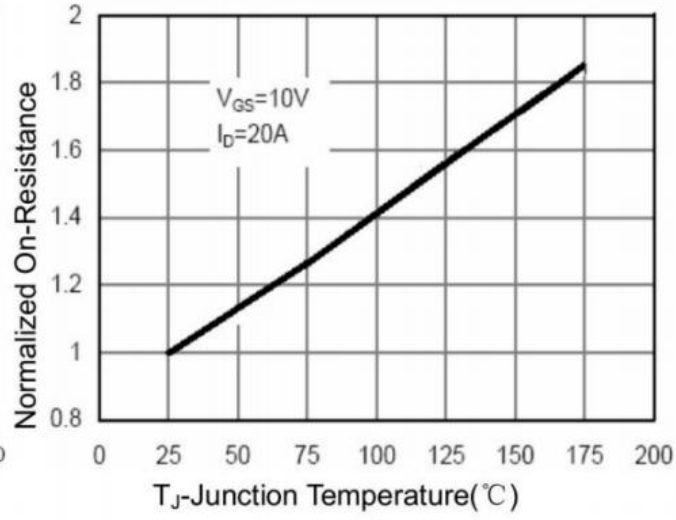


Figure 4 Rdson-Junction Temperature

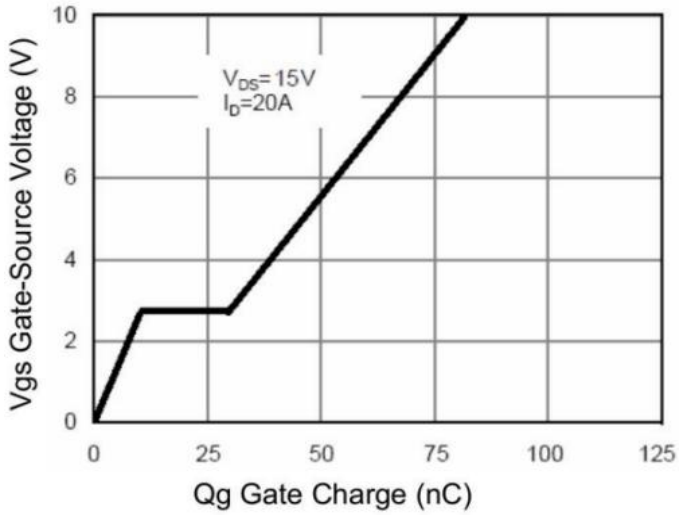


Figure 5 Gate Charge

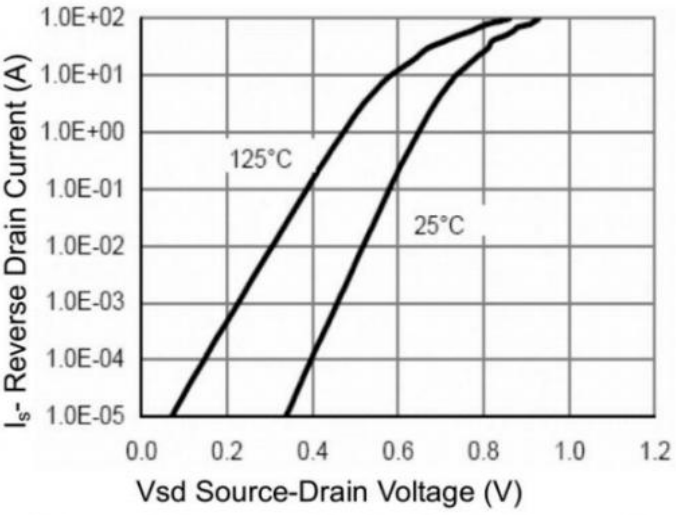


Figure 6 Source- Drain Diode Forward

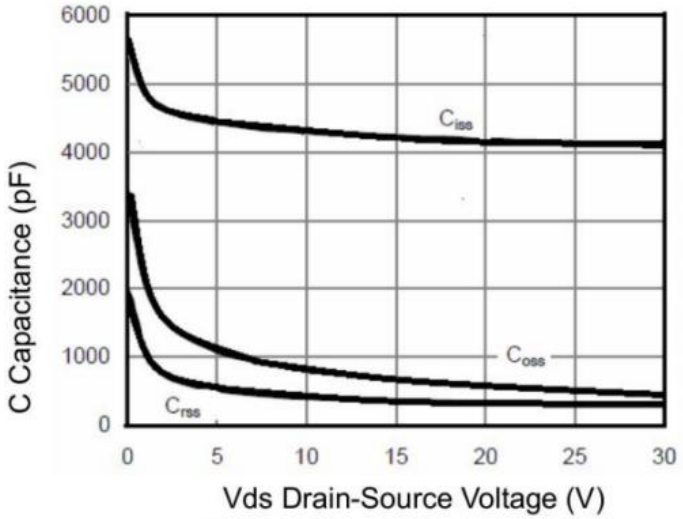


Figure 7 Capacitance vs Vds

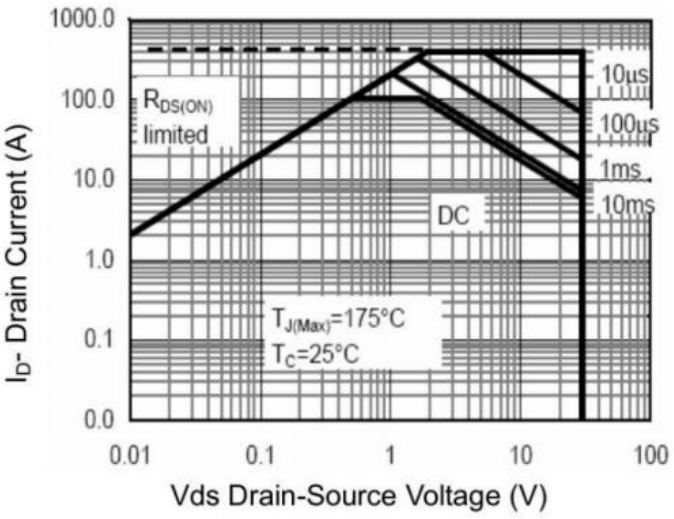


Figure 8 Safe Operation Area

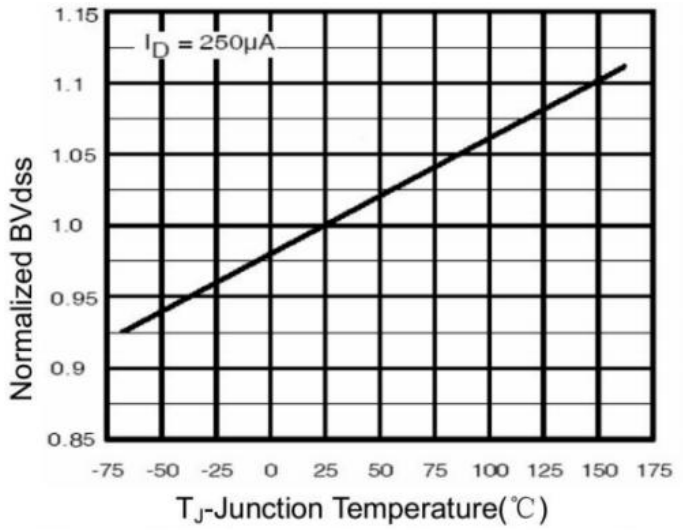


Figure 9 BV_{DSS} vs Junction Temperature

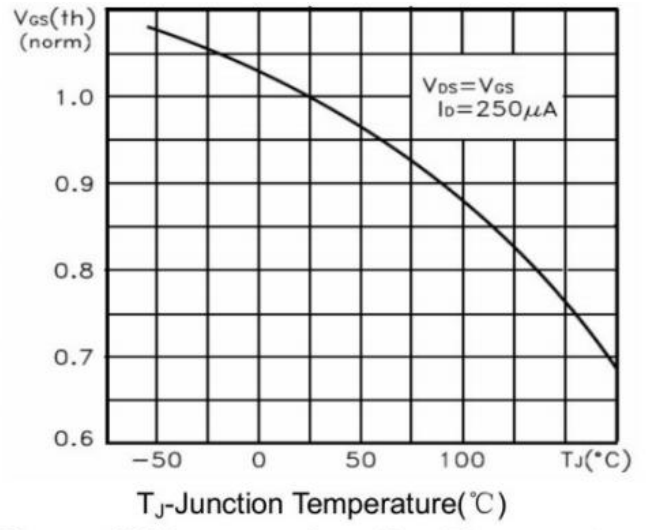


Figure 10 $V_{GS(th)}$ vs Junction Temperature

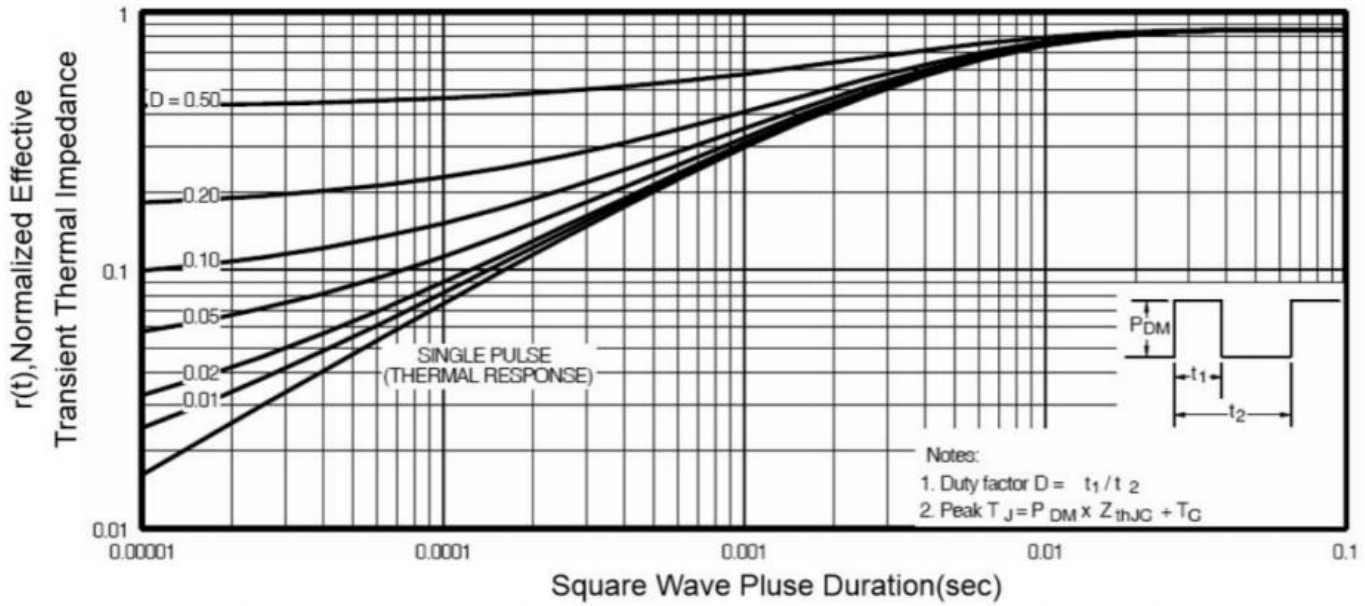


Figure 11 Normalized Maximum Transient Thermal Impedance

Test ircuits and Waveforms

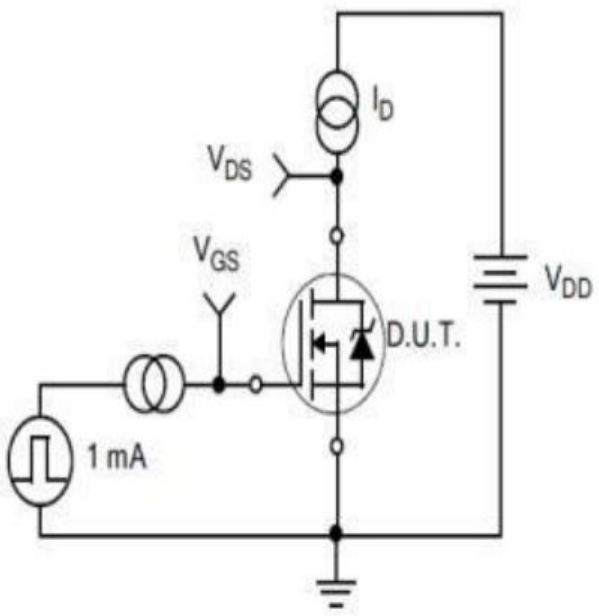


Figure A.
Gate Charge Test Circuit

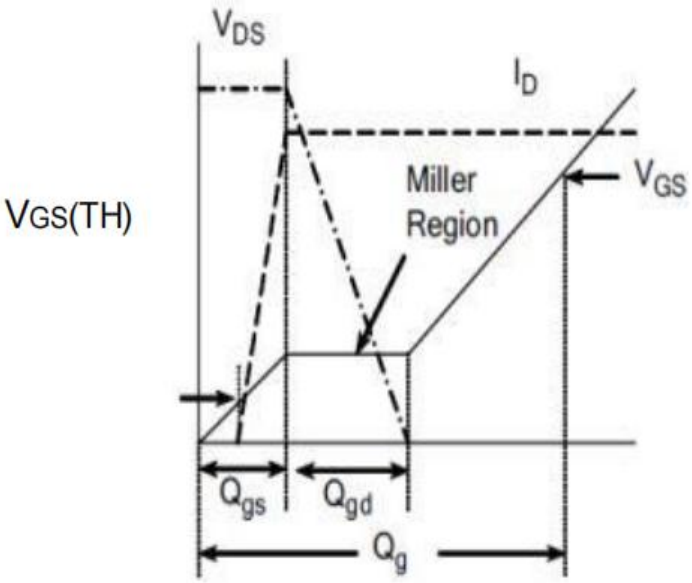


Figure B.
Gate Charge Waveform

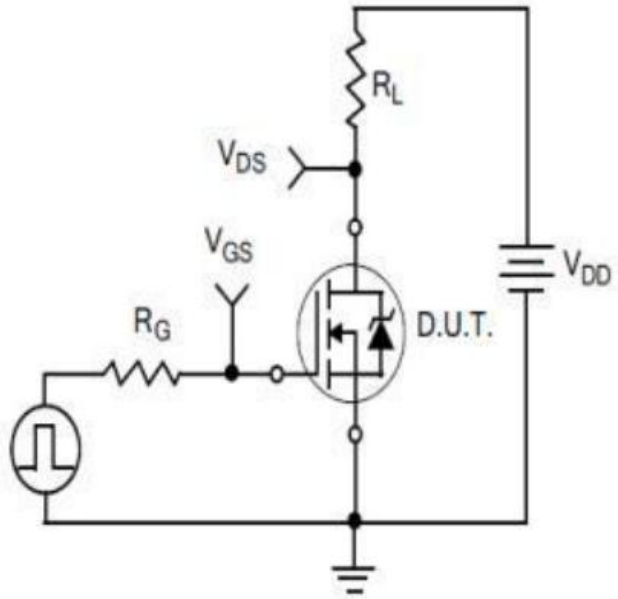


Figure C.
Resistive Switching Test Circuit

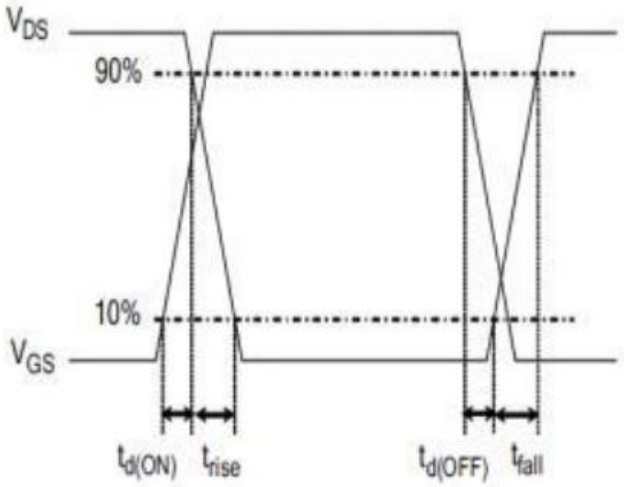


Figure D.
Resistive Switching Waveforms

Test ircuits and Waveforms

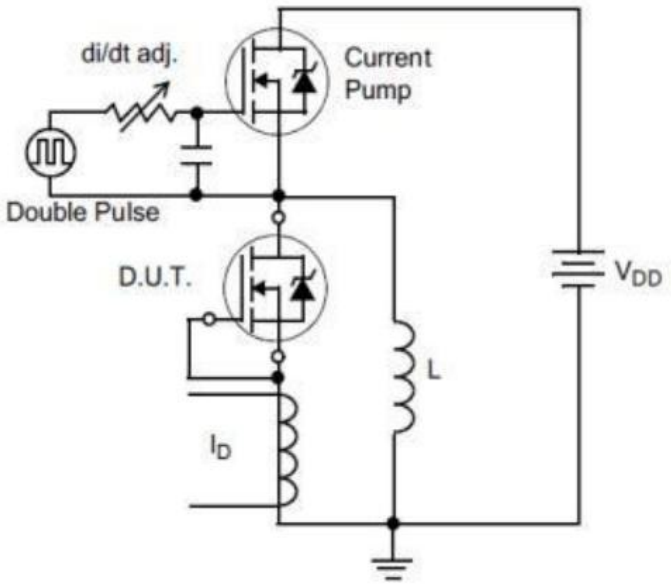


Figure E.Diode Reverse Recovery Test Circuit

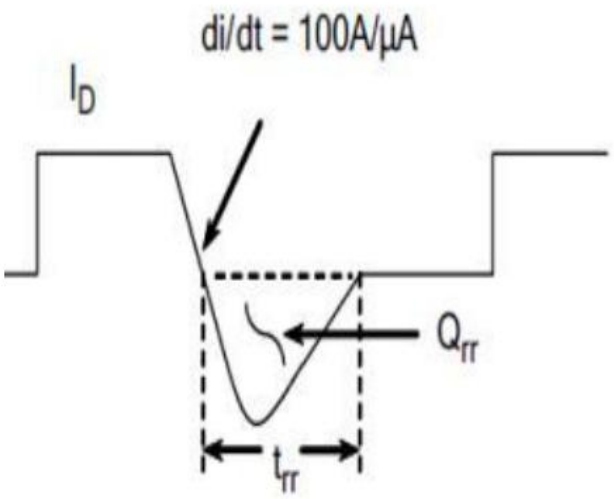


Figure F.Diode Reverse Recovery Waveform

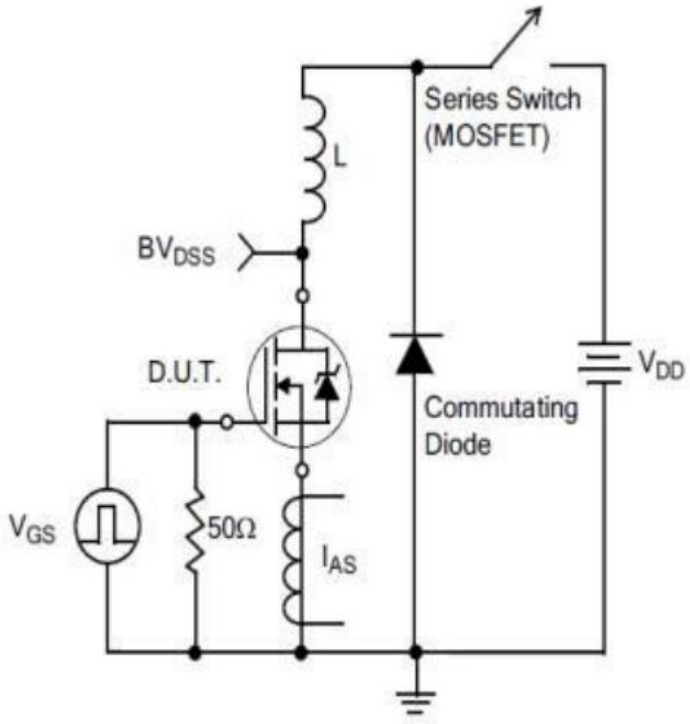
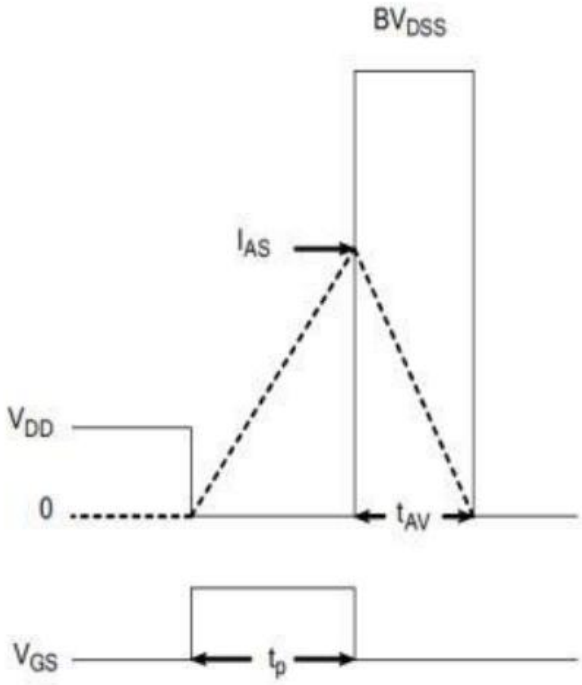


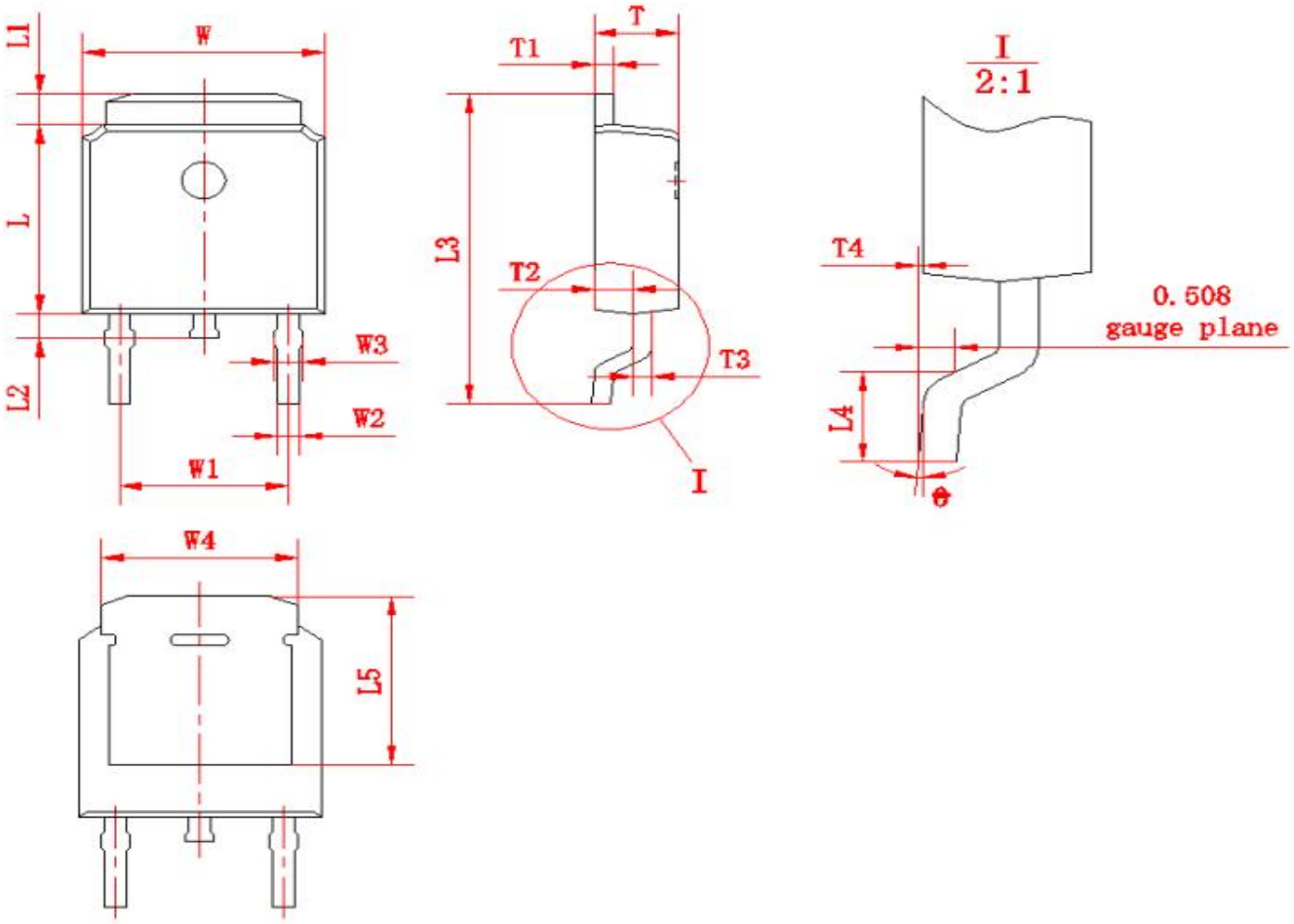
Figure G.Unclamped Inductive Switching Test Circuit



$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure H.Unclamped Inductive Switching Waveforms

Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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