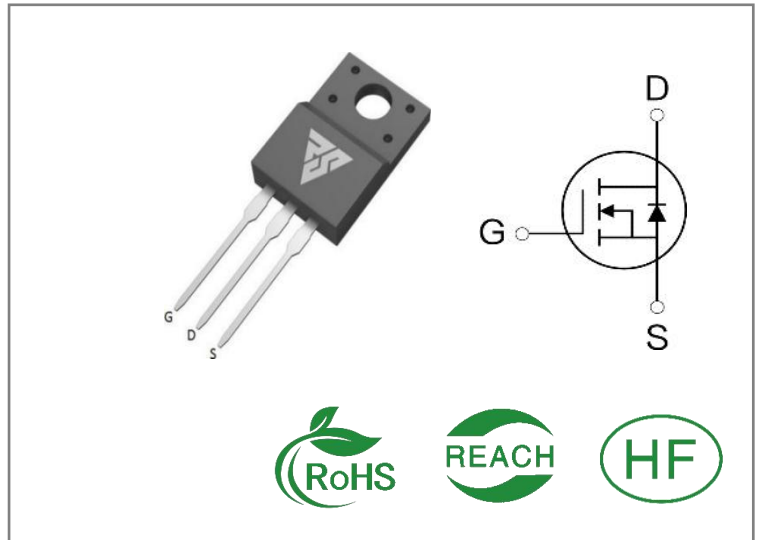


ID	R <sub>DS(ON)</sub> (Typ)	VDSS
4A	3Ω	900V


**Applications:**

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

**Features:**

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

**Ordering Information**

Part Number	Package	Marking	Packing	Qty.
RS4N90F	T0-220F	RS4N90F	Tube	50 PCS

**Absolute Maximum Ratings** T<sub>c</sub>= 25°C unless otherwise specified

Symbol	Parameter	RS4N90F	Units
VDSS	Drain-to-Source Voltage	900	V
ID	Continuous Drain Current T <sub>C</sub> =25°C	4	A
IDM	Pulsed Drain Current (Note*1)	16	
PD	Power Dissipation	70	W
VGS	Gate- to- Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy L = 10mH, VDD = 50V, R <sub>G</sub> = 25 Ω	125	mJ
TL TPKG	Maximum Temperature for Soldering	300	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

\* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.

**Thermal Resistance**

Symbol	Parameter	RS4N90F	Units	Test Conditions
R $\theta$ JC	Junction-to-Case	1.78	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 °C
R $\theta$ JA	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.

**OFF Characteristics** T<sub>J</sub>= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	900	--	--	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	V <sub>D</sub> S=900V, V <sub>GS</sub> =0 V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	V <sub>GS</sub> =30V , V <sub>D</sub> S=0V
	Gate- to- Source Reverse Leakage	--	--	-100		V <sub>GS</sub> =-30V , V <sub>D</sub> S=0 V

**ON Characteristics** T<sub>J</sub>=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R <sub>DS(on)</sub>	Static Drain- to- Source On-Resistance(Note*2)	--	3	3.5	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =2A
V <sub>GS(TH)</sub>	Gate Threshold Voltage	3	--	4	V	V <sub>GS</sub> =V <sub>D</sub> S, I <sub>D</sub> =250μA

**Resistive Switching Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t <sub>d(ON)</sub>	Turn- on Delay Time	--	37	--	nS	V <sub>D</sub> S=450V I <sub>D</sub> =4A R <sub>G</sub> =25Ω
t <sub>rise</sub>	Rise Time	--	15	--		
t <sub>d(OFF)</sub>	Turn- OFF Delay Time	--	144	--		
t <sub>fall</sub>	Fall Time	--	36	--		

**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	674	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	71	--		
Crss	Reverse Transfer Capacitance	--	13	--		
Qg	Total Gate Charge	--	27	--	nC	VDS=720V ID=4A VGS=10V
Qgs	Gate- to- Source Charge	--	3.5	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	14	--		

**Source- Drain Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	4	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	16	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=2A,VGS=0V
trr	Reverse Recovery Time	--	1018	--	nS	VGS=0V IS=4A,di/dt=100A/ μs
Qrr	Reverse Recovery Charge	--	2.2	--	μC	

**Notes:**

- \* 1. Repetitive rating, pulse width limited by maximum junction temperature.
- \* 2. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 1\%$

Typical Feature Curve

Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )

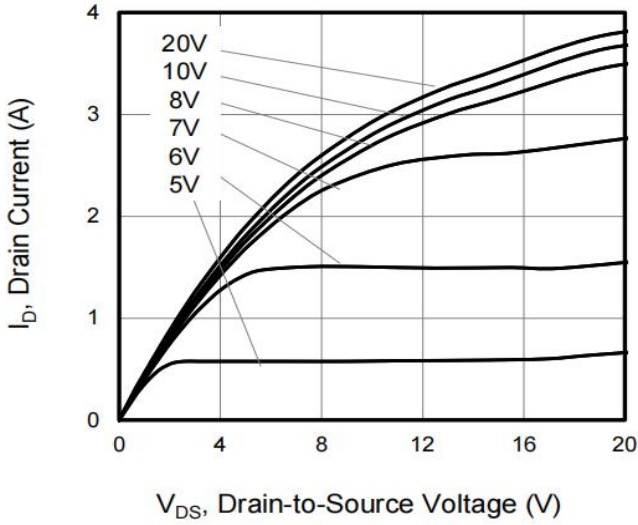


Figure 2. Body Diode Forward Voltage

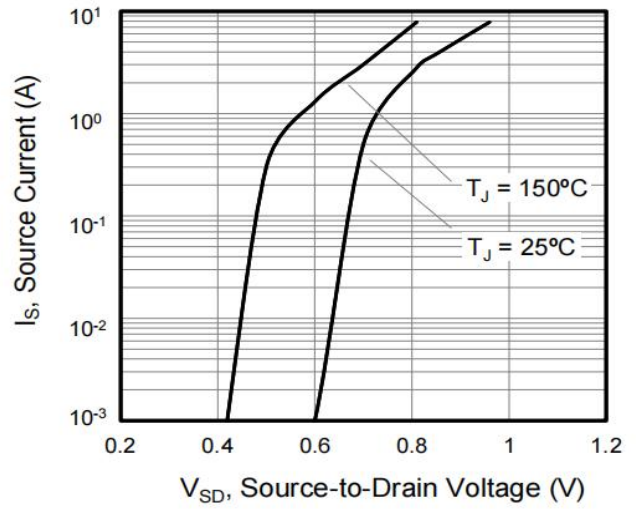


Figure 3. Drain Current vs. Temperature

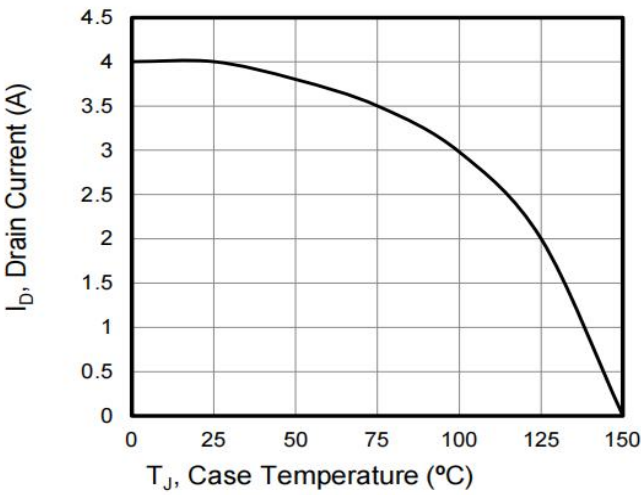


Figure 4.  $BV_{DSS}$  Variation vs. Temperature

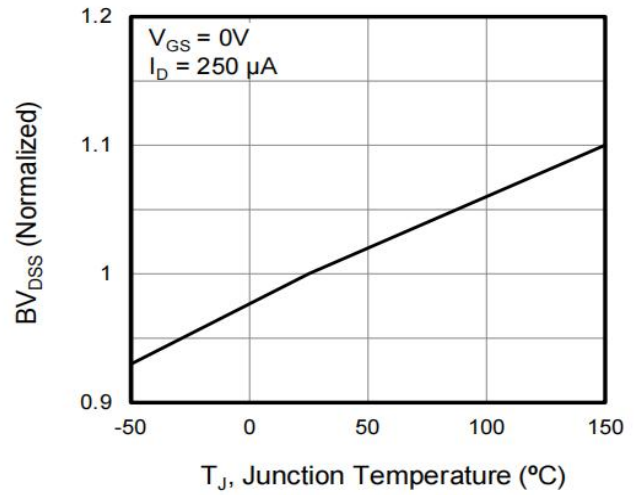


Figure 5. Transfer Characteristics

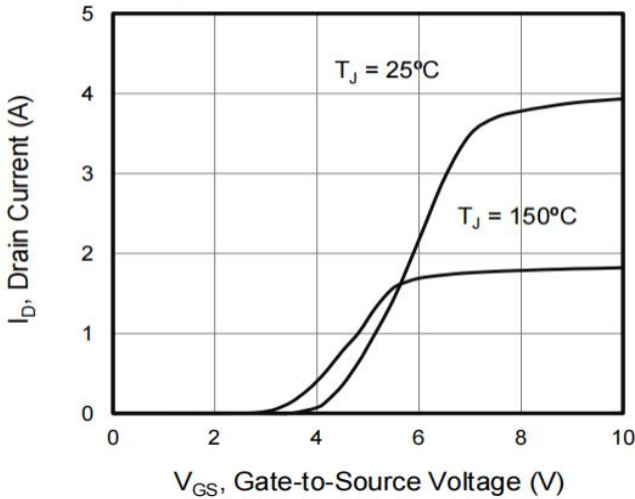


Figure 6. On-Resistance vs. Temperature

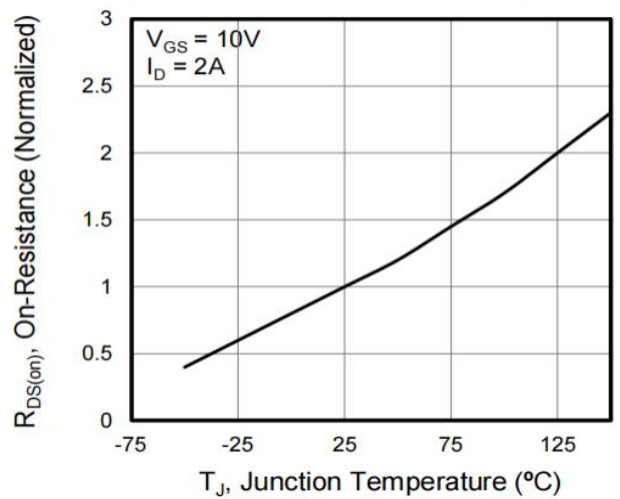


Figure 7. Capacitance

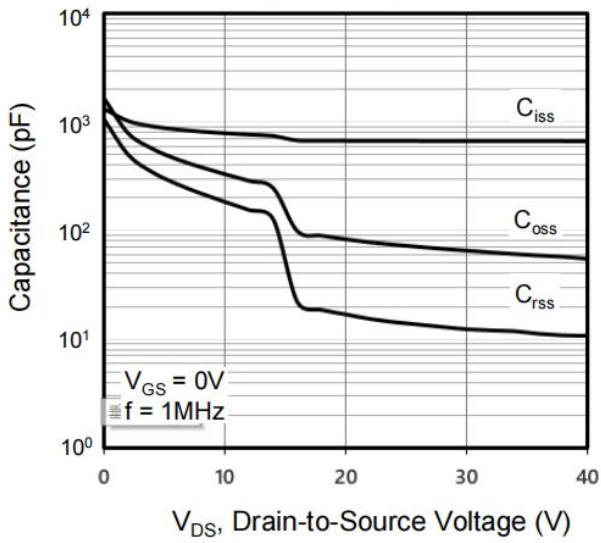


Figure 8. Gate Charge

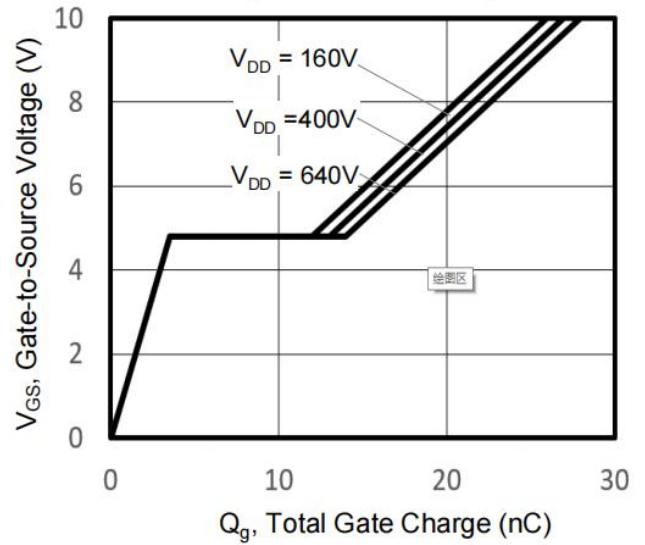
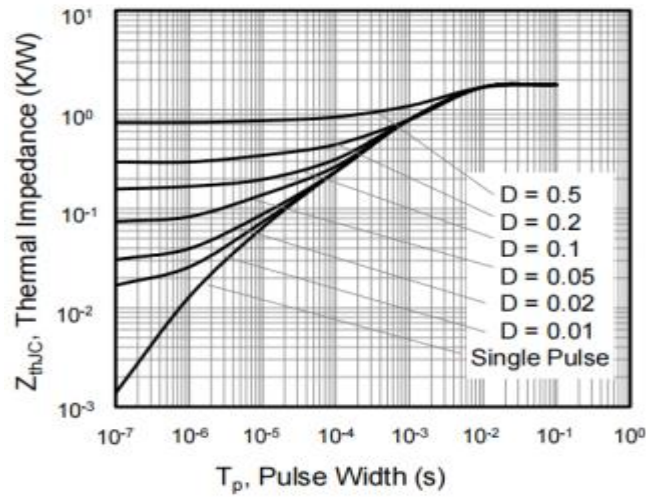


Figure 9. Transient Thermal Impedance



Test Circuits and Waveforms

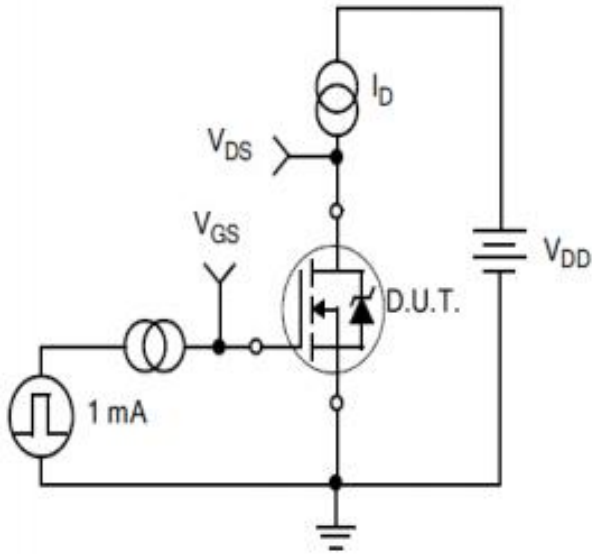


Figure10.  
Gate Charge Test Circuit

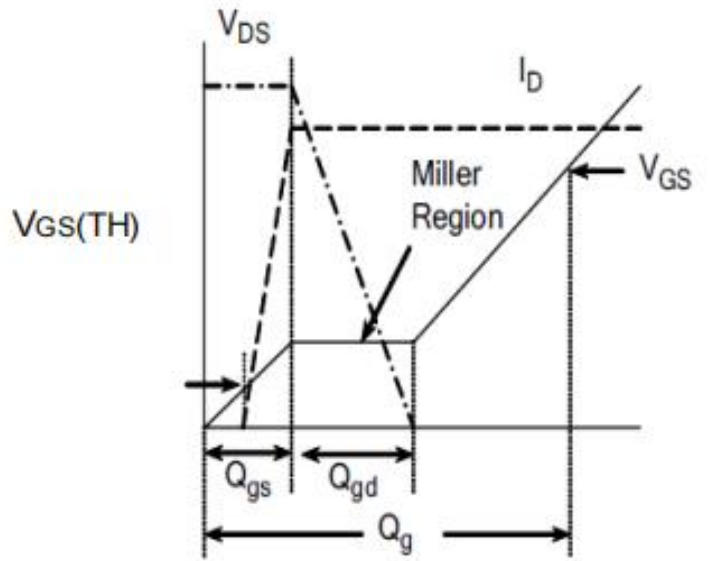


Figure11.  
Gate Charge Waveform

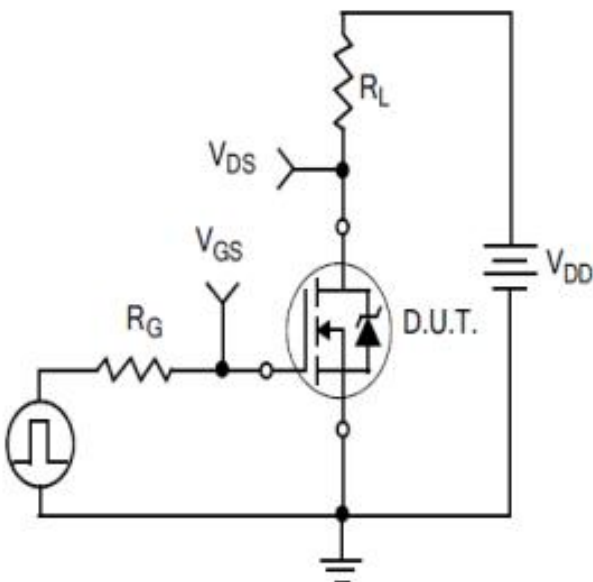


Figure12.  
Resistive Switching Test Circuit

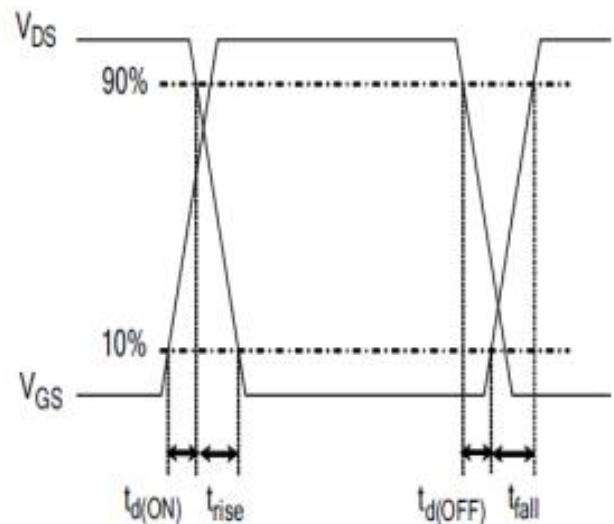
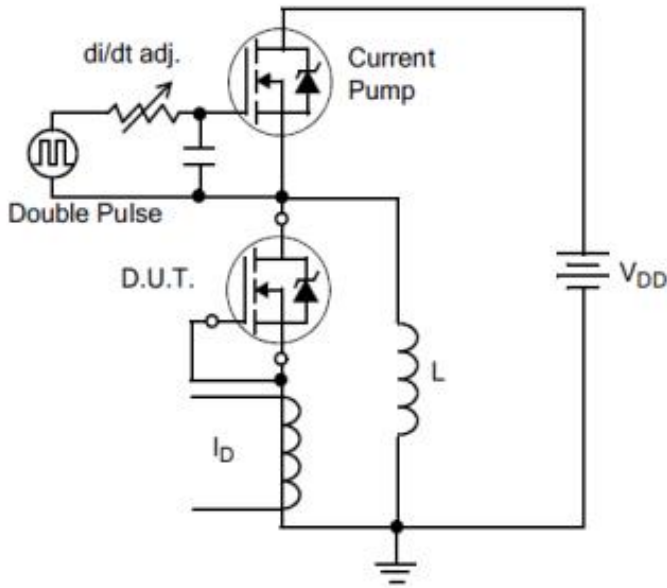
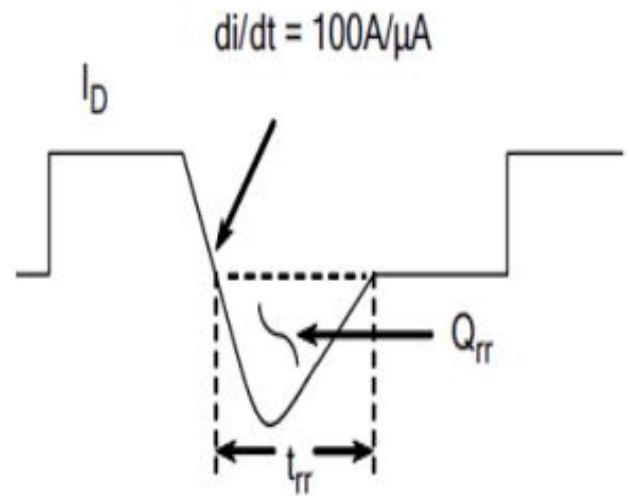


Figure13.  
Resistive Switching Waveforms

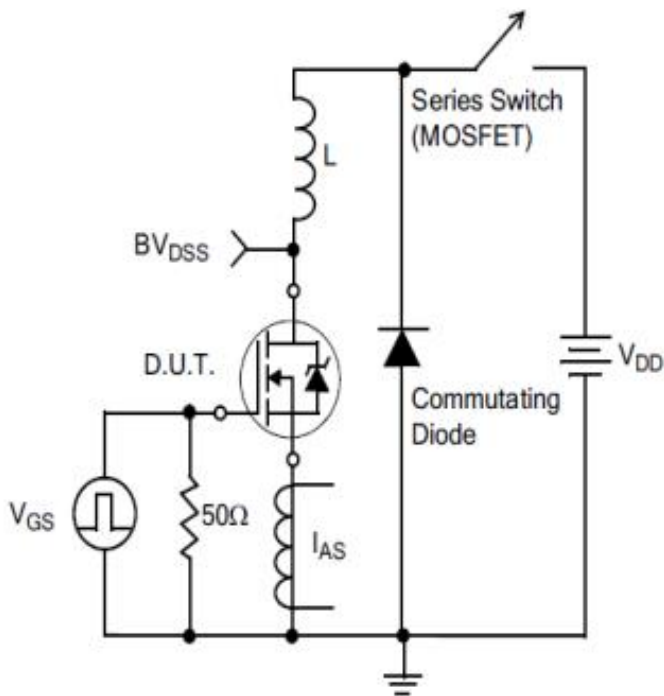
**Test Circuits and Waveforms**



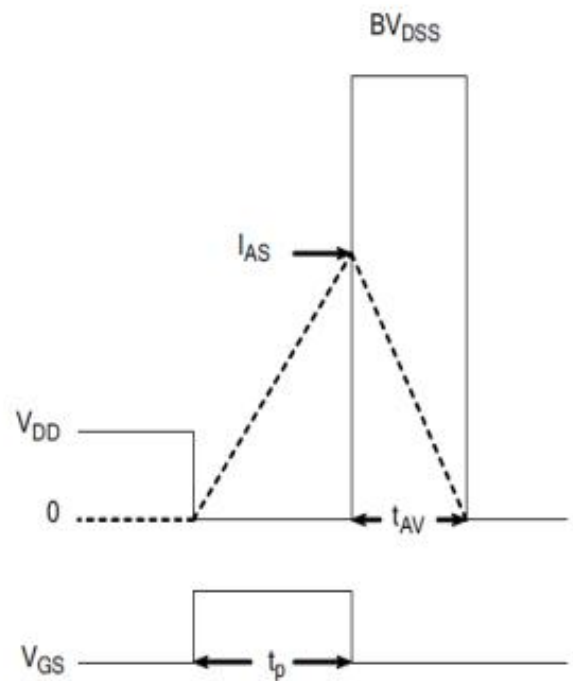
**Figure 14. Diode Reverse Recovery Test Circuit**



**Figure 15. Diode Reverse Recovery Waveform**



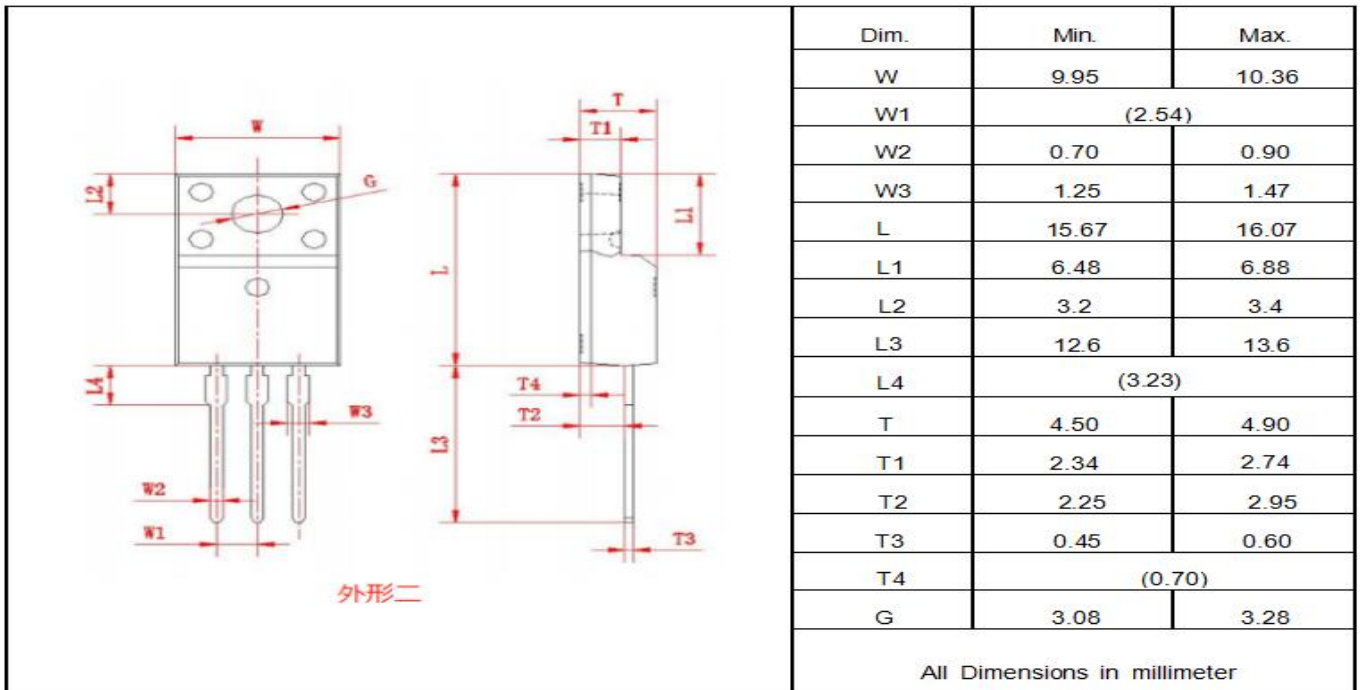
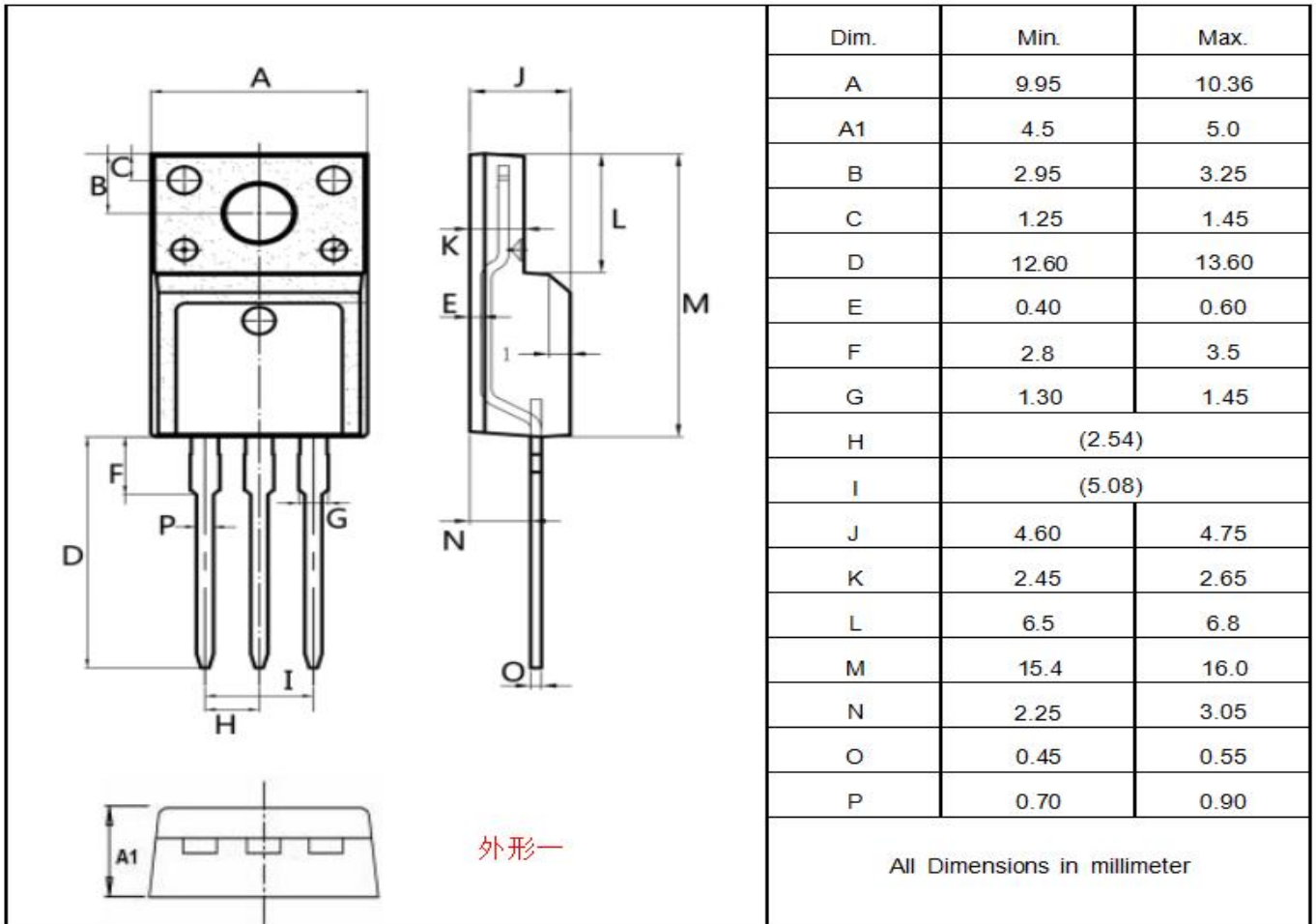
**Figure 16. Unclamped Inductive Switching Test Circuit**



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

**Figure 17. Unclamped Inductive Switching Waveforms**

Package outline drawing (TO-220F Unit: mm)





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