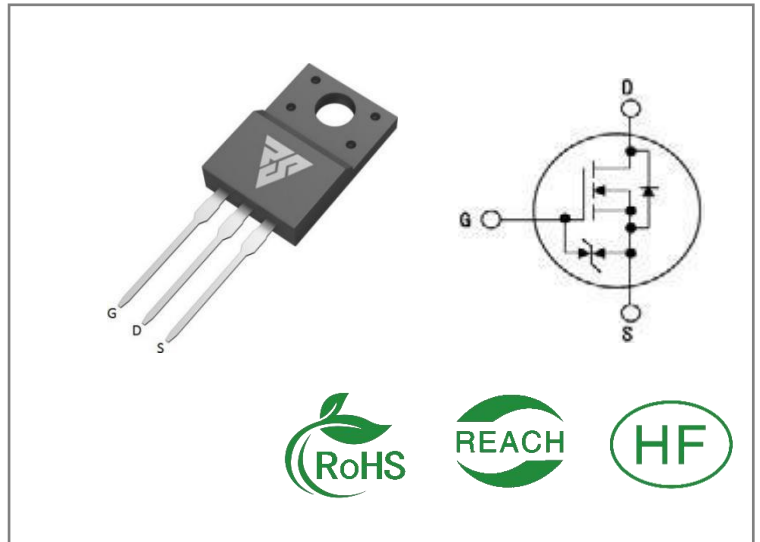


ID	R <sub>DS(ON)</sub> (Typ)	VDSS
17.6A	165mΩ	600V


**Applications:**

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- AC-DC Switching Power Supply

**Features:**

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability
- Built-in ESD Diode

**Ordering Information**

Part Number	Package	Marking	Packing	Qty.
RSE60R190F	T0-220F	RSE60R190F	Tube	50 PCS

**Absolute Maximum Ratings** Tc= 25°C unless otherwise specified

Symbol	Parameter	RSE60R190F	Units
VDSS	Drain-to-Source Voltage	600	V
ID	Continuous Drain Current TC=25°C	17.6	A
ID	Continuous Drain Current TC=100°C	11.2	
IDM	Pulsed Drain Current (Note*1)	53	
PD	Power Dissipation	33	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy IAS=2.45A,VDD = 50V, RG = 25 Ω, TC=25°C	262	mJ
dv/dt	MOSFET dv/ dt ruggedness VDS = 0..400V	50	V/ns
dv/dt	Reverse diode dv/dt VDS = 0..400V, Tj = 25°C, ISD≤ID	15	V/ns
VESD(G-S)	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000	V
TL TPKG	Maximum Temperature for Soldering	300	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

\* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.

**Thermal Resistance**

Symbol	Parameter	RSE60R190F	Units	Test Conditions
R $\theta$ JC	Junction-to-Case	3.77	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 150 °C
R $\theta$ JA	Junction-to-Ambient	80		1 cubic foot chamber, free air.

**OFF Characteristics** T<sub>J</sub>= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	600	--	--	V	VGS=0V, ID=1mA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=600V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	1	μA	VGS=20V, VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-1		VGS=-20V, VDS=0V

**ON Characteristics** T<sub>J</sub>=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	165	190	mΩ	VGS=10V, ID=6.9A
VGS(TH)	Gate Threshold Voltage	2	--	4	V	VGS=VDS, ID=670μA

**Resistive Switching Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	39	--	nS	VDS=300V ID=8.7A RG=25Ω
trise	Rise Time	--	21	--		
td(OFF)	Turn- OFF Delay Time	--	171	--		
tfall	Fall Time	--	18	--		

**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1750	--	pF	VGS=0V VDS=400V f=1.0MHz
Coss	Output Capacitance	--	41	--		
Crss	Reverse Transfer Capacitance	--	2.4	--		
Qg	Total Gate Charge	--	40	--	nC	VDS=480V ID=8.7A VGS=10V
Qgs	Gate- to- Source Charge	--	8	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	12	--		

**Source- Drain Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	17.6	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	53	A	
VSD	Diode Forward Voltage	--	--	1.3	V	IS=8.7A,VGS=0V
trr	Reverse Recovery Time	--	340	--	nS	VR=400V IS=8.7A,di/dt=100 A/μs
Qrr	Reverse Recovery Charge	--	4.7	--	μC	

**Notes:**

- \* 1. Repetitive rating, pulse width limited by maximum junction temperature.
- \* 2. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$

Typical Feature Curve

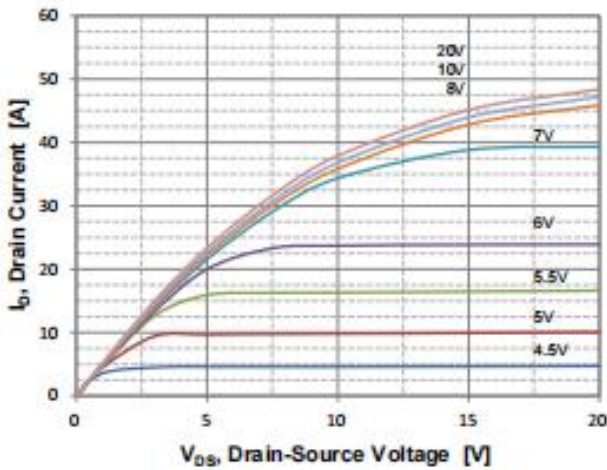


Figure 1. On Region Characteristics

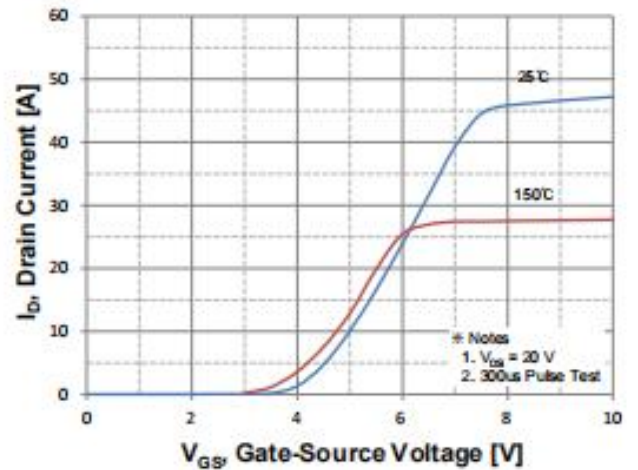


Figure 2. Transfer Characteristics

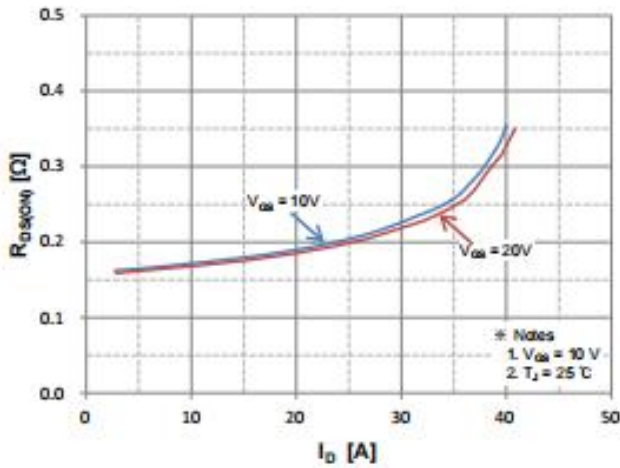


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

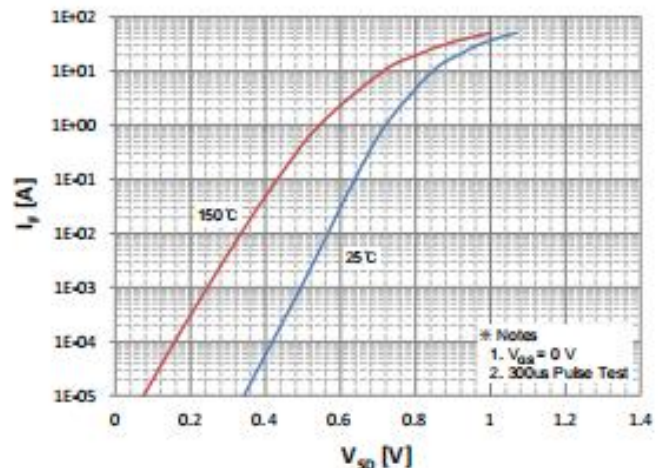


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

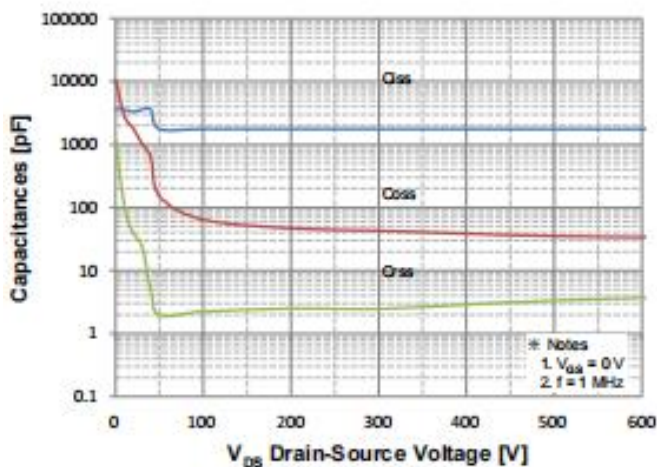


Figure 5. Capacitance Characteristics

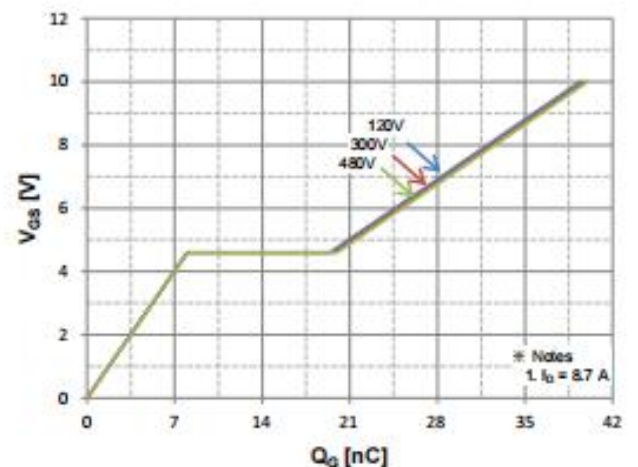


Figure 6. Gate Charge Characteristics



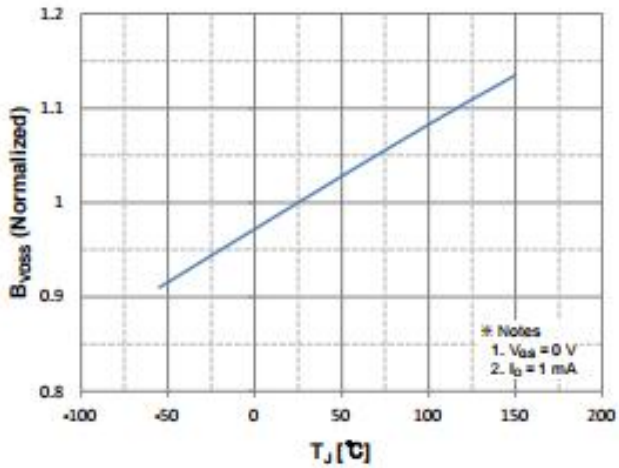


Figure 7. Breakdown Voltage Variation vs. Temperature

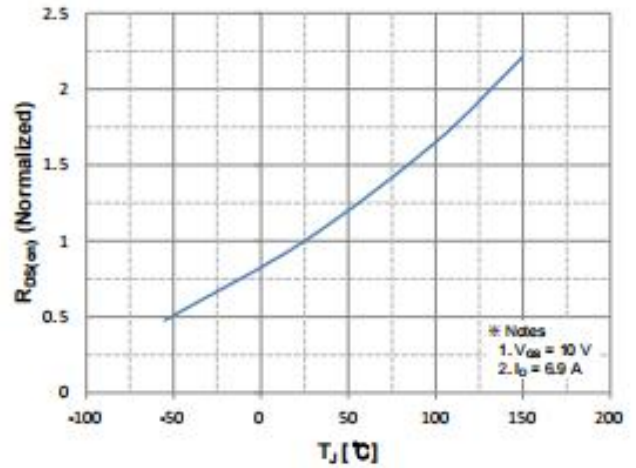


Figure 8. On-Resistance Variation vs. Temperature

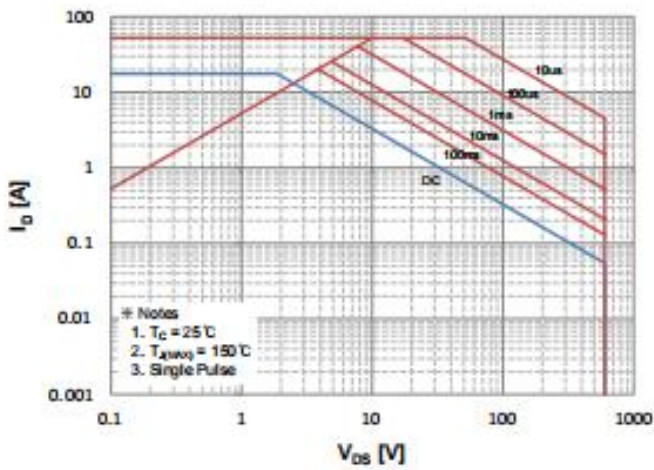


Figure 9. Maximum Safe Operating Area

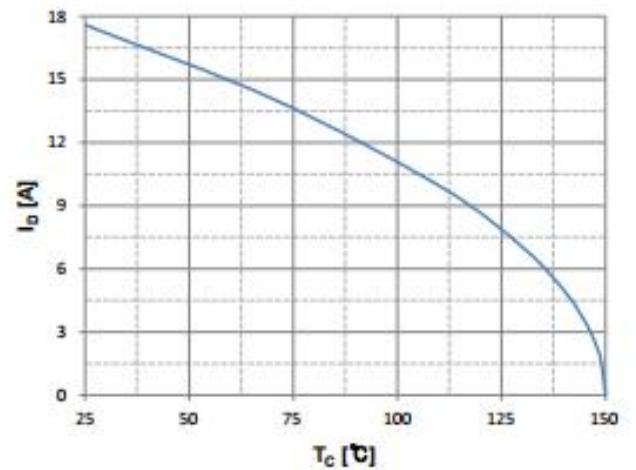


Figure 10. Maximum Drain Current vs. Case Temperature

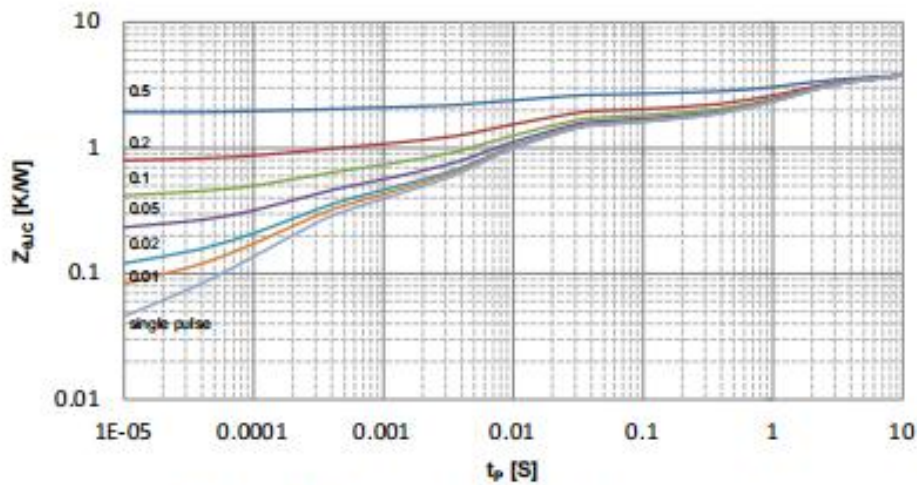


Figure 11. Transient Thermal Response Curve

Test Circuits and Waveforms

Fig 12. Gate Charge Test Circuit & Waveform

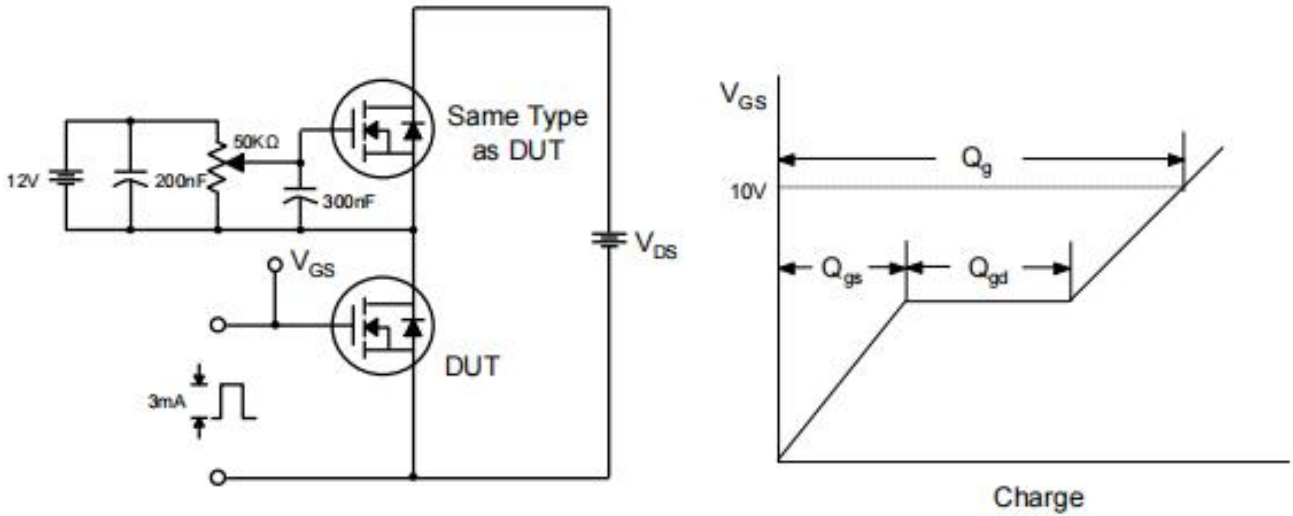


Fig 13. Resistive Switching Test Circuit & Waveforms

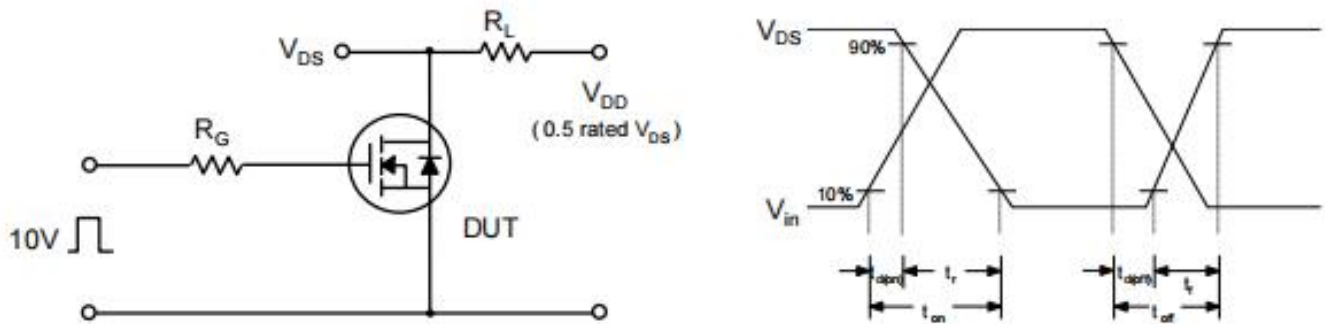
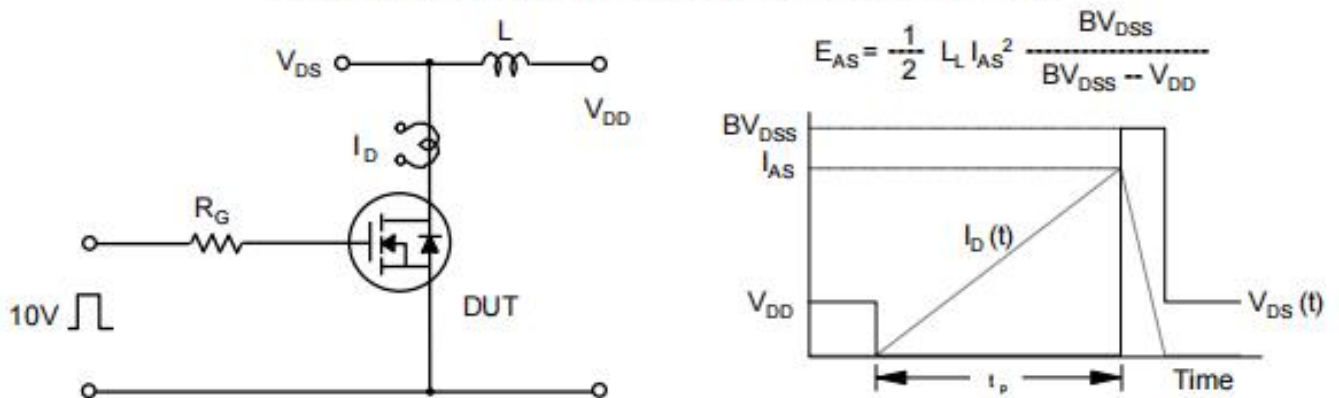
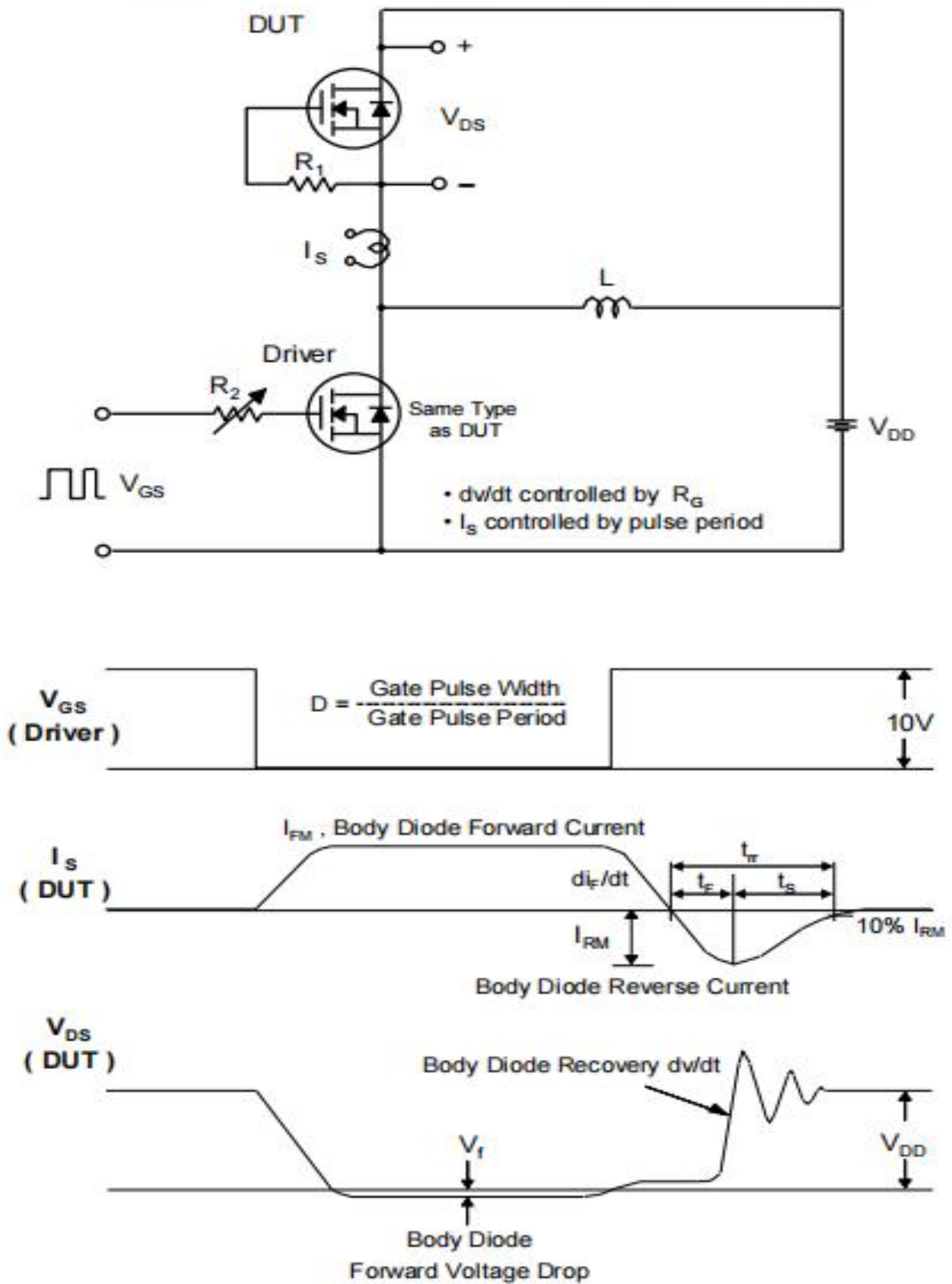


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

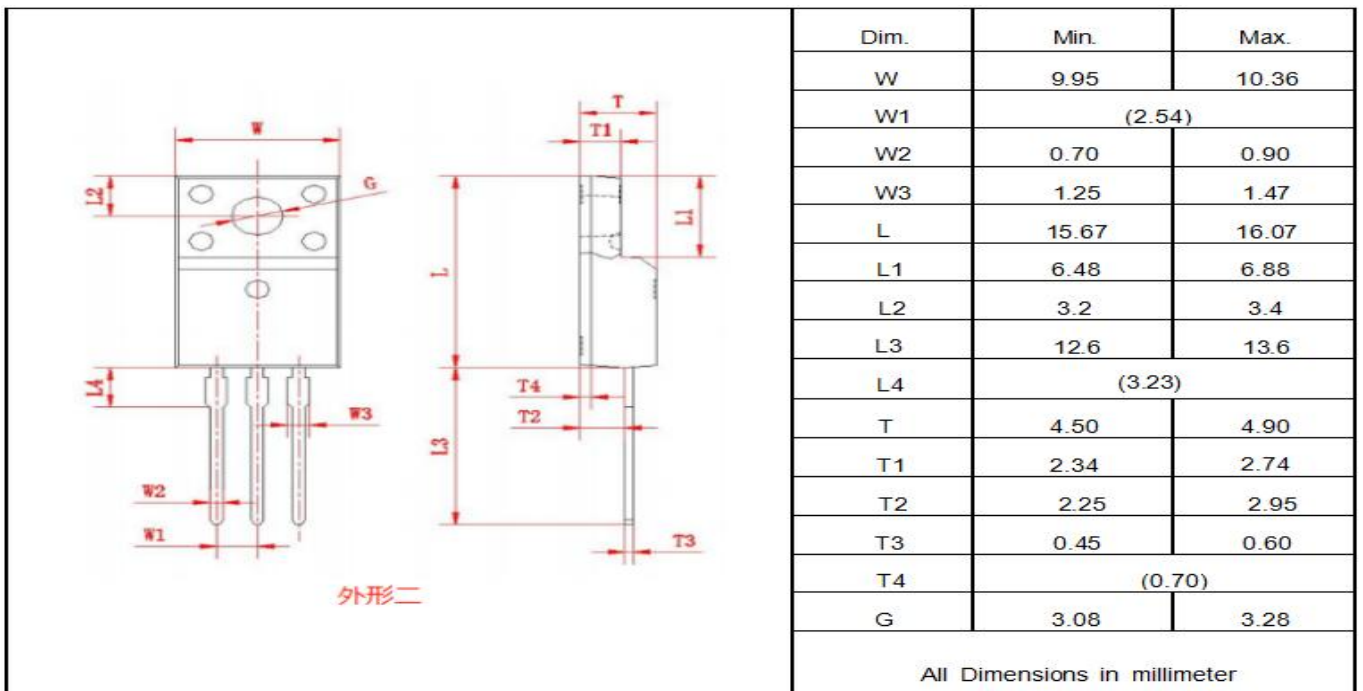
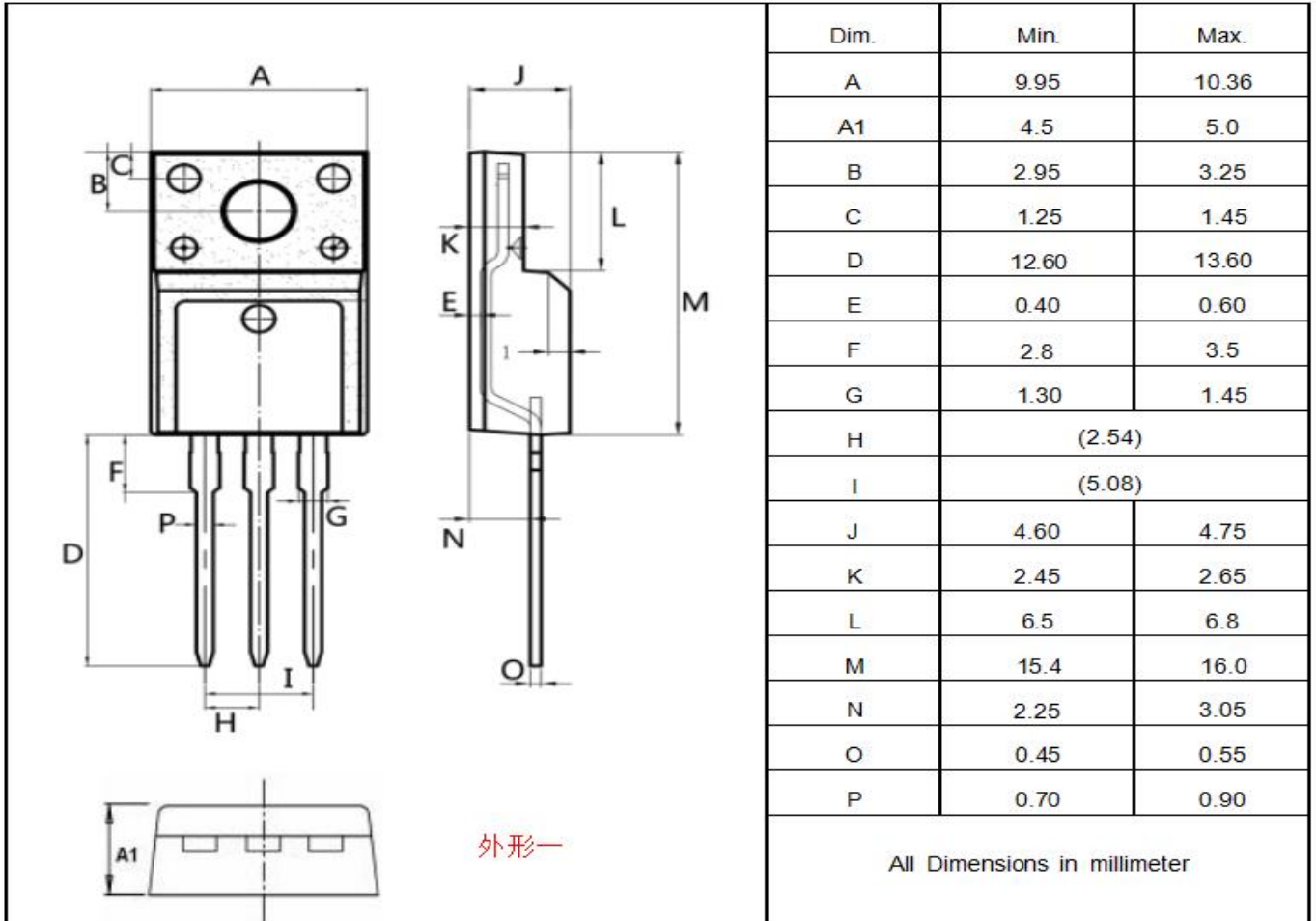


Test Circuits and Waveforms

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package outline drawing (TO-220F Unit: mm)





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