RT7306D

Primary-Side Regulation Dimmable LED Driver Controller with Active-PFC

General Description

The RT7306D is a constant current LED driver with active power factor correction. It supports high power factor across a wide range of line voltages, and it drives the converter in the Quasi-Resonant (QR) mode to achieve higher efficiency. By using Primary Side Regulation (PSR), the RT7306D controls the output current accurately without a shunt regulator and an opto-coupler at the secondary side, reducing the external component count, the cost, and the volume of the driver board.

The RT7306D is compatible with analog dimming. The output current can be modulated by the DIM pin. An in-house design high voltage (HV) start-up device is integrated in the RT7306D to minimize the power loss and shorten the start-up time.

The RT7306D embeds comprehensive protection functions for robust designs, including LED open-circuit protection, LED short-circuit protection, output diode short-circuit protection, VDD Under-Voltage Lockout (UVLO), VDD Over-Voltage Protection (VDD OVP), Over-Temperature Protection (OTP), and cycle-by-cycle current limitation.

Features

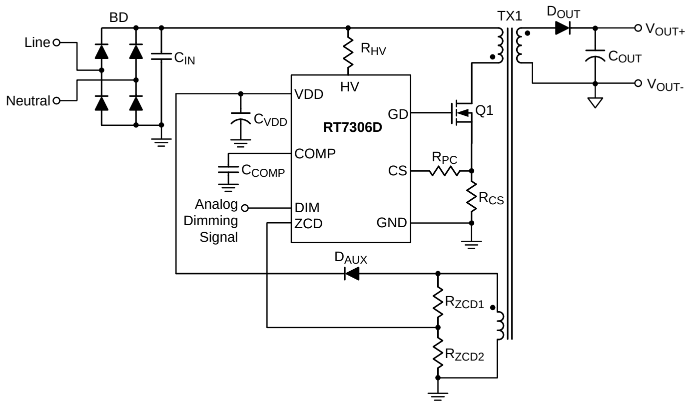
- **Tight LED Current Regulation**
- **No Opto-Coupler and TL431 Required**
- **Power Factor Correction (PFC)**
- **Compatible with Analog Dimming**
- **Built-In HV Start-Up Device**
- **Quasi-Resonant**
- **Maximum/Minimum Switching Frequency Clamping**
- **Maximum/Minimum On-Time Limitation**
- **Wide VDD Range (up to 34V)**
- **THD Optimization**
- **Input-Voltage Feed-Forward Compensation**
- **Multiple Protection Features**
  - **LED Open-Circuit Protection**
  - **LED Short-Circuit Protection**
  - **Output Diode Short-Circuit Protection**
  - **VDD Under-Voltage Lockout**
  - **VDD Over-Voltage Protection**
  - **Over-Temperature Protection**
  - **Cycle-by-Cycle Current Limitation**

Applications

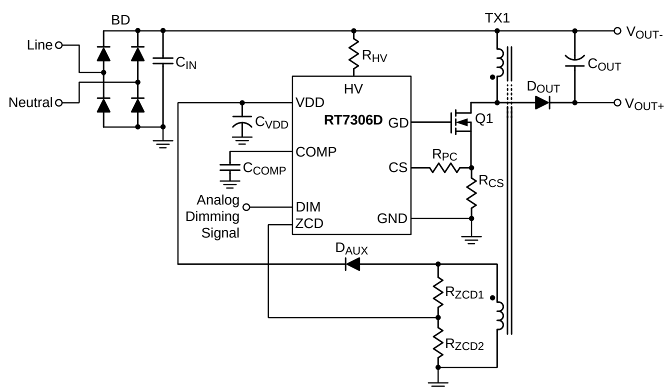
- AC-DC LED Lighting Driver

Simplified Application Circuit

Flyback Application Circuit



Buck-Boost Application Circuit



Ordering Information

RT7306D□□
- Package Type
  S : SOP-8
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

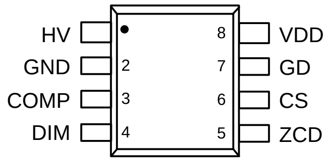
Marking Information

RT7306D
GSYMDNN

RT7306DGS : Product Number
YMDNN : Date Code

Pin Configuration

(TOP VIEW)

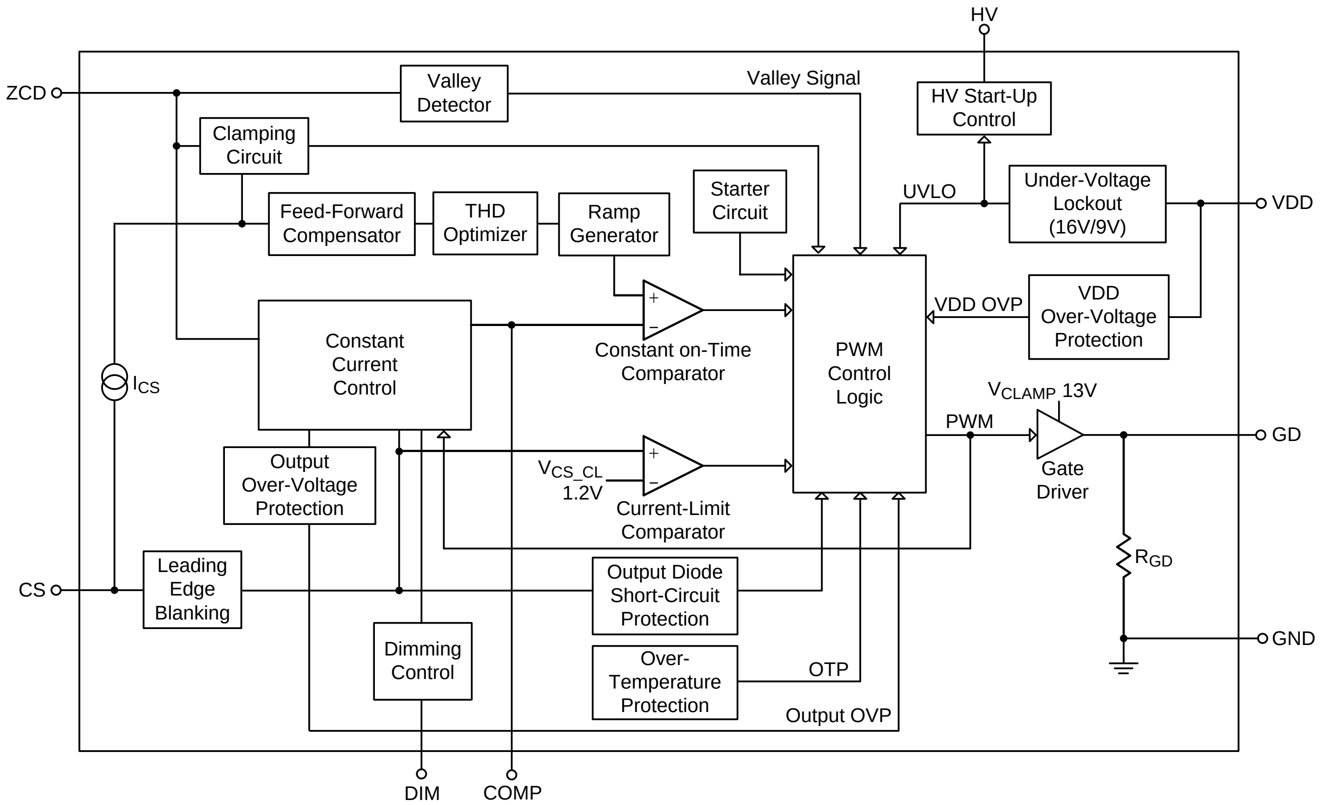


SOP-8

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	HV	High voltage input for startup.
2	GND	Ground of the controller.
3	COMP	Compensation node. Output of the internal trans-conductance amplifier.
4	DIM	Analog dimming signal input. LED driving current can be adjusted by an analog voltage.
5	ZCD	Zero current detection input. This pin is used to sense the voltage at auxiliary winding of the transformer.
6	CS	Current sense input. Connect this pin to the current sense resistor.
7	GD	Gate driver output for external power MOSFET.
8	VDD	Supply voltage (V_{DD}) input. The controller will be enabled when V_{DD} exceeds V_{TH_ON} and disabled when V_{DD} is lower than V_{TH_OFF}.

Functional Block Diagram



Operation

Critical-Conduction Mode (CRM) with Constant On-Time Control

Figure 1 shows a typical flyback converter with input voltage (V_{IN}). When main switch Q1 is turned on with a fixed on-time (t_{ON}), the peak current (I_{L_PK}) of the magnetic inductor (L_m) can be calculated by the following equation :

$$I_{L\_PK} = \frac{V_{IN}}{L_m} \times t_{ON}$$

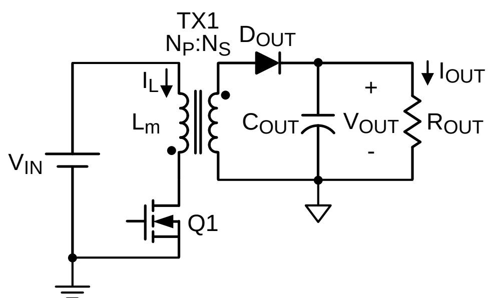


Figure 1. Typical Flyback Converter

If the input voltage is the output voltage of the full-bridge rectifier with sinusoidal input voltage ($V_{IN\_PK} \cdot \sin(\theta)$), the inductor peak current (I_{L_PK}) can be expressed as the following equation :

$$I_{L\_PK} = \frac{V_{IN\_PK} \times |\sin(\theta)| \times t_{ON}}{L_m}$$

When the converter operates in CRM with constant on-time control, the envelope of the peak inductor current will follow the input voltage waveform with in-phase. Thus, high power factor can be achieved, as shown in Figure 2.

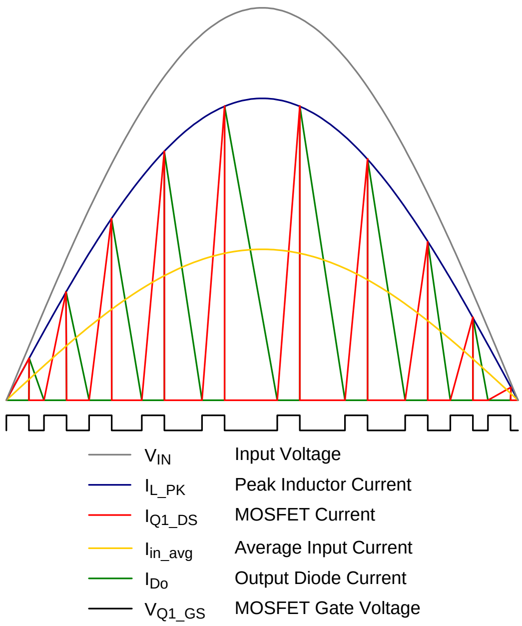


Figure 2. Inductor Current of CRM with Constant On-Time Control

The RT7306D needs no shunt regulator and opto-coupler at the secondary side to achieve the output current regulation. Figure 3 shows several key waveforms of a conventional flyback converter in Quasi-Resonant (QR) mode, in which V_{AUX} is the voltage on the auxiliary winding of the transformer.

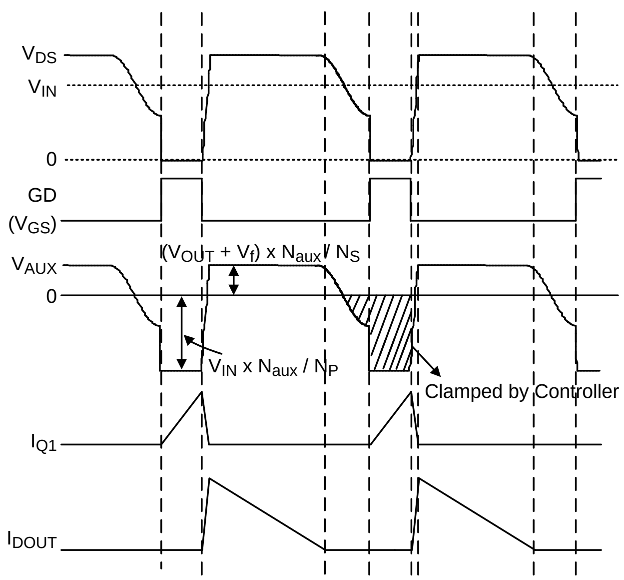


Figure 3. Key Waveforms of a Flyback Converter

Voltage Clamping Circuit

The RT7306D provides a voltage clamping circuit at ZCD pin since the voltage on the auxiliary winding is negative when the main switch is turned on. The lowest voltage on ZCD pin is clamped near zero to prevent the IC from being damaged by the negative voltage. Meanwhile, the sourcing ZCD current (I_{ZCD_SH}), flowing through the upper resistor (R_{ZCD1}), is sampled and held to be a line-voltage-related signal for propagation delay compensation. The RT7306D embeds the programmable propagation delay compensation through CS pin. A sourcing current I_{CS} (equal to I_{ZCD_SH} x K_{PC}) applies a voltage offset (I_{CS} x R_{PC}) which is proportional to line voltage on CS to compensate the propagation delay effect. Thus, the output current can be equal at high and low line voltage.

Quasi-Resonant Operation

Figure 4 illustrates how valley signal triggers PWM. If no valley signal detected for a long time, the next PWM is triggered by a starter circuit at end of the interval (t_{START}, 130μs typ.) which starts at the rising edge of the previous PWM signal. A blanking time ($t_{S(MIN)}$, 8.5μs typ.), which starts at the rising edge of the previous PWM signal, limits minimum switching period. When the $t_{S(MIN)}$ interval is on-going, all of valley signals are not allowed to trigger the next PWM signal. After the end of the $t_{S(MIN)}$ interval, the coming valley will trigger the next PWM signal. If one or more valley signals are detected during the $t_{S(MIN)}$ interval and no valley is detected after the end of the $t_{S(MIN)}$ interval, the next PWM signal will be triggered automatically at end of the $t_{S(MIN)}$ + 5μs (typ.).

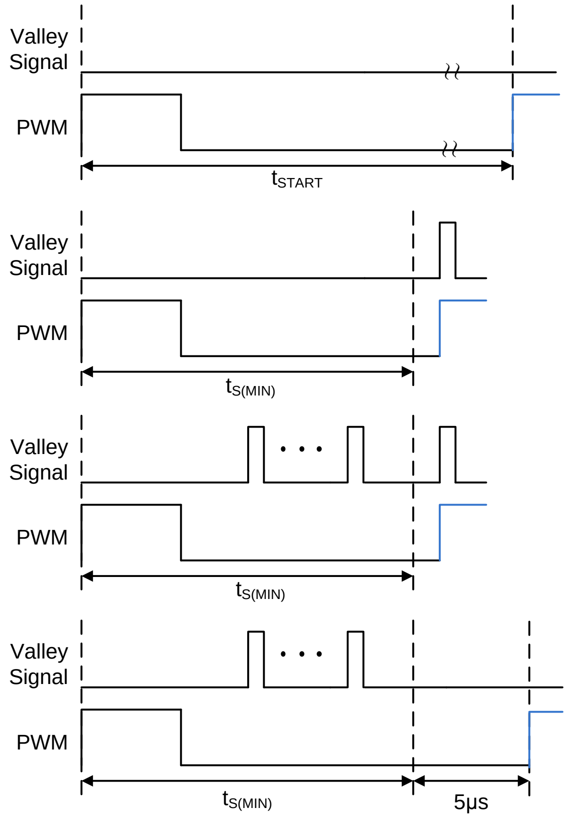


Figure 4. PWM Triggered Method

HV Start-Up Device

An in-house design 500V start-up device is integrated in the RT7306D to minimize the power loss and shorten the start-up time. The HV start-up device will be turned on during start-up period and be turned off during normal operation. It provides fast start-up time and no power loss in this path during normal operation. A 10kΩ resistor is recommended to be connected in series with HV pin.

Dimming Function

An analog dimming function is embedded in the RT7306D. When the voltage on the DIM pin (V_{DIM}) is within V_{DIM_LOW} and V_{DIM_HIGH}, the regulation factor of constant current control (K_{CC}) is linearly proportional to V_{DIM}, as shown in Figure 5.

DIM pin sourcing a current (1μA typ.) when VDD > V_{TH_ON}, and the sourcing current is shut down after 100ms (typ.)

The external equivalent resistance of DIM pin is recommended to be higher than 430kΩ.

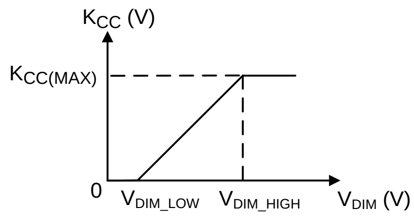


Figure 5. Dimming Curve

Protections

LED Open-Circuit Protection

In an event of output open circuit, the converter will be shut down to prevent being damaged, and it will be auto-restarted when the output is recovered. Once the LED is open-circuit, the output voltage keeps rising, causing the voltage on ZCD pin V_{ZCD} rising accordingly. When the sample-and-hold ZCD voltage (V_{ZCD_SH}) exceeds its OV threshold (V_{ZCD_OVP}, 3.2V typ.), output OVP will be activated and the PWM output (GD pin) will be forced low to turn off the main switch. If the output is still open-circuit when the converter restarts, the converter will be shut down again.

Output Diode Short-Circuit Protection

When the output diode is damaged as short-circuit, the transformer will be led to magnetic saturation and the main switch will suffer from a high current stress. To avoid the above situation, an output diode short-circuit protection is built-in. When CS voltage V_{CS} exceeds the threshold (V_{CS_SD} 1.7 typ.) of the output diode short-circuit protection, the RT7306D will shut down the PWM output (GD pin) in few cycles to prevent the converter from damage. It will be auto-restarted when the failure condition is recovered.

VDD Under-Voltage Lockout (UVLO) and Over-Voltage Protection (VDD OVP)

The RT7306D will be enabled when VDD voltage (V_{DD}) exceeds rising UVLO threshold (V_{TH_ON}, 17V typ.) and disabled when V_{DD} is lower than falling UVLO threshold (V_{TH_OFF}, 8.5V typ.).

When V_{DD} exceeds its over-voltage threshold (V_{OVP}, 37.4V typ.), the PWM output of the RT7306D is shut down. It will be auto-restarted when the VDD is recovered to a normal level.

Over-Temperature Protection (OTP)

The RT7306D provides an internal OTP function to protect the controller itself from suffering thermal stress and permanent damage. It's not suggested to use the function as precise control of over temperature. Once the junction temperature is higher than the OTP threshold (T_{SD}, 150°C typ.), the controller will shut down until the temperature cools down by 30°C (typ.). Meanwhile, if V_{DD} reaches falling UVLO threshold voltage (V_{TH_OFF}), the controller will hiccup till the over temperature condition is removed.

Absolute Maximum Ratings (Note 1)

- HV Pin ---------- –0.3V to 500V
- Supply Voltage, V_{DD} ---------- –0.3V to 40V
- Gate Driver Output, GD ---------- –0.3V to 20V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  SOP-8 ---------- 0.48W
- Package Thermal Resistance (Note 2)

  SOP-8, θ_{JA} ---------- 206.9°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) (Except HV pin) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{DD} ---------- 11V to 34V
- COMP Voltage, V_{COMP} ---------- 0.7V to 4.3V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
HV Section						
HV Start-Up Average Current	I_{HV_ST}	$V_{DD} < V_{TH\_ON}$, V_{HV} = 100V	1	--	--	mA
Off State Leakage Current		$V_{DD} = V_{TH\_ON}$ + 1V, V_{HV} = 500V	--	--	30	μA
VDD Section						
VDD OVP Threshold Voltage	V_{OVP}	V_{DD} rising	35.4	37.4	39.4	V
Rising UVLO Threshold Voltage	V_{TH_ON}		16	17	18	V
Falling UVLO Threshold Voltage	V_{TH_OFF}		7.5	8.5	9.5	V
Fault Released Voltage	V_{TH_FR}		--	6	--	V
VDD Holdup Mode Entry Point	V_{DD_ET}		--	10	--	V
VDD Holdup Mode Ending Point	V_{DD_ED}		--	10.5	--	V
Operating Current	I_{DD_OP}	V_{DD} = 15V, I_{ZCD} = 0, GD open	--	2	3	mA
Operating Current at Shutdown		$V_{DD} = V_{TH\_OFF}$	--	60	--	μA
Start-Up Current	I_{VDD_ST}	$V_{DD} = V_{TH\_ON}$ – 1V	--	15	30	μA
ZCD Section						
Lower Clamp Voltage	V_{ZCDL}	I_{ZCD} = 0 to –2.5mA	–50	0	60	mV
ZCD OVP Threshold Voltage	V_{ZCD_OVP}		3.04	3.2	3.36	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dimming Control Section						
Analog Dimming Low Threshold Voltage	V_{DIM_LOW}		250	300	350	mV
Analog Dimming High Threshold Voltage	V_{DIM_HIGH}		--	2.8	--	V
DIM Sourcing Current			0.5	1	2	μA
Constant Current Control Section						
Maximum Regulated Factor for Constant-Current Control	$K_{CC(MAX)}$	V_{DIM} = 3V	246.25	250	253.75	mV
Maximum Comp Voltage	$V_{COMP(MAX)}$		4.8	5.5	--	V
Minimum Comp Voltage	$V_{COMP(MIN)}$		--	0.5	--	V
Maximum Sourcing Current	$I_{COMP(MAX)}$	During start-up period	--	100	--	μA
Current Sense Section						
Leading Edge Blanking Time	t_{LEB}		240	400	570	ns
Peak Current Shutdown Voltage Threshold	V_{CS_SD}		1.53	1.7	1.87	V
Peak Current Limitation at Normal Operation	V_{CS_CL}		1.08	1.2	1.32	V
Propagation Delay Compensation Factor	K_{PC}	$I_{CS} = K_{PC} \times I_{ZCD}$, I_{ZCD} = –150μA	--	0.042	--	A/A
Gate Driver Section						
Rising Time	t_R	V_{DD} = 15V, C_L = 1nF	--	140	250	ns
Falling Time	t_F	V_{DD} = 15V, C_L = 1nF	--	40	70	ns
Gate Output Clamping Voltage	V_{CLAMP}	V_{DD} = 15V, C_L = 1nF	10.8	12	13.2	V
Internal Pull Low Resistor	R_{GD}		--	40	--	kΩ
Timing Control Section						
Minimum On-Time	$t_{ON(MIN)}$	I_{ZCD} = –150μA	0.9	1.25	1.6	μs
Minimum Switching Period	$t_{S(MIN)}$		7	8.5	10	μs
Duration of Starter at Normal Operation	t_{START}		75	130	300	μs
Maximum On-Time	$t_{ON(MAX)}$		29	47	65	μs
Over-Temperature Protection (OTP) Section						
OTP Temperature Threshold	T_{OTP}	(Note 5)	--	150	--	°C
OTP Temperature Hysteresis	$T_{OTP-HYS}$	(Note 5)	--	30	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity two-layer test board on a JEDEC thermal measurement standard.

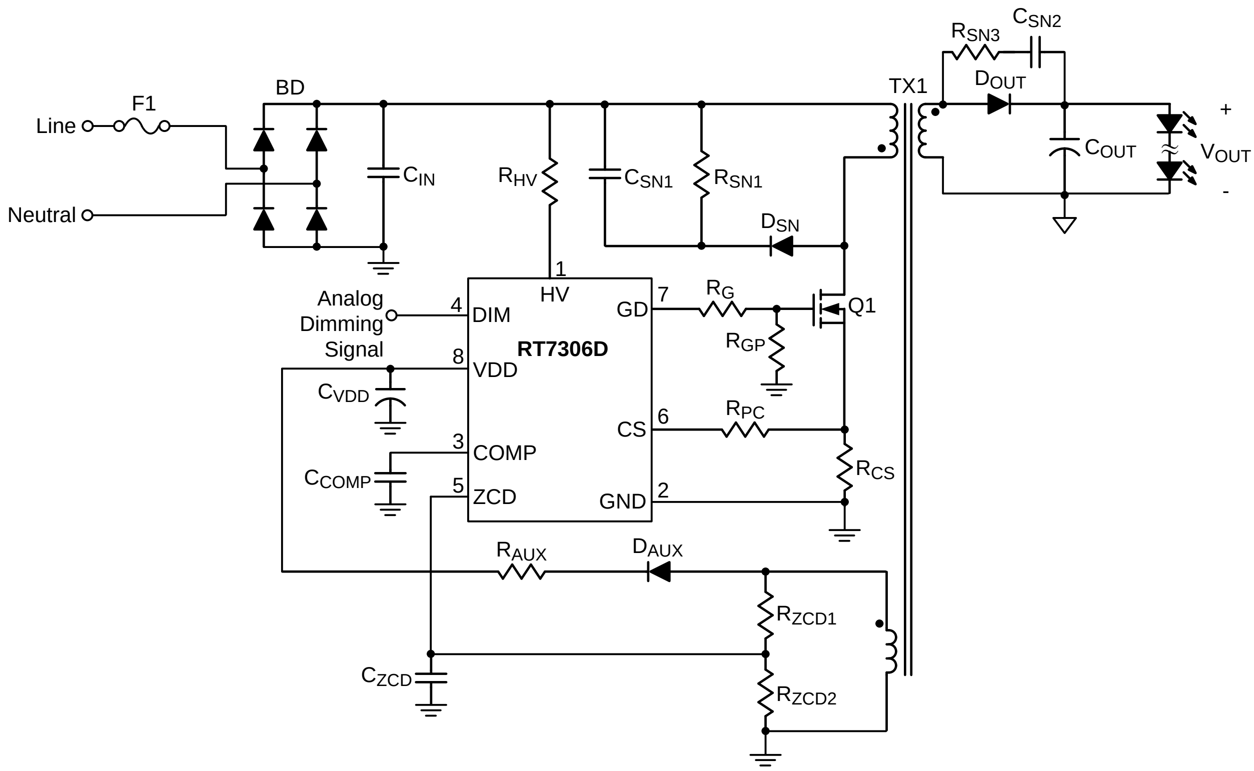
Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

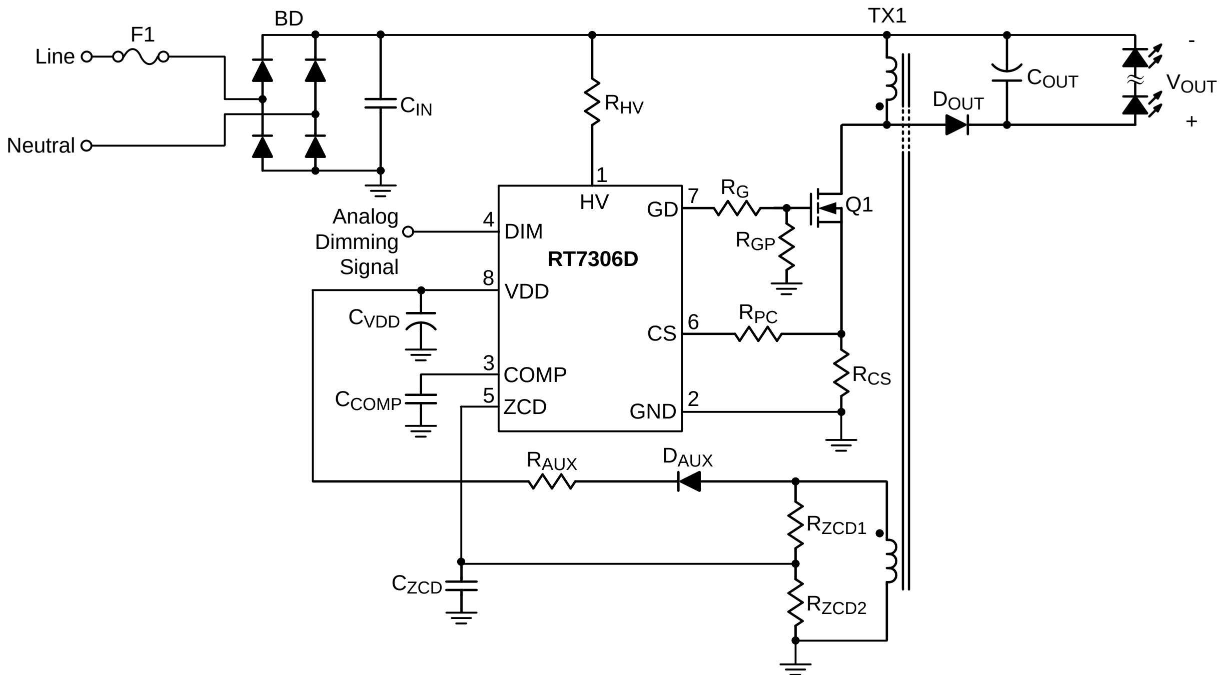
Note 5. Guarantee by design.

Typical Application Circuit

Flyback Application Circuit

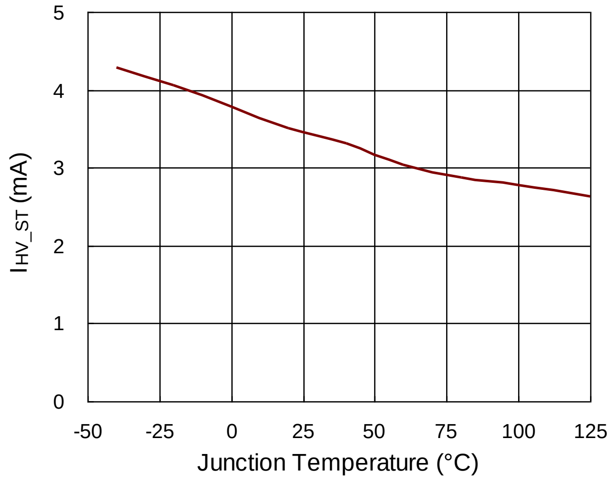


Buck-Boost Application Circuit

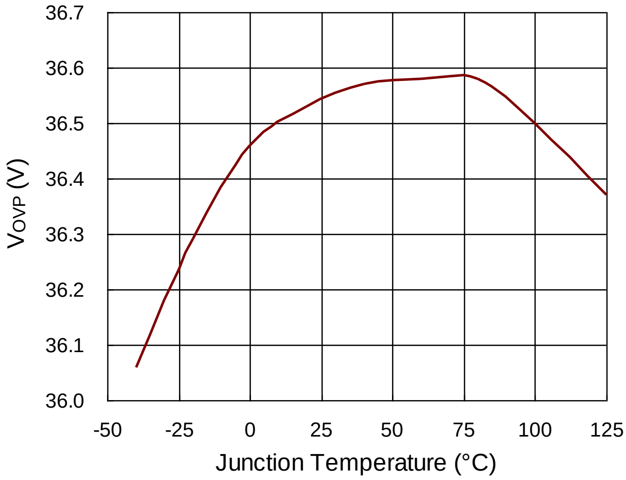


Typical Operating Characteristics

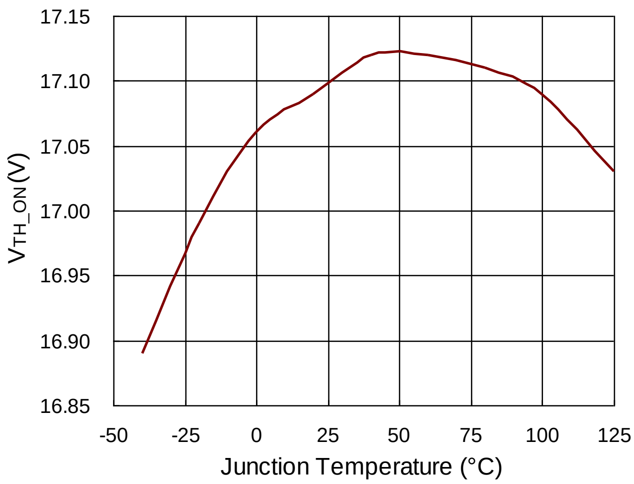
I_{HV_ST} vs. Junction Temperature



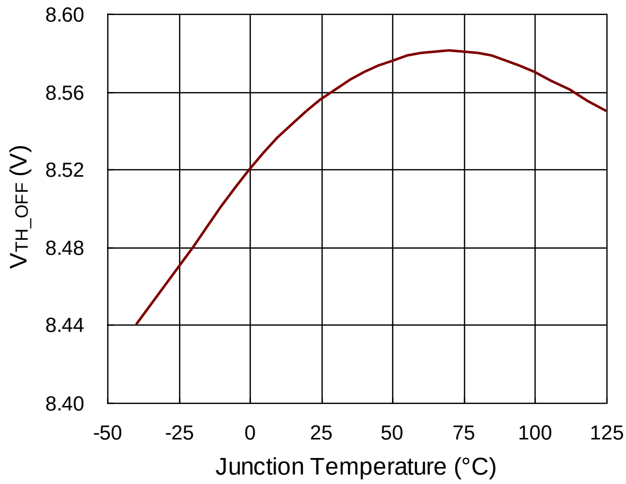
V_{OVP} vs. Junction Temperature



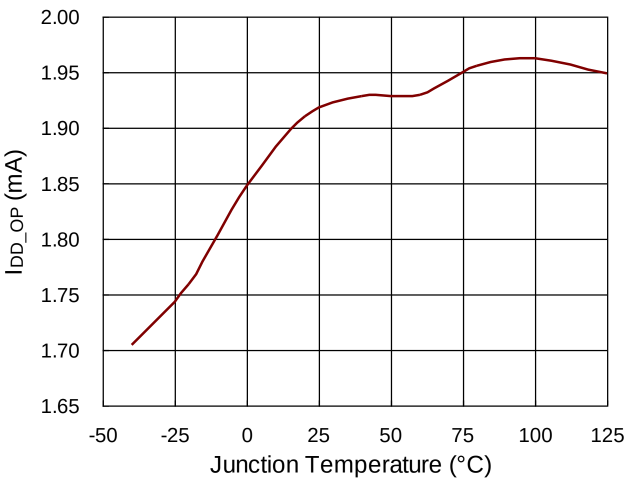
V_{TH_ON} vs. Junction Temperature



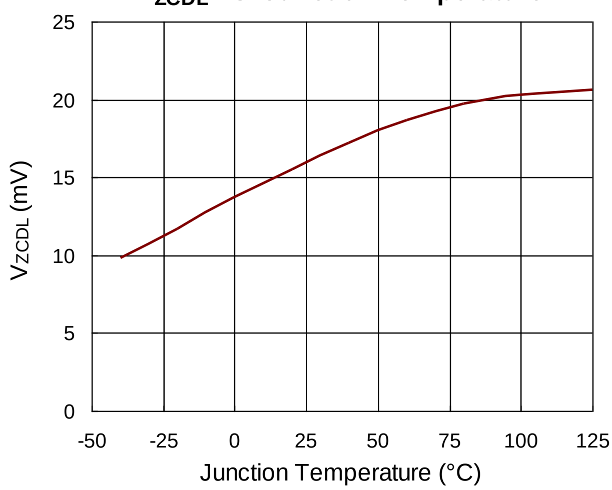
V_{TH_OFF} vs. Junction Temperature

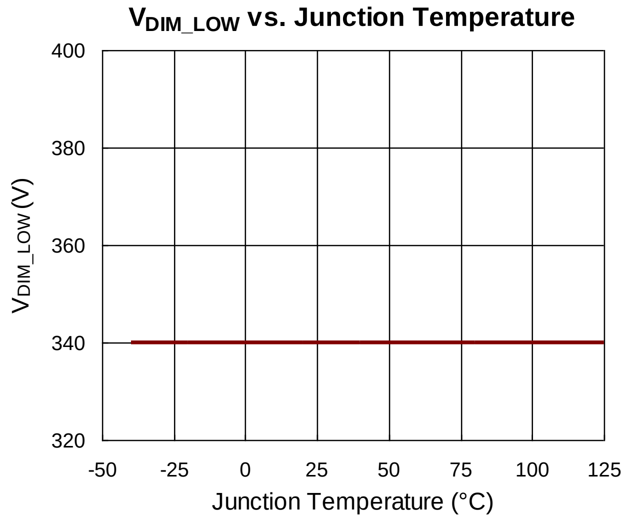


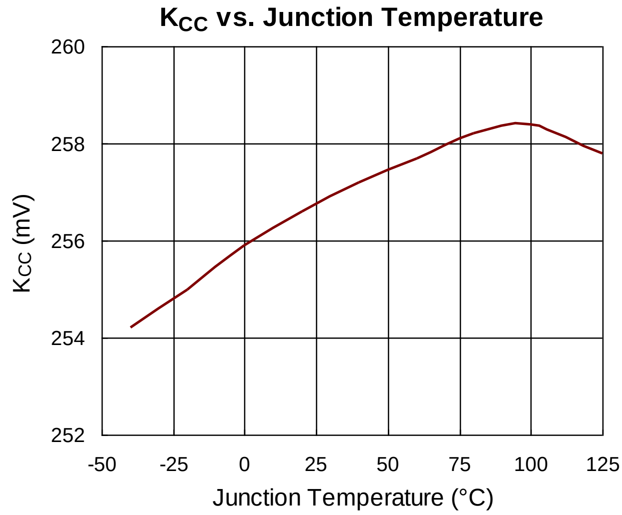
I_{DD_OP} vs. Junction Temperature

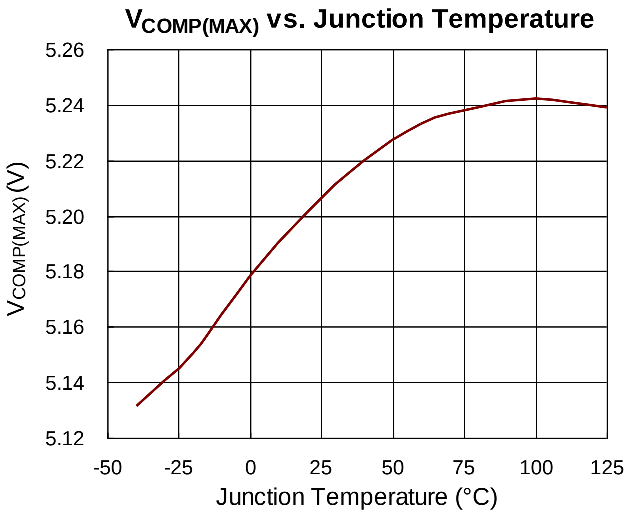


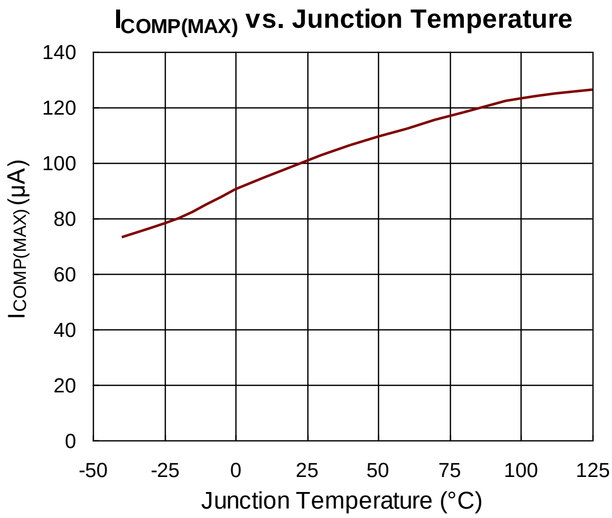
V_{ZCDL} vs. Junction Temperature

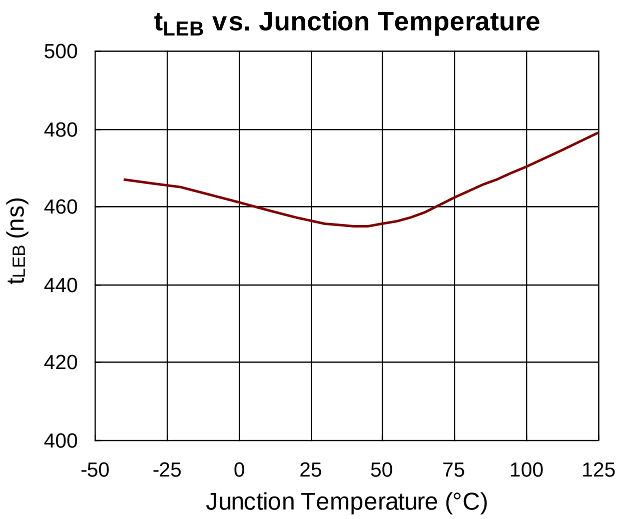


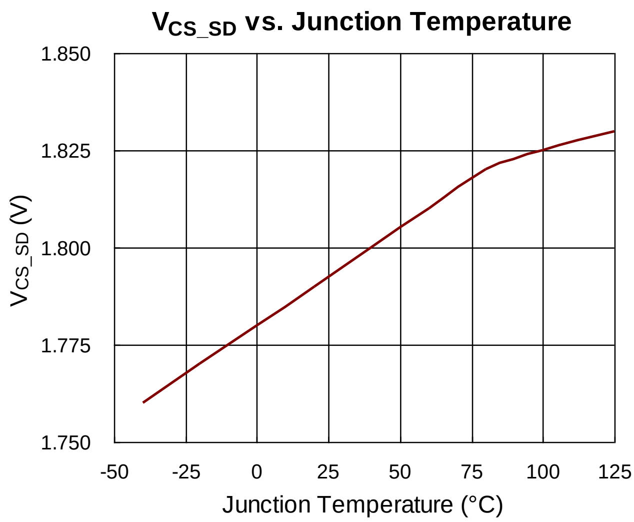

V_{DIM_LOW} vs. Junction Temperature
V_{DIM_LOW} (V)
400
380
360
340
320
-50
-25
0
25
50
75
100
125
Junction Temperature (°C)

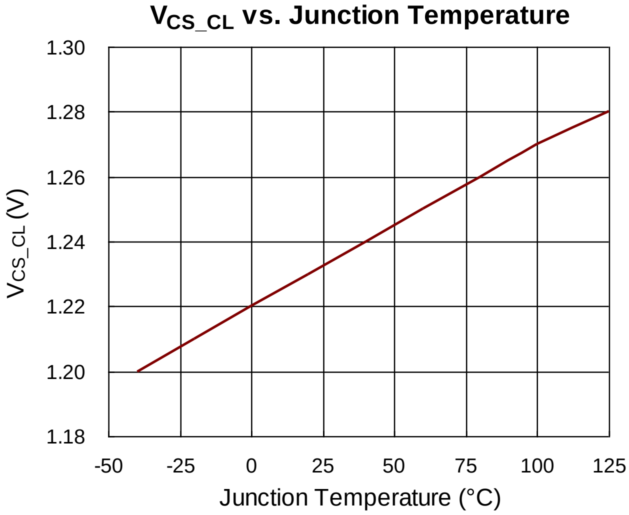

K_{CC} vs. Junction Temperature
K_{CC} (mV)
260
258
256
254
252
-50
-25
0
25
50
75
100
125
Junction Temperature (°C)


$V_{COMP(MAX)}$ vs. Junction Temperature
$V_{COMP(MAX)}$ (V)
5.26
5.24
5.22
5.20
5.18
5.16
5.14
5.12
-50
-25
0
25
50
75
100
125
Junction Temperature (°C)

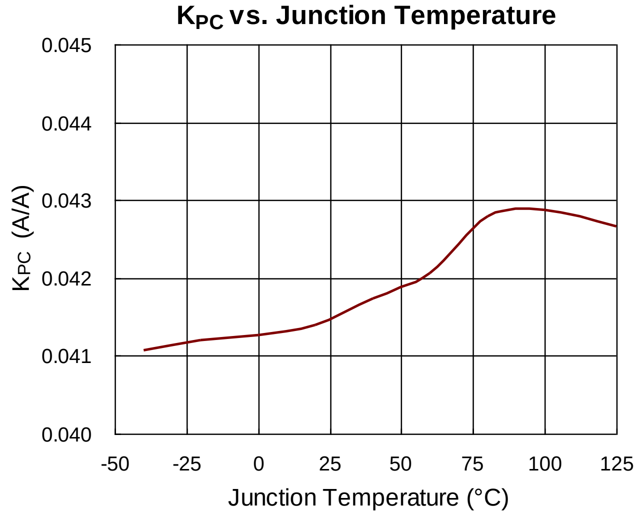

$I_{COMP(MAX)}$ vs. Junction Temperature
$I_{COMP(MAX)}$ (μA)
140
120
100
80
60
40
20
0
-50
-25
0
25
50
75
100
125
Junction Temperature (°C)


t_{LEB} vs. Junction Temperature
t_{LEB} (ns)
500
480
460
440
420
400
-50
-25
0
25
50
75
100
125
Junction Temperature (°C)

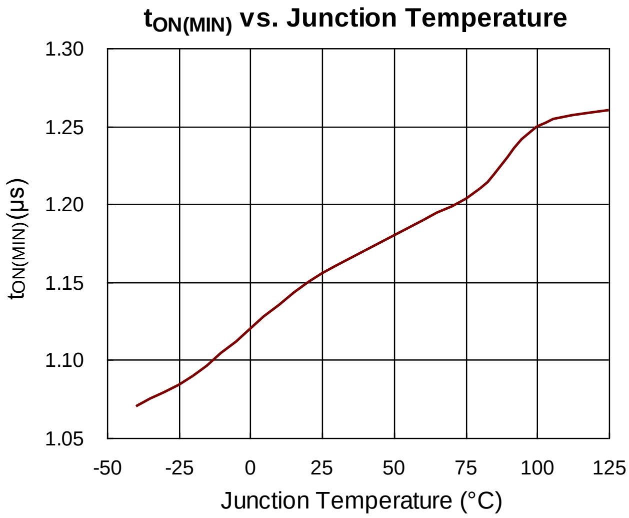

V_{CS_SD} vs. Junction Temperature
V_{CS_SD} (V)
1.850
1.825
1.800
1.775
1.750
-50
-25
0
25
50
75
100
125
Junction Temperature (°C)



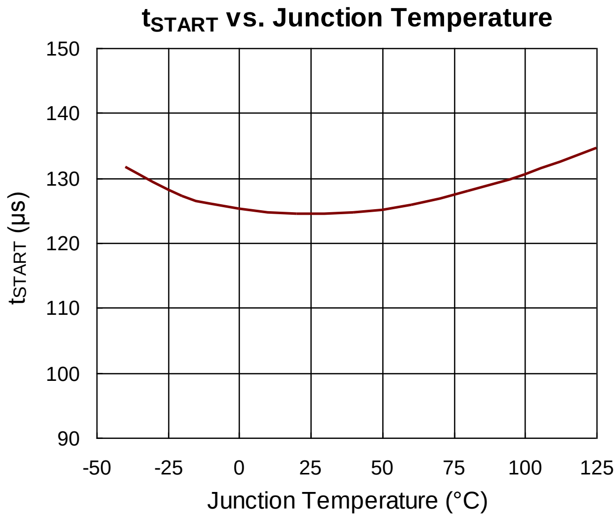
V_{CS_CL} vs. Junction Temperature
V_{CS_CL} (V)
1.30
1.28
1.26
1.24
1.22
1.20
1.18
-50 -25 0 25 50 75 100 125
Junction Temperature (°C)



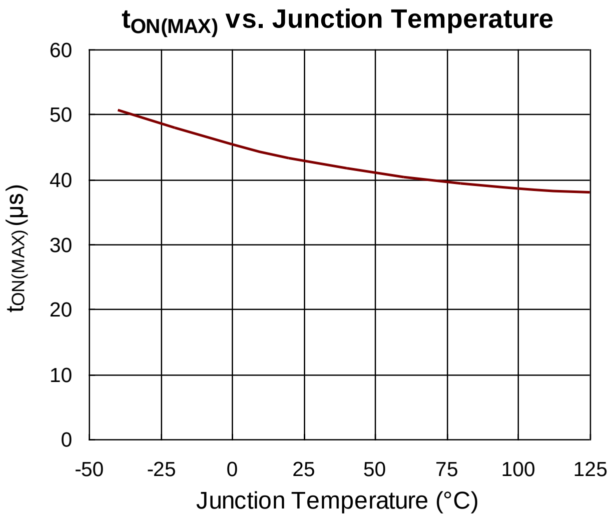
K_{PC} vs. Junction Temperature
K_{PC} (A/A)
0.045
0.044
0.043
0.042
0.041
0.040
-50 -25 0 25 50 75 100 125
Junction Temperature (°C)



$t_{ON(MIN)}$ vs. Junction Temperature
$t_{ON(MIN)}$(μs)
1.30
1.25
1.20
1.15
1.10
1.05
-50 -25 0 25 50 75 100 125
Junction Temperature (°C)



t_{START} vs. Junction Temperature
t_{START} (μs)
150
140
130
120
110
100
90
-50 -25 0 25 50 75 100 125
Junction Temperature (°C)



$t_{ON(MAX)}$ vs. Junction Temperature
$t_{ON(MAX)}$ (μs)
60
50
40
30
20
10
0
-50 -25 0 25 50 75 100 125
Junction Temperature (°C)

Application Information

Output Current Setting

Considering the conversion efficiency, the programmed DC level of the average output current ($I_{OUT}(t)$) can be derived as :

$$I_{OUT\_CC}=\frac{1}{2}\times\frac{N_P}{N_S}\times\frac{K_{CC}}{R_{CS}}\times CTR_{TX1}$$

$$CTR_{TX1}=\frac{I_{SEC\_PK}}{I_{PRI\_PK}}\times\frac{N_S}{N_P}$$

in which CTR_{TX1} is the current transfer ratio of the transformer TX1, I_{SEC_PK} is the peak current of the secondary side, and I_{PRI_PK} is the peak current of the primary side. CTR_{TX1} can be estimated to be 0.9. According to the above parameters, current sense resistor R_{CS} can be determined as the following equation :

$$R_{CS}=\frac{1}{2}\times\frac{N_P}{N_S}\times\frac{K_{CC}}{I_{OUT\_CC}}\times CTR_{TX1}$$

Propagation Delay Compensation Design

The V_{CS} deviation (ΔV_{CS}) caused by propagation delay effect can be derived as:

$$\Delta V_{CS}=\frac{V_{IN}\cdot t_D\cdot R_{CS}}{L_m},$$

in which t_D is the delay period which includes the propagation delay of the RT7306D and the turn-off transition of the main MOSFET. The sourcing current from CS pin of the RT7306D (I_{CS}) can be expressed as :

$$I_{CS}=K_{PC}\cdot V_{IN}\cdot\frac{N_A}{N_P}\cdot\frac{1}{R_{ZCD1}}$$

where N_A is the turns number of the auxiliary winding.

R_{PC} can be designed by :

$$R_{PC}=\frac{\Delta V_{CS}}{I_{CS}}=\frac{t_D\cdot R_{CS}\cdot R_{ZCD1}}{L_m\cdot K_{PC}}\cdot\frac{N_P}{N_A}$$

Feed-Forward Compensation Design

The COMP voltage, V_{COMP}, is a function of the resistor R_{ZCD1} as following :

$$R_{ZCD1}=\left(V_{IN\_pk}\times\frac{N_A}{N_P}\times K_{IV}\right)\times\sqrt{\frac{\left(\frac{t_{ON}}{t_S}\right)\times Gm_{ramp}\times t_{ON}}{2\times C_{ramp}\times\left(V_{COMP}-V_D\right)}}$$

in which K_{IV}, Gm_{ramp}, and C_{ramp} are fixed parameters in the RT7306D, and the typical value are : K_{IV} = 2.5V/mA, Gm_{ramp} = 8μA/V, C_{ramp} = 6.5pF.

V_D is the offset of the constant on-time comparator, and its typical value is 0.63V. It is recommended to design V_{COMP} = 2 to 3V. If the COMP voltage is over its recommended operating range (0.7 to 4.3V), output current regulation may be affected. Thus, the resistors R_{ZCD1} can be determined according to the above parameters.

Minimum On-Time Setting

The RT7306D limits a minimum on-time ($t_{ON(MIN)}$) for each switching cycle. The $t_{ON(MIN)}$ can be derived from the following equations.

$$t_{ON(MIN)}\times I_{ZCD\_SH}=187.5p\cdot sec\cdot A\ \text{(typ.)}$$

Thus, R_{ZCD1} can be determined by:

$$R_{ZCD1}=\frac{t_{ON(MIN)}\times V_{IN}}{187.5p}\times\frac{N_A}{N_P}\ \text{(typ.)}$$

In addition, the current flowing out of ZCD pin must be lower than 2.5mA (typ.). Thus, the R_{ZCD1} is also determined by :

$$R_{ZCD1}>\frac{\sqrt{2}\cdot V_{AC(MAX)}}{2.5m}\times\frac{N_A}{N_P}$$

where the $V_{AC(MAX)}$ is maximum input AC voltage.

Output Over-Voltage Protection Setting

Output OVP is achieved by sensing the voltage on the auxiliary winging. It is recommended that output OV level (V_{OUT_OVP}) is set at 120% of nominal output voltage (V_{OUT}). Thus, R_{ZCD1} and R_{ZCD2} can be determined by the equation as :

$$V_{OUT}\times\frac{N_A}{N_S}\times\frac{R_{ZCD2}}{R_{ZCD1}+R_{ZCD2}}\times 120\%=3.2V\text{(typ.)}$$

Adaptive Blanking Time

When the MOSFET is turned off, the leakage inductance of the transformer and parasitic capacitance (C_{OSS}) of the MOSFET induce resonance waveform on the ZCD pin. The resonance waveform may make the controller false trigger the ZCD OVP, and it may cause the controller operate in unstable condition. As load increases, the resonance time also increases. It is recommended to add a 10pF to 47pF bypass capacitor, and it should be as close to ZCD pin as possible. The larger bypass capacitor may cause phase shift on ZCD waveform, so the MOSFET is not turned on at exact valley point.

To avoid the above issue, the RT7306D provides adaptive blanking time (t_{BK}). It varies with the peak voltage of the CS pin (V_{CS_PK}), as shown by the following formula :

$t_{BK} = 2\mu s + V_{CS\_PK} \times 2\mu s/V$ (typ.)

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOP-8 package, the thermal resistance, θ_{JA}, is 206.9°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (206.9°C/W) = 0.48W for a SOP-8 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

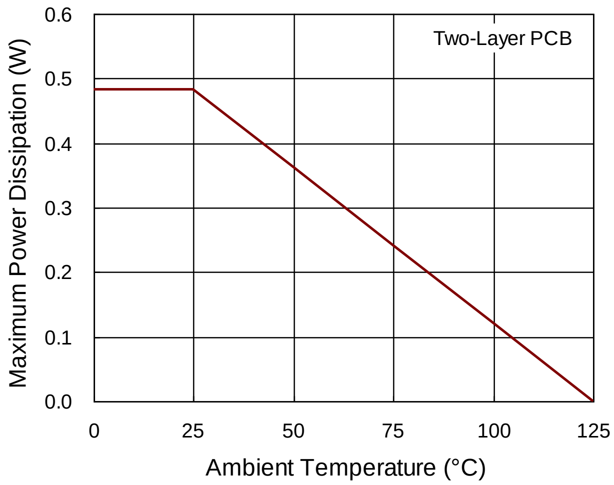


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when designing a PCB layout for switching power supply :

- The current path(1) from input capacitor, transformer, MOSFET, R_{CS} return to input capacitor is a high frequency current loop. The path(2) from GD pin, MOSFET, R_{CS} return to the ground of the IC is also a high frequency current loop. They must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path(3) between MOSFET ground(b) and IC ground(d) is recommended to be as short as possible, too.
- The path(4) from RCD snubber circuit to MOSFET is a high switching loop. Keep it as small as possible.
- The path(5) from input capacitor to HV pin is a high voltage loop. Keep a space from path(5) to other low voltage traces.
- It is good for reducing noise, output ripple and EMI issue to separate ground traces of input capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d). Finally, connect them together on input capacitor ground(a). The areas of these ground traces should be kept large.
- To minimize parasitic trace inductance and EMI, minimize the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor. In addition, apply sufficient copper area at the anode and cathode terminal of the diode for heat-sinking. It is recommended to apply a larger area at the quiet cathode terminal. A large anode area will induce high-frequency radiated EMI.

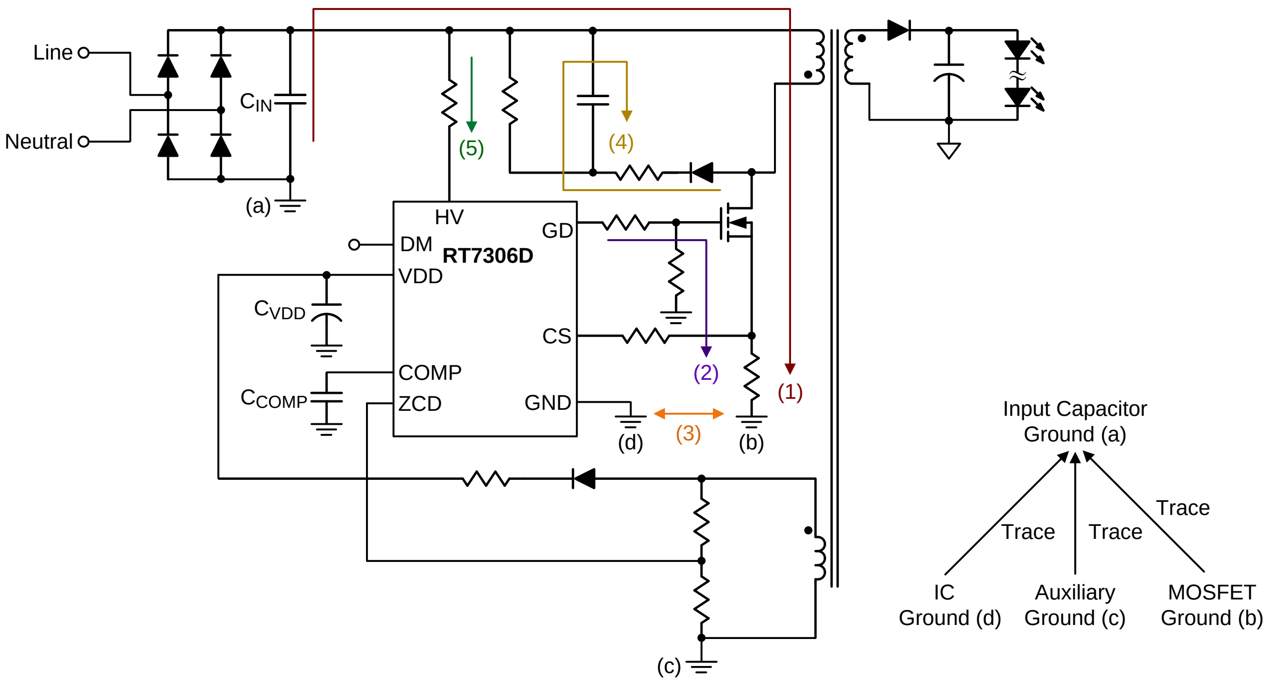
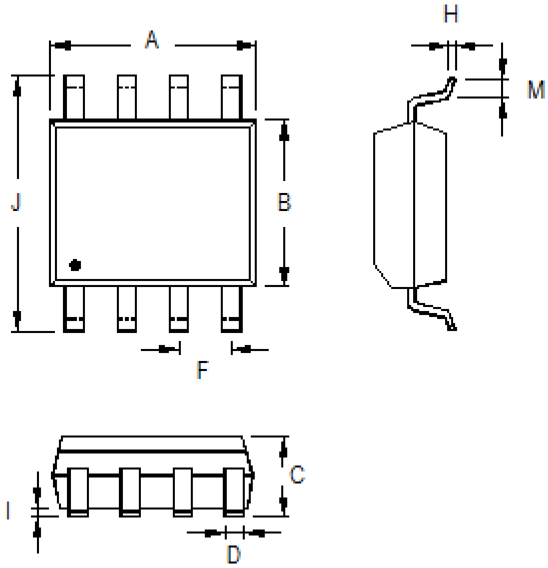


Figure 7. PCB Layout Guide

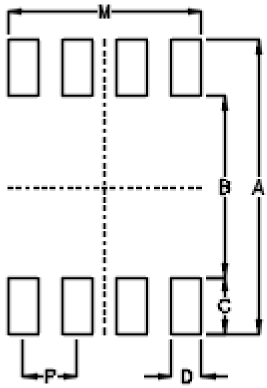
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-8	8	1.27	6.80	4.20	1.30	0.70	4.51	±0.10

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

单击下面可查看定价，库存，交付和生命周期等信息

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