

Integrated PMIC with 4-Channel Synchronous Buck Converters, 8 LDOs, and MTP Non-Volatile Memory for Industrial and Automotive Applications

General Description

The RTQ5115 is a highly-integrated low-power high-performance analog SOC with PMIC in one single chip designed for industrial/automotive applications.

The RTQ5115 includes four synchronous step-down DC-DC converters and eight LDOs for system power.

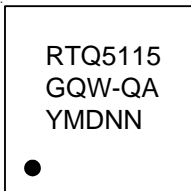
The RTQ5115 also embeds one EEPROM (MTP) for setting sequence and timing etc.

Additionally, the RTQ5115 PMIC also includes one IRQ report.

Applications

- Industrial/Automotive

Marking Information

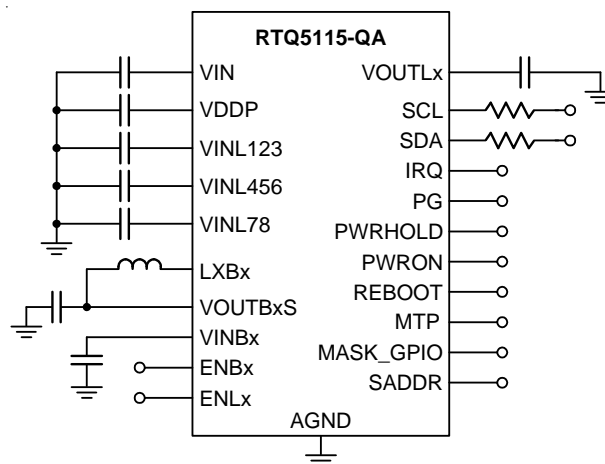


RTQ5115GQW-QA : Product Number
YMDNN : Date Code

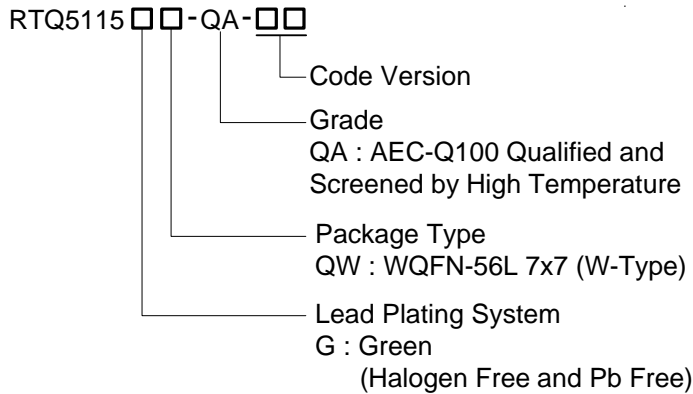
Features

- Input Voltage Operating Range is 3.15V to 5.5V
- Step-Down Regulator : V_{IN} Range is 3.15V to 5.5V
 - Max Current 2.4A/2A/1.6A/2A
 - Programmable Frequency from 500kHz to 2MHz
 - I²C Programmable Output Level
 - I²C Programmable Operation Mode (Force PWM or Auto PSM/PWM)
 - I²C Programmable Output Discharge Mode (Discharge or Floating)
- Linear Regulators : V_{IN} Range is 2.5V to 5.5V
 - Max Current 0.3A
 - I²C Programmable Output Level
- Embedded 32Bytes MTP for Factory Tuning
 - External MTP Pin for Write Protection
- Sequence can be Controlled by I²C or each EN pins Defined by MASK_GPIO Pin
- OT/UVP/VIN LV/POWRON Press Time Interrupt (IRQ)
 - I²C Control Interface : Support Fast Mode Up to 400kb/s
- AEC-Q100 Grade 2 Qualified
- RoHS Compliant and Halogen Free

Simplified Application Circuit



Ordering Information

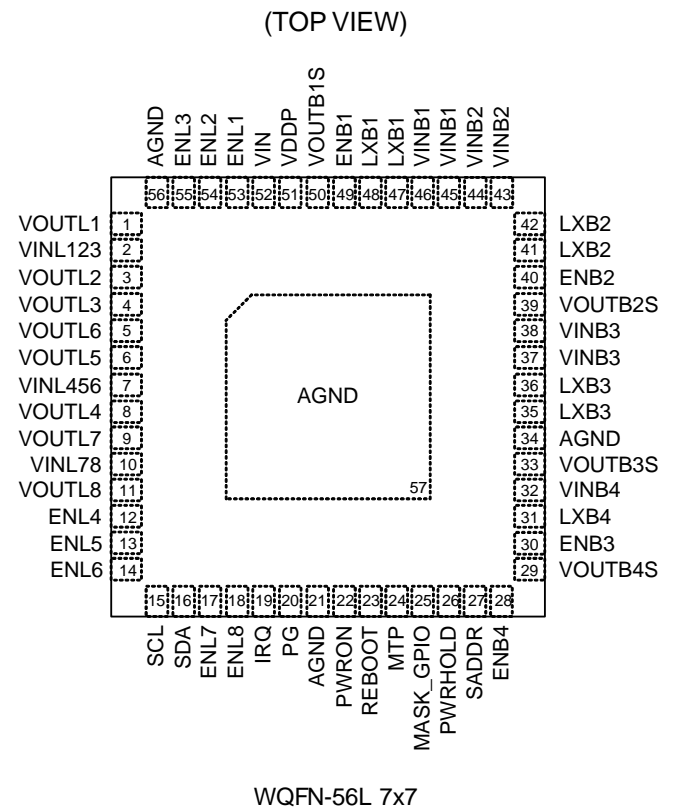


Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

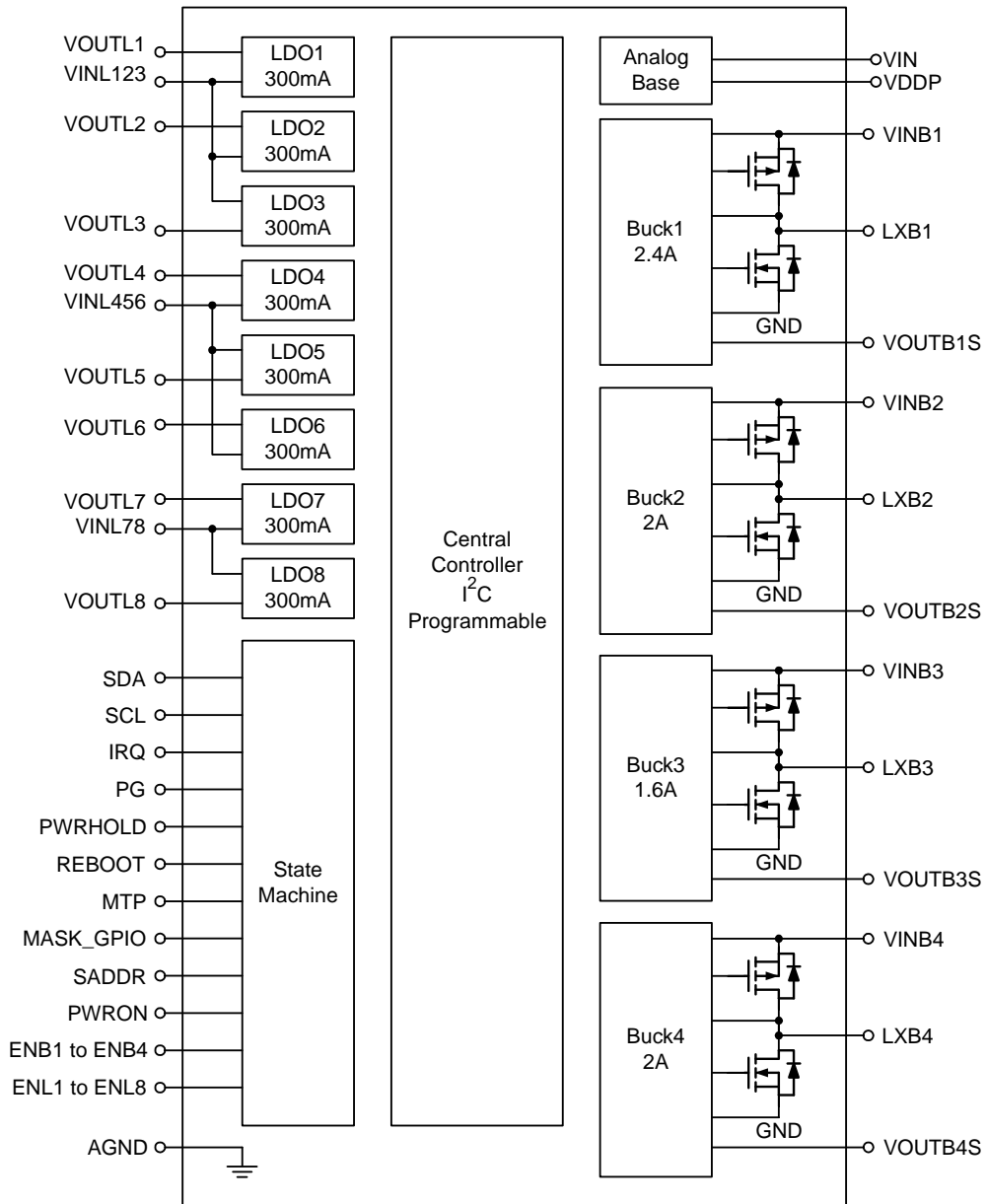


Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---------|----------|--|
| 1 | VOUTL1 | Output voltage regulation node for LDO1. |
| 2 | VINL123 | Input power for LDO1, LDO2 and LDO3. |
| 3 | VOUTL2 | Output voltage regulation node for LDO2. |
| 4 | VOUTL3 | Output voltage regulation node for LDO3. |
| 5 | VOUTL6 | Output voltage regulation node for LDO6. |
| 6 | VOUTL5 | Output voltage regulation node for LDO5. |
| 7 | VINL456 | Input power for LDO4, LDO5 and LDO6. |
| 8 | VOUTL4 | Output voltage regulation node for LDO4. |
| 9 | VOUTL7 | Output voltage regulation node for LDO7. |
| 10 | VINL78 | Input power for LDO7 and LDO8. |
| 11 | VOUTL8 | Output voltage regulation node for LDO8. |
| 12 | ENL4 | Enable control input for LDO4. |
| 13 | ENL5 | Enable control input for LDO5. |
| 14 | ENL6 | Enable control input for LDO6. |
| 15 | SCL | Clock input for I ² C. Open-drain output. |

| Pin No. | Pin Name | Pin Function |
|---------------------------------|-----------|--|
| 16 | SDA | Data input for I ² C. Open-drain output. |
| 17 | ENL7 | Enable control input for LDO7. |
| 18 | ENL8 | Enable control input for LDO8. |
| 19 | IRQ | Open-drain IRQ output node. |
| 20 | PG | Power good indicator. |
| 21, 34, 56, 57 (Exposed Pad) | AGND | Analog ground. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation. |
| 22 | PWRON | Manual power on. |
| 23 | REBOOT | System power reboot. |
| 24 | MTP | MTP write protection pin. Logic low is inhibited and logic high is permit to write. |
| 25 | MASK_GPIO | Select I ² C or EN pin for Bucks and LDOs. Connect a 100kΩ pull-low resistor. As MASK_GPIO is high, ignore all EN pins. As MASK_GPIO is low, EN pins and I ² C both can control. EN pins priority is higher than I ² C. |
| 26 | PWRHOLD | Power hold input. |
| 27 | SADDR | I ² C slave address. |
| 28 | ENB4 | Enable control input for Buck4. |
| 29 | VOUTB4S | Output voltage regulation node for Buck4. |
| 30 | ENB3 | Enable control input for Buck3. |
| 31 | LXB4 | Internal switch node to output inductor connection for Buck4. |
| 32 | VINB4 | Input power for Buck4. |
| 33 | VOUTB3S | Output voltage regulation node for Buck3. |
| 35, 36 | LXB3 | Internal switch node to output inductor connection for Buck3. |
| 37, 38 | VINB3 | Input power for Buck3. |
| 39 | VOUTB2S | Output voltage regulation node for Buck2. |
| 40 | ENB2 | Enable control input for Buck2. |
| 41, 42 | LXB2 | Internal switch node to output inductor connection for Buck2. |
| 43, 44 | VINB2 | Input power for Buck2. |
| 45, 46 | VINB1 | Input power for Buck1. |
| 47, 48 | LXB1 | Internal switch node to output inductor connection for Buck1. |
| 49 | ENB1 | Enable control input for Buck1. |
| 50 | VOUTB1S | Output voltage regulation node for Buck1 |
| 51 | VDDP | Internal bias regulator voltage. External load on this pin is not allowed. |
| 52 | VIN | Input power for analog base. |
| 53 | ENL1 | Enable control input for LDO1. |
| 54 | ENL2 | Enable control input for LDO2. |
| 55 | ENL3 | Enable control input for LDO3. |

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Analog Base Input Voltage, VIN ----- -0.3V to 6V
- PMIC Input Voltage, VINL123/456/78, VINB1/2/3/4 ----- -0.3V to 6V
- PMIC Output Voltage, VOUTLx, VOUTBxS, LXBx ----- -0.3V to 6V
- PMIC related Other Pins ----- -0.3V to 6V
- Power Dissipation, PD @ TA = 25°C
 WQFN-56L 7x7 ----- 3.7W
- Package Thermal Resistance (Note 2)
 WQFN-56L 7x7, θJA ----- 27°C/W
 WQFN-56L 7x7, θJC ----- 7°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 105°C

Electrical Characteristics

(TJ = -40°C to 105°C, VIN = 3.15V to 5.5V (Note 5, 6))

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------|--|------|-----|-----|------|
| AMR for VIN | | | -- | -- | 6 | V |
| Operation Voltage of VIN | | As fsw > 1MHz, 3.15V ≤ VIN ≤ 5.5V. If fsw ≤ 1MHz, VIN ≥ 4V. | 3.15 | -- | 5.5 | V |
| PMIC | | | | | | |
| Quiescent Current | IIN | VIN = 5V, LDOs, Bucks are ON with no load. Bucks operate in auto mode (Reg 0x06 = FFh) | 350 | 700 | 950 | µA |
| | | VIN = 5V, SCL = SDA = 0V, LDO and Bucks are OFF, Disable PMIC (Reg0x15[7] = 1) | 5 | 30 | 60 | |
| Warning for Die Temperature | OTW | Temperature 1 | -- | 100 | -- | °C |
| | | Temperature 2 | -- | 125 | -- | |
| Over-Temperature Protection | OTP | | -- | 165 | -- | °C |
| OTP and Warning Hysteresis | | | -- | 10 | -- | °C |
| Input Pull-Low 100kΩ Resistor | RLow | VIN = 5V, temperature = -40°C to 105°C | 70 | 115 | 160 | kΩ |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|--------------------|--|------|------|------|-----------|
| Buck1 to Buck4 | | | | | | |
| Input Voltage | V_{INB} | | 3.15 | -- | 5.5 | V |
| Consumption Current | I_{VINB} | AUTO mode $I_{OUT} = 0mA$, each Buck | 10 | 30 | 50 | μA |
| Output Voltage Accuracy | V_{OUTAcc} | $3.1V < V_{IN} < 5.5V$, $1mA < I_{OUT} < I_{MAX}$, $-40^{\circ}C < T_A < 105^{\circ}C$ | -3 | -- | 3 | % |
| Switching Frequency | f_{SW} | I ² C programmable | 0.5 | -- | 2.00 | MHz |
| Switching Frequency Accuracy | | $1MHz < f_{SW}$ | -10 | -- | 10 | % |
| | | $f_{SW} \leq 1MHz$ | -20 | -- | 20 | |
| Peak Current Limit | OCP | Buck1 | 3.1 | 4.4 | 5.8 | A |
| | | Buck2 | 2.8 | 4 | 5.2 | |
| | | Buck3 | 2.6 | 3.7 | 4.8 | |
| | | Buck4 | 2.8 | 4 | 5.2 | |
| Under-Voltage Protection | UVP | V_{OUTB1S} to $V_{OUTB4S} < 0.66 \times (V_{OUT}$ target) | 56 | 66 | 76 | % |
| Maximum Output Current | I_{MAX} | Buck1 | 2.4 | -- | -- | A |
| | | Buck2 | 2 | -- | -- | |
| | | Buck3 | 1.6 | -- | -- | |
| | | Buck4 | 2 | -- | -- | |
| High-Side On-Resistance | R_{pon} | $V_{IN} = 3.7V$ | 50 | 150 | 250 | $m\Omega$ |
| Low-Side On-Resistance | R_{non} | $V_{IN} = 3.7V$ | 40 | 110 | 160 | $m\Omega$ |
| LDO1 to LDO8 | | | | | | |
| Input Voltage for VINL123/456/78 | V_{INL} | | 2.5 | -- | 5.5 | V |
| Output Voltage LDO123/78 | V_{OUTL} | $3.1V \leq V_{IN} \leq 5.5V$, $50\mu A \leq I_{OUT} \leq I_{MAX}$ $-40 < T_A < 105^{\circ}C$ | -3 | -- | 3 | % |
| Output Voltage LDO456 | V_{OUTL} | $3.1V \leq V_{IN} \leq 5.5V$, $50\mu A \leq I_{OUT} \leq I_{MAX}$ $-40 < T_A < 105^{\circ}C$ | -3 | -- | 3 | % |
| Output Current | I_{OUT} | | 300 | -- | -- | mA |
| Output Short Current | I_{sht} | | 330 | 450 | 600 | mA |
| Voltage Difference | $V_{IN} - V_{OUT}$ | $V_{IN} > 3.1V$ | 0.05 | 0.10 | 0.30 | V |
| | | $V_{IN} > 2.5V$ | | | | |
| Supply Current | I_{SS} | $I_{OUT} = 0mA$ | 10 | 50 | 75 | μA |
| Shutdown Current | I_{OFF} | | 0 | 1 | 2 | μA |
| Control Input Pin Electrical Characteristics | | | | | | |
| Voltage Output Low | V_{OL} | | -- | -- | 0.4 | V |
| Input Voltage | High-Level | V_{IH} | 1.5 | -- | -- | V |
| | Low-Level | V_{IL} | -- | -- | 0.7 | |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|--------|---|-----|-----|-----|---------|
| PG Pin Electrical Characteristics | | | | | | |
| Output Low Voltage PG | | $I_{sink} = 1mA, V_{IN} = 3.15V \text{ to } 5.5V$ | -- | -- | 0.2 | V |
| Output High Leakage PG | | $T_A = 25^{\circ}C, V_{IN} = 3.15V \text{ to } 5.5V$ | -1 | 0 | 1 | μA |
| | | $T_A = 105^{\circ}C, V_{IN} = 3.15V \text{ to } 5.5V$ | -- | 0.1 | -- | |

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at $T_A = 25^{\circ}C$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

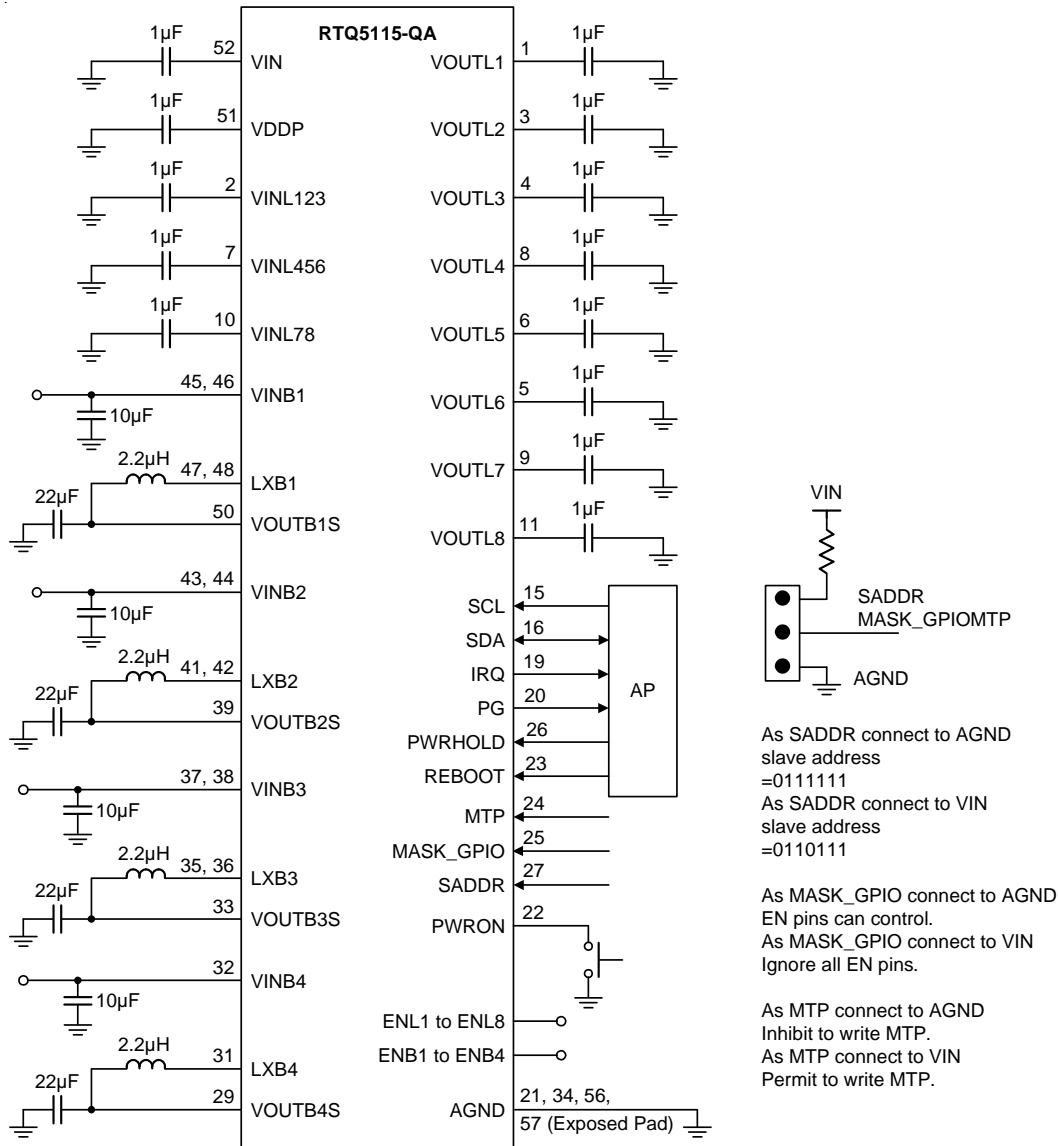
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Limits apply to the recommended operating temperature range of $-40^{\circ}C$ to $105^{\circ}C$, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_A = 25^{\circ}C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply : $V_{IN} = 3.15V \text{ to } 5.5V$.

Note 6. In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX} = 125^{\circ}C$), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta_{JA}}$), as given by the following equation : $T_{A-MAX} = T_{J-MAX} - (R_{\theta_{JA}} \times P_{D-MAX})$.

Typical Application Circuit

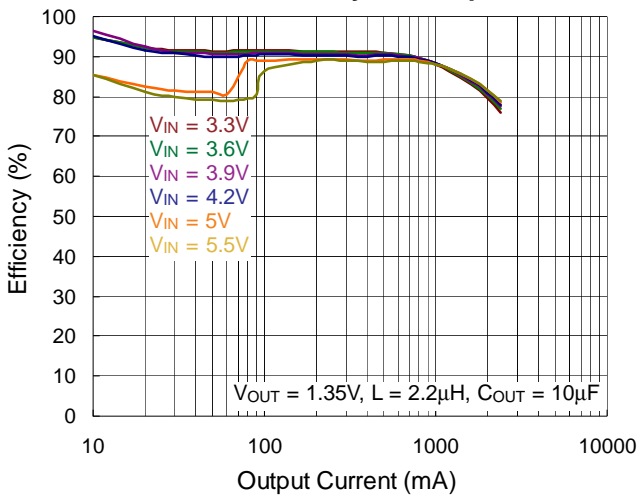


Suggested Components for Typical Application Circuit

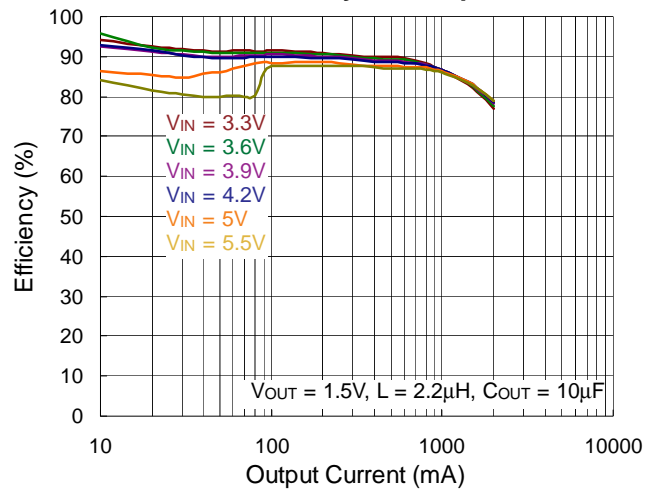
| Description | Part Number | Manufacturer |
|---|-------------------|--------------|
| Inductor for Buck-2.2µH | MDWK4040T2R2MMV | TAIYO |
| | NRS5030T2R2NMGJV | TAIYO |
| C _{IN} for Buck-10µF | C1206X7R1E516DT | Murata |
| | EMK316AB7106KL-T | TAIYO |
| C _{OUT} for Buck-22µF | C1206X7R22E416DT | Murata |
| | JMK316AB7226KL-TR | TAIYO |
| C _{IN} /C _{OUT} for LDO-1µF | C0603X7R1E216DT | Murata |
| | EMK107B7105KA-T | TAIYO |

Typical Operating Characteristics

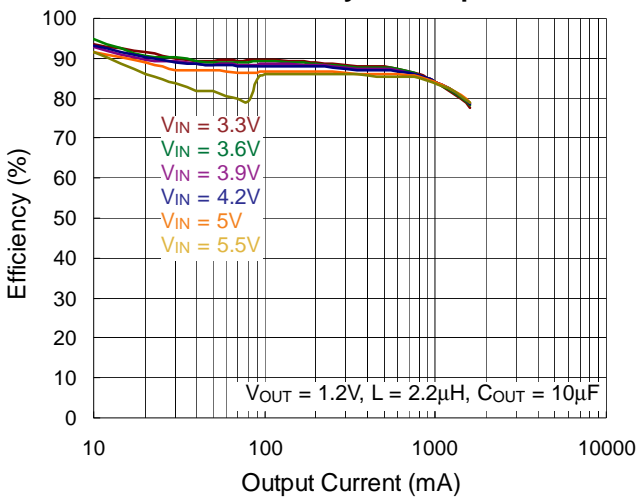
CH1 Buck Efficiency vs. Output Current



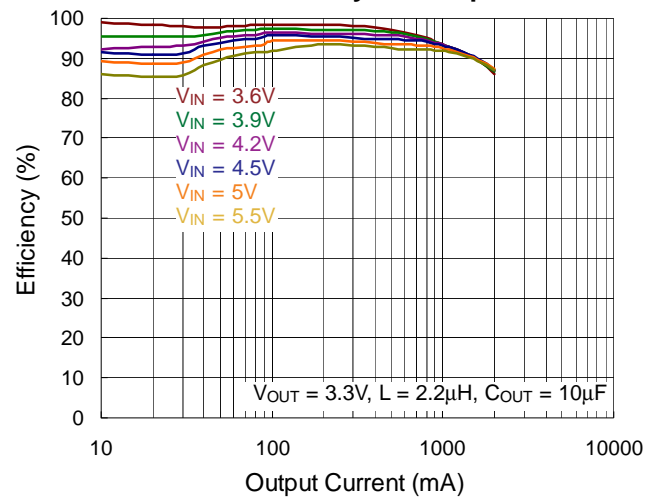
CH2 Buck Efficiency vs. Output Current



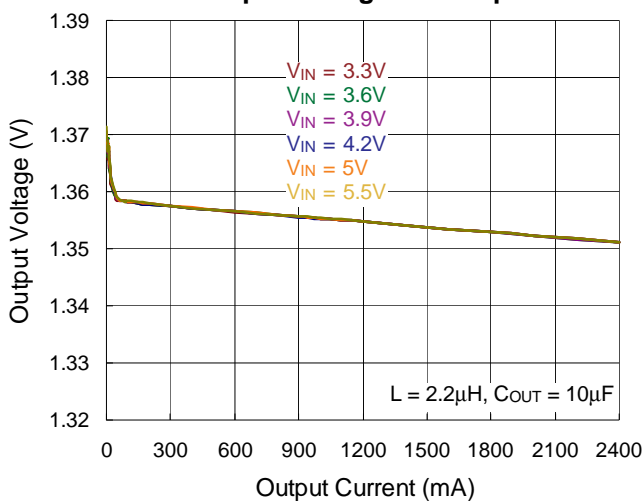
CH3 Buck Efficiency vs. Output Current



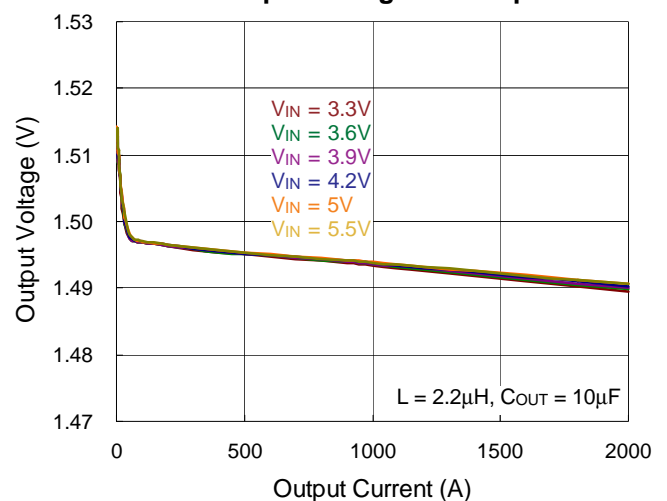
CH4 Buck Efficiency vs. Output Current



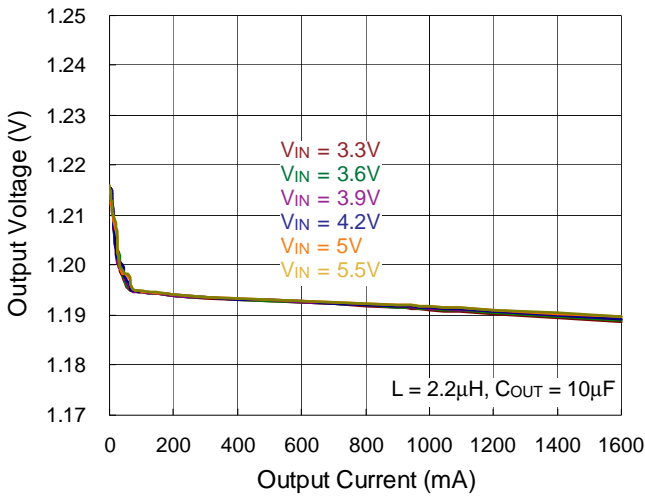
CH1 Buck Output Voltage vs. Output Current



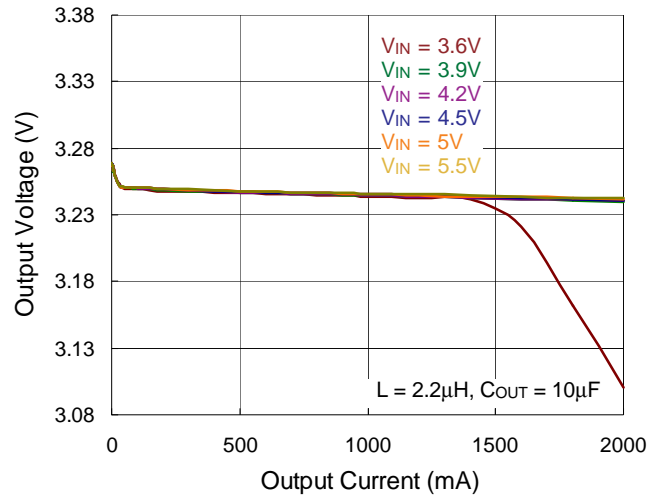
CH2 Buck Output Voltage vs. Output Current



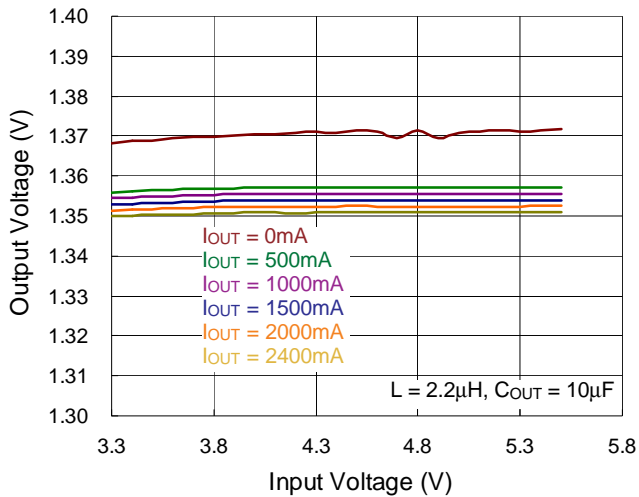
CH3 Buck Output Voltage vs. Output Current



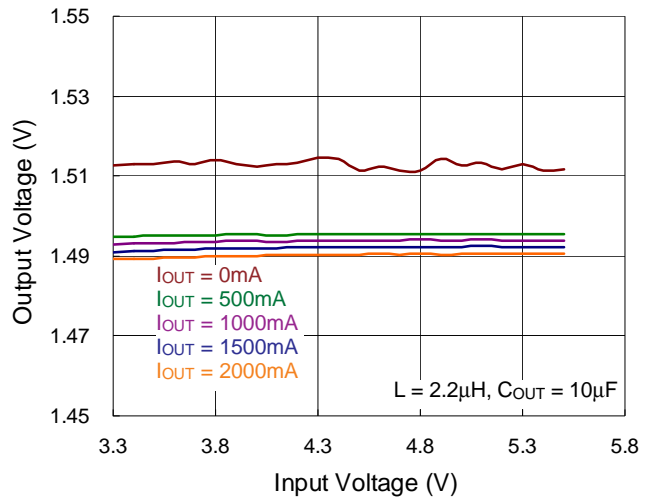
CH4 Buck Output Voltage vs. Output Current



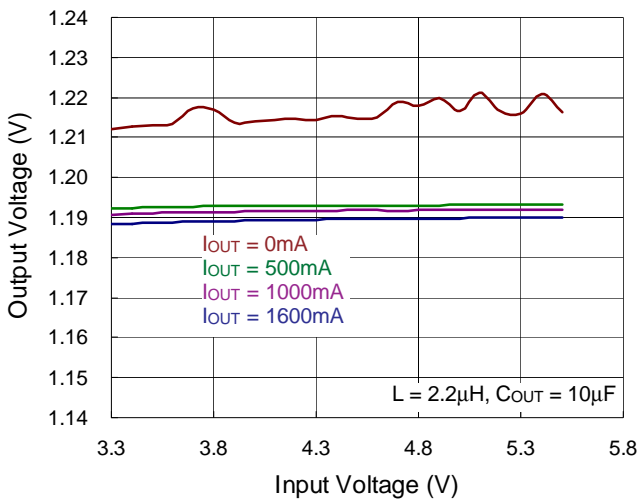
CH1 Buck Output Voltage vs. Input Voltage



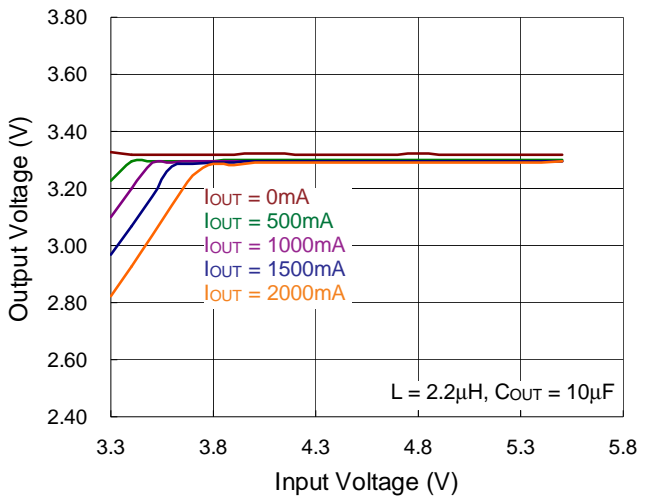
CH2 Buck Output Voltage vs. Input Voltage



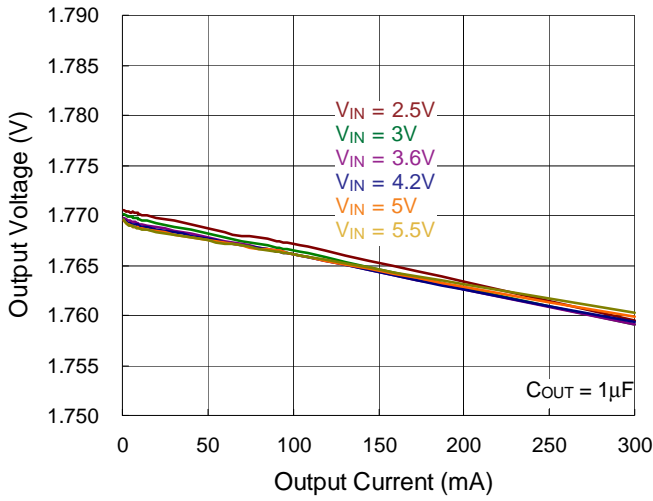
CH3 Buck Output Voltage vs. Input Voltage



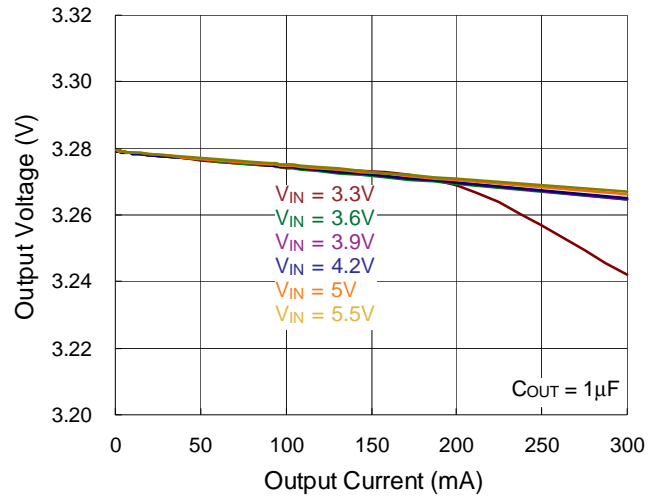
CH4 Buck Output Voltage vs. Input Voltage



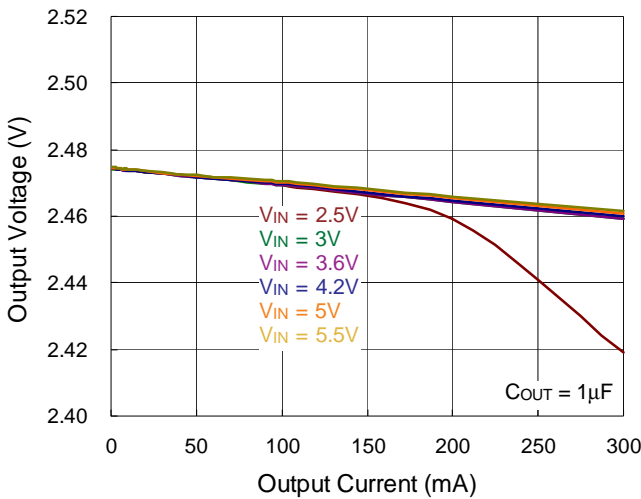
LDO2 Output Voltage vs. Output Current



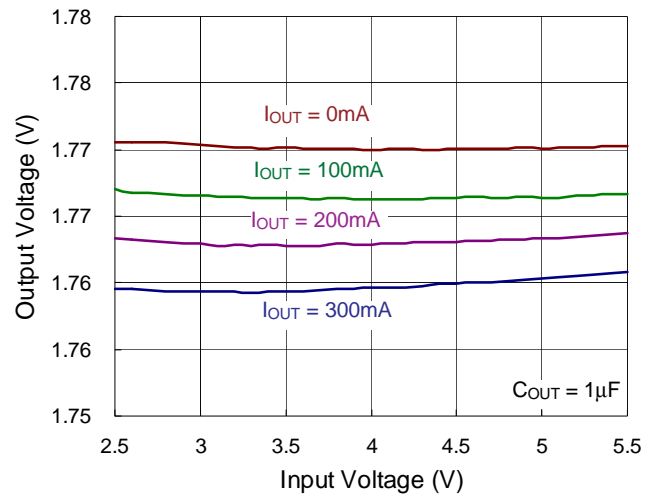
LDO5 Output Voltage vs. Output Current



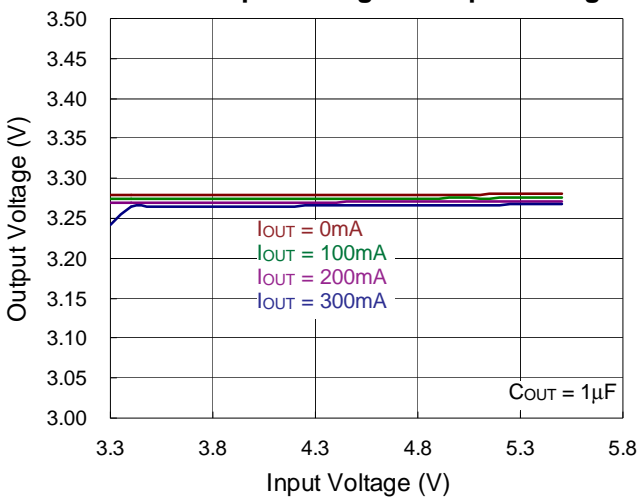
LDO7 Output Voltage vs. Output Current



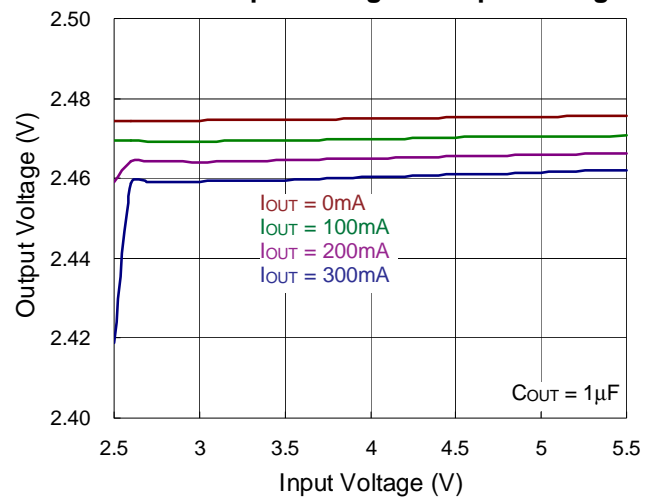
LDO2 Output Voltage vs. Input Voltage



LDO5 Output Voltage vs. Input Voltage



LDO7 Output Voltage vs. Input Voltage



Application Information

The RTQ5115 is a highly-integrated solution for automotive system including PMIC and memory system. The RTQ5115 application mechanism and I²C compatible interface are introduced in later sections. The system's slave address is 0110111 (As SADDR = high) or 0111111 (As SADDR = low).

PMIC - Power management system provides 8 low dropout linear regulator and 4 high efficiency synchronous step-down DC-DC converters. Power-On and Power-Off sequences are control by PWRON and REBOOT input

pins. Detail time sequence control is described in Power ON/OFF diagram. The I²C interface can program individual regulator output voltage as well as on/off control and voltage setting.

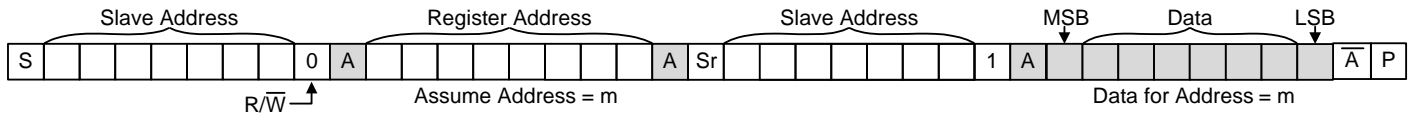
I²C Interface Timing Diagram

The RTQ5115 acts as an I²C -bus slave. The I²C-bus master configures the settings for all function blocks by sending command bytes to the RTQ5115 via the 2-wire I²C-bus. The I²C timing diagrams are list in the following.

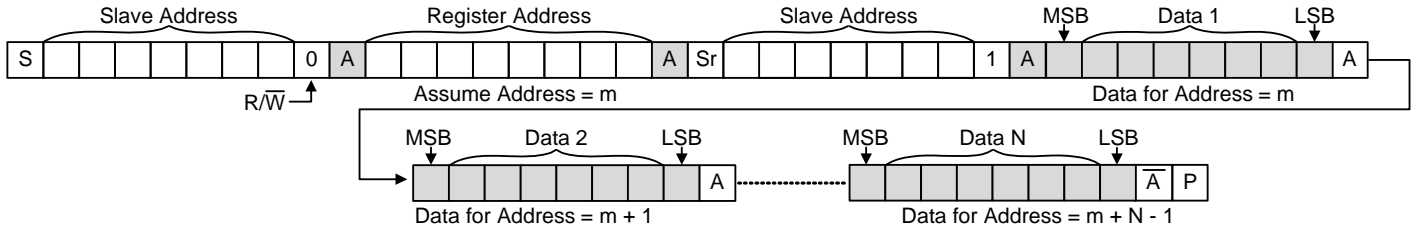
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|---------------------|---------------------------|-----|-----|-----|------|
| I²C Interface Electrical Characteristics | | | | | | |
| SDA, SCLK Input High Level Threshold | | | 1.5 | -- | -- | V |
| SDA, SCLK Input Low Level Threshold | | | -- | -- | 0.4 | V |
| SCLK Clock Rate | f _{SCL} | | -- | -- | 400 | kHz |
| Hold Time (Repeated) START Condition. After this period, the first clock pulse is generated | t _{HD;STA} | | 0.6 | -- | -- | μs |
| LOW Period of the SCL Clock | t _{LOW} | | 1.3 | -- | -- | μs |
| HIGH Period of the SCL Clock | t _{HIGH} | | 0.6 | -- | -- | μs |
| Set-Up Time for a Repeated START Condition | t _{SU;STA} | | 0.6 | -- | -- | μs |
| Data Hold Time | t _{HD;DAT} | | 0 | -- | 0.9 | μs |
| Data Set-Up Time | t _{SU;DAT} | | 100 | -- | -- | ns |
| Set-Up Time for STOP Condition | t _{SU;STO} | | 0.6 | -- | -- | μs |
| Bus Free Time Between a STOP and START Condition | t _{BUF} | | 1.3 | -- | -- | μs |
| Rise Time of Both SDA and SCL Signals | t _R | | 20 | -- | 300 | ns |
| Fall Time of Both SDA and SCL Signals | t _F | | 20 | -- | 300 | ns |
| SDA and SCL Output Low Sink Current | I _{OL} | SDA or SCL voltage = 0.4V | 2 | -- | -- | mA |

Read and Write Function

Read single byte of data from Register



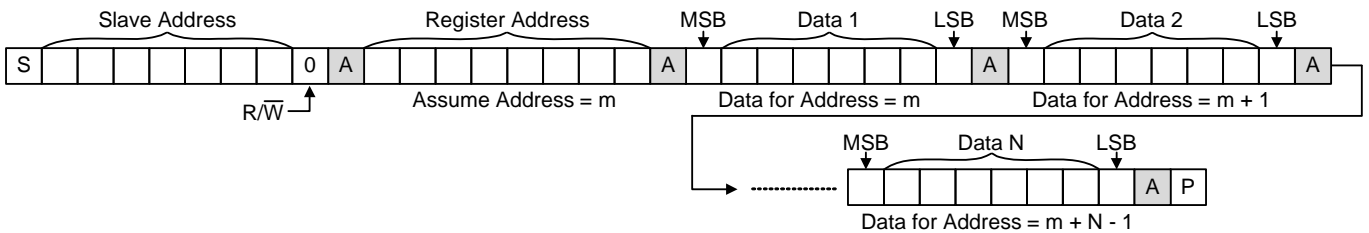
Read N bytes of data from Registers



Write single byte of data to Register

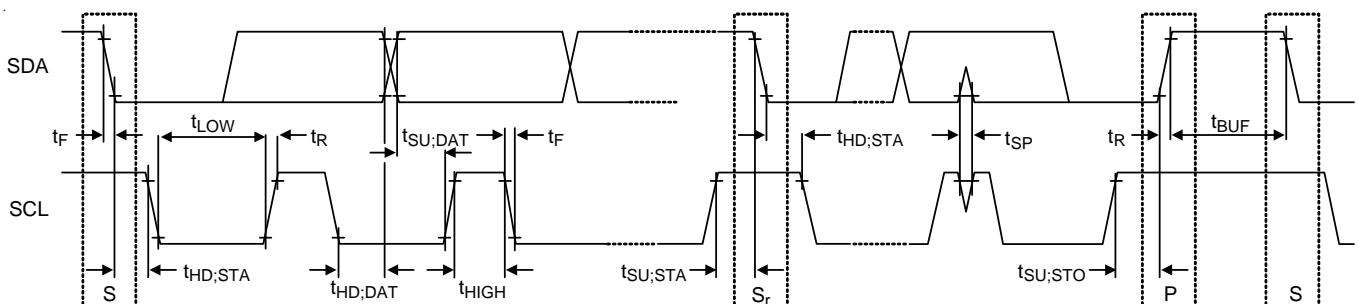


Write N bytes of data to Registers



□ Driven by Master, ■ Driven by Slave, □ P Stop, □ S Start, □ Sr Repeat Start

I²C Waveform Information



PMIC

Power Channels Control Methodology

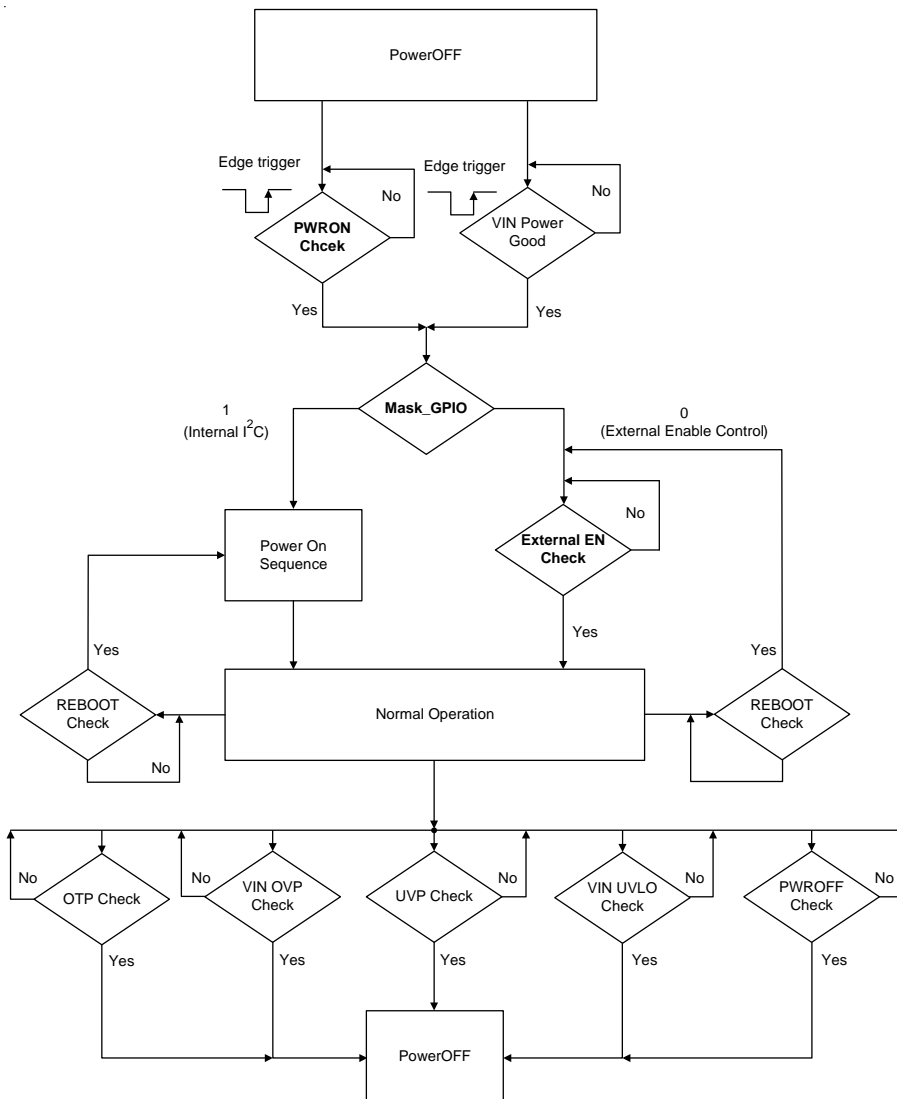
When VIN power Good or PWRON event occurs, the PMIC will follow the power on sequence to turn on channels. During normal operation, users can use the REBOOT pin to restart PMIC again. Another PWROFF event, OTP or UVP occurs, PMIC will execute the power off. In the RTQ5115 PMIC, the UVP event will be set out when the Buck1 to Buck4s' output voltage is lower than $1/2 \times (V_{OUT})$.

VIN Over-Voltage Protection

The device has a built-in OVP circuit which monitors the

input voltage. If the voltage exceeds the OVP threshold (typ value = 5.95V), the device stops operating. As soon as the voltage drops below the low threshold (typ value = 5.65V), the device starts to operate again. Therefore, over-voltage protection is implemented to prevent the input voltage from exceeding critical values to damage the device.

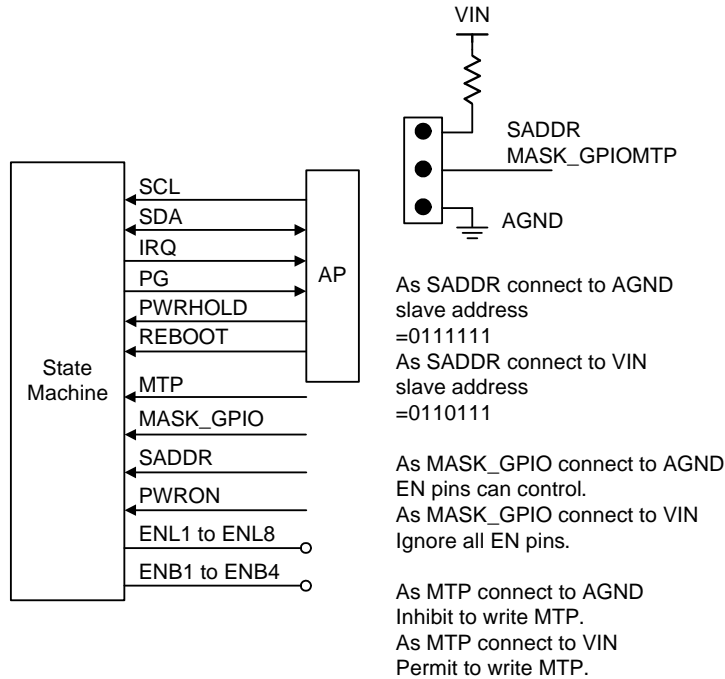
Base on ISO 7637 test case, if VIN vary violently, the device will trigger UVP or OVP (VIN rising up slew rate should be less than 5V/1ms) and then stops operating. The device needs to do power reset (VIN < 1.7V) to resume operation.



OTP function can be controlled by 0x16[2]
 VOUT UVP function can be controlled by 0x16 [7:4]
 VIN_UVLO threshold can be controlled by 0x 0x12[7:5]

PMIC - POWER ON/OFF Setting

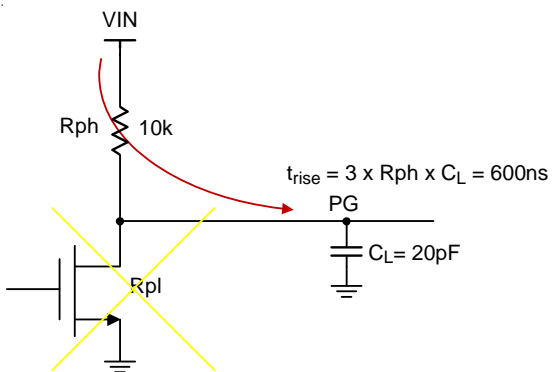
The circuit setting for communication between the RTQ5115 and AP is showed as below.



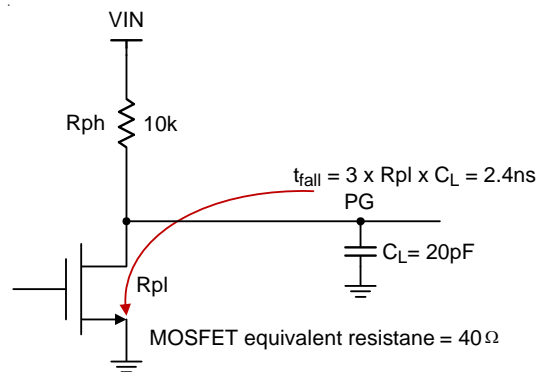
PG Pin

The PG comparator features an open drain output. The PG pin pull high to input voltage with 10kΩ which slew rate define as follow.

PG Rising Slew Rate



PG Falling Slew Rate



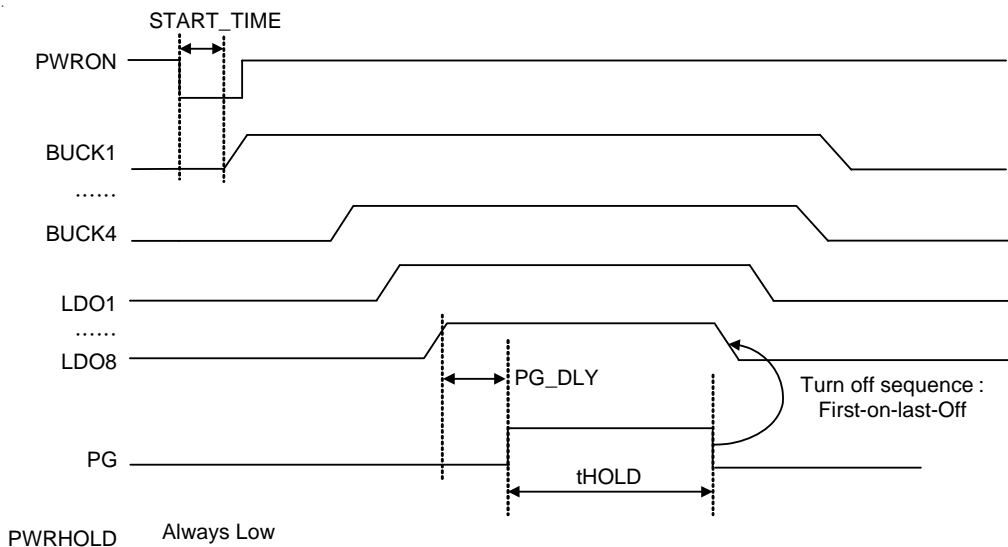
GPIO Pin Pull-Up/Down Defined

| Pin No. | Pin Name | GPIO Pin Pull-Up/Down Defined | Resistor |
|---------|----------|--|----------|
| 12 | ENL4 | Internal 100kΩ pull low resistor | Internal |
| 13 | ENL5 | Internal 100kΩ pull low resistor | Internal |
| 14 | ENL6 | Internal 100kΩ pull low resistor | Internal |
| 15 | SCL | Open drain, need to connect pull up resistor with range from 2.2kΩ to 10kΩ | External |
| 16 | SDA | Open drain, need to connect pull up resistor with range from 2.2kΩ to 10kΩ | External |
| 17 | ENL7 | Internal 100kΩ pull low resistor | Internal |
| 18 | ENL8 | Internal 100kΩ pull low resistor | Internal |
| 22 | PWRON | Internal 100kΩ pull up resistor | Internal |
| 23 | REBOOT | Internal 100kΩ pull low resistor | Internal |
| 24 | MTP | Internal 100kΩ pull low resistor | Internal |
| 26 | PWRHOLD | Internal 100kΩ pull low resistor | Internal |
| 27 | SADDR | Internal 100kΩ pull low resistor | Internal |
| 28 | ENB4 | Internal 100kΩ pull low resistor | Internal |
| 30 | ENB3 | Internal 100kΩ pull low resistor | Internal |
| 40 | ENB2 | Internal 100kΩ pull low resistor | Internal |
| 49 | ENB1 | Internal 100kΩ pull low resistor | Internal |
| 53 | ENL1 | Internal 100kΩ pull low resistor | Internal |
| 54 | ENL2 | Internal 100kΩ pull low resistor | Internal |
| 55 | ENL3 | Internal 100kΩ pull low resistor | Internal |

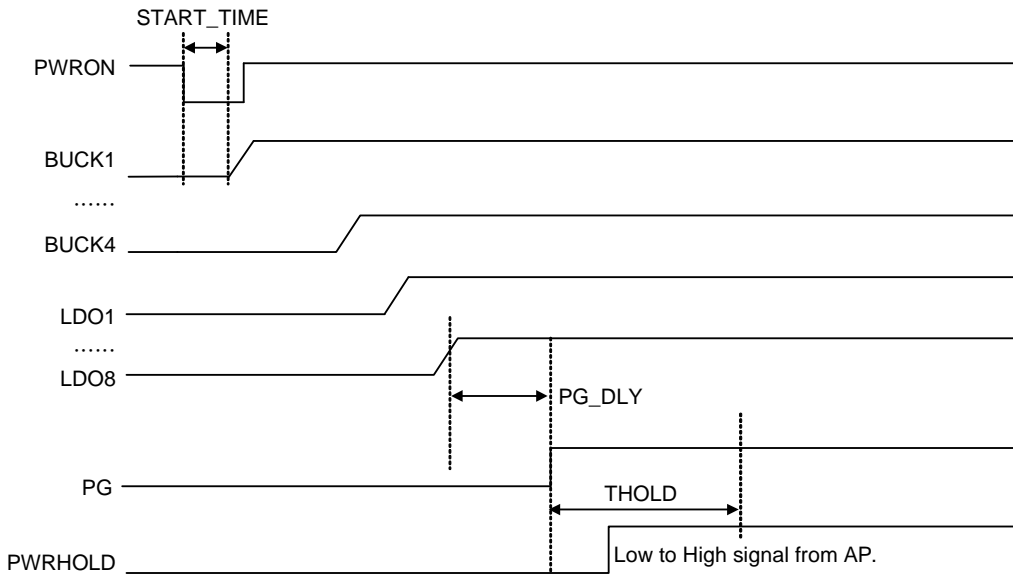
Power Hold Function

When the "PWRHOLD" signal does not come during THOLD time, the RTQ5115 will do shutdown sequence.

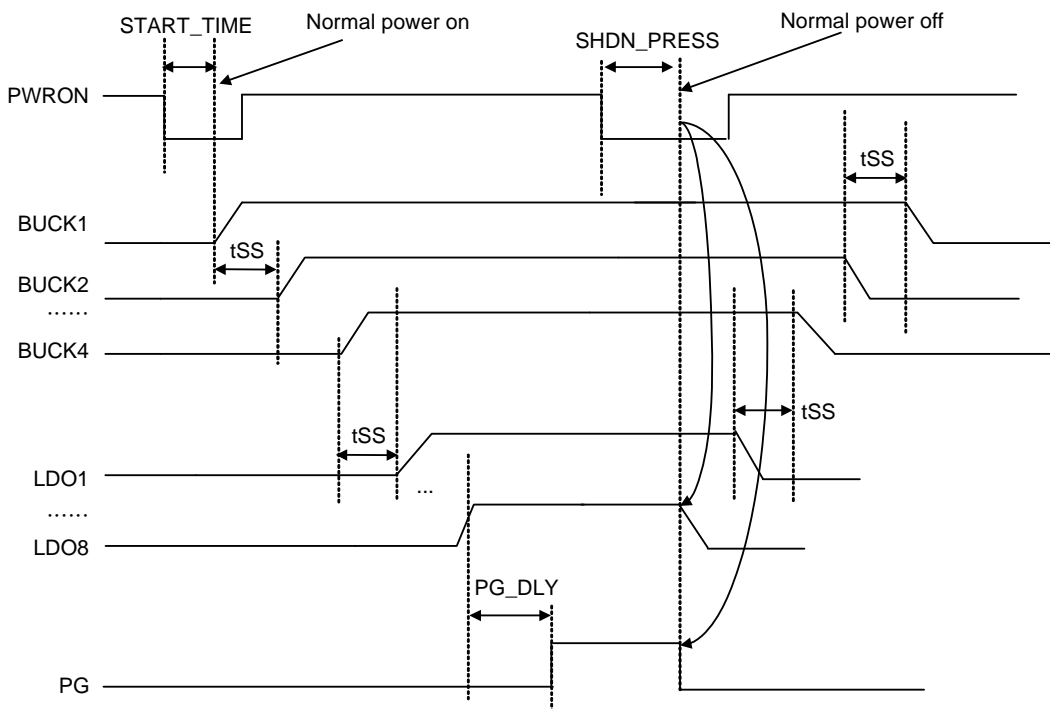
If users want to disable power hold function, set "DisTHOLD" bit in I²C register 0x10 bit[0] to disable this function. In the timing diagram below, the "THOLD" and "PG_DLY" can be set by MTP program.



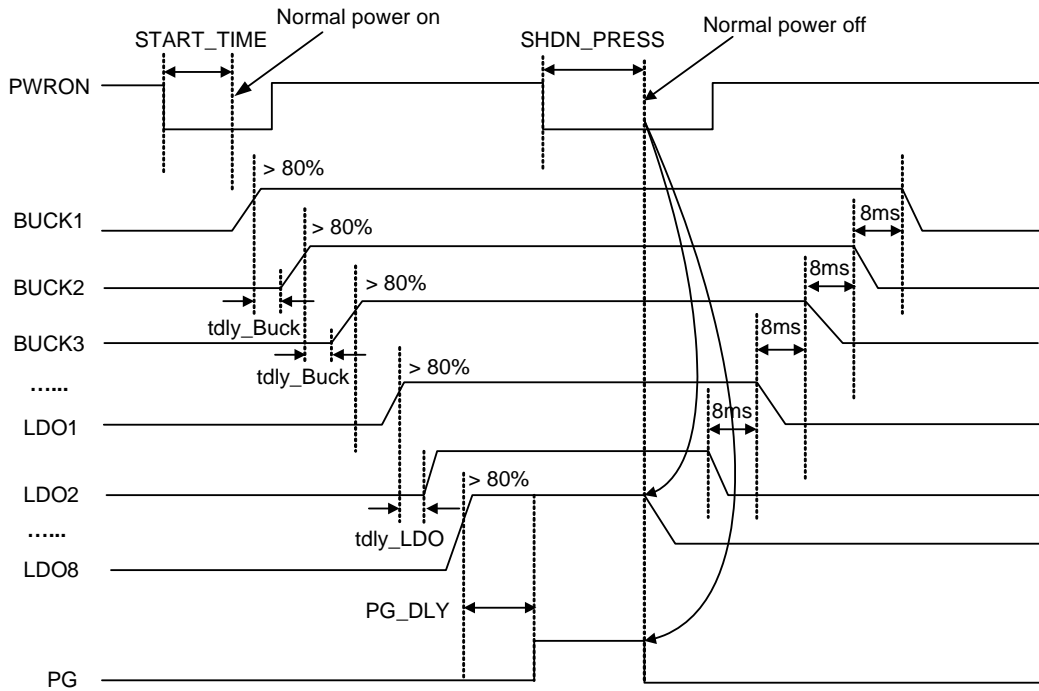
When AP sends the "PWRHOLD" signal during THOLD time, the RTQ5115 will keep power-on.



Timing Based ON/OFF Sequence (PWRON_NORMOFF_EN, Reg0x15[0] = 1)



Level Based ON/OFF Sequence (PWRON_NORMOFF_EN, Reg0x15[0] = 1)



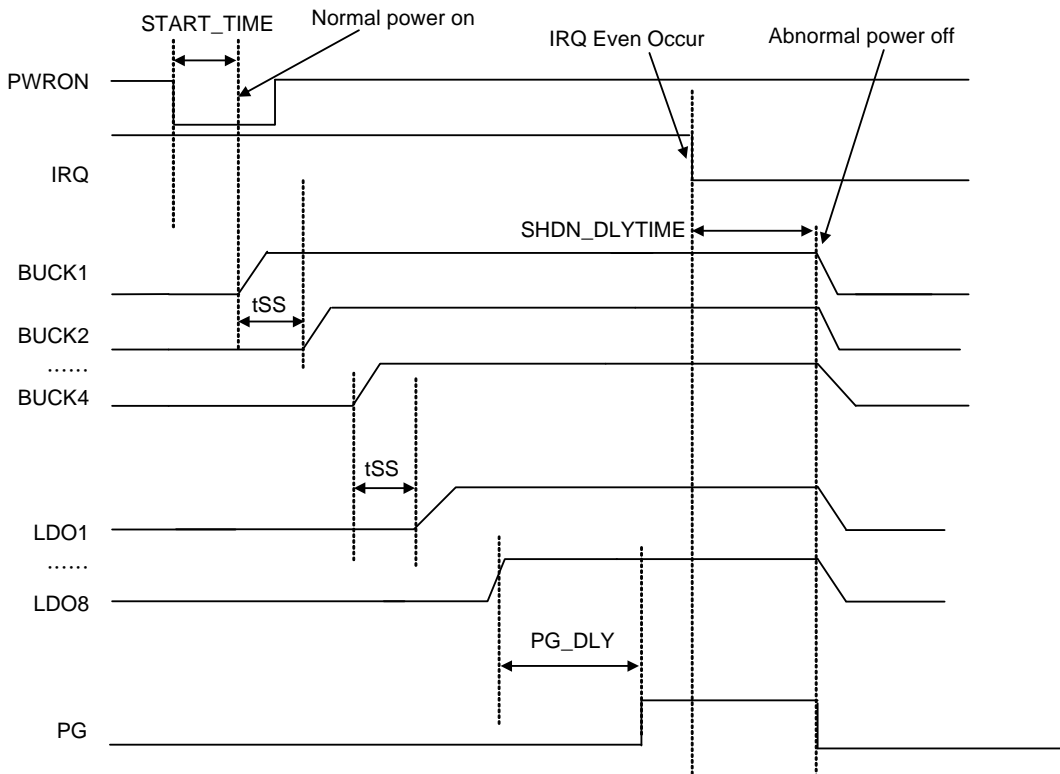
Note.

Sequence : BUCK1→BUCK2→BUCK3→BUCK4→LDO1→LDO2→LDO3→LDO4→LDO5→LDO6→LDO7→LDO8

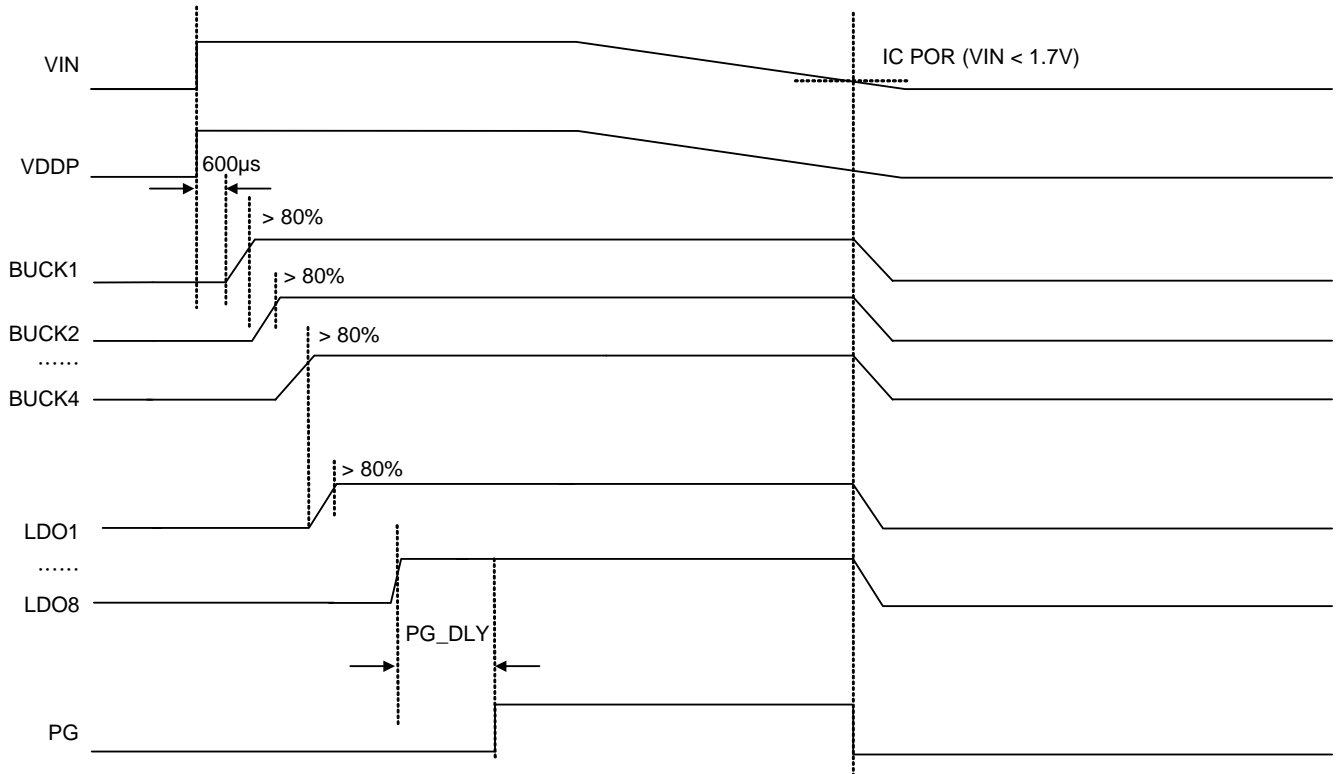
$t_{dy_Buck} : 192 \times (1/f_{sw}) + 40\mu s \pm 35\%$

$t_{dy_LDO} : 110\mu s \pm 20\%$ (If previous one channel is Buck, additional delay time $32 \times (1/f_{sw})$ need to be added to t_{dy_LDO} .)

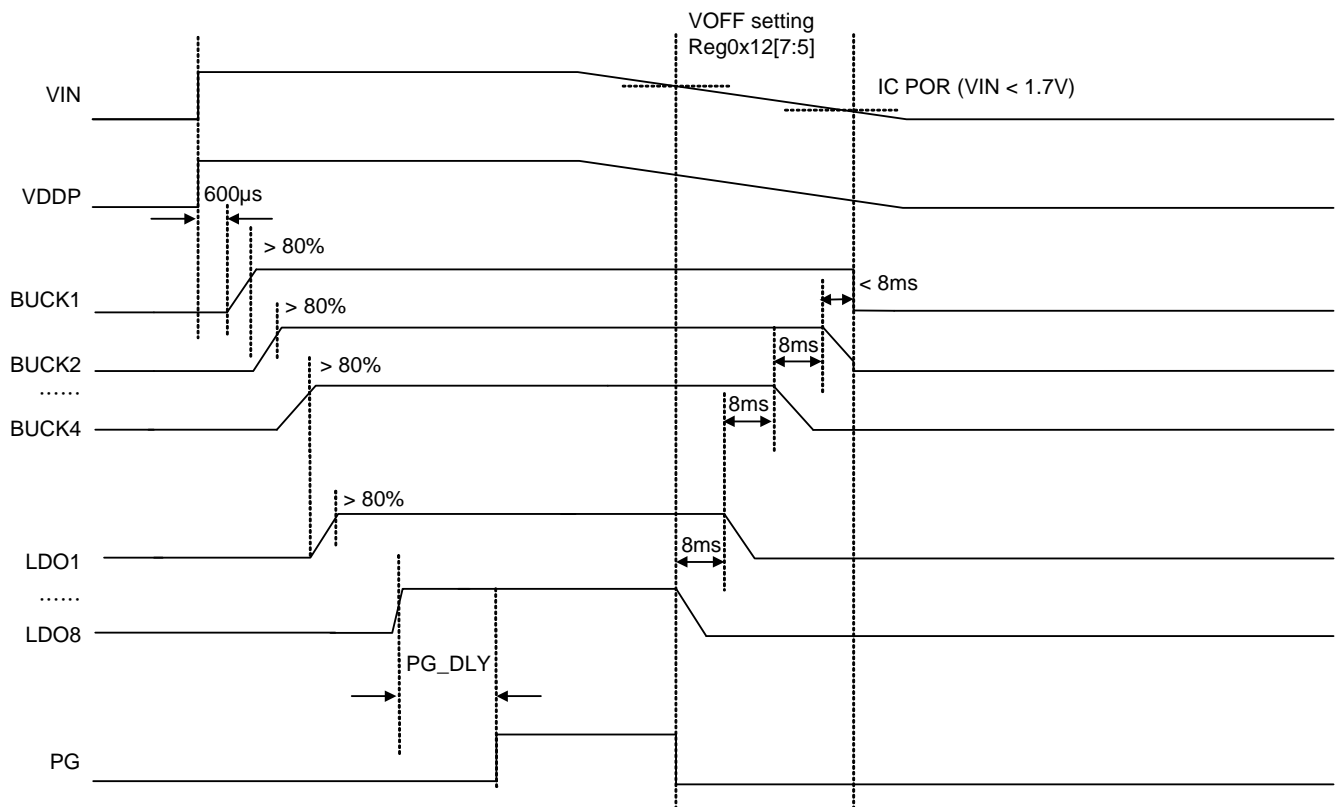
Abnormal OFF (OTP, Buck 1/2/3/4 UVP)



Based ON/OFF Sequence by VIN (VINLV_ENSHDN, Reg0x16[1] = 0)



(VINLV_ENSHDN, Reg0x16[1] = 1; VINLV_SEQ_EN, Reg0x16[0] = 1)



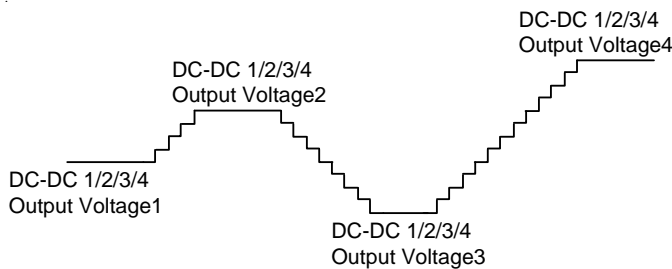
PMU On/Off Sequence Setting

In the RTQ5115, users can set the power on/off sequence and output voltage by I²C register 0x01 to 0x04 for Buck output voltage, 0x07 to 0x0E for LDO output voltage and 0x2C to 0x32 for startup sequence setting.

Synchronous Step-Down DC-DC Converter

Four current mode synchronous step-down DC-DC converters operate with internal power MOSFETs and compensation network. These channels supply the power core chip of portable system. They can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple. The operating frequency range of step-down converter is 0.5MHz to 2MHz.

Four step-down converters have RAMP control function as the following diagram.



Input and Output Capacitors Selection

The RTQ5115 is designed to work with low ESR ceramic capacitors. The *effective* value of these capacitors is defined as the actual capacitance under voltage bias and temperature. All ceramic capacitors have a large voltage coefficient, in addition to normal tolerances and temperature coefficients. Under D.C. bias, the capacitance value drops considerably. Larger case sizes or higher voltage capacitors are better in this regard. To help mitigate these effects, multiple small capacitors can be used in parallel to bring the minimum *effective* capacitance up to the desired value.

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. A low ESR input capacitor with larger ripple current rating should be used for the maximum RMS current. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2V_{OUT}, where I_{RMS} = I_{OUT} / 2. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to either further derate the capacitor or choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design. The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple, load step transients, and the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be examined by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since DIL increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part. Page 8 shows the nominal values of input/output capacitance recommended for the RTQ5115.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔIL increases with higher VIN and decreases with higher inductance :

$$\Delta I_L = \left[\frac{V_{OUT}}{f_{OSC} \times L} \right] \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor. A reasonable starting point for selecting the ripple current is ΔIL = 0.4 (IMAX). The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f_{OSC} \times \Delta I_L(MAX)} \right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or permalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. However, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation.

Ferrite core material saturates "hard" which means that inductance collapses abruptly when the peak design current is exceeded.

This results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depend on the price vs. size requirements and any radiated field/EMI requirements.

REBOOT Function

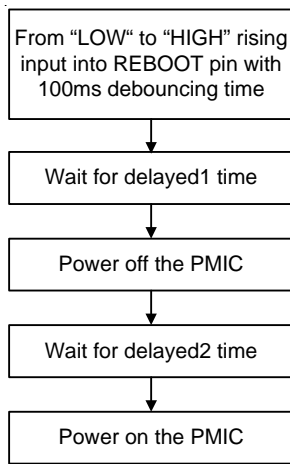
As the REBOOT pin is set from low to high, the REBOOT function will be active. The REBOOT's FSM is shown as below. It concludes 100ms de-bouncing time and delay1/delay2 power off delay time.

Table 1. REBOOT Input Control Setting

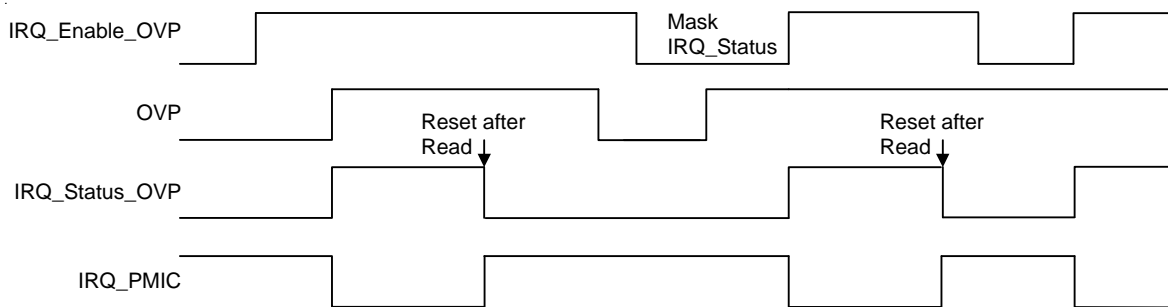
| | Description | Default |
|----------|---|---------|
| delayed2 | 00 : 100ms 10 : 1s | Option |
| delayed1 | 01 : 500ms 11 : 2s | Option |
| Action | delayed1 power-off then delayed2 power-on PMIC | |

IRQ Table

We summarize all IRQ items in the register table. All IRQ_status registers are implemented as reset after read. If IRQ_enable bit is Low, the IRQ_status bit will not update status. IRQ_enable will mask IRQ_status to trigger IRQ_PMIC Low, so the system can decide which interrupt is necessary.



Waveform - (when the other IRQ_status are low)



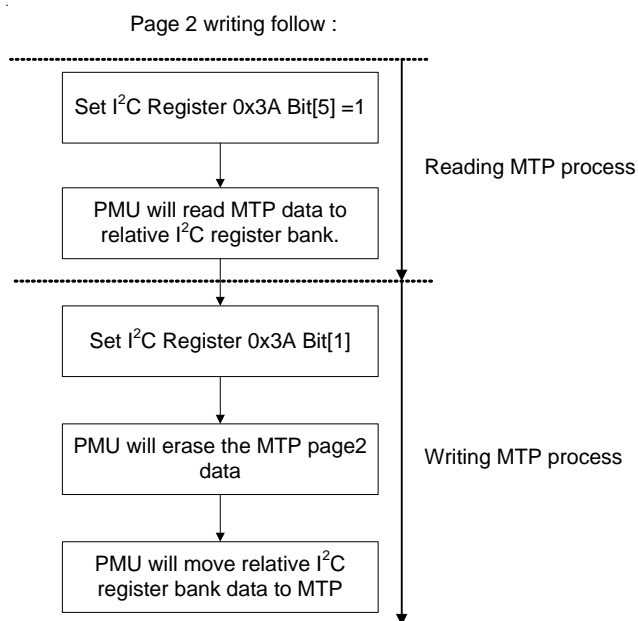
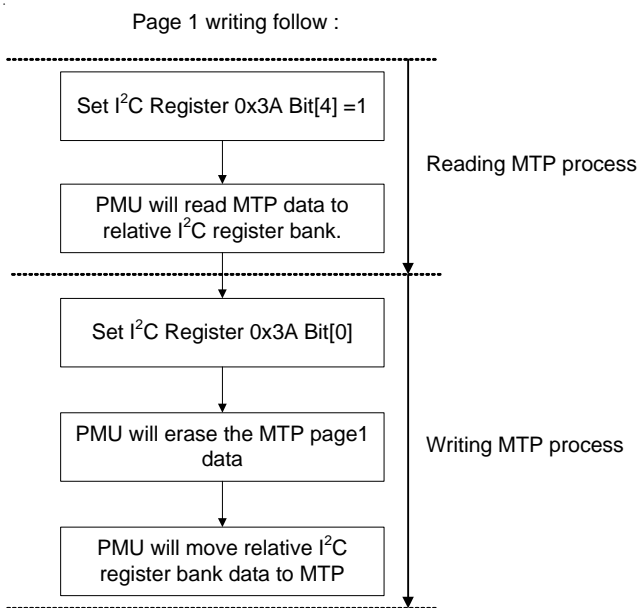
Waveform - (when the other IRQ_status are low)

* OTW125/OTW100 means the 125°C/100°C pre-warming over-temperature.

EEPROM (MTP) Control Flow

The RTQ5115 embeds 32 bytes MTP memory, and it allows users to save some I²C register bank data to MTP. When the I²C register 0x3A Bit[0]/Bit[1] is wrote to "1", the MTP Page1/Page2 will execute erase process firstly.

Because the erase process will be done in every writing time, the MTP data will be missed. So it would be best for users to read data from MTP to I²C first before executing writing process.



Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-56L 7x7 package, the thermal resistance, θ_{JA} , is 27°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (27^\circ\text{C/W}) = 3.7\text{W for a WQFN-56L 7x7 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

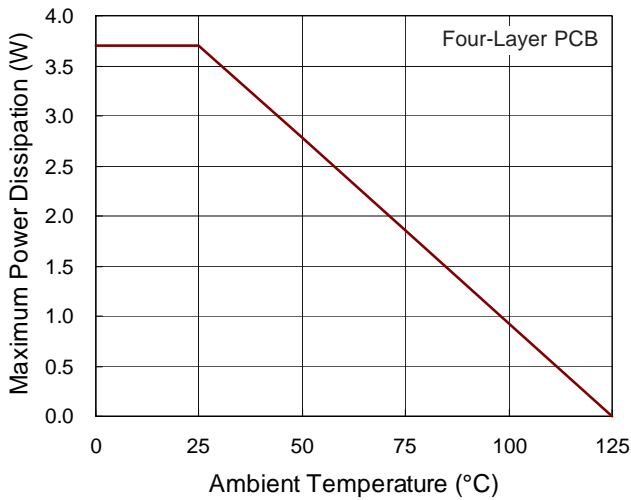


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RTQ5115, the following PCB layout guidelines must be strictly followed.

- ▶ Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- ▶ Keep the main power traces as wide and short as possible.
- ▶ The switching node area connected to LX and inductor should be minimized for lower EMI.
- ▶ Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- ▶ Directly connect the output capacitors to the feedback network of each channel to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

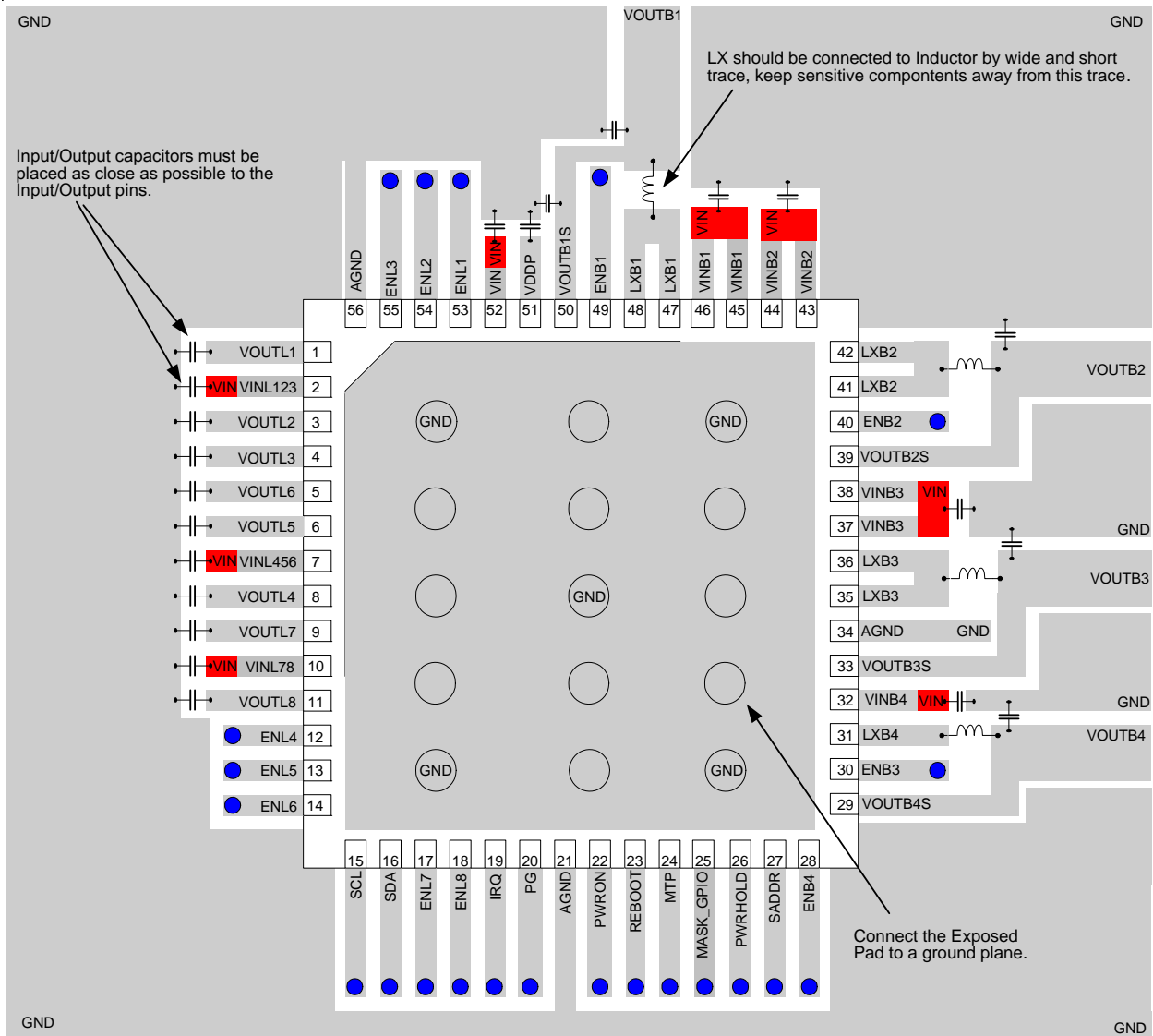


Figure 2. PCB Layout Guide

Table 2. I²C Register Table

| Detail Description | | | | |
|--------------------|------------------|--|------------|-------------|
| Address | 00 | Device ID | | |
| Bit | Name | Description | Read/Write | Reset Value |
| [7:4] | VENDOR_ID | Vendor Identification : Telechips : 1000b | R | 1000 |
| [3:0] | CHIP_REV | Chip Revision | R | 0110 |
| Address | 01 | BUCKcontrol1 | | |
| Bit | Name | Description | R/W | Reset Value |
| [7:2] | Buck1Output[5:0] | Buck1 output voltage regulation 000000 : 0.7V, 25mV per step 000001 : 0.725V ... 101100 : 1.8V ... 111111 : 1.8V | R/W | Option |
| [1:0] | Buck1VRC | VRC setting 00 : 25mV/10μs, 01 : 50mV/10μs, 10 : 100mV/10μs, 11 : 200mV/10μs | R/W | Option |
| Address | 02 | BUCKcontrol2 | | |
| Bit | Name | Description | R/W | Reset Value |
| [7:2] | Buck2Output[5:0] | Buck2 output voltage regulation 000000 : 0.7V, 25mV per step 000001 : 0.725V ... 101100 : 1.8V ... 111111 : 1.8V | R/W | Option |
| [1:0] | Buck2VRC | VRC setting 00 : 25mV/10μs, 01 : 50mV/10μs, 10 : 100mV/10μs, 11 : 200mV/10μs | R/W | Option |
| Address | 03 | BUCKcontrol3 | | |
| Bit | Name | Description | R/W | Reset Value |
| [7:2] | Buck3Output[5:0] | Buck3 output voltage regulation 000000 : 0.7V, 50mV per step 000001 : 0.75V ... 111010 : 3.6V ... 111111 : 3.6V | R/W | Option |
| [1:0] | Buck3VRC | VRC setting 00 : 50mV/10μs, 01 : 100mV/10μs, 10 : 200mV/10μs, 11 : 400mV/10μs | R/W | Option |

| Address | 04 | BUCKcontrol4 | | |
|---------|------------------|---|-----|-------------|
| Bit | Name | Description | R/W | Reset Value |
| [7:2] | Buck4Output[5:0] | Buck4 output voltage regulation 000000 : 0.7V, 50mV per step 000001 : 0.75V ... 111010 : 3.6V ... 111111 : 3.6V | R/W | Option |
| [1:0] | Buck4VRC | VRC setting 00 : 50mV/10μs, 01 : 100mV/10μs, 10 : 200mV/10μs, 11 : 400mV/10μs | R/W | Option |
| Address | 05 | VRC Control | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Buck1VRC_EN | Buck1 VRC 0 : Disable - voltage ramps up to target voltage with one time 1 : Enable - voltage ramps up to target voltage with slope control | R/W | Option |
| 6 | Buck2VRC_EN | Buck2 VRC 0 : Disable - voltage ramps up to target voltage with one time 1 : Enable - voltage ramps up to target voltage with slope control | R/W | Option |
| 5 | Buck3VRC_EN | Buck3 VRC 0 : Disable - voltage ramps up to target voltage with one time 1 : Enable - voltage ramps up to target voltage with slope control | R/W | Option |
| 4 | Buck4VRC_EN | Buck4 VRC 0 : Disable - voltage ramps up to target voltage with one time 1 : Enable - voltage ramps up to target voltage with slope control | R/W | Option |
| [3:0] | Reserved | | R/W | 0000 |
| Address | 06 | BUCK Mode | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Buck1mode | Buck1 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM) | R/W | Option |
| 6 | Buck2mode | Buck2 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM) | R/W | Option |
| 5 | Buck3mode | Buck3 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM) | R/W | Option |

| | | | | |
|---------|--------------|---|-----|-------------|
| 4 | Buck4mode | Buck4 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM) | R/W | Option |
| 3 | Buck1oms | Buck1 output off mode state 0 : Floating 1 : Ground-discharged | R/W | Option |
| 2 | Buck2oms | Buck2 output off mode state 0 : Floating 1 : Ground-discharged | R/W | Option |
| 1 | Buck3oms | Buck3 output off mode state 0 : Floating 1 : Ground-discharged | R/W | Option |
| 0 | Buck4oms | Buck4 output off mode state 0 : Floating 1 : Ground-discharged | R/W | Option |
| Address | 07 | LDOcontrol1 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO1OUT[6:0] | LDO1 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 1010000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 08 | LDOcontrol2 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO2OUT[6:0] | LDO2 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 1010000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 09 | LDOcontrol3 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO3OUT[6:0] | LDO3 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 1010000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |

| Address | 0A | LDOcontrol4 | | |
|---------|--------------|---|-----|-------------|
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO4OUT[6:0] | LDO4 output voltage regulation 0000000 : 3 V, 25mV per step 0000001 : 3.025V ... 0011000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 0B | LDOcontrol5 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO5OUT[6:0] | LDO5 output voltage regulation 0000000 : 3V, 25mV per step 0000001 : 3.025V ... 0011000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 0C | LDOcontrol6 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO6OUT[6:0] | LDO6 output voltage regulation 0000000 : 3.0V, 25mV per step 0000001 : 3.025V ... 0011000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 0D | LDOcontrol7 | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO7OUT[6:0] | LDO7 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 1010000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |

| Address | 0E | LDOcontrol8 | | |
|---------|---------------|---|-----|-------------|
| Bit | Name | Description | R/W | Reset Value |
| 7 | Reserved | | R/W | 0 |
| [6:0] | LDO8OUT[6:0] | LDO8 output voltage regulation 0000000 : 1.6V, 25mV per step 0000001 : 1.625V ... 1010000 : 3.6V (MAX) ... 1111111 : 3.6V (MAX) | R/W | Option |
| Address | 0F | LDOs off mode state | | |
| Bit | Name | Description | R/W | Reset Value |
| 7 | LDO8oms | LDO8 output off mode state 0 : Floating 1 : Ground-discharged | R/W | 1 |
| 6 | LDO7oms | LDO7 output off mode state 0 : Floating 1 : Ground-discharged | R/W | 1 |
| 5 | LDO6oms | LDO6 output off mode state 0 : Floating 1 : Ground-discharged | R/W | 1 |
| 4 | LDO5oms | LDO5 output off mode state 0 : Floating 1 : Ground-discharged | R/W | 1 |
| 3 | LDO4oms | LDO4 output off mode state 0 : Floating 1 : Ground-discharged | R/W | 1 |
| 2 | LDO3oms | LDO3 output off mode state 0 : Floating 1 : Ground-discharged | R/W | 1 |
| 1 | LDO2oms | LDO2 output off mode state 0 : Floating 1 : Ground-discharged | R/W | 1 |
| 0 | LDO1ms | LDO1 output off mode state 0 : Floating 1 : Ground-discharged | R/W | 1 |
| Address | 10 | REBOOT/PWRHOLD delay time control | | |
| Bit | Name | Description | R/W | Reset Value |
| [7:6] | Delayed2[1:0] | Delayed2 setting (00 : 100ms/01 : 500ms/10 : 1s/11 : 2s) | R/W | Option |
| [5:4] | Delayed1[1:0] | Delayed1 setting (00 : 100ms/01 : 500ms/10 : 1s/11 : 2s) | R/W | Option |
| [3:2] | THOLD[1:0] | THOLD setting (00 : 100ms/01 : 500ms/10 : 1s/11 : 2s) | R/W | Option |
| 1 | Reserved | | R/W | 0 |
| 0 | DisTHOLD | Ignore THOLD Time. 0 : Keep PWRHOLD function. 1 : Ignore PWRHOLD function. | R/W | Option |

| Address | 11 | ON Event Setting | | |
|---------|--------------|--|-----|-------------|
| Bit | Name | Description | R/W | Reset Value |
| [7:5] | On_Event | Powered on because of 000 : PWRON key-pressed 001 : VIN plugged in 010 : From REBOOT pin event 111 : No event happen | R | 111 |
| [4:0] | Reserved | | R/W | 0 |
| Address | 12 | VIN UVLO/Buck On/Off | | |
| Bit | Name | Description | R/W | Reset Value |
| [7:5] | VOFF setting | VIN UVLO 2.8V to 3.5V per 0.1V to power off PMIC (Hysteresis = VOFF setting + 0.35V) 000 : 2.8V 001 : 2.9V 010 : 3V 011 : 3.1V 100 : 3.2V 101 : 3.3V 110 : 3.4V 111 : 3.5V | R/W | Option |
| 4 | Reserved | | R/W | 0 |
| 3 | Buck4 | Buck4 control (0 : Disable Buck4/1 : Enable Buck4) | R/W | Option |
| 2 | Buck3 | Buck3 control (0 : Disable Buck3/1 : Enable Buck3) | R/W | Option |
| 1 | Buck2 | Buck2 control (0 : Disable Buck2/1 : Enable Buck2) | R/W | Option |
| 0 | Buck1 | Buck1 control (0 : Disable Buck1/1 : Enable Buck1) | R/W | Option |

| Address | 13 | LDOs On/Off | | |
|---------|------|--|-----|-------------|
| Bit | Name | Description | R/W | Reset Value |
| 7 | LDO8 | LDO8 control (0 : Disable LDO8 / 1 : Enable LDO8) | R/W | Option |
| 6 | LDO7 | LDO7 control (0 : Disable LDO7 / 1 : Enable LDO7) | R/W | Option |
| 5 | LDO6 | LDO6 control (0 : Disable LDO6 / 1 : Enable LDO6) | R/W | Option |
| 4 | LDO5 | LDO5 control (0 : Disable LDO5 / 1 : Enable LDO5) | R/W | Option |
| 3 | LDO4 | LDO4 control (0 : Disable LDO4 / 1 : Enable LDO4) | R/W | Option |
| 2 | LDO3 | LDO3 control (0 : Disable LDO3 / 1 : Enable LDO3) | R/W | Option |
| 1 | LDO2 | LDO2 control (0 : Disable LDO2 / 1 : Enable LDO2) | R/W | Option |
| 0 | LDO1 | LDO1 control (0 : Disable LDO1 / 1 : Enable LDO1) | R/W | Option |

| Address | 14 | PWRON(Power On Key) time Parameters Setting / PG delay | | |
|---------|--------------|--|-----|-------------|
| Bit | Name | Description | R/W | Reset Value |
| [7:6] | START_TIME | Startup time setting 00 : 100μs (pressing time - low level) 01 : 100ms 10 : 1s 11 : 2s | R/W | Option |
| [5:4] | L_PRESS_TIME | Long-press time setting (after Power-On, 00 : 1s (falling edge to rising edge) 01 : 1.5s 10 : 2s 11 : 2.5s Sending short/long-press IRQ to CPU ex : 1.5s → low time < 1.5s (short IRQ) → low time > 1.5s but < 6s (shutdown time) (long IRQ) → low time > 6s (shutdown time) (shutdown) | R/W | Option |
| [3:2] | SHDN_PRESS | Key-press forced shutdown time setting 00 : 4s/0ms (pressing time : low level) 01 : 6s/1ms 10 : 8s/1ms 11 : 10s/2ms (allow option 0/1/1/2ms by SHDN_PRESS_SHORT) | R/W | Option |
| [1:0] | PG_DLY | PG signal delay after the last power startup is done 00 : 10ms 01 : 50ms 10 : 100ms 11 : 200ms/5ms (allow option 5ms by PG_DLY_5ms_EN) | R/W | Option |

| Address | 15 | SHDN Control | | |
|---------|------------------|--|------------|-------------|
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | SHDN_CTRL | Power off setting by CPU, after set, 100ms delayed power off 0 : Normal operation 1 : Disable the PMIC output | R/W | 0 |
| 6 | SHDN_TIMING | Disable Buck/LDO only for normal power off (SHDN_CTRL = 1) 0 : Disable at the same time 1 : Contrary to the startup timing (first_on-last_off) | R/W | Option |
| [5:4] | SHDN_DLYTIME | Delayed shutdown time after send the (PWRON)key-press-forced-shutdown IRQ (when IRQ is disable, there is no delay) 00 : 100ms 01 : 500ms 10 : 1s 11 : 2s | R/W | Option |
| 3 | Reserved | | R/W | 0 |
| 2 | PG_DLY_5ms_EN | 0 : 0x14[1:0] = 11, delay is 200ms 1 : 0x14[1:0] = 11, delay is 5ms | R/W | Option |
| 1 | SHDN_PRESS_SHORT | 0 : 0x14[3:2], SHDN_PRESS time is 4s/6s/8s/10s 1 : 0x14[3:2], SHDN_PRESS time is 0ms/1ms/1ms/2ms | R/W | Option |
| 0 | PWRON_NORMOFF_EN | PWRON off sequence 0 : Disable this event. 1 : Enable this event | R/W | Option |
| Address | 16 | Powered off conditions enable setting | | |
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | BCK1LV_ENSHDN | Buck1 output voltage low SHDN 0 : Disable this event. 1 : Enable this event | R/W | 0 |
| 6 | BCK2LV_ENSHDN | Buck2 output voltage low SHDN 0 : Disable this event. 1 : Enable this event | R/W | 0 |
| 5 | BCK3LV_ENSHDN | Buck3 output voltage low SHDN 0 : Disable this event. 1 : Enable this event | R/W | 0 |
| 4 | BCK4LV_ENSHDN | Buck4 output voltage low SHDN 0 : Disable this event. 1 : Enable this event | R/W | 0 |
| 3 | PWRON_ENSHDN | PWRON key-pressed forced SHDN 0 : Disable this event. 1 : Enable this event | R/W | 1 |
| 2 | OT_ENSHDN | Over temperature SHDN 0 : Disable this event. 1 : enable this event | R/W | 1 |
| 1 | VINLV_ENSHDN | VIN voltage low (VOFF) SHDN 0 : Disable this event. 1 : Enable this event | R/W | Option |
| 0 | VINLV_SEQ_EN | Off sequence after VIN voltage low (VOFF) 0 : Disable this event. 1 : Enable this event | R/W | Option |

| Address | 17 | OFF Event (Only reset by POR) | | |
|---------|-------------|--|------------|-------------|
| Bit | Name | Description | Read/Write | Reset Value |
| [7:4] | OFF_Event | Powered off because of (Only shows last power-off event) 0000 : VIN voltage low (VOFF) (Set by reg) 0001 : Buck1 output voltage low 0010 : Buck2 output voltage low 0011 : Buck3 output voltage low 0100 : PWRON key-pressed forced shutdown 0101 : Power Off register setting 0110 : Over-temperature event 0111 : Reboot restart. 1000 : Buck4 output voltage low 1001 : PWR_HOLD fail. 1010 : No event happen. 1111 : No event happen | R | 1111 |
| [3:0] | Reserved | | R | 0000 |
| Address | 28 | IRQ Enable1 | | |
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | OT_IRQ | Internal over-temperature was triggered, IRQ enable | R/W | 1 |
| 6 | Bck1LV_IRQ | Buck1 output voltage equal 66% x V _{Target} , IRQ enable | R/W | 1 |
| 5 | Bck2LV_IRQ | Buck2 output voltage equal 66% x V _{Target} , IRQ enable | R/W | 1 |
| 4 | Bck3LV_IRQ | Buck3 output voltage equal 66% x V _{Target} , IRQ enable | R/W | 1 |
| 3 | Bck4LV_IRQ | Buck4 output voltage equal 66% x V _{Target} , IRQ enable | R/W | 1 |
| 2 | PWRONSP_IRQ | PWRON short press, IRQ enable (32μs deglitch time) | R/W | 0 |
| 1 | PWRONLP_IRQ | PWRON long press, IRQ enable (32μs deglitch time) | R/W | 0 |
| 0 | SYSLV_IRQ | VIN voltage is lower than VOFF, IRQ enable | R/W | 0 |

| Address | 29 | IRQ Status1 | | |
|---------|----------------|--|------------|-------------|
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | OT | Internal over-temperature | R | 0 |
| 6 | Bck1LV | Buck1 output voltage equal 66% x V _{Target} | R | 0 |
| 5 | Bck2LV | Buck2 output voltage equal 66% x V _{Target} | R | 0 |
| 4 | Bck3LV | Buck3 output voltage equal 66% x V _{Target} | R | 0 |
| 3 | Bck4LV | Buck4 output voltage equal 66% x V _{Target} | R | 0 |
| 2 | PWRONSP | PWRON short press (32μs deglitch time) | R | 0 |
| 1 | PWRONLP | PWRON long press (32μs deglitch time) | R | 0 |
| 0 | VINLV | VIN voltage is lower than VOFF | R | 0 |
| Address | 2A | IRQ Enable2 | | |
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | KPSHDN_IRQ | Key-press forced shutdown, IRQ enable | R/W | 1 |
| 6 | PWRONR_IRQ | PWRON press rising edge, IRQ enable | R/W | 0 |
| 5 | PWRONF_IRQ | PWRON press falling edge, IRQ enable | R/W | 0 |
| [4:0] | Reserved | | R | 0000 |
| Address | 2B | IRQ Status2 | | |
| Bit | Name | Description | Read/Write | Reset Value |
| 7 | KPSHDN | Key-press forced shutdown | R | 0 |
| 6 | PWRONR | PWRON press rising edge | R | 0 |
| 5 | PWRONF | PWRON press falling edge | R | 0 |
| [4:2] | Reserved | | R | 000 |
| 1 | OTW125 | Internal 125°C pre-warning over-temperature. | R | 0 |
| 0 | OTW100 | Internal 100°C pre-warning over-temperature. | R | 0 |
| Address | 2C | PMU On/Off Sequence1 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | Read/Write | Reset Value |
| [7:4] | Buck2_Seq[3:0] | Setting Buck2 on/off sequence priority | R/W | Option |
| [3:0] | Buck1_Seq[3:0] | Setting Buck1 on/off sequence priority | R/W | Option |
| Address | 2D | PMU On/Off Sequence2 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | Read/Write | Reset Value |
| [7:4] | Buck4_Seq[3:0] | Setting Buck4 on/off sequence priority | R/W | Option |
| [3:0] | Buck3_Seq[3:0] | Setting Buck3 on/off sequence priority | R/W | Option |

| | | | | |
|---------|--|--|------------|-------------|
| Address | 2E | PMU On/Off Sequence3 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | Read/Write | Reset Value |
| [7:4] | LDO2_Seq[3:0] | Setting LDO2 on/off sequence priority | R/W | Option |
| [3:0] | LDO1_Seq[3:0] | Setting LDO1 on/off sequence priority | R/W | Option |
| Address | 2F | PMU On/Off Sequence4 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | Read/Write | Reset Value |
| [7:4] | LDO4_Seq[3:0] | Setting LDO4 on/off sequence priority | R/W | Option |
| [3:0] | LDO3_Seq[3:0] | Setting LDO3 on/off sequence priority | R/W | Option |
| Address | 30 | PMU On/Off Sequence5 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | Read/Write | Reset Value |
| [7:4] | LDO6_Seq[3:0] | Setting LDO6 on/off sequence priority | R/W | Option |
| [3:0] | LDO5_Seq[3:0] | Setting LDO5 on/off sequence priority | R/W | Option |
| Address | 31 | PMU On/Off Sequence5 | | |
| Bit | Name | Description (Setting on/off sequence priority) (0000 : off, 0001 : first on, 1100 : last on) (The sequence is planed by first on last off) | Read/Write | Reset Value |
| [7:4] | LDO8_Seq[3:0] | Setting LDO8 on/off sequence priority | R/W | Option |
| [3:0] | LDO7_Seq[3:0] | Setting LDO7 on/off sequence priority | R/W | Option |
| Address | 32 | Soft-Start Control | | |
| Bit | Name | Description | Read/Write | Reset Value |
| [7:6] | Reserved | | R | Option |
| [5:2] | Soft-Start End Control @ MASK_GPIO = 0 (External Enable pin define) | 0000 : First turn on channel decide the PG_DLY time. 0001 : Buck1 decide the PG_DLY time. 0100 : Buck1 decide the PG_DLY time. 0101 : LDO1 decide the PG_DLY time. 1100 : LDO8 decide the PG_DLY time. 1111 : LDO8 decide the PG_DLY time. | R/W | Option |
| [1:0] | Soft-Start Voltage level / time soft-start control. | Voltage Level 00 : When output voltage arrives to 80% VTarget, next channel will turn on. Soft-start time interval (TSS) : 01 : 1ms 10 : 4ms 11 : 8ms | R/W | Option |

| Address | 33 | Buck Syn-Clock Control | | |
|---------|------------------|---|------------|-------------|
| Bit | Name | Description | Read/Write | Reset Value |
| [7:6] | VCO_VRC | VCO input voltage slop. 00 : 25mV/10µs, 01: 25mV/20µs 10 : 25mV/40µs, 11: 25mV/80µs Note : The VCO's voltage input range is 0.375V to 1.8V and the output frequency is 500kHz to 2.18MHz. | R/W | Option |
| [5:0] | VCO_DVS | VCO input voltage DVS control 000000 : 0.375V (500kHz) 111001 : 1.8V (2MHz) 111111 : 1.8V (2MHz) | R/W | Option |
| Address | 34 | Buck Syn-Clock Spread Spectrum Control | | |
| Bit | Name | Description | Read/Write | Reset Value |
| [7:1] | Reserved | | R/W | 0000000 |
| 0 | SSOSC | Buck Clock Spread Spectrum Control 0 : Disable spread spectrum function. 1 : Turn on spread spectrum function. | R/W | Option |
| Address | 3A | EEPROM (MTP) Control | | |
| Bit | Name | Description | Read/Write | Reset Value |
| [7:6] | Reserved | | R/W | 00 |
| 5 | MTP Page 2 Read | Read MTP Page 2 | R | 0 |
| 4 | MTP Page 1 Read | Read MTP Page 1 | R | 0 |
| [3:2] | Reserved | | R/W | 00 |
| 1 | MTP Page 2 write | Write MTP Page 2, and MTP also needs to be logic high. | W | 0 |
| 0 | MTP Page 1 write | Write MTP Page 1, and MTP also needs to be logic high. | W | 0 |

Table 3. I²C to MTP Mapping Table
MTP Page-1

| I ² C Register Address | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-----------------------------------|-----------------|------------------|--------------|-------------|-------------|----------|----------|----------|----------|
| 0x01 | Function | BUCKcontrol1 | | | | | | | |
| | Meaning | Buck1Output[5:0] | | | | | | Buck1VRC | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x02 | Function | BUCKcontrol2 | | | | | | | |
| | Meaning | Buck2Output[5:0] | | | | | | Buck2VRC | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x03 | Function | BUCKcontrol3 | | | | | | | |
| | Meaning | Buck3Output[5:0] | | | | | | Buck3VRC | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x04 | Function | BUCKcontrol4 | | | | | | | |
| | Meaning | Buck4Output[5:0] | | | | | | Buck4VRC | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x05 | Function | VRC Control | | | | | | | |
| | Meaning | Buck1VRC_EN | Buck2VRC_EN | Buck3VRC_EN | Buck4VRC_EN | Reserved | Reserved | Reserved | Reserved |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x06 | Function | Buck Mode | | | | | | | |
| | Meaning | Buck1 mode | Buck2 mode | Buck3 mode | Buck4 mode | Buck1oms | Buck2oms | Buck3oms | Buck4oms |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x07 | Function | LDOcontrol1 | | | | | | | |
| | Meaning | Reserved | LDO1OUT[6:0] | | | | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x08 | Function | LDOcontrol2 | | | | | | | |
| | Meaning | Reserved | LDO2OUT[6:0] | | | | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |

| I ² C Register Address | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-----------------------------------|-----------------|--|--------------|---------------|----------|----------|----------|----------|----------|
| 0x09 | Function | LDOcontrol3 | | | | | | | |
| | Meaning | Reserved | LDO3OUT[6:0] | | | | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x0A | Function | LDOcontrol4 | | | | | | | |
| | Meaning | Reserved | LDO4OUT[6:0] | | | | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x0B | Function | LDOcontrol5 | | | | | | | |
| | Meaning | Reserved | LDO5OUT[6:0] | | | | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x0C | Function | LDOcontrol6 | | | | | | | |
| | Meaning | Reserved | LDO6OUT[6:0] | | | | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x0D | Function | LDOcontrol7 | | | | | | | |
| | Meaning | Reserved | LDO7OUT[6:0] | | | | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x0E | Function | LDOcontrol8 | | | | | | | |
| | Meaning | Reserved | LDO8OUT[6:0] | | | | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x10 | Function | REBOOT/PWRHOLD delay time control | | | | | | | |
| | Meaning | Delayed2[1:0] | | Delayed1[1:0] | | THOLD | | Reserved | DisTHOLD |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x12 | Function | VIN UVLO (update default value after power on) | | | | | | | |
| | Meaning | VOFF setting | | | Reserved | Reserved | Reserved | Reserved | Reserved |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | B | B | B | B |

MTP Page-2

| I ² C Register Address | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-----------------------------------|-----------------|--|-------------|--------------|----------|----------------|---------------|------------------|------------------|
| 0x14 | Function | PWRON time Parameters Setting / PG delay | | | | | | | |
| | Meaning | START_TIME | | L_PRESS_TIME | | SHDN_PRESS | | PG_DLY | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x15 | Function | SHDN Control | | | | | | | |
| | Meaning | Reserved | SHDN_TIMING | SHDN_DLYTIME | | Reserved | PG_DLY_5ms_EN | SHDN_PRESS_SHORT | PWRON_NORMOFF_EN |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | B | A | A | A | A | A | A | A |
| 0x16 | Function | Powered Off conditions enable setting | | | | | | | |
| | Meaning | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | VINLV_ENSHDN | VINLV_SEQ_EN |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x2C | Function | PMU On/Off Sequence1 | | | | | | | |
| | Meaning | Buck2_Seq[3:0] | | | | Buck1_Seq[3:0] | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x2D | Function | PMU On/Off Sequence2 | | | | | | | |
| | Meaning | Buck4_Seq[3:0] | | | | Buck3_Seq[3:0] | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x2E | Function | PMU On/Off Sequence3 | | | | | | | |
| | Meaning | LDO2_Seq[3:0] | | | | LDO1_Seq[3:0] | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x2F | Function | PMU On/Off Sequence4 | | | | | | | |
| | Meaning | LDO4_Seq[3:0] | | | | LDO3_Seq[3:0] | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |

| I ² C Register Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
|-----------------------------------|-----------------|--|----------|---------------------------------------|----------|---------------|----------|--------------------|-------|
| 0x30 | Function | PMU On/Off Sequence5 | | | | | | | |
| | Meaning | LDO6_Seq[3:0] | | | | LDO5_Seq[3:0] | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x31 | Function | PMU On/Off Sequence6 | | | | | | | |
| | Meaning | LDO8_Seq[3:0] | | | | LDO7_Seq[3:0] | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x32 | Function | Soft-Start Control | | | | | | | |
| | Meaning | Reversed | Reversed | Soft-Start End Select @ MASK_GPIO = 1 | | | | Soft-Start Control | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x33 | Function | Buck Syn-Clock Control | | | | | | | |
| | Meaning | VCO_VRC | | | VCO_DVS | | | | |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |
| 0x34 | Function | Buck Syn-Clock Spread Spectrum Control | | | | | | | |
| | Meaning | Reversed | Reversed | Reversed | Reversed | Reversed | Reversed | Reversed | SSOSC |
| | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset Condition | A | A | A | A | A | A | A | A |

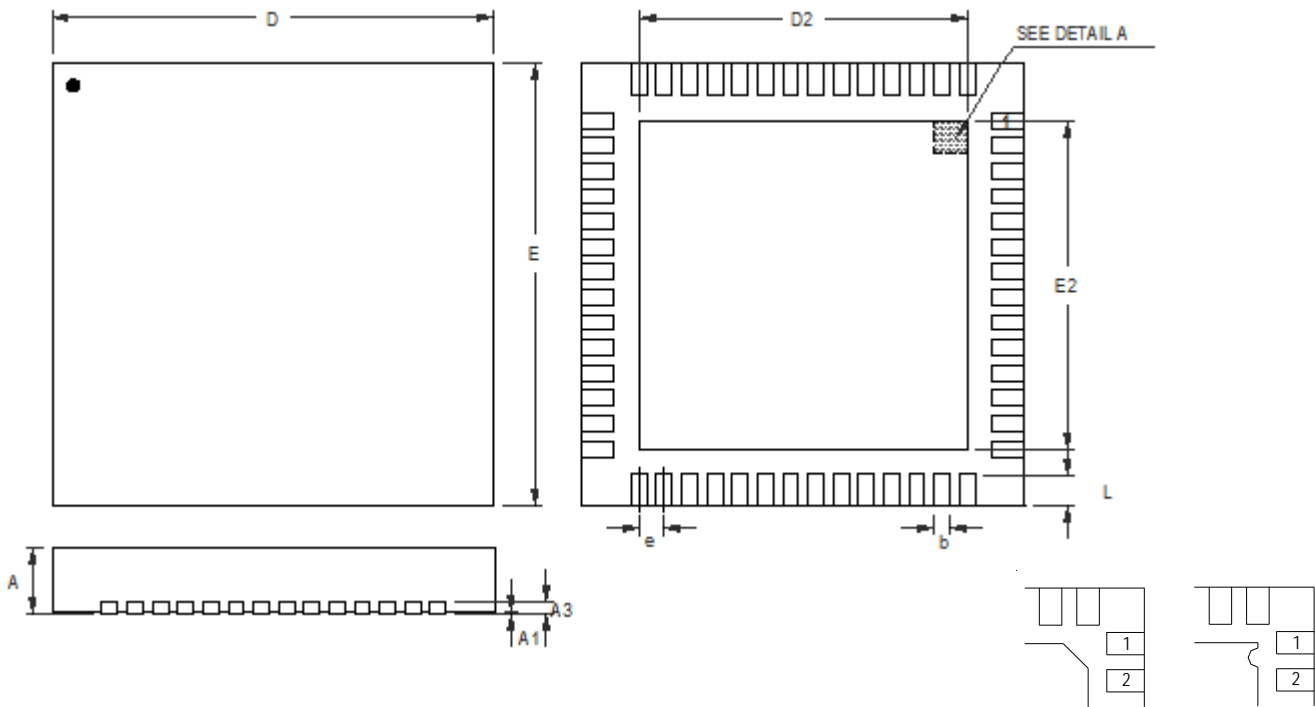
Reset Condition

| | |
|---|--|
| A | Reset by MTP (Register 0x12 VOFF Setting). |
| B | Reset when VIN < 1.7V. |

Table 4. MTP Code Table

| Code No. | 00 | 02 | 04 | 05 | 06 |
|----------|-----------|-----------|-----------|-----------|-----------|
| Register | MTP Value | MTP Value | MTP Value | MTP Value | MTP Value |
| 0x01 | B0 | 48 | B0 | B0 | B0 |
| 0x02 | B0 | 68 | 50 | 40 | 50 |
| 0x03 | 20 | 58 | 20 | 1C | 1C |
| 0x04 | D0 | 18 | D0 | D0 | D0 |
| 0x05 | 5 | 5 | 5 | 5 | 5 |
| 0x06 | 0F | 0F | 0F | 4F | 4F |
| 0x07 | 16 | 8 | 16 | 16 | 16 |
| 0x08 | 8 | 8 | 8 | 8 | 8 |
| 0x09 | 8 | 10 | 8 | 8 | 8 |
| 0x0A | 0C | 0C | 0C | 0C | 0C |
| 0x0B | 0C | 0C | 0C | 0C | 0C |
| 0x0C | 0C | 0C | 0C | 0C | 0C |
| 0x0D | 44 | 8 | 44 | 44 | 24 |
| 0x0E | 8 | 8 | 44 | 44 | 44 |
| 0x10 | 61 | 61 | 61 | 61 | 61 |
| 0x12 | C9 | CF | CB | CF | CF |
| 0x14 | 40 | 41 | 40 | 40 | 40 |
| 0x15 | 49 | 49 | 49 | 49 | 49 |
| 0x16 | 0E | 0E | 0E | 0E | 0E |
| 0x2C | 4 | 42 | 84 | 64 | 74 |
| 0x2D | 50 | 35 | 50 | 53 | 53 |
| 0x2E | 43 | 51 | 43 | 42 | 42 |
| 0x2F | 54 | 65 | 54 | 54 | 54 |
| 0x30 | 16 | 6 | 16 | 16 | 19 |
| 0x31 | 72 | 65 | 72 | 78 | 86 |
| 0x32 | 32 | 32 | 32 | 2E | 2E |
| 0x33 | 39 | 39 | 39 | 39 | 39 |
| 0x34 | 0 | 0 | 0 | 0 | 0 |

Outline Dimension



DETAIL A

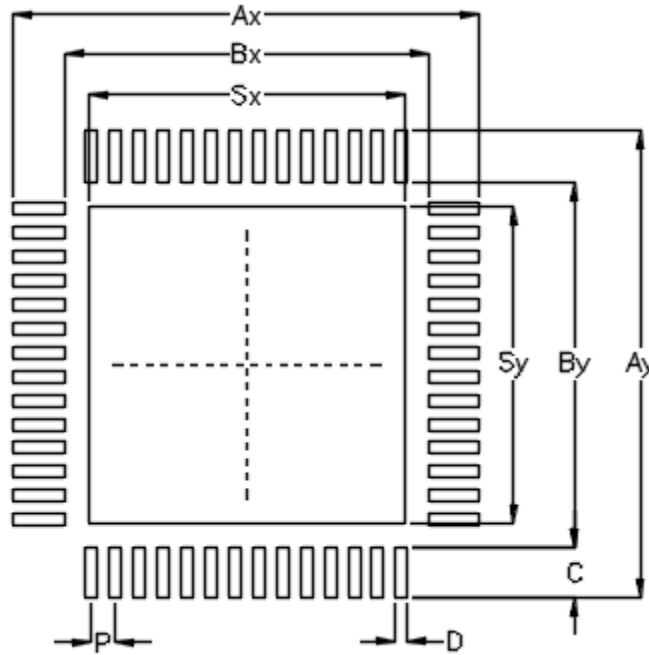
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 6.900 | 7.100 | 0.272 | 0.280 |
| D2 | 5.150 | 5.250 | 0.203 | 0.207 |
| E | 6.900 | 7.100 | 0.272 | 0.280 |
| E2 | 5.150 | 5.250 | 0.203 | 0.207 |
| e | 0.400 | | 0.016 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

W-Type 56L QFN 7x7 Package

Footprint Information



| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | | Tolerance |
|------------------|---------------|--------------------------|------|------|------|------|------|------|------|------|-----------|
| | | P | Ax | Ay | Bx | By | C | D | Sx | Sy | |
| V/W/U/XQFN7*7-56 | 56 | 0.40 | 7.80 | 7.80 | 6.10 | 6.10 | 0.85 | 0.20 | 5.30 | 5.30 | ±0.05 |

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