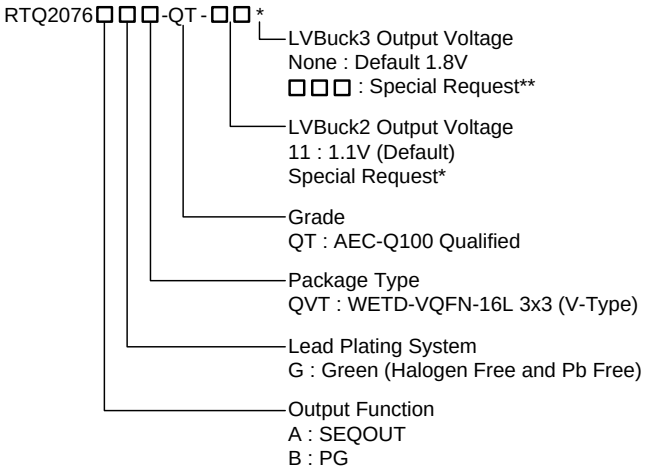
Automotive CIS/CCM PMIC for Ultra Compact Camera and High Image Quality System

General Description

The RTQ2076 is an integrated PMIC with three step down converters and one high PSRR low-dropout (LDO) regulator for automotive camera applications. The high-voltage step down converter is operated with input voltage range up to 18.5V for Power Over Coax (POC) connection. Two low-voltage step down converters provide constant output voltage. All step down converters operate in a forced fixed-frequency PWM mode. The LDO output voltage is easily set via an external resistor. The RTQ2076 provides 10 power sequences by a resistor for flexibility. The RTQ2076 is available in a WETD-VQFN-16L 3x3 package with dimple lead type wettable flanks.

Ordering Information



Note :

*Special Request : Available voltage between 0.6V to 2.1V with 100mV step under specific business agreement.

**Special Request : For example, 095 means 0.95V.

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

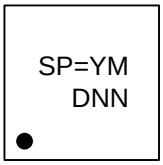
- **AEC-Q100 Grade 1**
- **FMEA Compliant Pin Placement and Protection Mechanisms**
- **Three Step-Down Converters (HVBuck1, LVBuck2 and LVBuck3)**
  - **Peak Current Mode PWM Operation**
  - **Fixed Switching Frequency at 2.1MHz**
  - **EMI Reduction with Spread Spectrum and Phase Shift**
  - **HVBuck1 Input Voltage from 4V to 18.5V, Adjustable Output Voltage and Up to 2A Output Current**
  - **LVBuck2 Input Voltage from 2.7V to 5V, Fixed Output Voltage and 1.5A Output Current**
  - **LVBuck3 Input Voltage from 2.7V to 5V, Fixed Output Voltage and 750mA Output Current**
  - **Pins Related to LVBuck2/LVBuck3 Allowable Floating if Channel Unused**
- **Low Dropout Regulator (LDO)**
  - **Input Voltage from 2.7V to 5V and 300mA Output Current**
  - **10 Adjustable Output Voltage Settings via RSET Pin**
  - **High PSRR : 60dB at 100kHz, 40dB at 1MHz**
- **Output Function**
  - **Sequence Control for External Power IC via SEQOUT (RTQ2076A-QT)**
  - **Power Status Indication via PG (RTQ2076B-QT)**
- **10 Flexible Power Sequence Settings via SEQ Pin**
- **Small Form Factor WETD-VQFN-16L 3x3 Wettable Flanks Package**

Applications

- Automotive Camera Modules
  - Surround View Camera
  - Front View Camera
  - Rear View Camera
  - Dash Cam DVR
  - Driver Monitoring System
  - Cabin Monitor
  - eMirror

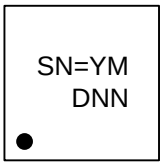
Marking Information

RTQ2076AGQVT-QT-11



SP= : Product Code
YMDNN : Date Code

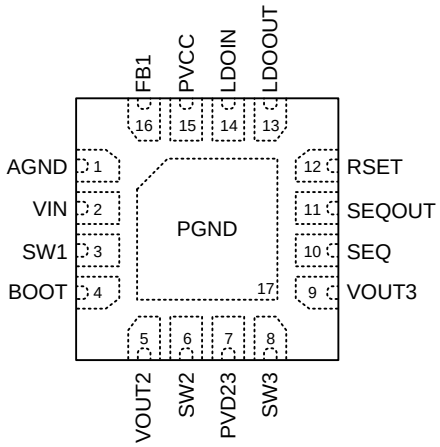
RTQ2076BGQVT-QT-11



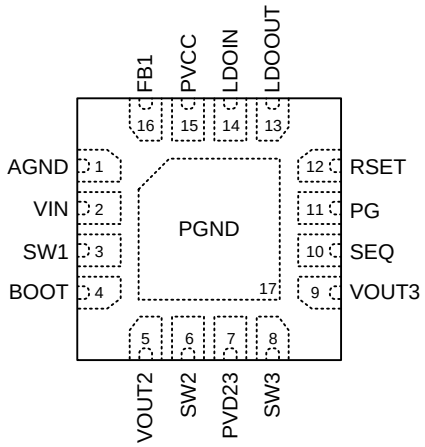
SN= : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)

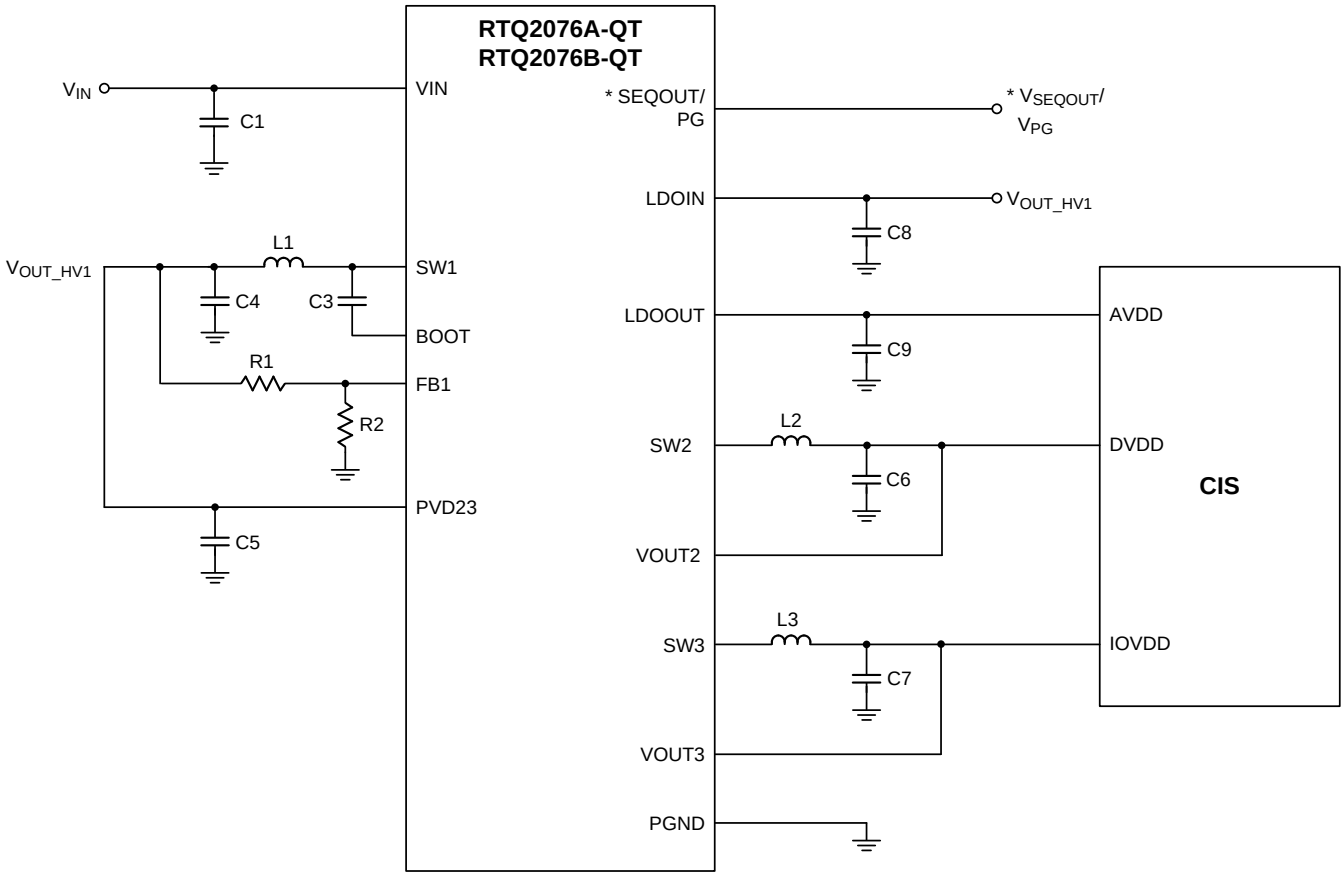


WETD-VQFN-16L 3x3 (RTQ2076A-QT)



WETD-VQFN-16L 3x3 (RTQ2076B-QT)

Simplified Application Circuit



* SEQOUT pinout is for RTQ2076A-QT; PG pinout is for RTQ2076B-QT.

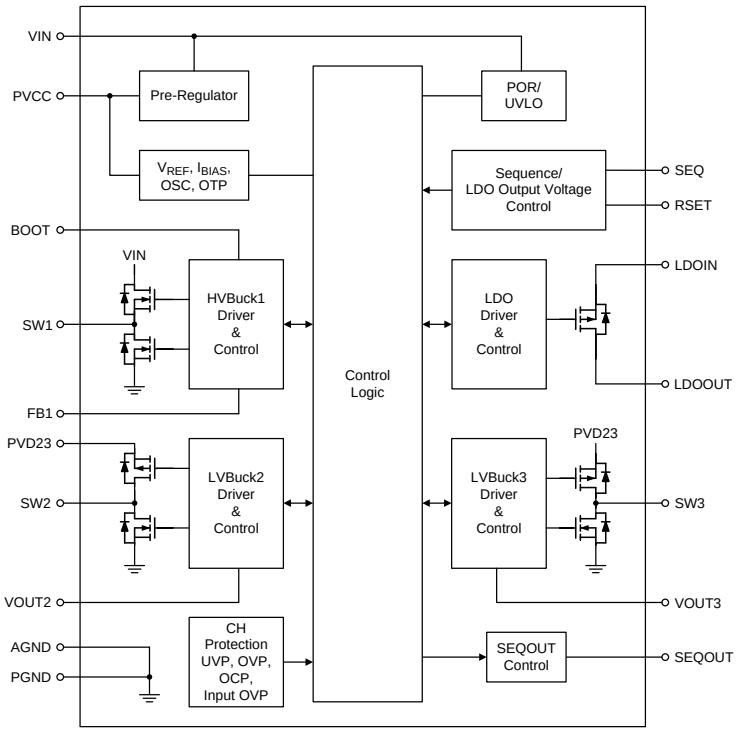
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	AGND	Analog ground.
2	VIN	Supply voltage input of HVBuck1. Connect a 4.7μF or larger decouple ceramic capacitor between this pin and ground.
3	SW1	HVBuck1 switch node.
4	BOOT	Bootstrap capacitor connection pin for HVBuck1. Connect a 0.1μF ceramic capacitor between this pin and SW1.
5	VOUT2	Output voltage feedback input of LVBuck2. Directly connect the output capacitor node to this pin for better regulation.
6	SW2	LVBuck2 switch node.
7	PVD23	Supply voltage input of LVBuck2 and LVBuck3. Connect a 4.7μF or larger decouple ceramic capacitor between this pin and ground.
8	SW3	LVBuck3 switch node.

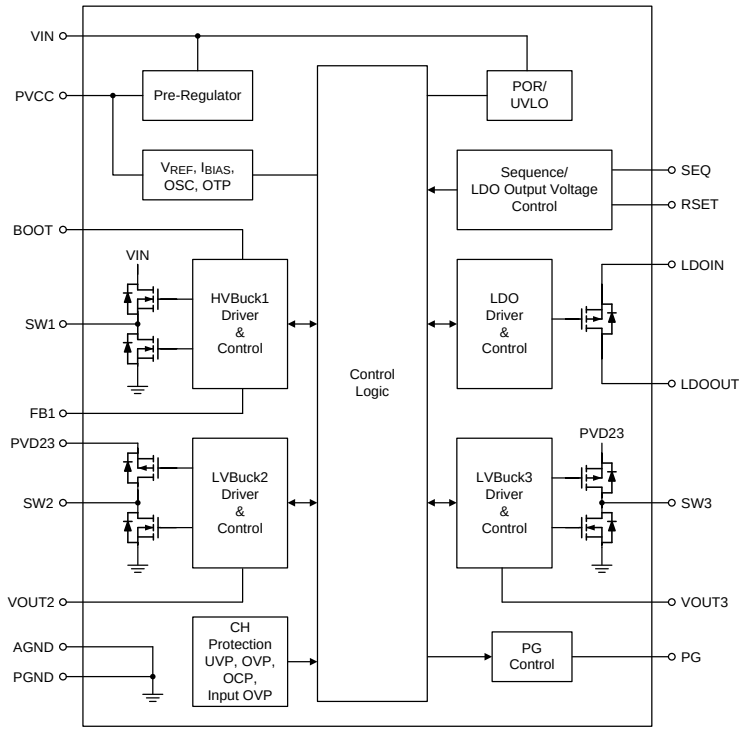
Pin No.	Pin Name	Pin Function
9	VOUT3	Output voltage feedback input of LVBuck3. Directly connect the output capacitor node to this pin for better regulation.
10	SEQ	Power sequence selection.
11	SEQOUT	Sequence control output with open drain structure for external power IC. (RTQ2076A-QT)
	PG	Power status indication pin with open drain structure for HVBuck1, LVBuck2, LVBuck3 and LDO. PG at high state indicates all outputs work well. (RTQ2076B-QT)
12	RSET	LDO output voltage selection.
13	LDOOUT	LDO output. Connect a 2.2μF ceramic decouple capacitor between this pin and ground.
14	LDOIN	Supply voltage input of LDO. Connect a 2.2μF or larger decouple ceramic capacitor between this pin and ground.
15	PVCC	Internal analog power output. Connect a 1μF ceramic decouple capacitor between this pin and ground. Note additional external loading on this pin is forbidden.
16	FB1	Output voltage feedback input of HVBuck1.
17 (Exposed Pad)	PGND	IC thermal pad and power ground. It must connect to main ground plane for proper operation.

Functional Block Diagram

RTQ2076A-QT



RTQ2076B-QT



Operation

The RTQ2076A-QT/RTQ2076B-QT is a highly integrated power-management integrated circuit (PMIC) for automotive camera system, which includes three step-down converters (CH1 HVBuck1, CH2 LVBuck2, CH3 LVBuck3) and one generic LDO (CH4 LDO).

System Under-Voltage Protection and Over-Voltage Protection

The RTQ2076A-QT/RTQ2076B-QT stops operating if V_{IN} voltage falls below the Under-Voltage Lock Out level (UVLO_L). There is a typical 500mV hysteresis implemented to avoid unstable on/off behaviors. The device is initialized in its default state after V_{IN} voltage recovering from UVLO_H. When V_{IN} voltage reaches the Over-Voltage Protection level, the step-down converters, LDO and SEQOUT (RTQ2076A-QT) are disabled immediately. Then the IC enters into latch off state and only can re-start with V_{IN} ON/OFF. Meanwhile, the PG status will be also set to 0V to indicate IC fault condition.

Thermal Protection

The RTQ2076A-QT/RTQ2076B-QT features an over-temperature protection (OTP). When the junction temperature is higher than 160°C typical value, OTP is triggered to disable all outputs and the device enters into a latch off state. When the RTQ2076A-QT/ RTQ2076B-QT recovers from OTP, the device only can re-start with V_{IN} ON/OFF.

Pre-Regulator

The device integrates a 4.45V linear regulator (PVCC) supplied by V_{IN} to provide power to the internal circuitry. The PVCC can be used as the RSET and SEQ pull-up supply but it is “NOT” allowed to power other device or circuitry. A 1μF decoupling capacitor must be connected between PVCC and AGND to filter the noise and it needs to be placed as close as possible to the PVCC pin.

Peak Current Mode Control

The three step-down converters utilize the peak current mode control. An internal oscillator initiates turn-on of the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp up in the inductor. With comparisons of the inductor peak current signal during high-side MOSFET switch on interval and the internal compensation signal derived from the sensed feedback voltage with reference voltage, the high-side MOSFET switch is turned off and inductor current continues to flow through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, the regulated inductor current controls duty-cycle and output voltage of the converter.

Spread-Spectrum Operation

Due to the periodicity of the switching signal, the energy concentrates in one particular frequency and its harmonics. The energy is radiated and possible to result in a potential EMI issue. The RTQ2076A-QT/ RTQ2076B-QT equips a spread-spectrum function to meet CISPR and automotive EMI compliances. The spread-spectrum function is implemented by a pseudo random sequence and uses +6% spread of the switching frequency. For example, when the switching frequency typical value is 2.1MHz, the frequency range varies from 2.1MHz to 2.226MHz. Therefore, the RTQ2076A-QT/RTQ2076B-QT can guarantee that the 2.1MHz switching frequency does not drop into the 1.8MHz AM band limit.

Phase-Shifted Operation

The RTQ2076A-QT/RTQ2076B-QT supports phase shift operations among the step-down converters for further easing the simultaneous switching energy radiation quantity. The internal clock is automatically shifted to different respective sub-clocks for step-down converters. For example, when two step-down converters application, the beginning turn-on time between two high-side MOSFETs will have a 180-degree phase difference. Likewise, a 120-degree phase difference when three step-down converters.

Allowable Channel Floating

For saving PCB layout space and material cost, the unused low-voltage step-down converter (CH2/CH3) is allowable to pin (SW2/SW3) floating without any inductor and output capacitor placement. The pin PVD23 is required to connect to a fixed voltage for floating detection and it is allowable without capacitor placement. The RTQ2076A-QT/RTQ2076B-QT automatically detects pin status during power-on procedure to determine whether the channel is used or not. In addition, the related failures on unused channels do not affect the device operation.

Power Good Indication

The RTQ2076B-QT features an open-drain power-good output (PG) to monitor the output voltage status. Connect a pull-up resistor from PG pin to an external voltage. Note it is forbidden to use PVCC as pulled-up voltage of PG pin. When the last channel of power-on sequence reaches 90% of its target output voltage, the PG signal is pulled up to indicate “Power Good” status after 10ms tills to device disabled or any other protection happens.

External Control Output

The RTQ2076A-QT features an open-drain external control output (SEQ) for external device. Connect a pull-up resistor from SEQ pin to an external voltage. Note it is forbidden to use PVCC as pulled-up voltage of SEQ pin. Referring to Table 3 for further information about power-on sequence.

Table 1. Unused Channel Pin Connection

Unused Channel	Unused Pin Number	Unused Pin Name	Pin Configuration
LVBuck2	5	VOUT2	Floating
	6	SW2	Floating
	7	PVD23	Connect to a fixed voltage
LVBuck3	7	PVD23	Connect to a fixed voltage
	8	SW3	Floating
	9	VOUT3	Floating

Absolute Maximum Ratings (Note 1)

- VIN ---------- –0.3V to 24V
- SW1 ---------- –0.3V to 24V
- BOOT ---------- –0.3V to 28V
- BOOT to SW1 ---------- –0.3V to 5V
- VOUT2, PVD23, VOUT3, SEQ, SEQOUT (RTQ2076A-QT),
  PG (RTQ2076B-QT), RSET, LDOOUT, LDOIN, PVCC, FB1 ---------- –0.3V to 6.5V
- SW2, SW3 ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WETD-VQFN-16L 3x3 ---------- 4.16W
- Package Thermal Resistance (Note 2)
  WETD-VQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  WETD-VQFN-16L 3x3, θ_{JC} ---------- 4.4°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ---------- 4V to 18.5V
- Supply Voltage, V_{PVD23}, V_{LDOIN} ---------- 2.7V to 5V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 150°C

Electrical Characteristics

(T_A = T_J = –40°C to 125°C, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Under-Voltage Lockout Threshold	UVLO_H	V_{IN} rising	3.6	3.8	4	V
	UVLO_L	V_{IN} falling	3.15	3.3	3.45	V
Input Over-Voltage Protection	V_{IN_OV}		18.6	20	21.5	V
CH1 HVBuck1						
Input Voltage Range	V_{IN}		4	--	18.5	V
Output Voltage Range	V_{OUT_HV1}	Buck mode operation. Switching frequency, minimum on time and minimum off time need to be considered.	2.7	--	5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Feedback Voltage Accuracy	V_{FB1}		0.788	0.8	0.812	V
Switching Frequency	f_{SW_HV1}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{\_HV1}$		--	6	--	%
Switching Minimum On Time	$t_{ON\_MIN\_HV1}$		--	--	55	ns
Switching Minimum Off Time	$t_{OFF\_MIN\_HV1}$		--	--	50	ns
High-Side MOSFET On Resistance	$R_{ON\_HS\_HV1}$	From VIN pin to SW1 pin	115	210	340	mΩ
Low-Side MOSFET On Resistance	$R_{ON\_LS\_HV1}$	From SW1 pin to PGND pin	40	110	200	mΩ
Inductor Peak Current Limit	$I_{CL\_PK\_HV1}$		2.4	3	3.6	A
Inductor Valley Current Limit	$I_{CL\_VL\_HV1}$		--	2.7	--	A
Negative Inductor Peak Current Limit	$I_{CL\_NPK\_HV1}$		1	2.5	4	A
Output Discharge Resistor	R_{DIS_HV1}		230	270	360	Ω
Output Under-Voltage Falling Threshold	$UVP_{\_F\_HV1}$		40	50	60	%
Output Feedback Over-Voltage Rising Threshold	$OVP_{\_R\_HV1}$		--	110	--	%
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7	--	5	V
Output Voltage	V_{OUT_LV2}		--	1.1	--	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LV2}$		–1.5	--	1.5	%
Switching Frequency	f_{SW_LV2}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{\_LV2}$		--	6	--	%
Switching Minimum On Time	$t_{ON\_MIN\_LV2}$		--	--	44	ns
High-Side MOSFET On Resistance	$R_{ON\_HS\_LV2}$	From PVD23 pin to SW2 pin	110	150	202	mΩ
Low-Side MOSFET On Resistance	$R_{ON\_LS\_LV2}$	From SW2 pin to PGND pin	60	90	133	mΩ
Inductor Peak Current Limit	$I_{CL\_PK\_LV2}$		1.8	2.2	2.6	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Inductor Valley Current Limit	$I_{CL\_VL\_LV2}$		--	1.8	--	A
Negative Inductor Peak Current Limit	$I_{CL\_NPK\_LV2}$		0.7	1.7	2.9	A
Output Discharge Resistor	R_{DIS_LV2}		6	9	14	Ω
Output Under-Voltage Falling Threshold	$UVP_{\_F\_LV2}$		40	50	60	%
Output Over-Voltage Rising Threshold	$OVP_{\_R\_LV2}$		--	120	--	%
Output Over-Voltage Falling Threshold	$OVP_{\_F\_LV2}$		--	110	--	%
Input Over-Voltage Rising Threshold	$OVP_{\_IN\_R\_LV2}$		5.35	5.8	6.25	V
Input Over-Voltage Hysteresis	$OVP_{\_IN\_HYS\_LV2}$	V_{IN_PVD23} falling	--	580	--	mV
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7	--	5	V
Output Voltage	V_{OUT_LV3}		--	1.8	--	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LV3}$		–1.5	--	1.5	%
Switching Frequency	f_{SW_LV3}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{\_LV3}$		--	6	--	%
Switching Minimum On Time	$t_{ON\_MIN\_LV3}$		--	--	44	ns
High-Side MOSFET On Resistance	$R_{ON\_HS\_LV3}$	From PVD23 pin to SW3 pin	240	310	423	mΩ
Low-Side MOSFET On Resistance	$R_{ON\_LS\_LV3}$	From SW3 pin to PGND pin	170	230	344	mΩ
Inductor Peak Current Limit	$I_{CL\_PK\_LV3}$		0.96	1.2	1.44	A
Inductor Valley Current Limit	$I_{CL\_VL\_LV3}$		--	1.08	--	A
Negative Inductor Peak Current Limit	$I_{CL\_NPK\_LV3}$		0.7	1.7	2.9	A
Output Discharge Resistor	R_{DIS_LV3}		7	10	15	Ω
Output Under-Voltage Falling Threshold	$UVP_{\_F\_LV3}$		40	50	60	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Over-Voltage Rising Threshold	$OVP_{\_R\_LV3}$		--	120	--	%
Output Over-Voltage Falling Threshold	$OVP_{\_F\_LV3}$		--	110	--	%
Input Over-Voltage Rising Threshold	$OVP_{\_IN\_R\_LV3}$		5.35	5.8	6.25	V
Input Over-Voltage Hysteresis	$OVP_{\_IN\_HYS\_LV3}$	V_{IN_PVD23} falling	--	580	--	mV
CH4 LDO (V_{IN_LDO} = 3.6V)						
Input Voltage Range	V_{IN_LDO}		2.7	--	5	V
Output Voltage Range	V_{OUT_LDO}	V_{OUT_LDO} setting via RSET	1.8	--	3.5	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LDO}$	V_{IN_LDO} - V_{OUT_LDO} > 0.3V, I_{OUT_LDO} = 0mA to 300mA	–1.5	--	1.5	%
Maximum Output Current	$I_{OUT\_MAX\_LDO}$		300	--	--	mA
Dropout Voltage	$V_{DROP\_300\_LDO}$	I_{OUT_LDO} = 300mA (Note 5)	--	--	300	mV
	$V_{DROP\_150\_LDO}$	I_{OUT_LDO} = 150mA (Note 5)	--	--	150	
Output Current Limit	I_{CL_LDO}		345	450	555	mA
Output Discharge Resistor	R_{DIS_LDO}		48	76	104	Ω
Output Under-Voltage Falling Threshold	$UVP_{\_F\_LDO}$		30	40	50	%
Output Over-Voltage Rising Threshold	$OVP_{\_R\_LDO}$		--	125	--	%
Output Over-Voltage Falling Threshold	$OVP_{\_F\_LDO}$		--	110	--	%
Input Over-Voltage Rising Threshold	$OVP_{\_IN\_R\_LDO}$		5.35	5.8	6.25	V
Input Over-Voltage Hysteresis	$OVP_{\_IN\_HYS\_LDO}$	V_{IN_LDO} falling	--	500	--	mV
PVCC (Note 6)						
Internal Regulator Output Voltage	V_{OUT_PVCC}		4.33	4.58	4.83	V
Over-Current Limit	I_{CL_PVCC}		150	--	300	mA
SEQOUT (RTQ2076A-QT)						
Output Low Voltage		Current into SEQOUT pin equal to 2mA	--	--	200	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LEAK_SEQOUT}	1.8V applied on SEQOUT pin	--	--	1	μA
Power Good (RTQ2076B-QT)						
Pull Down Voltage	$V_{OUT\_L\_PG}$	Current into PG pin equal to 5mA	--	--	200	mV
Input Leakage Current	I_{LEAK_PG}	1.8V applied on PG pin	--	--	1	μA
Timing						
Soft-Start Time	t_{SS_HV1}	Time from V_{OUT_HV1} 0% rise to 90% of target value, no load	500	1000	1500	μs
	t_{SS_LV2}	Time from V_{OUT_LV2} 0% rise to 90% of target value, no load	500	1000	1500	
	t_{SS_LV3}	Time from V_{OUT_LV3} 0% rise to 90% of target value, no load	500	1000	1500	
	t_{SS_LDO}	Time from the previous turn on channel's output voltage reaching 90% of target value to V_{OUT_LDO} rise to 90% of target value.	200	700	1100	
PG Delay Time	t_{DLY_PG}	(RTQ2076B-QT)	9	10	11	ms

System Characteristics

The following specifications are guaranteed by design and are not performed in production testing. (T_A = T_J = –40°C to 125°C, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Over-Temperature Protection	OTP		--	160	--	°C
Over-Temperature Protection Hysteresis	OTP_H		--	20	--	°C
CH1 HVBuck1						
Maximum Output Current	$I_{OUT\_MAX\_HV1}$		2	--	--	A
Load Regulation	$V_{LOAD\_REG\_HV1}$	I_{OUT_HV1} = 0A to 2A	--	--	0.1	%/A
Line Regulation	$V_{LINE\_REG\_HV1}$	V_{IN} = 5V to 18.5V, I_{OUT_HV1} = 2A	--	--	1	%
Load Transient	$V_{LOAD\_TRAIN\_HV1}$	I_{OUT_HV1} = 10mA to 500mA to 10mA, 1μs	–150	--	150	mV
Line Transient	$V_{LINE\_TRAIN\_HV1}$	V_{IN} = 5V to 18.5V to 5V, 100μs, I_{OUT_HV1} = 10mA/500mA	–50	--	50	mV
Output Ripple	V_{RIPPLE_HV1}	Peak to peak in one switching cycle	--	--	20	mVpp

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)						
Maximum Output Current	$I_{OUT\_MAX\_LV2}$		1.5	--	--	A
Load Regulation	$V_{LOAD\_REG\_LV2}$	I_{OUT_LV2} = 0A to 1.5A	--	--	0.1	%/A
Line Regulation	$V_{LINE\_REG\_LV2}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV2} = 1.5A	--	--	1	%
Load Transient	$V_{LOAD\_TRAIN\_LV2}$	I_{OUT_LV2} = 10mA to 500mA to 10mA, 1μs	–50	--	50	mV
Line Transient	$V_{LINE\_TRAIN\_LV2}$	V_{IN_PVD23} = 3V to 5V to 3V, 50μs, I_{OUT_LV2} = 10mA/1A	–50	--	50	mV
Output Ripple	V_{RIPPLE_LV2}	Peak to peak in one switching cycle	--	--	10	mVpp
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)						
Maximum Output Current	$I_{OUT\_MAX\_LV3}$		750	--	--	mA
Load Regulation	$V_{LOAD\_REG\_LV3}$	I_{OUT_LV3} = 0A to 750mA	--	--	0.1	%/A
Line Regulation	$V_{LINE\_REG\_LV3}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV3} = 750mA	--	--	1	%
Load Transient	$V_{LOAD\_TRAIN\_LV3}$	I_{OUT_LV3} = 10mA to 300mA to 10mA, 1μs	–50	--	50	mV
Line Transient	$V_{LINE\_TRAIN\_LV3}$	V_{IN_PVD23} = 3V to 5V to 3V, 50μs, I_{OUT_LV3} = 10mA/300mA	–50	--	50	mV
Output Ripple	V_{RIPPLE_LV3}	Peak to peak in one switching cycle	--	--	10	mVpp
CH4 LDO (V_{IN_LDO} = 3.6V)						
Power Supply Rejection Ratio	$PSRR_{LDO}$	I_{OUT_LDO} = 100mA, f = 100kHz	--	60	--	dB
		I_{OUT_LDO} = 100mA, f = 1MHz	--	40	--	
Output Noise Voltage	eN_{LDO}	I_{OUT_LDO} = 100mA, f = 100Hz to 100kHz	--	60	--	μV
Load Transient	$V_{LOAD\_TRAIN\_LDO}$	I_{OUT_LDO} = 10mA to 200mA to 10mA, 1μs	–25	--	25	mV
Line Transient	$V_{LINE\_TRAIN\_LDO}$	All V_{OUT_LDO}, V_{IN_LDO} step 600mV, LDO not in dropout condition, 10μs, I_{OUT_LDO} = 1mA/300mA	–25	--	25	mV
Component Requirement (Note 4)						
Effective Input Capacitance	C_{IN_HV1}		1.5	4.7	10	μF
	C_{IN_PVD23}		1.5	4.7	10	
	C_{IN_LDO}		0.7	2.2	4	
Effective Output Capacitance	C_{OUT_HV1}		3.3	10	14	μF
	C_{OUT_LV2}		4.5	10	14	
	C_{OUT_LV3}		4.5	10	14	
	C_{OUT_LDO}		0.7	2.2	4	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Inductance	L_{HV1}		1	1.5	2	μH
	L_{LV2}		0.68	1	1.2	
	L_{LV3}		0.68	1	1.2	
Effective Boot Capacitance	C_{BOOT}		0.07	0.1	0.13	μF
Effective PVCC Capacitance	C_{PVCC}		0.3	1	1.4	μF

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

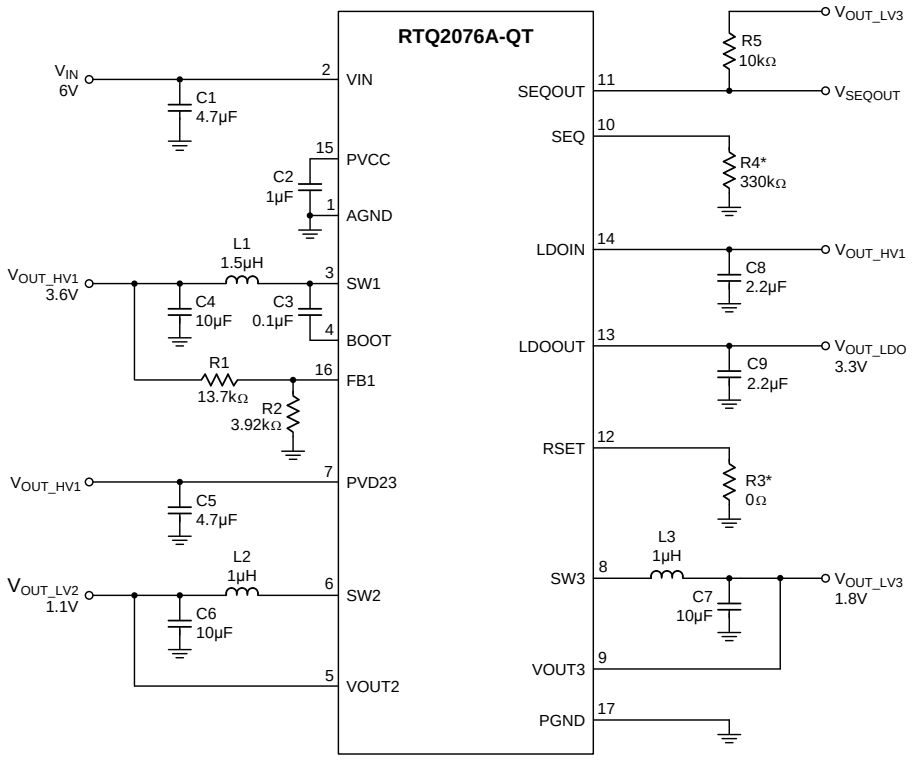
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

Note 6. PVCC is the pre-regulator output voltage only for internal circuitry. External loading on PVCC pin is forbidden.

Typical Application Circuit

RTQ2076A-QT



RTQ2076B-QT

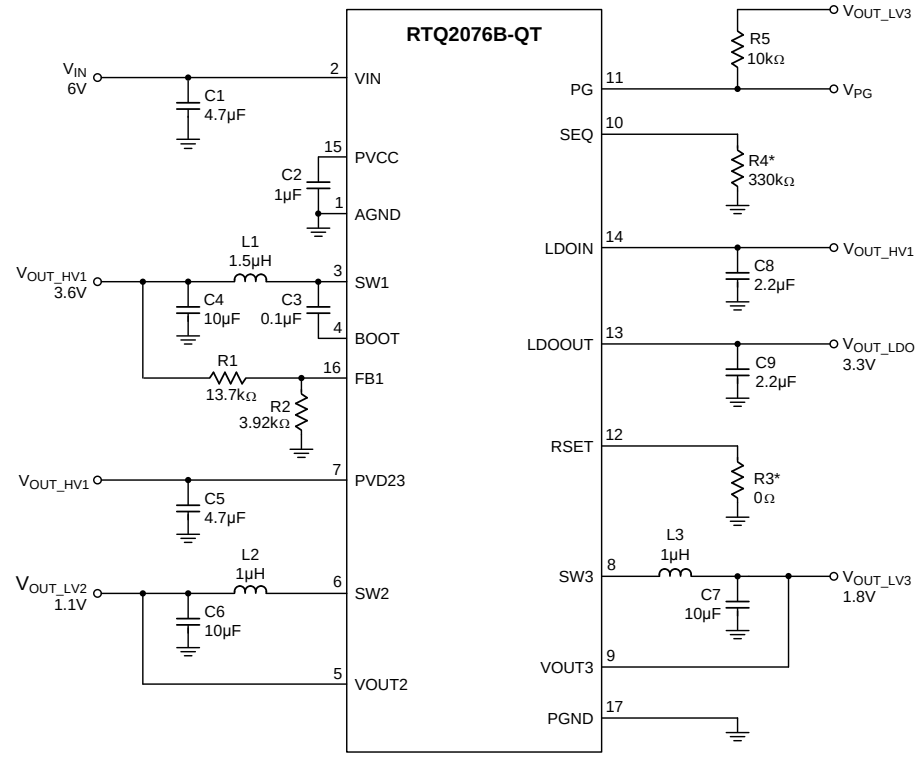


Table 2. Component List of Evaluation Board

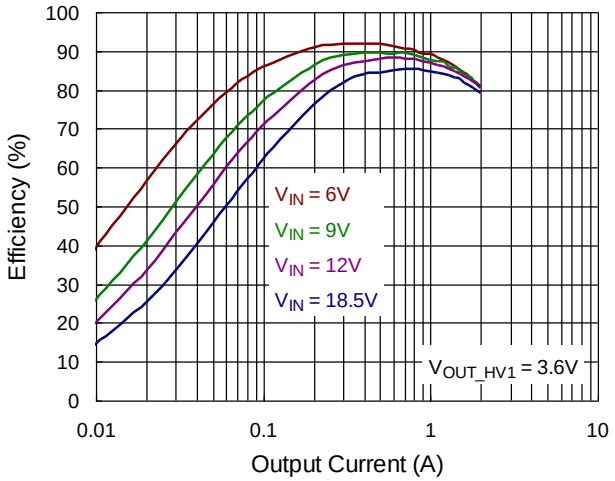
Reference	Qty	Part Number	Description	Package	Manufacturer
C1	1	GCJ31CR71E475KA12	4.7μF/25V/X7R	1206	MURATA
C2	1	GRT155C81A105KE01	1μF/10V/X6S	0402	MURATA
C3	1	GRT155R71C104KE01	0.1μF/16V/X7R	0402	MURATA
C4, C6, C7	1	GRT188C81A106ME13	10μF/10V/X6S	0603	MURATA
C5	1	GRT188C81C475KE13	4.7μF/16V/X6S	0603	MURATA
C8, C9	1	GRT155C81A225KE13	2.2μF/10V/X6S	0402	MURATA
L1	1	TFM201610ALMA1R5MTAA	1.5μH/3.1A/85mΩ	0806	TDK
L2, L3	1	TFM201610ALMA1R0MTAA	1μH/3.7A/50mΩ	0806	TDK
R1	1	MR02X1372FAL	13.7kΩ/1%	0201	WALSIN
R2	1	MR02X3921FAL	3.92kΩ/1%	0201	WALSIN
R3*	1	MR02X000 PAL	0Ω/Jumper	0201	WALISN
R4*	1	MR02X3303FAL	330kΩ/1%	0201	WALSIN
R5	1	MR02X1002FAL	10kΩ/1%	0201	WALSIN

R3* : Resistor is adjustable with different LDO output voltages.

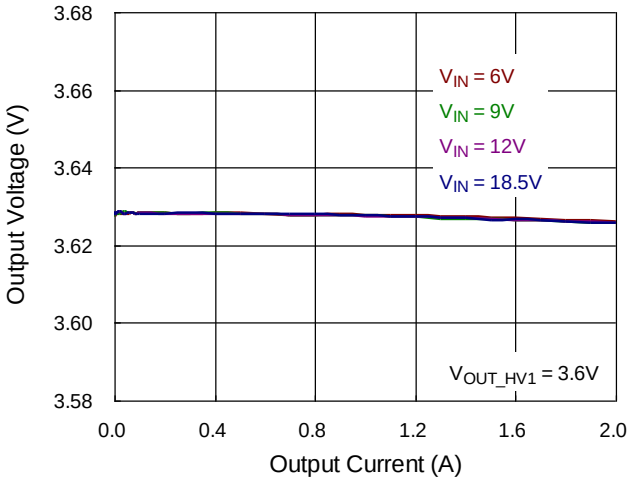
R4* : Resistor is adjustable with different power on sequences.

Typical Operating Characteristics

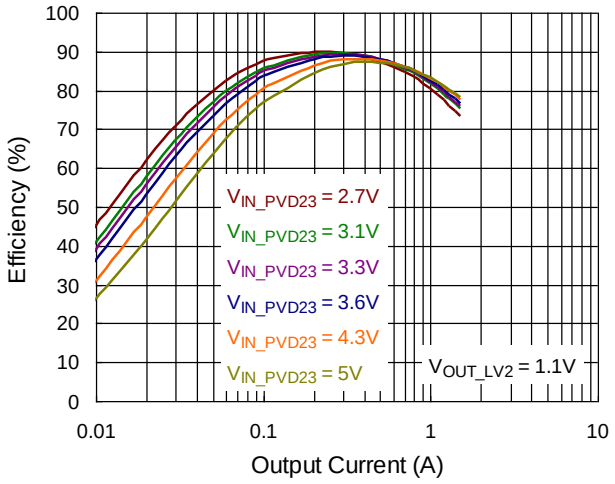
HVBuck1 Efficiency



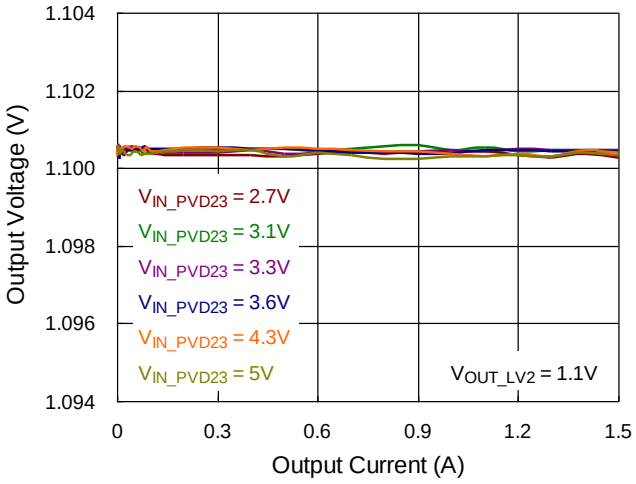
HVBuck1 Load Regulation



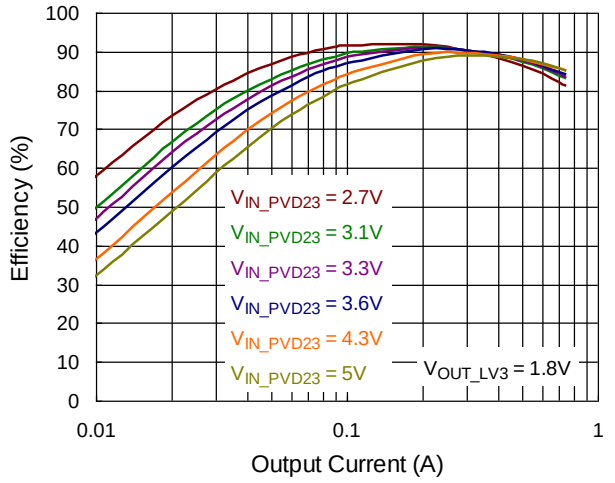
LVBuck2 Efficiency



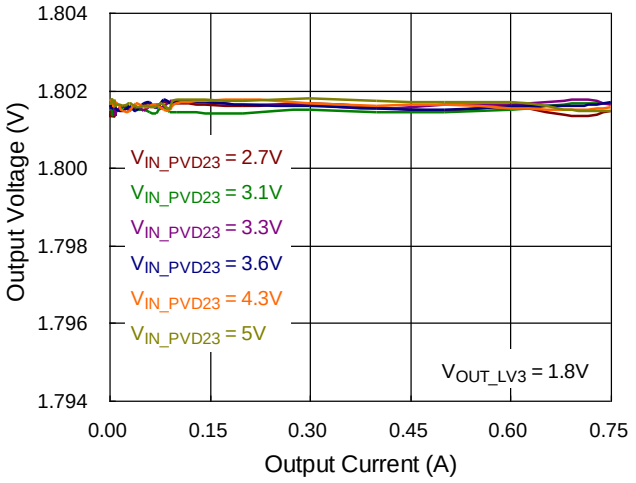
LVBuck2 Load Regulation



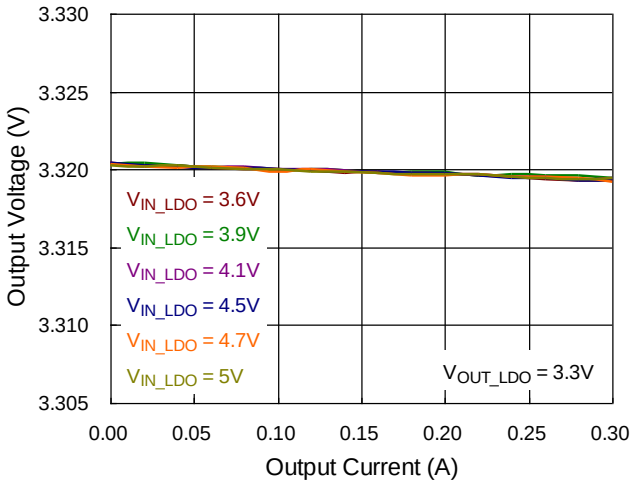
LVBuck3 Efficiency



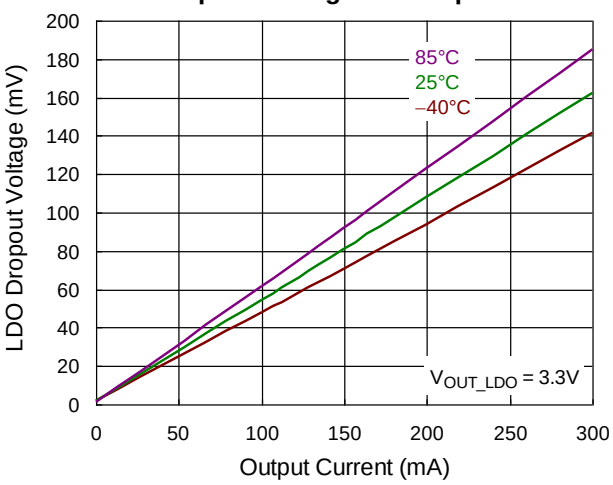
LVBuck3 Load Regulation



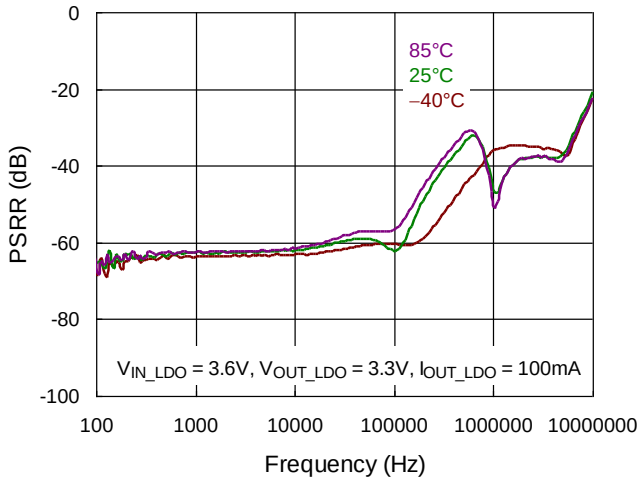
LDO Load Regulation



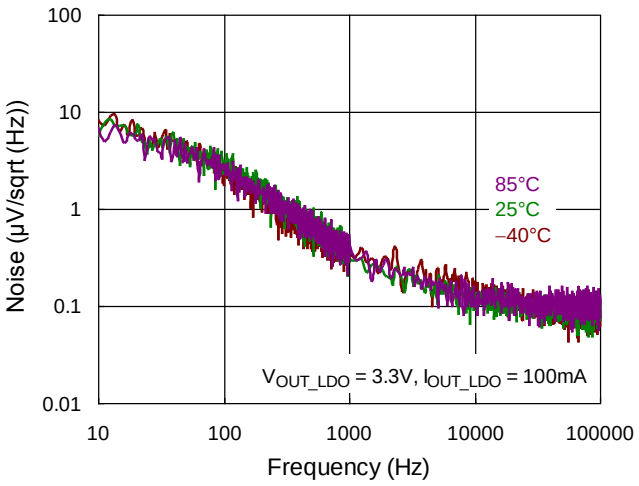
LDO Dropout Voltage vs. Output Current



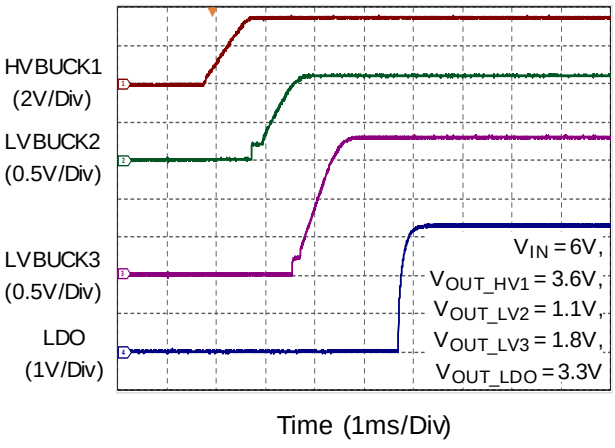
LDO PSRR



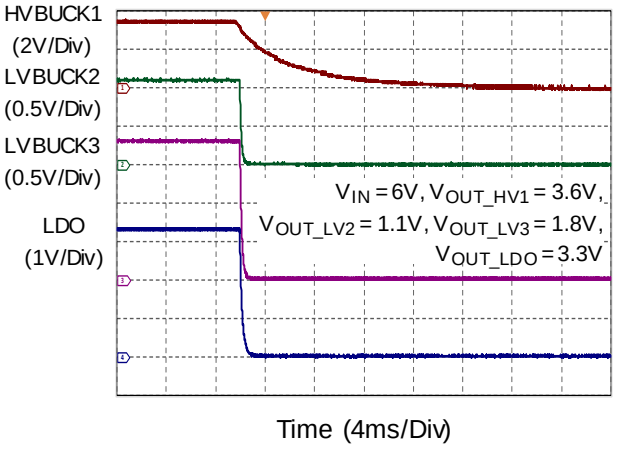
LDO Output Noise



SEQ9 Power On



SEQ9 Power Off



Application Information

Power Sequence Control

The RTQ2076A-QT/RTQ2076B-QT supports 10 power-on sequences for the step-down converters and LDO via the dedicated resistor on SEQ pin. SEQ pin is not allowable at floating state and resistance selected out of range is not guaranteed to correct power-on sequence. In addition, there is only simultaneous power-off for all outputs. To fix the resistor selection on SEQ pin before enabling the device. Any change during the power on procedure is not guarantee to the correct power-on sequence. Below table shows the power-on sequence with its corresponding resistance.

Table 3. Power-On Sequence Control

SEQ No.	Resistance on SEQ (Ω)			Sequence				
	Min	Typ	Max					
SEQ0	1.07M	1.1M	1.13M	CH1	CH4	CH3	CH2	SEQOUT
SEQ1	319k	330k	341k	CH1	CH2	CH3	SEQOUT	CH4
SEQ2	164k	169k	174k	CH1	CH2	SEQOUT	CH3	CH4
SEQ3	81.6k	84.5k	87.4k	CH1	SEQOUT	CH2	CH4	CH3
SEQ4	45.4k	47k	48.6k	CH1	CH2, CH3, CH4, SEQOUT			
SEQ5	26.1k	27k	27.9k	CH1, CH2, CH3, CH4, SEQOUT				
SEQ6	14.5k	15k	15.5k	CH1	CH3	CH2	CH4	SEQOUT
SEQ7	7.78k	8.06k	8.34k	CH1	CH3	CH4	CH2	SEQOUT
SEQ8	Short to PVCC			CH1	SEQOUT	CH2	CH3	CH4
SEQ9	Short to PGND			CH1	CH2	CH3	CH4	SEQOUT

Note :

(1) The SEQOUT output exists only in RTQ2076A-QT. After SEQOUT output high state 1ms passed, the next channel continues to proceed power on sequence.

(2) For RTQ2076B-QT, 1ms time interval will substitute the SEQOUT output. Below is the SEQ1 example.

For RTQ2076A-QT, CH1 → CH2 → CH3 → SEQOUT → CH4

For RTQ2076B-QT, CH1 → CH2 → CH3 → 1ms → CH4

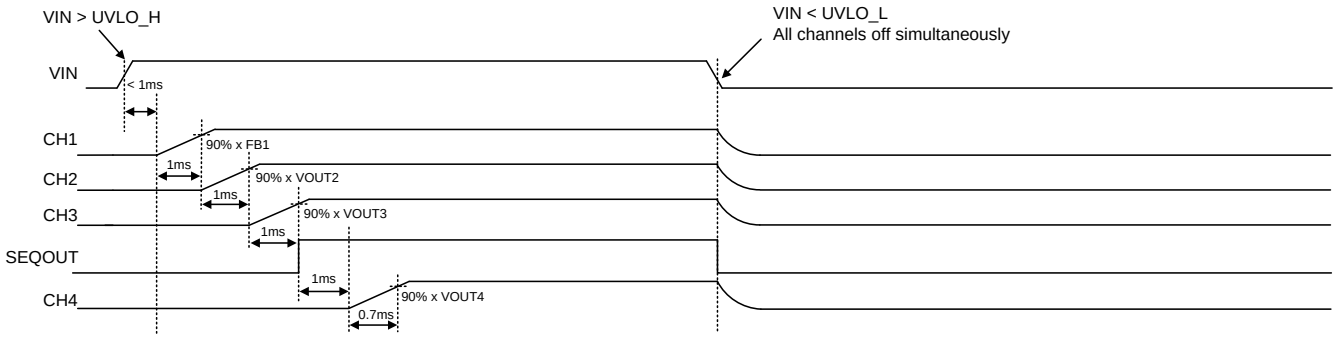


Figure 1. Example SEQ1 for RTQ2076A-QT

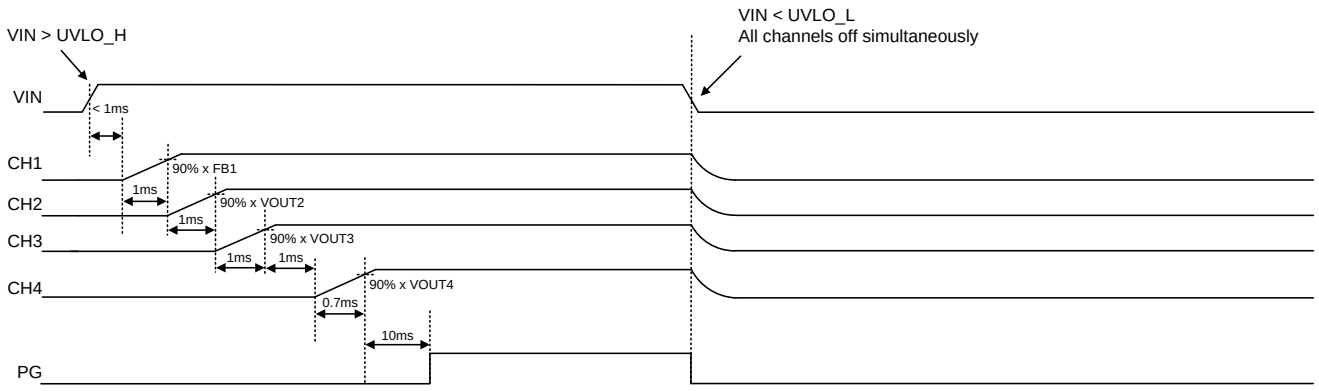


Figure 2. Example SEQ1 for RTQ2076B-QT

Output Voltage Setting

- **HVBuck1**

  The output voltage set by external feedback resistors expressed in the following equation.

$$V_{OUT\_HV1} = \left(1 + \frac{R1}{R2}\right) \times V_{FB1}$$

  Where the reference voltage V_{FB1} is 0.8V (typ.)

  The placement of the resistive divider should be as close as possible to the FB1 pin. For better output voltage accuracy, the divider resistors with ±1% tolerance or better should be used. The resistance ranges from few kΩ to hundreds of kΩ is recommended.

- **LVBuck2 and LVBuck3**

  The output voltage of LVBuck2 is fixed 1.1V.

  The output voltage of LVBuck3 is fixed 1.8V.

- **LDO**

  The LDO output voltage is controlled by setting the dedicated resistor on RSET pin. RSET pin is not allowable at floating state and resistance selected out of range is not guaranteed to correct output voltage. Changing of the output voltage real time is not recommended. To fix the resistor selection on RSET pin before enabling the device.

Table 4. LDO Output Voltage

RSET No.	Resistor on REST (Ω)			Voltage (V)
	Min	Typ	Max	
RSET0	1.07M	1.1M	1.13M	3.5
RSET1	319k	330k	341k	3.4
RSET2	164k	169k	174k	3.2
RSET3	81.6k	84.5k	87.4k	3.1
RSET4	45.4k	47k	48.6k	3.0
RSET5	26.1k	27k	27.9k	2.8
RSET6	14.5k	15k	15.5k	2.7
RSET7	7.78k	8.06k	8.34k	1.8
RSET8	Short to PVCC			2.9
RSET9	Short to PGND			3.3

Channel Protection Features

The RTQ2076A-QT/RTQ2076B-QT equips protections to prevent the device from damages causing by abnormal operations or fault conditions. (Over-load, Short-circuit, Soldering issue…etc.)

- **Under-Voltage Protection (UVP)**
  - **HVBuck1, LVBuck2, LVBuck3 and LDO**

    The device disables all channels and enters into latch off state if step-down converter or LDO output under voltage fault detected continuously over deglitch time and the device only can re-start with V_{IN} ON/OFF.

- **Over-Voltage Protection (OVP)**
  - ▸ **HVBuck1**

    When FB1 pin over-voltage fault detected, the high-side and low-side MOSFETs turn off immediately and auto-recover to switch until FB1 pin's voltage decrease to the reset level.

  - ▸ **LVBuck2, LVBuck3 and LDO**

    The device disables all channels when step-down converter or LDO output over-voltage fault detected continuously over deglitch time. When the fault released, the device auto-restarts all channels in sequence.

- **Over-Current Protection (OCP)**
  - ▸ **HVBuck1, LVBuck2 and LVBuck3**

    The step-down converter includes a cycle-by-cycle high-side MOSFET peak current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. If an over-current condition occurs, the controller will immediately turn off the high-side MOSFET and turn on the low-side MOSFET to prevent the inductor current exceeding the peak current limit level. After inductor current decreasing to below the valley current limit, the high-side MOSFET resume switching on. If over-current fault further detected continuously over than deglitch time, the device disables all channels and enters into latch off state and the device only can re-start with V_{IN} ON/ OFF.

  - ▸ **LDO**

    When the load reaches the current limit threshold, the current sent to the output will kept at current limit level. If over-current fault detected continuously over than the deglitch time, the device disables all channels and enters into latch off state and the device only can re-start with V_{IN} ON/ OFF.

- **Input Over-Voltage Protection (OVP)**
  - ▸ **LVBuck2, LVBuck3 and LDO**

    If the input voltage of step-down converters (LVBuck2, LVBuck3) or LDO reaches over-voltage protection level, the device disables all channels. After fault removed, it auto-restarts all channels in sequence.

Table 5. Protection

Channel	Type	Threshold (Typ.)	Deglitch Time (Typ.)	Protection	Reset and Threshold (Typ.)
System	UVLO	V_{IN} ≤ 3.3V (after IC Operation)	32µs	Disable all channels	V_{IN} ≥ 3.8V
	OVP	V_{IN} ≥ 20V	5ms	Disable all channels then latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OTP	T_J ≥ 160°C	5µs	Disable all channels then latch-off protection	T_J ≤ 140°C and V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
CH1 HVBuck1	UVP	V_{FB1} ≤ 0.8V x 50%	5µs	Disable all channels then latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{FB1} ≥ 0.8V x 110%	NA	High/Low-side MOSFETs off, low-side MOSFET conditionally ON to charge the BOOT capacitor for driving high-side MOSFET.	V_{FB1} < 0.8V x 110%
	OCP	I_{L1_peak} ≥ 3A	10ms	Cycle-by-cycle detection If keep 10ms, disable all channels then latch-off protection.	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
CH2 LVBuck2	UVP	V_{OUT_LV2} ≤ 1.1V x 50%	5µs	Disable all channels then latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{OUT_LV2} ≥ 1.1V x 120%	5ms	Disable all channels	V_{OUT2} ≤ 1.1V x 110% with deglitch 5ms
	OCP	I_{L2_peak} ≥ 2A	10ms	Cycle-by-cycle detection If keep 10ms, disable all channels then latch-off protection.	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	Input OVP	V_{IN_PVD23} ≥ 5.8V	5µs	Disable all channels	V_{IN_PVD23} ≤ 5.22V with deglitch 5µs
CH3 LVBuck3	UVP	V_{OUT_LV3}≤1.8V x 50%	5µs	Disable all channels then latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{OUT_LV3} ≥ 1.8V x 120%	5ms	Disable all channels	V_{OUT3} ≤ 1.8V x 110% with deglitch 5ms
	OCP	I_{L3_peak} ≥ 1.2A	10ms	Cycle-by-cycle detection If keep 10ms, disable all channels then latch-off protection.	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	Input OVP	V_{IN_PVD23} ≥ 5.8V	5µs	Disable all channels	V_{IN_PVD23} ≤ 5.22V with deglitch 5µs

Channel	Type	Threshold (Typ.)	Deglitch Time (Typ.)	Protection	Reset and Threshold (Typ.)
CH4 LDO	UVP	$V_{OUT\_LDO} \leq V_{OUT\_LDO}$ setting x 40%	5µs	Disable all channels then latch-off protection	$V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$
	OVP	$V_{OUT\_LDO} \geq V_{OUT\_LDO}$ x 125%	5ms	Disable all channels	$V_{OUT\_LDO} \leq V_{OUT\_LDO}$ x 110% with deglitch 5ms
	OCP	$I_{OUT\_LDO} \geq 450mA$	10ms	Disable all channels then latch-off protection	$V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$
	Input OVP	$V_{IN\_LDO} \geq 5.8V$	5µs	Disable all channels	$V_{IN\_LDO} \leq 5.3V$ with deglitch 5µs

Input and Output Capacitor Selection

- **HVBuck1, LVBuck2 and LVBuck3**

  It is recommended at least a 4.7µF input capacitor with a 10µF output capacitor for step-down converters. The ripple voltage is an important index for choosing output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The output ripple can be calculated as below.

$$\Delta V_{OUTRipple} = \Delta V_{ESR} + \Delta V_{OUT} = \Delta V_{ESR} + \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

  where $\Delta V_{ESR} = I_{Crms} \times R_{CESR}$

- **LDO**

  Like any low dropout regulator, the external capacitor of the RTQ2076A-QT/RTQ2076B-QT must be carefully selected for regulator stability and performance. Using a 2.2µF capacitor for the LDO's input and output is suitable.

  Additional capacitor paralleled on the output may get better noise suppression but also lead to higher input inrush current when LDO outputs. It should be taken into consideration carefully.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WETD-VQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (150°C – 25°C) / (30°C/W) = 4.16W for a WETD-VQFN-16L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

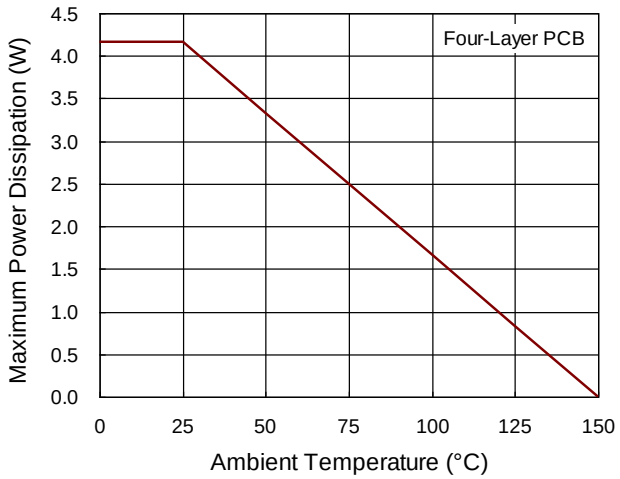


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

The PCB layout is an important step to maintain the high performance of the RTQ2076A-QT/ RTQ2076B-QT. Both the high current and the fast switching nodes demand full attention to the PCB layout to keep the robustness of the RTQ2076A-QT/ RTQ2076B-QT through the PCB layout. Improper layout might lead to the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RTQ2076A-QT/RTQ2076B-QT, the following PCB layout guidelines must be strictly followed.

- The trace from switching node to inductor should be as short as possible to minimized the switching loop for better EMI.
- Place the input and output capacitors close to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- Connect the AGND and PGND to a strong ground plane for maximum thermal dissipation and noise protection.
- Directly connect the step-down converter's output capacitor to the feedback network to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

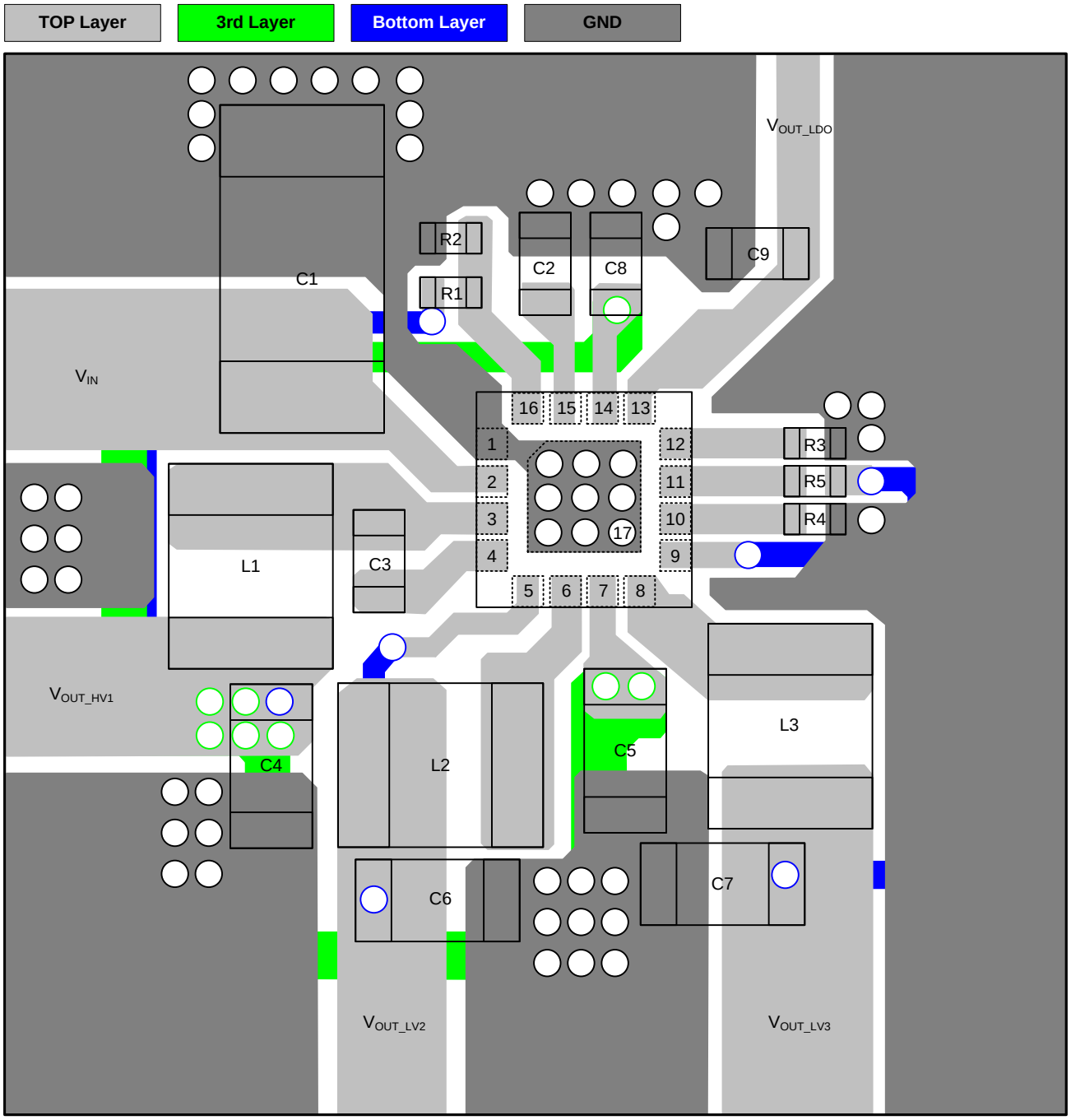
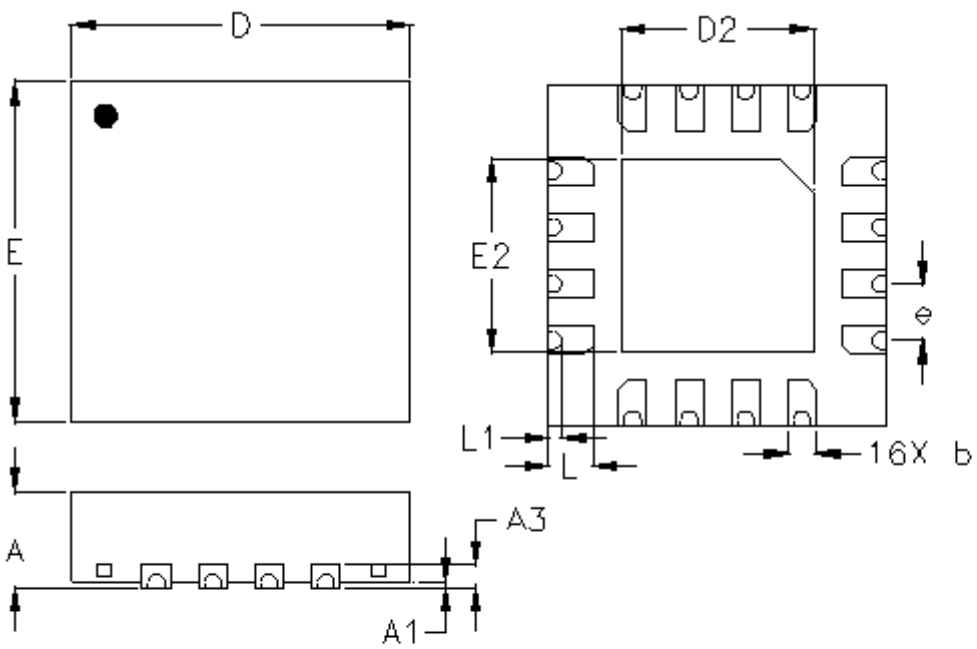


Figure 4. PCB Layout Guide

Outline Dimension



DETAIL A

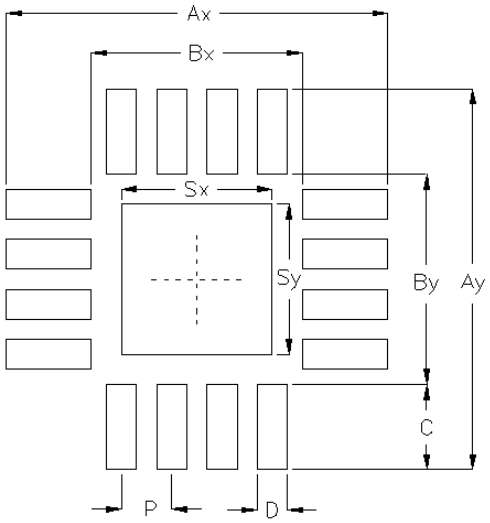
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.650	1.750	0.065	0.069
E	2.950	3.050	0.116	0.120
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018
L1	0.075	0.175	0.003	0.007

WETD V-Type 16L QFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
WETD-V/W/U/XQFN3x3-16	16	0.50	3.80	3.80	2.10	2.10	0.85	0.30	1.50	1.50	±0.05

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单击下面可查看定价，库存，交付和生命周期等信息

>>Richtek(台湾立锜)