9A, 18V, 500kHz, ACOT™ Synchronous Step-Down Converter

General Description

The RT6239A/B is a high-performance 500kHz, 9A step-down regulator with internal power switches and synchronous rectifiers. It features quick transient response using its Advanced Constant On-Time (ACOT™) control architecture that provides stable operation with small ceramic output capacitors and without complicated external compensation, among other benefits. The input voltage range is from 4.5V to 18V and the output is adjustable from 0.7V to 8V. The proprietary ACOT™ control improves upon other fast response constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance. The RT6239A/B is stable with and optimized for ceramic output capacitors. With internal 30mΩ switches and 12mΩ synchronous rectifiers, the RT6239A/B displays excellent efficiency and good behavior across a range of applications, especially for low output voltages and low duty cycles. Cycle-by-cycle current limit provides protection against shorted outputs, input under-voltage lockout, externally-adjustable soft-start, output under- and over-voltage protection, and thermal shutdown provide safe and smooth operation in all operating conditions. The RT6239A/B is available in the UQFN-14L 2x3 (FC) package, with exposed thermal pad.

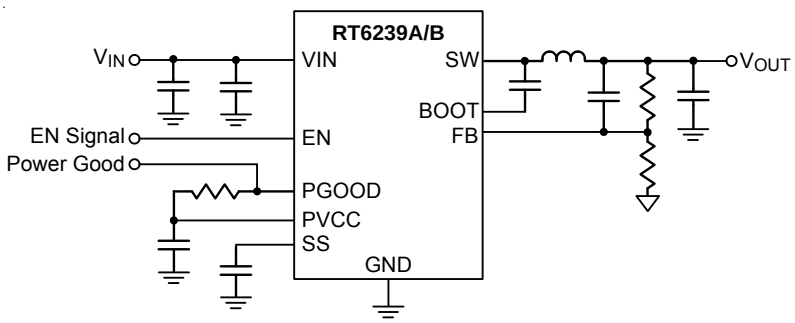
Features

- **Fast Transient Response**
- **Advanced Constant On-Time (ACOT™) Control**
- **4.5V to 18V Input Voltage Range**
- **Adjustable Output Voltage from 0.7V to 8V**
- **9A Output Current**
- **30mΩ Internal High-Side N-MOSFET and 12mΩ Internal Low-Side N-MOSFET**
- **Steady 500kHz Switching Frequency**
- **Up to 95% Efficiency**
- **Optimized for All Ceramic Capacitors**
- **Externally-Adjustable, Pre-Biased Compatible Soft-Start**
- **Cycle-by-Cycle Current Limit**
- **Input Under-Voltage Lockout**
- **Output Over- and Under-Voltage Protection**
- **Power Good Output**
- **Thermal Shutdown**

Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

Simplified Application Circuit



Ordering Information

RT6239A/B□□□

- Package Type
  QUF : UQFN-14L 2x3 (U-Type) (FC)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Option
  H : Hiccup Mode UVP
  L : Latched OVP & UVP
- A : PSM
  B : PWM

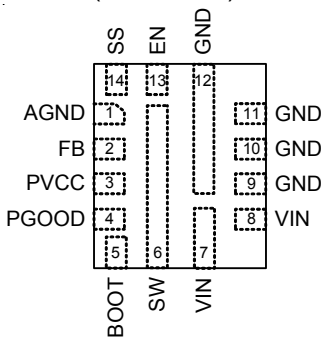
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

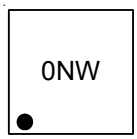
(TOP VIEW)



UQFN-14L 2x3 (FC)

Marking Information

RT6239ALGQUF



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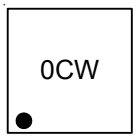
RT6239BLGQUF



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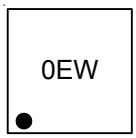

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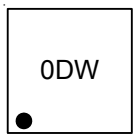

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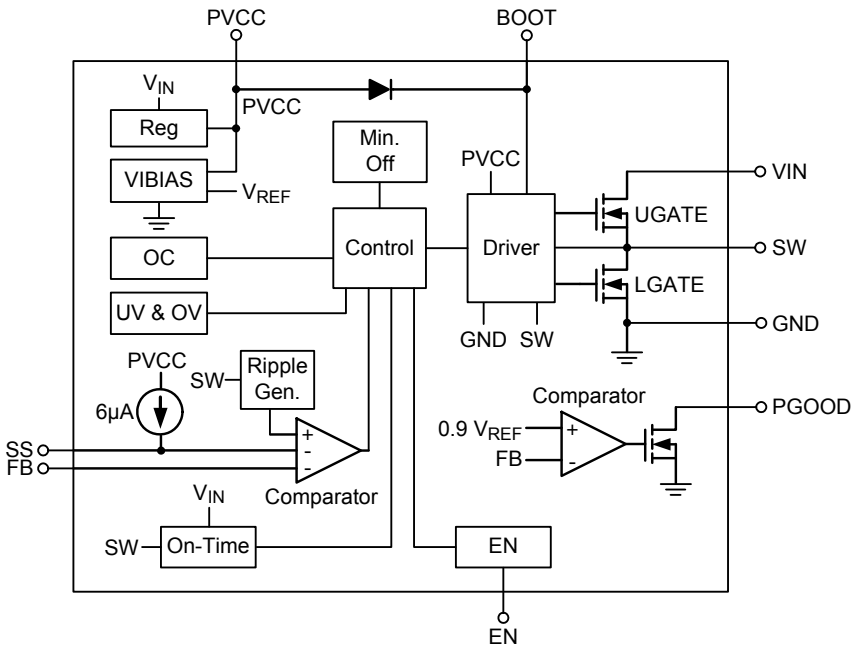
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	AGND	Analog GND.
2	FB	Feedback Voltage Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback reference voltage is 0.7V typically.
3	PVCC	Internal Regulator Output. Connect a 1μF capacitor to GND to stabilize output voltage.
4	PGOOD	Power Good Indicator Open-Drain Output.
5	BOOT	Bootstrap Supply for High-Side Gate Driver. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between the SW and BOOT pins to form a floating supply across the power switch driver. A 0.1μF capacitor is recommended for use.
6	SW	Switch Node. Connect this pin to an external L-C filter.
7, 8	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitor.
9, 10, 11, 12	GND	Ground.
13	EN	Enable Control Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
14	SS	Soft-Start Time Setting. An external capacitor should be connected between this pin and GND.

Function Block Diagram



Detailed Description

The RT6239A/B is a high-performance 500kHz 9A step-down regulators with internal power switches and synchronous rectifiers. It features an Advanced Constant On-Time (ACOT™) control architecture that provides stable operation with ceramic output capacitors without complicated external compensation, among other benefits. The ACOT™ control mode also provides fast transient response, especially for low output voltages and low duty cycles.

The input voltage range is from 4.5V to 18V and the output is adjustable from 0.7V to 8V. The proprietary ACOT™ control scheme improves upon other constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. The RT6239A/B are optimized for ceramic output capacitors. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

Constant On-Time (COT) Control

The heart of any COT architecture is the on-time one shot. Each on-time is a pre-determined "fixed" period that is triggered by a feedback comparator. This robust arrangement has high noise immunity and is ideal for low duty cycle applications. After the on-time one-shot period, there is a minimum off-time period before any further regulation decisions can be considered. This arrangement avoids the need to make any decisions during the noisy time periods just after switching events, when the switching node (SW) rises or falls. Because there is no fixed clock, the high-side switch can turn on almost immediately after load transients and further switching pulses can ramp the inductor current higher to meet load requirements with minimal delays.

Traditional current mode or voltage mode control schemes typically must monitor the feedback voltage, current signals (also for current limit), and internal ramps and compensation signals, to determine when to turn off the high-side switch and turn on the synchronous rectifier. Weighing these small signals in a switching environment is difficult to do just after switching large currents, making those architectures problematic at low duty cycles and in less than ideal board layouts.

Because no switching decisions are made during noisy time periods, COT architectures are preferable in low duty cycle and noisy applications. However, traditional COT control schemes suffer from some disadvantages that preclude their use in many cases. Many applications require a known switching frequency range to avoid interference with other sensitive circuitry. True constant on-time control, where the on-time is actually fixed, exhibits variable switching frequency. In a step-down converter, the duty factor is proportional to the output voltage and inversely proportional to the input voltage. Therefore, if the on-time is fixed, the off-time (and therefore the frequency) must change in response to changes in input or output voltage.

Modern pseudo-fixed frequency COT architectures greatly improve COT by making the one-shot on-time proportional to VOUT and inversely proportional to VIN. In this way, an on-time is chosen as approximately what it would be for an ideal fixed-frequency PWM in similar input/output voltage conditions. The result is a big improvement but the switching frequency still varies considerably over line and load due to losses in the switches and inductor and other parasitic effects.

Another problem with many COT architectures is their dependence on adequate ESR in the output capacitor, making it difficult to use highly-desirable, small, low-cost, but low-ESR ceramic capacitors. Most COT architectures use AC current information from the output capacitor, generated by the inductor current passing through the ESR, to function in a way like a current mode control system. With ceramic capacitors the inductor current information is too small to keep the control loop stable, like a current mode system with no current information.

ACOT™ Control Architecture

Making the on-time proportional to VOUT and inversely proportional to VIN is not sufficient to achieve good constant-frequency behavior for several reasons. First, voltage drops across the MOSFET switches and inductor

cause the effective input voltage to be less than the measured input voltage and the effective output voltage to be greater than the measured output voltage. As the load changes, the switch voltage drops change causing a switching frequency variation with load current. Also, at light loads if the inductor current goes negative, the switch dead-time between the synchronous rectifier turn-off and the high-side switch turn-on allows the switching node to rise to the input voltage. This increases the effective on time and causes the switching frequency to drop noticeably.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. ACOT™ uses this method, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

To achieve good stability with low-ESR ceramic capacitors, ACOT™ uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

ACOT™ One-Shot Operation

The RT6239A/B control algorithm is simple to understand. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference and the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (230ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

Discontinuous Operating Mode (RT6239A Only)

After soft-start, the RT6239A operates in fixed frequency mode to minimize interference and noise problems. The RT6239A uses variable-frequency discontinuous switching at light loads to improve efficiency. During discontinuous switching, the on-time is immediately increased to add "hysteresis" to discourage the IC from switching back to continuous switching unless the load increases substantially.

The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for 500kHz switching and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

Current Limit

The RT6239A/B current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between Source and Drain of the synchronous rectifier**.** If the inductor current exceeds the current limit, the on-time one-shot is inhibited (Mask high side signal) until the inductor current ramps down below the current limit. Thus, only when the inductor current is well below the current limit is another on time permitted. This arrangement prevents the average output current from greatly exceeding the guaranteed current limit value, as typically occurs with other valley-type current limits. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level the IC will stop switching (see next section).

Output Under-Voltage Protection

Hiccup Mode

The RT6239AH/RT6239BH provide Hiccup Mode Under-Voltage Protection (UVP). When the FB voltage drops below 60% of the feedback reference voltage, the output

voltage drops below the UVP trip threshold for longer than 270μs (typical) then IC's UVP is triggered. UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RT6239 will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during soft-start period. During hiccup mode, the shutdown time is determined by the capacitor at SS. A 2μA current source discharges VSS from its starting voltage (normally VPVCC). The IC remains shut down until VSS reaches 0.2V, about 10ms for a 3.9nF capacitor. At that point the IC begins to charge the SS capacitor at 6μA, and a normal start-up occurs. If the fault remains, UVP protection will be enabled when VSS reaches 2.2V (typical). The IC will then shut down and discharge the SS capacitor from the 2.2V level, taking about 4ms for a 3.9nF SS capacitor.

Latch Mode

For the RT6239AL/RT6239BL, it provides Latch-Off Mode Under Voltage Protection (UVP). When the FB voltage drops below 60% of the feedback reference voltage, the output voltage drops below the UVP trip threshold for longer than 270μs (typical) then IC's UVP is triggered. UVP function will be triggered to shut down switching operation. In shutdown condition, the RT6239 can be reset by EN pin or power input VIN.

Output Over-Voltage Protection

If the output voltage VOUT rises above the regulation level and lower 1.2 times regulation level, the high-side switch naturally remains off and the synchronous rectifier turns on. For RT6239BL, if the output voltage remains high, the synchronous rectifier remains on until the inductor current reaches the low side current limit. If the output voltage still remains high, then IC's switches remain that the synchronous rectifier turns on and high-side MOS keeps off to operate at typical 500kHz switching protection, again if inductor current reaches low side current limit, the synchronous rectifier will turn off until next protection clock. If the output voltage exceeds the OVP trip threshold (1.2 times regulation level) for longer than 10μs (typical), then IC's output Over-Voltage Protection (OVP) is triggered. RT6239BL chip enters latch mode.

For RT6239AL, if the output voltage VOUT rises above the regulation level and lower 1.2 times regulation level, the high-side switch naturally remains off and the synchronous rectifier turns on until the inductor current reaches zero current. If the output voltage remains high, then IC's switches remain off. If the output voltage exceeds the OVP trip threshold (1.2 times regulation level) for longer than 10μs (typical), the IC's OVP is triggered. RT6239AL chip enters latch mode.

For RT6239BH, if the output voltage remains high, the synchronous rectifier remains on until the inductor current reaches the low side current limit. If the output voltage still remains high, the synchronous rectifier turns on and high-side MOSFET keeps off to operate at typical 500kHz switching protection, again if inductor current reaches low side current limit, the synchronous rectifier will turn off until next protection clock. RT6239BH is without OVP latch function and recover when OV condition release.

For RT6239AH, if the output voltage remains high, the synchronous rectifier remains on until the inductor current reaches zero current. If the output voltage still remains high, then IC's switches remain off. RT6239AH is without OVP latch function and recover when OV condition release.

Latch-Off Mode

The RT6239AL/BL uses latch-off mode OVP and UVP. When the protection function is triggered, the IC will shut down in Latch-Off Mode. The IC stops switching, leaving both switches open, and is latched off. To restart operation, toggle EN or power the IC off and then on again.

Shut-Down, Start-Up and Enable (EN)

The enable input (EN) has a logic-low level of 0.4V. When V_{EN} is below this level the IC enters shutdown mode and supply current drops to less than 10μA. When V_{EN} exceeds its logic-high level of 1.2V the IC is fully operational.

Between these 2 levels there are 2 thresholds (1V typical and 1.2V typical). Switching operation begins when V_{EN} exceeds the upper threshold, and then switching operation stops when V_{EN} decreases to the lower threshold. Since EN is a low voltage input, it must be connected to VIN (up to 18V) with a pull-up resistor for automatic start-up.

Input Under-Voltage Lockout

In addition to the enable function, the RT6239A/B feature an Under-Voltage Lockout (UVLO) function that monitors the internal linear regulator output (VIN). To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when VIN drops below the UVLO-falling threshold. The IC resumes switching when VIN exceeds the UVLO-rising threshold

Soft-Start (SS)

The RT6239A/B soft-start uses an external pin (SS) to clamp the output voltage and allow it to slowly rise. After V_{EN} is high and VIN exceeds its UVLO threshold, the IC begins to source 6μA from the SS pin. An external capacitor at SS is used to adjust the soft-start timing. Following below equation to get the minimum capacitance range in order to avoid UV occur.

$$T = \frac{C_{OUT} \times V_{OUT} \times 0.75 \times 1.2}{(I_{LIM} - \text{Load Current}) \times 0.8}$$

$$C_{SS} \geq \frac{T \times 6\mu A}{V_{REF}}$$

Do not leave SS unconnected. During start-up, while the SS capacitor charges, the RT6239A/B operates in discontinuous switching mode with very small pulses. This prevents negative inductor currents and keeps the circuit from sinking current. Therefore, the output voltage may be pre-biased to some positive level before start-up. Once the VSS ramp charges enough to raise the internal reference above the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated level. After VSS rises above about 2.2V output over- and under-voltage protections are enabled and the RT6239A/B begins continuous-switching operation.

Internal Regulator (PVCC)

An internal linear regulator (PVCC) produces a 5V supply from VIN. The 5V power supplies the internal control circuit, such as internal gate drivers, PWM logic, reference, analog circuitry, and other blocks. 1μF ceramic capacitor for decoupling and stability is required.

PGOOD Comparator

PGOOD is an open-drain output controlled by a comparator connected to the feedback signal. If FB exceeds 90% of the internal reference voltage, PGOOD will be high impedance. Otherwise, the PGOOD output is connected to GND.

External Bootstrap Capacitor (C_{BOOT})

Connect a 0.1μF low ESR ceramic capacitor between BOOT and SW. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET switch.

Some of case, such like duty ratio is higher than 65% application or input voltage is lower than 5.5V which are recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT6239A/B. Note that the external boot voltage must be lower than 5.5V

Over-Temperature Protection

The RT6239A/B includes an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 21V
- Switch Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
- Switch Voltage, <10ns ---------- –3V to (V_{IN} + 0.3V)
- BOOT Voltage ---------- –0.3V to 27.3V
- EN to GND ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  UQFN-14L 2x3 (FC) ---------- 2.1W
- Package Thermal Resistance (Note 2)
  UQFN-14L 2x3 (FC), θ_{JA} ---------- 47.5°C/W
  UQFN-14L 2x3 (FC), θ_{JC} ---------- 4.1°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Supply Current (Shutdown)		I_{SHDN}	V_{EN} = 0V	--	1.5	6	μA
Supply Current (Quiescent)		I_Q	V_{EN} = 2V, V_{FB} = 0.7V	--	0.6	0.9	mA
Logic Threshold							
EN Input Voltage	Logic-High			1.1	1.2	1.3	V
	Logic-Low			--	0.2	--	
V_{FB} Voltage and Discharge Resistance							
Feedback Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 18V	0.692	0.7	0.708	V
Feedback Current		I_{FB}	V_{FB} = 0.71V	–0.1	--	0.1	μA
V_{PVCC} Output							
V_{PVCC} Output Voltage		V_{PVCC}	6V ≤ V_{IN} ≤ 18V, 0 < I_{PVCC} < 5mA	--	5	--	V
Line Regulation			6V ≤ V_{IN} ≤ 18V, I_{PVCC} = 5mA	--	--	5	mV
Load Regulation			0 < I_{PVCC} < 20mA	--	--	20	mV
Output Current		I_{PVCC}	V_{IN} = 6V, V_{PVCC} = 4V, T_A = 25°C	--	210	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$R_{DS(ON)}$						
Switch On-Resistance	$R_{DS(ON)\_H}$	$V_{BOOT} - V_{SW}$ = 5V	--	30	--	mΩ
	$R_{DS(ON)\_L}$		--	12	--	
Current Limit						
Valley Current Limit	I_{LIM}		10.5	12.25	14	A
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	
On-Time Timer Control						
On-Time	t_{ON}	V_{IN} = 12V, V_{OUT} = 1.05V	--	175	--	ns
Minimum On-Time	$t_{ON(MIN)}$		--	60	--	ns
Minimum Off-Time	$t_{OFF(MIN)}$		--	200	--	ns
Soft-Start						
SS Charge Current		V_{SS} = 0V	5	6	7	μA
UVLO						
UVLO Threshold		Wake Up V_{PVCC}	4	4.2	4.4	V
		Hysteresis	--	0.5	--	
Power Good						
PGOOD Threshold		FB Rising	85	90	95	%
		FB Falling	--	80	--	%
PGOOD Sink Current		PGOOD = 0.1V	10	20	--	mA
Output Under-Voltage and Over-Voltage Protection						
OVP Trip Threshold		OVP Detect	115	120	125	%
OVP Propagation Delay			--	10	--	μs
UVP Trip Threshold		UVP Detect	55	60	65	%
		Hysteresis	--	17	--	
UVP Propagation Delay			--	270	--	μs
UVP Enable Delay		Relative to Soft-Start Time	--	t_{SS} x 1.7	--	--

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a highly thermal conductive four-layer test board. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

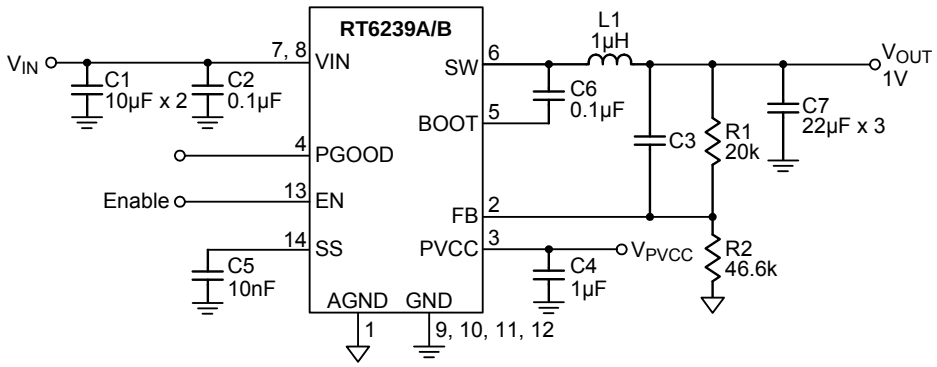
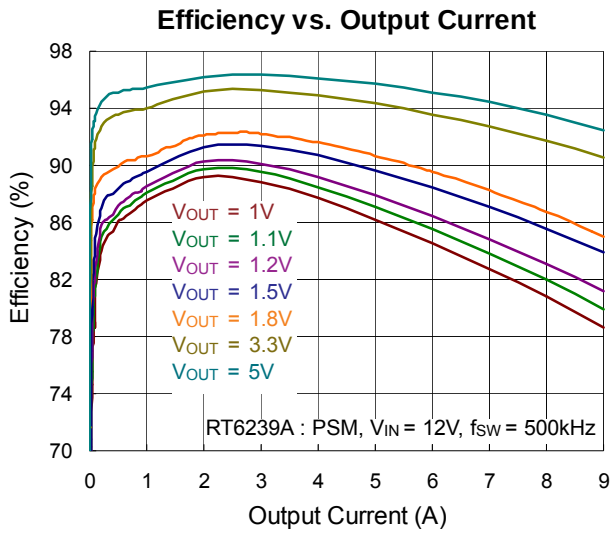
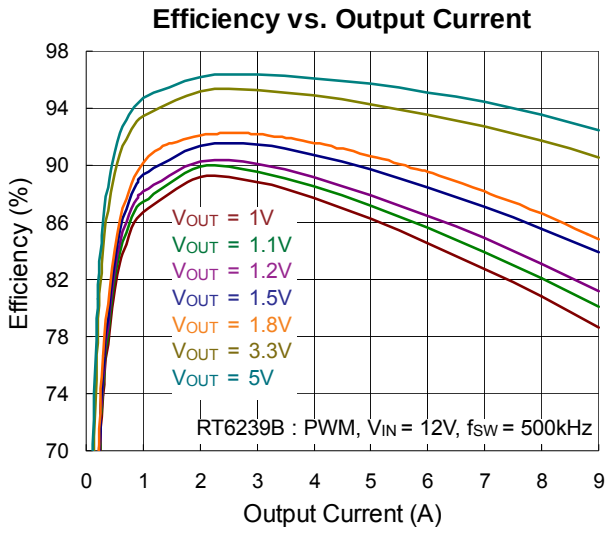


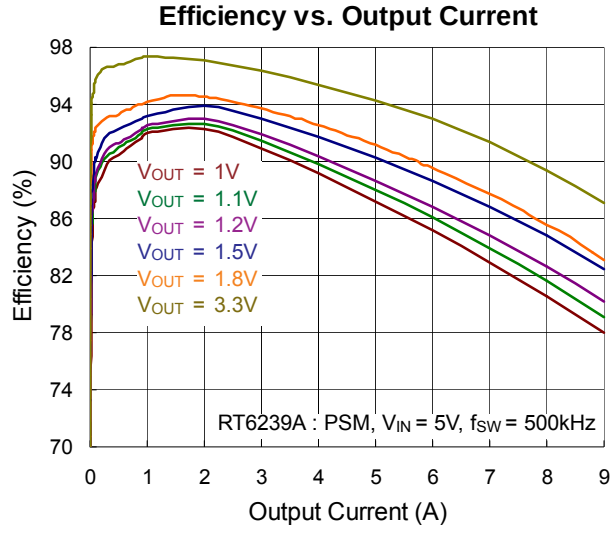
Table 1. Suggested Component Values

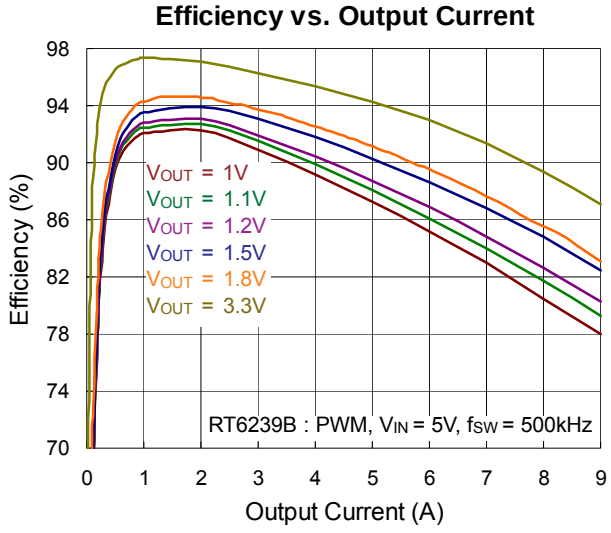
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C3 (pF)	L1 (µH)	C7 (µF)
1	20	46.4	--	1	66
1.5	53.6	46.4	10	1	66
1.8	73.2	46.4	10	1	66
2.5	120	46.4	10	1.5	66
5	287	46.4	10	2	66

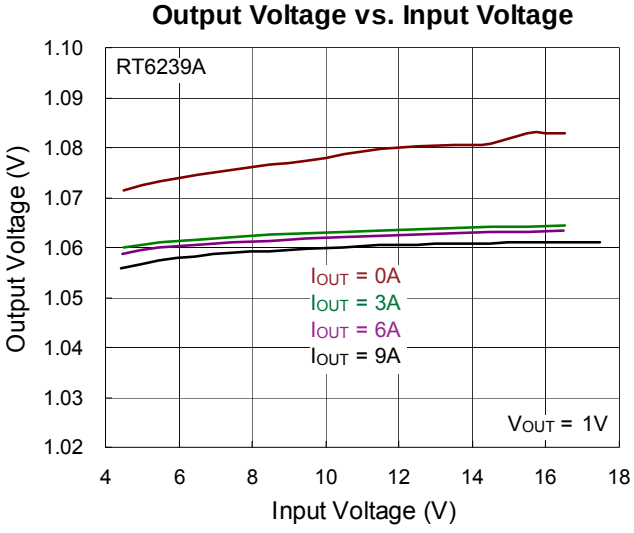
Typical Operating Characteristics

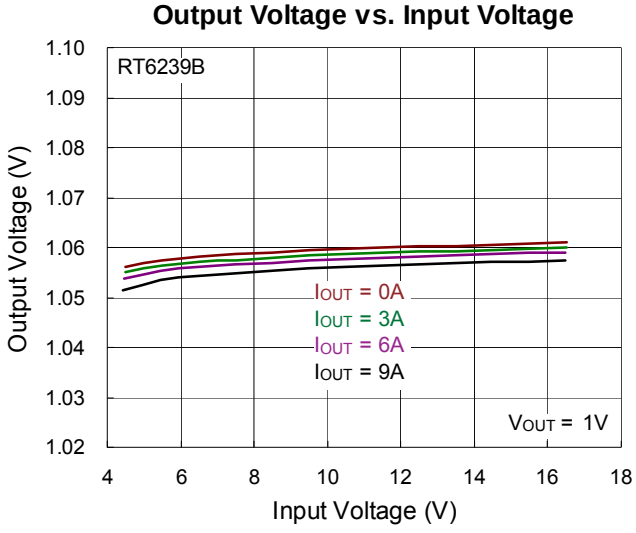




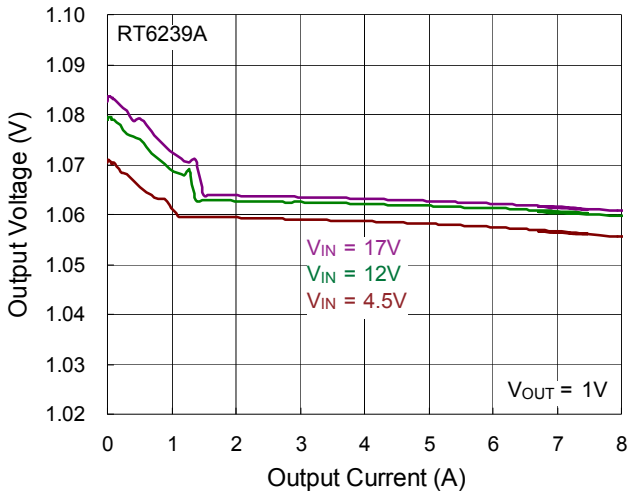




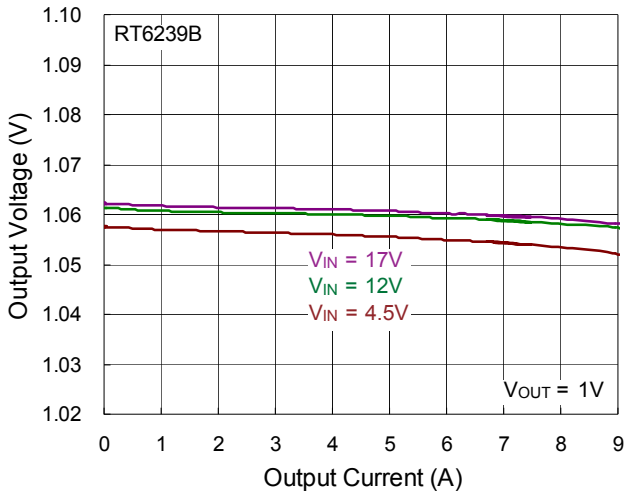




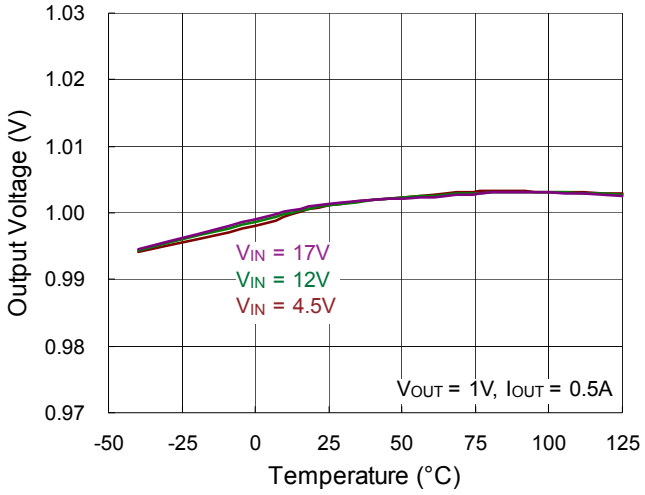
Output Voltage vs. Output Current



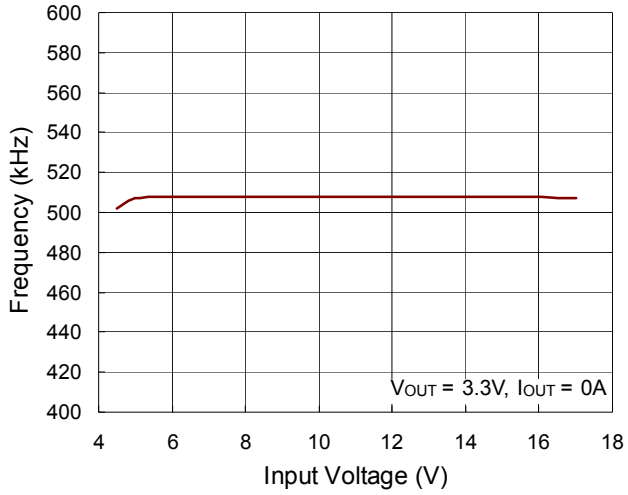
Output Voltage vs. Output Current



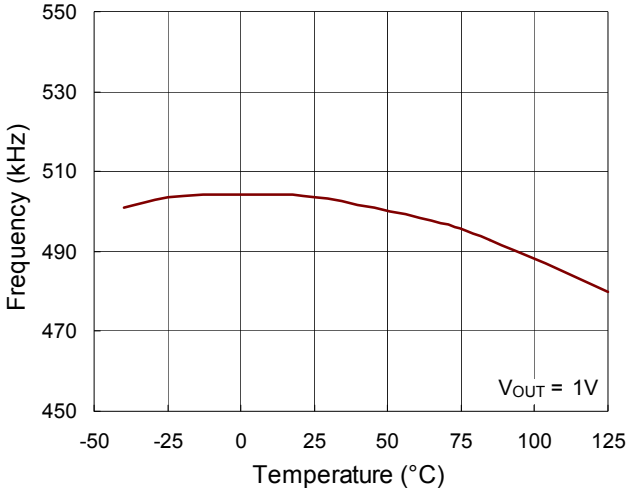
Output Voltage vs. Temperature



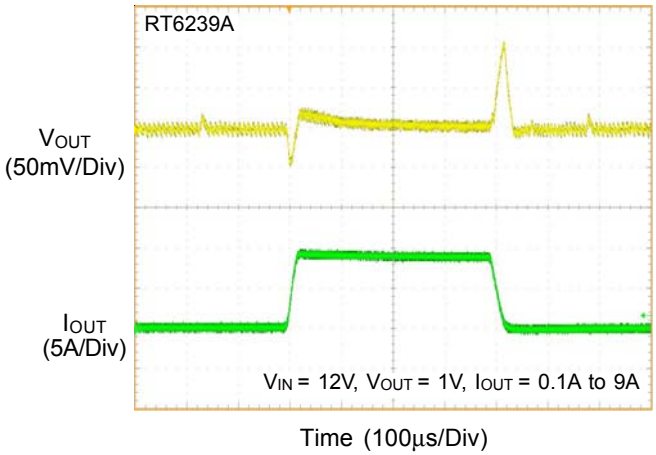
Frequency vs. Input Voltage



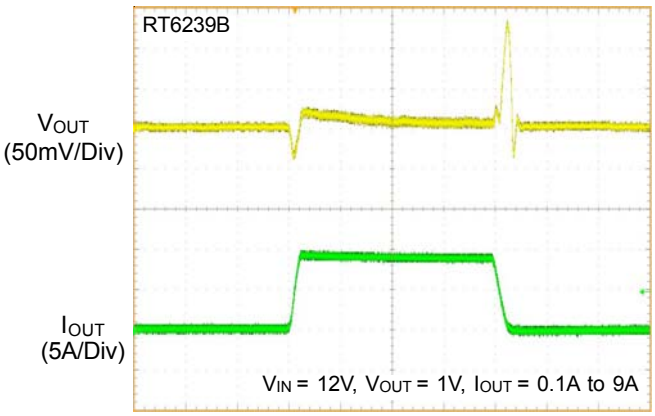
Frequency vs. Temperature



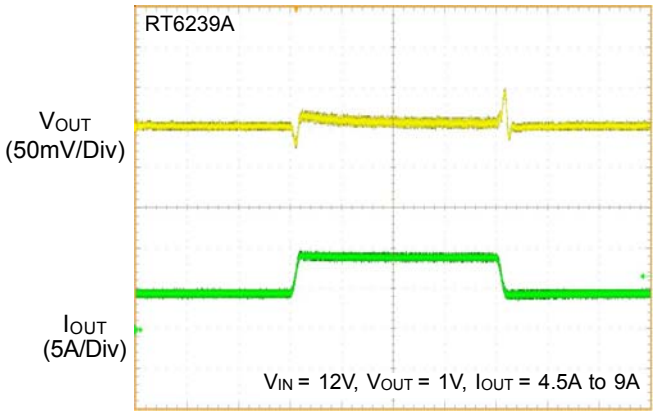
Load Transient Response



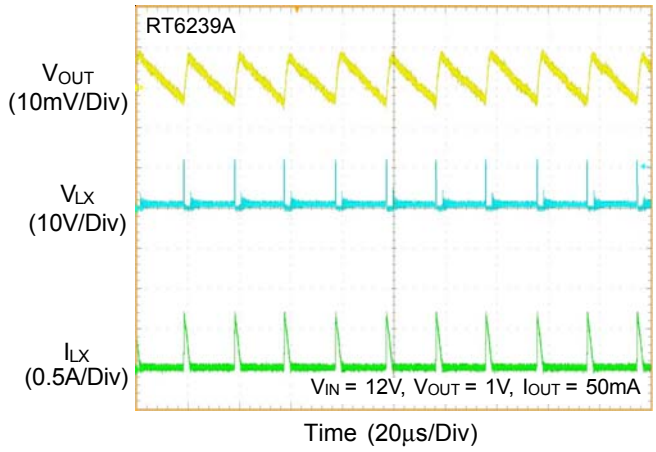
Load Transient Response



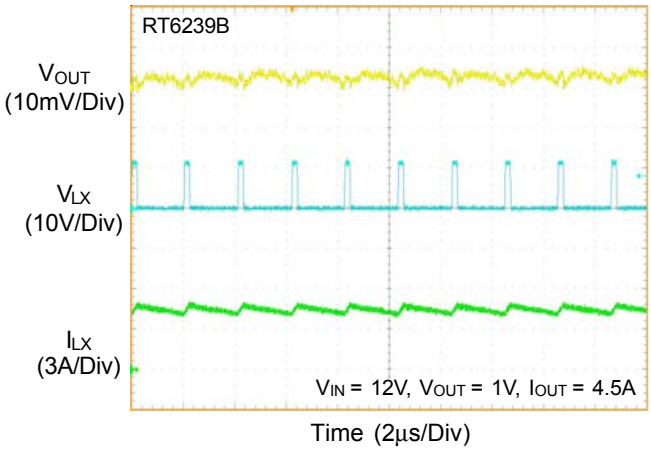
Load Transient Response



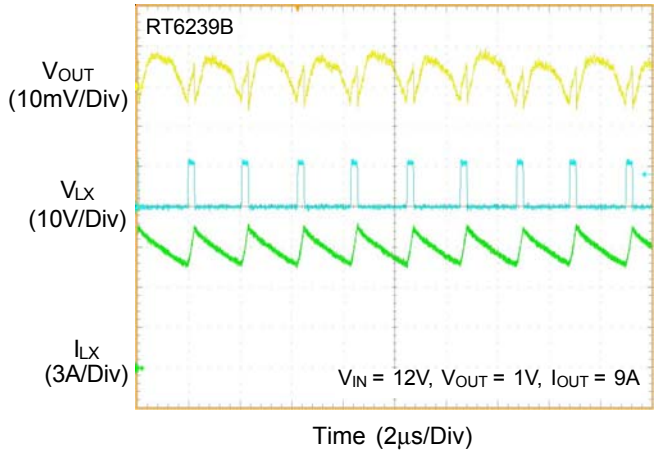
Output Ripple Voltage



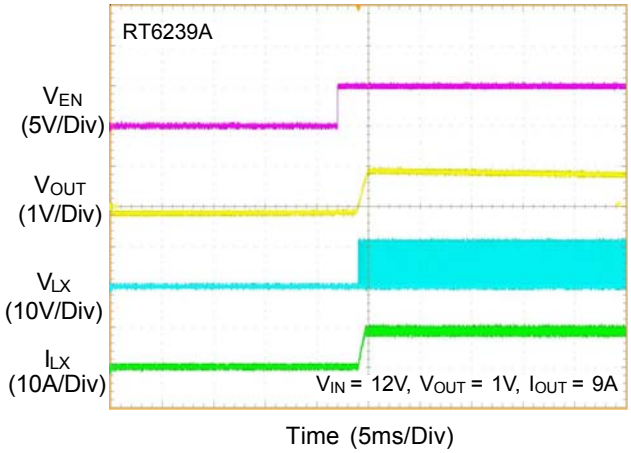
Output Ripple Voltage



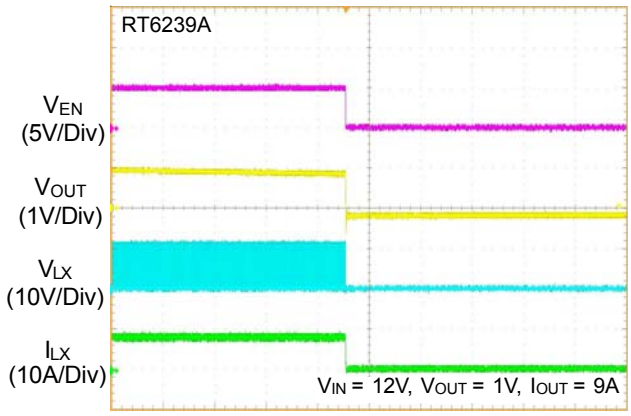
Output Ripple Voltage



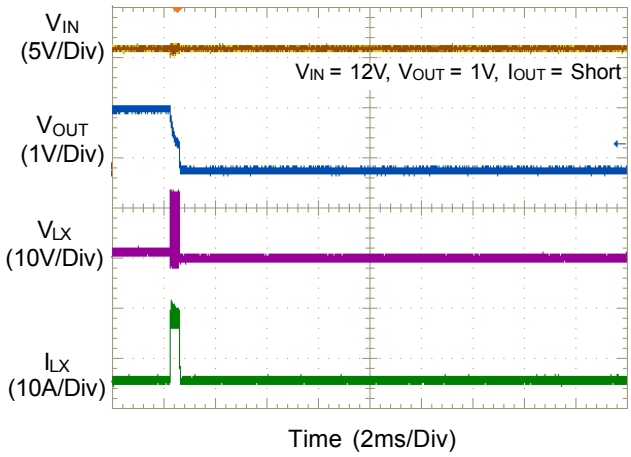
Power On from EN



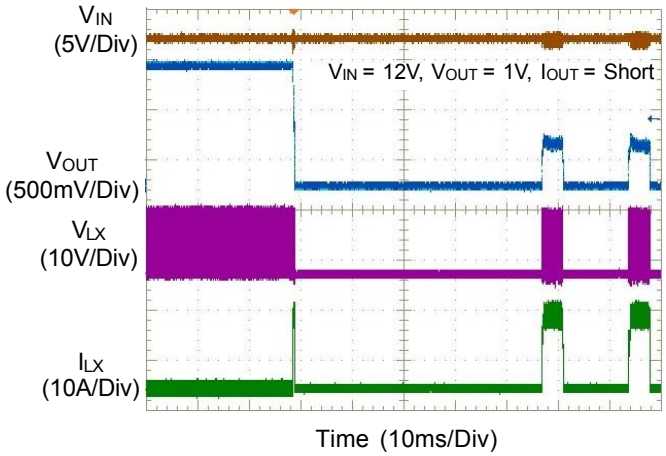
Power Off from EN



UVP Short (Latch Mode)



UVP Short (Hiccup Mode)



Application information

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 15% to 40% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

$$I_{L(VALLEY)} = I_{OUT(MAX)} - \frac{\Delta I_L}{2}$$

Inductor saturation current should be chosen over IC's current limit.

Input Capacitor Selection

The input filter capacitors are needed to smooth out the switched current drawn from the input power source and to reduce voltage ripple on the input. The actual capacitance value is less important than the RMS current rating (and voltage rating, of course). The RMS input ripple current (I_{RMS}) is a function of the input voltage, output voltage, and load current :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. However, take care when these capacitors are used at the input of circuits supplied by a wall adapter or other supply connected through long, thin wires. Current surges through the inductive wires can induce ringing at the RT6239A/B input which could potentially cause large, damaging voltage spikes at VIN. If this phenomenon is observed, some bulk input capacitance may be required. Ceramic capacitors (to meet the RMS current requirement) can be placed in parallel with other types such as tantalum, electrolytic, or polymer (to reduce ringing and overshoot).

Choose capacitors rated at higher temperatures than required. Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application. The typical operating circuit uses two 10μF and one 0.1μF low ESR ceramic capacitors on the input.

Output Capacitor Selection

The RT6239A/B are optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output Ripple

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Feed-forward Capacitor (C_{ff})

The RT6239A/B are optimized for ceramic output capacitors and for low duty cycle applications. However for high-output voltages, with high feedback attenuation, the circuit's response becomes over-damped and transient response can be slowed. In high-output voltage circuits (V_{OUT} > 3.3V) transient response is improved by adding a small "feed-forward" capacitor (C_{ff}) across the upper FB divider resistor (Figure 1), to increase the circuit's Q and reduce damping to speed up the transient response without affecting the steady-state stability of the circuit. Choose a suitable capacitor value that following below step.

- Get the BW the quickest method to do transient response form no load to full load. Confirm the damping frequency. The damping frequency is BW.

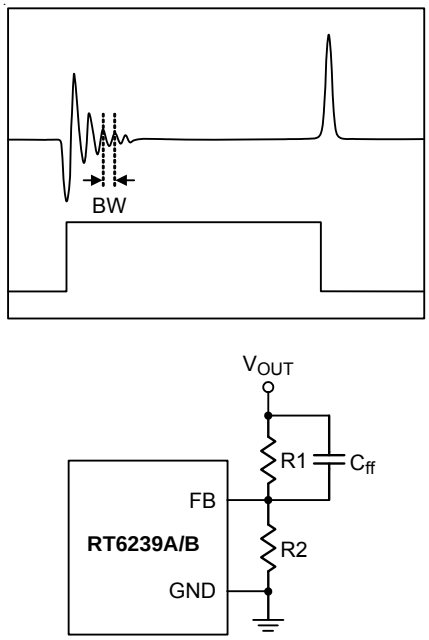


Figure 1. C_{ff} Capacitor Setting

- C_{ff} can be calculated base on below equation :

$$C_{ff} = \frac{1}{2 \times 3.1412 \times R1 \times BW \times 0.8}$$

Soft-Start (SS)

The RT6239A/B soft-start uses an external capacitor at SS to adjust the soft-start timing according to the following equation :

$$t\,(ms) = \frac{C_{SS}\,(nF) \times 0.7}{I_{SS}\,(\mu A)}$$

Following below equation to get the minimum capacitance range in order to avoid UV occur.

$$T = \frac{C_{OUT} \times V_{OUT} \times 0.6 \times 1.2}{(I_{LIM} - \text{Load Current}) \times 0.8}$$

$$C_{SS} \geq \frac{T \times 6\mu A}{V_{REF}}$$

Do not leave SS unconnected.

Enable Operation (EN)

For automatic start-up, the low-voltage EN pin must be connected to VIN with a 100kΩ resistor. EN can be externally pulled to VIN by adding a resistor-capacitor delay (R_{EN} and C_{EN} in Figure 2). Calculate the delay time using EN's internal threshold where switching operation begins (1.2V, typical).

An external MOSFET can be added to implement digital control of EN (Figure 3). In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input under voltage lockout threshold (Figure 4).

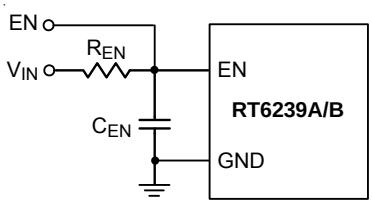


Figure 2. External Timing Control

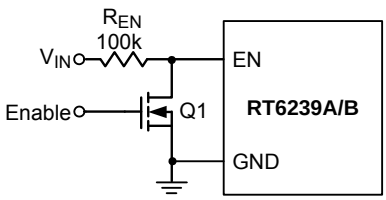


Figure 3. Digital Enable Control Circuit

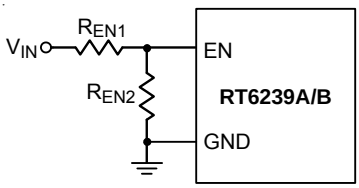


Figure 4. Resistor Divider for Lockout Threshold Setting

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

V_{OUT} = 0.7 x (1 + R1 / R2)

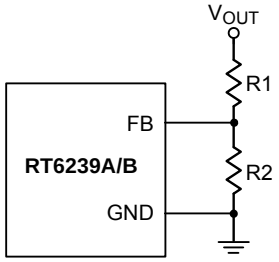


Figure 5. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \times (V_{OUT} - 0.7)}{0.7}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

External BOOT Bootstrap Diode

When the input voltage is lower than 5.5V it is recommended to add an external bootstrap diode between VIN (or VINR) and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

External BOOT Capacitor Series Resistance

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{SW} rises rapidly. During switch turn-off, SW is discharged relatively slowly by the inductor current during the dead time between high-side and low-side switch on-times. In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<47Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and V_{SW}'s rise. To remove the resistor from the capacitor charging path (avoiding poor enhancement due to undercharging the BOOT capacitor), use the external diode shown in figure 6 to charge the BOOT capacitor and place the resistance between BOOT and the capacitor/diode connection.

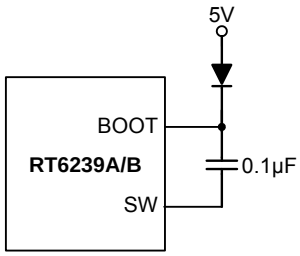


Figure 6. External Bootstrap Diode

PVCC Capacitor Selection

Decouple PVCC to GND with a 1µF ceramic capacitor. High grade dielectric (X7R, or X5R) ceramic capacitors are recommended for their stable temperature and bias voltage characteristics.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For UQFN-14L 2x3 (FC) package, the thermal resistance, θ_{JA}, is 47.5°C/W on a standard four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (47.5°C/W) = 2.1W for UQFN-14L 2x3 (FC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

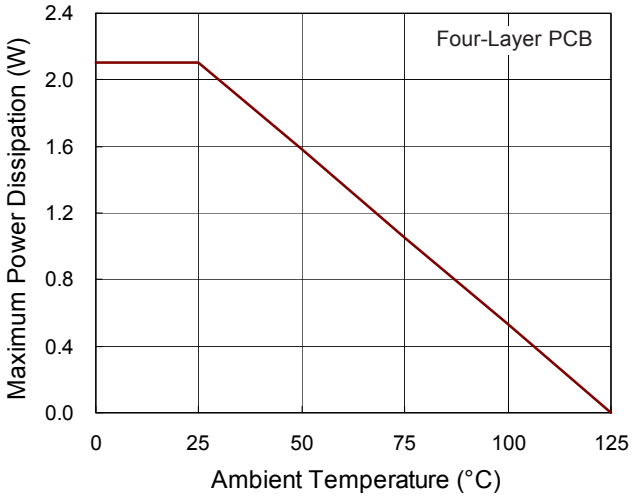


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Consideration

- Follow the PCB layout guidelines for optimal performance of the device.
- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to VIN and VIN pins.
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the device.
- Connect all analog grounds to common node and then connect the common node to the power ground behind the output capacitors.
- An example of PCB layout guide is shown in Figure 8 and Figure 9 for reference.

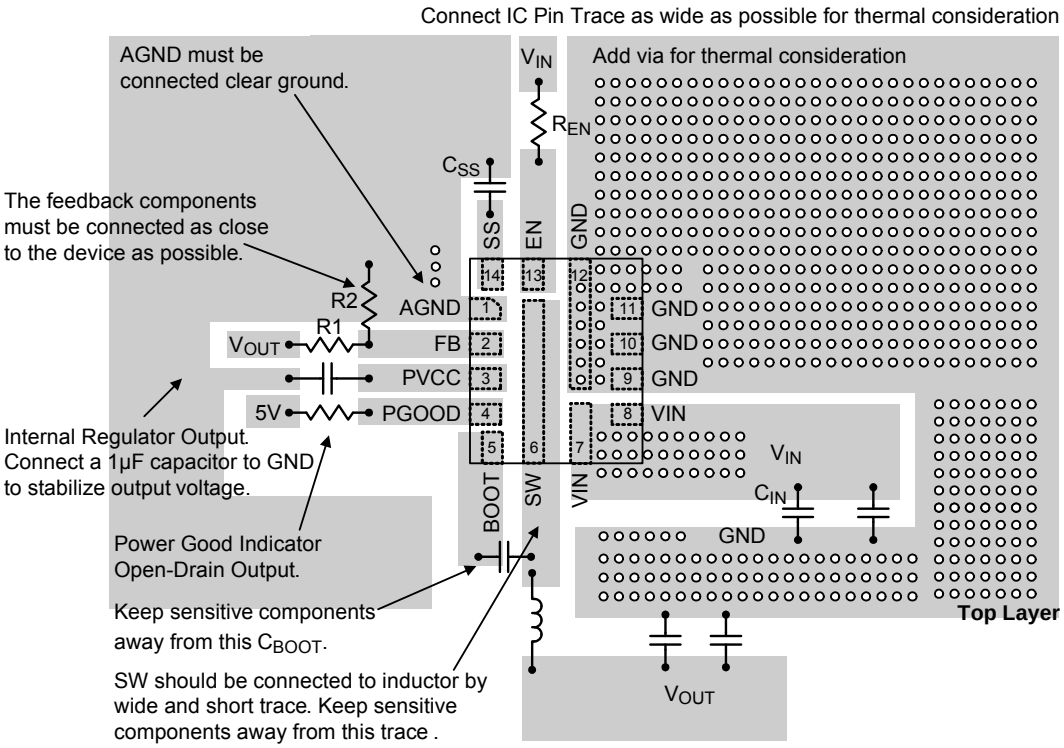


Figure 8. PCB Layout Guide (Top Layer)

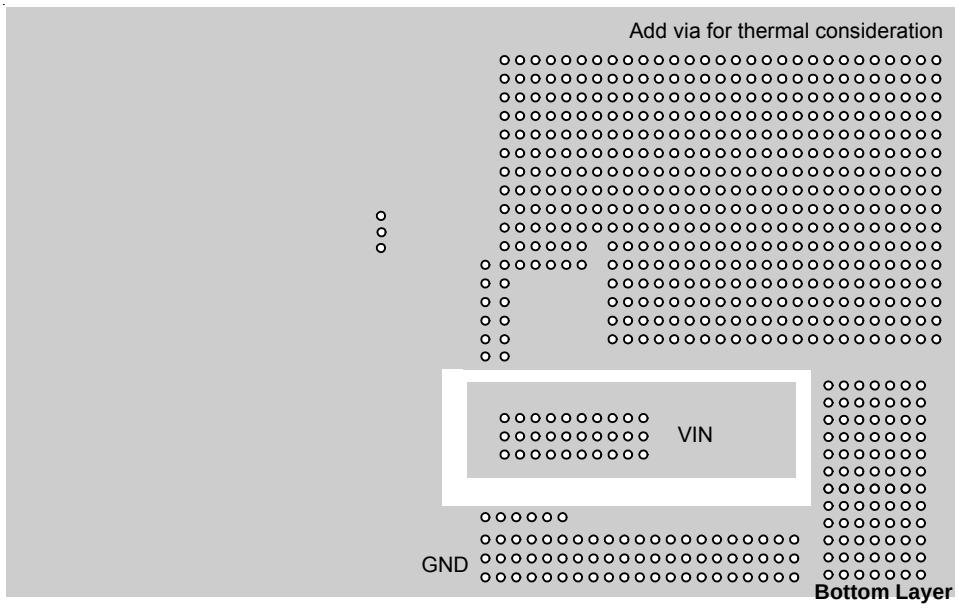


Figure 9. PCB Layout Guide (Bottom Layer)

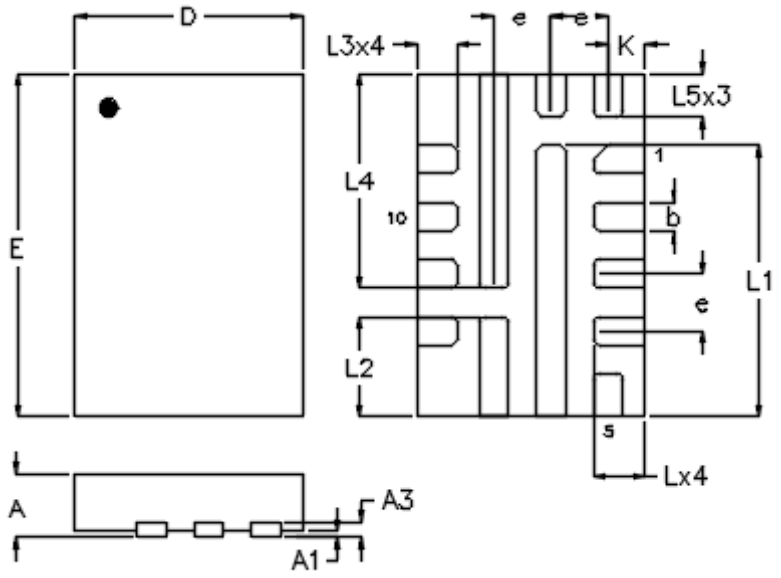
Suggested Inductors for Typical Application Circuit

Component Supplier	Part No.	Inductance (μH)	DCR (mΩ)	Dimensions (mm)
WE	7443320100	1	1.85	12.1 x 11.4 x 9.5
WE	744325120	1.2	1.8	10.2 x 10.2 x 4.7
WE	7443551200	2	2.6	12.8 x 12.8 x 6.2

Recommended component selection for Typical Application.

Component Supplier	Part No.	Capacitance (μF)	Case Size
MURATA	GRM31CR61E106K	10	1206
TDK	C3225X5R1E106K	10	1206
TAIYO YUDEN	TMK316BJ106ML	10	1206
MURATA	GRM31CR60J476M	47	1206
TDK	C3225X5R0J476M	47	1210
TAIYO YUDEN	EMK325BJ476MM	47	1210
MURATA	GRM32ER71C226M	22	1210
TDK	C3225X5R1C226M	22	1210

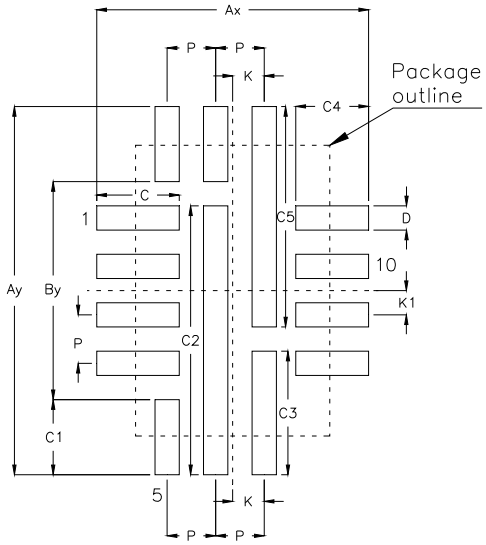
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.152	0.004	0.006
b	0.200	0.300	0.008	0.012
D	1.900	2.100	0.075	0.083
E	2.900	3.100	0.114	0.122
e	0.500		0.020	
K	0.325		0.013	
L	0.400	0.500	0.016	0.020
L1	2.325	2.425	0.092	0.095
L2	0.825	0.925	0.032	0.036
L3	0.300	0.400	0.012	0.016
L4	1.825	1.925	0.072	0.076
L5	0.325	0.425	0.013	0.017

U-Type 14L QFN 2x3 (FC) Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)													Tolerance
		P	Ax	Ay	By	C*4	C1*3	C2	C3	C4*4	C5	D*14	K	K1	
UQFN2*3-14(FC)	14	0.500	2.800	3.800	2.250	0.850	0.775	2.775	1.275	0.750	2.275	0.250	0.325	0.250	±0.050

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单击下面可查看定价，库存，交付和生命周期等信息

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