

## 3A, 18V, 700kHz ACOT™ Synchronous Step-Down Converter

### General Description

The RT7277 is a synchronous step-down DC/DC converter with Advanced Constant On-Time (ACOT™) mode control. It achieves high power density to deliver up to 3A output current from a 4.5V to 18V input supply. The proprietary ACOT™ mode offers an optimal transient response over a wide range of loads and all kinds of ceramic capacitors, which allows the device to adopt very low ESR output capacitors for ensuring performance stabilization. In addition, RT7277 keeps an excellent constant switching frequency under line and load variation and the integrated synchronous power switches with the ACOT™ mode operation provides high efficiency in whole output current load range. Cycle-by-cycle current limit provides an accurate protection by a valley detection of low side MOSFET and external soft-start setting eliminates input current surge during startup. Protection functions also include output under voltage protection, output over voltage protection, and thermal shutdown.

### Marking Information

RT7277 GSPYMDNN •
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RT7277GSP : Product Number  
 YMDNN : Date Code

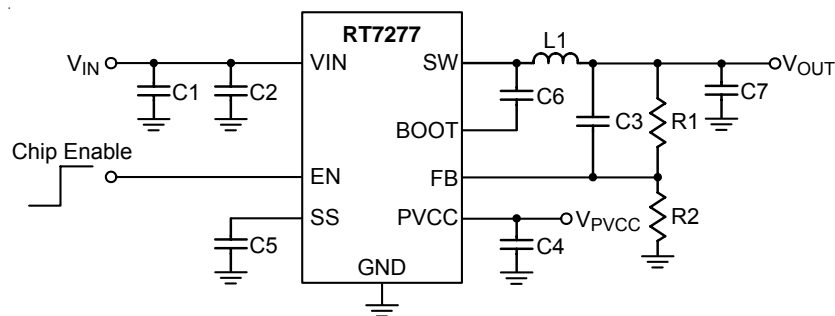
### Features

- ACOT™ Mode Enables Fast Transient Response
- 4.5V to 18V Input Voltage Range
- 3A Output Current
- 60mΩ Internal Low Side N-MOSFET
- Advanced Constant On-Time Control
- Support All Ceramic Capacitors
- Up to 95% Efficiency
- 700kHz Switching Frequency
- Adjustable Output Voltage from 0.765V to 8V
- Adjustable Soft-Start
- Cycle-by-Cycle Current Limit
- Input Under Voltage Lockout
- Thermal Shutdown
- RoHS Compliant and Halogen Free

### Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

### Simplified Application Circuit



## Ordering Information

RT7277□□

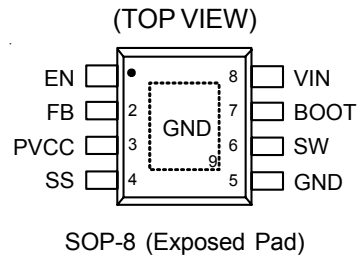
- Package Type  
SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System  
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

## Pin Configurations



## Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
2	FB	Feedback Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback threshold voltage is 0.765V typically.
3	PVCC	Internal Regulator Output. Connect a 1μF capacitor to GND to stabilize output voltage.
4	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 3.9nF capacitor sets the soft-start period of V <sub>OUT</sub> to 2.6ms.
5, 9 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
6	SW	Switch Node. Connect this pin to an external L-C filter.
7	BOOT	Bootstrap Supply for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pins.
8	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitor.



**Absolute Maximum Ratings** (Note 1)

- Supply Voltage,  $V_{IN}$  ----- -0.3V to 21V
- Switch Voltage,  $SW$  ----- -0.8V to ( $V_{IN} + 0.3V$ )
- <10ns ----- -5V to 25V
- BOOT to SW,  $PVCC$  ----- -0.3V to 6V
- Other Pins Voltage ----- -0.3V to 21V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ C$
- SOP-8 (Exposed Pad) ----- 2.041W
- Package Thermal Resistance (Note 2)
- SOP-8 (Exposed Pad),  $\theta_{JA}$  ----- 49°C/W
- SOP-8 (Exposed Pad),  $\theta_{JC}$  ----- 15°C/W
- Junction Temperature Range ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
- HBM (Human Body Model) ----- 2kV

**Recommended Operating Conditions** (Note 4)

- Supply Voltage,  $V_{IN}$  ----- 4.5V to 18V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

**Electrical Characteristics**

( $V_{IN} = 12V$ ,  $T_A = 25^\circ C$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Supply Current</b>						
Shutdown Current	$I_{SHDN}$	$V_{EN} = 0V$	--	1.5	10	$\mu A$
Quiescent Current	$I_Q$	$V_{EN} = 3V$ , $V_{FB} = 1V$	--	0.7	--	mA
<b>Logic Threshold</b>						
EN Voltage	Logic-High		2	--	18	V
	Logic-Low		--	--	0.4	
<b><math>V_{FB}</math> Voltage and Discharge Resistance</b>						
Feedback Threshold Voltage	$V_{FB}$	$4.5V \leq V_{IN} \leq 18V$	0.757	0.765	0.773	V
Feedback Input Current	$I_{FB}$	$V_{FB} = 0.8V$	-0.1	0	0.1	$\mu A$
<b><math>V_{PVCC}</math> Output</b>						
$V_{PVCC}$ Output Voltage	$V_{PVCC}$	$6V \leq V_{IN} \leq 18V$ , $0 < I_{PVCC} < 5mA$	4.7	5.1	5.5	V
Line Regulation		$6V \leq V_{IN} \leq 18V$ , $I_{PVCC} = 5mA$	--	--	20	mV
Load Regulation		$0 < I_{PVCC} < 5mA$	--	--	100	mV
Output Current	$I_{PVCC}$	$V_{IN} = 6V$ , $V_{PVCC} = 4V$	--	110	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>R<sub>DS(ON)</sub></b>						
Switch On Resistance	High Side	R <sub>DS(ON)_H</sub>	--	90	--	mΩ
	Low Side	R <sub>DS(ON)_L</sub>	--	60	--	
<b>Current Limit</b>						
Current Limit	I <sub>LIM</sub>		3.5	4.1	5.7	A
<b>Thermal Shutdown</b>						
Thermal Shutdown Threshold	T <sub>SD</sub>		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT <sub>SD</sub>		--	20	--	°C
<b>On-Time Timer Control</b>						
On-Time	t <sub>ON</sub>	V <sub>IN</sub> = 12V, V <sub>OUT</sub> = 1.05V	--	145	--	ns
Minimum On-Time	t <sub>ON(MIN)</sub>		--	60	--	ns
Minimum Off-Time	t <sub>OFF(MIN)</sub>		--	230	--	ns
<b>Soft-Start</b>						
SS Charge Current		V <sub>SS</sub> = 0V	1.4	2	2.6	μA
SS Discharge Current		V <sub>SS</sub> = 0.5V	0.05	0.1	--	mA
<b>UVLO</b>						
UVLO Threshold		V <sub>IN</sub> Rising to Wake up V <sub>PVCC</sub>	3.55	3.85	4.15	V
Hysteresis			--	0.3	--	

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** θ<sub>JA</sub> is measured at T<sub>A</sub> = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ<sub>JC</sub> is measured at the exposed pad of the package. The PCB copper area of exposed pad is 70mm<sup>2</sup>.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

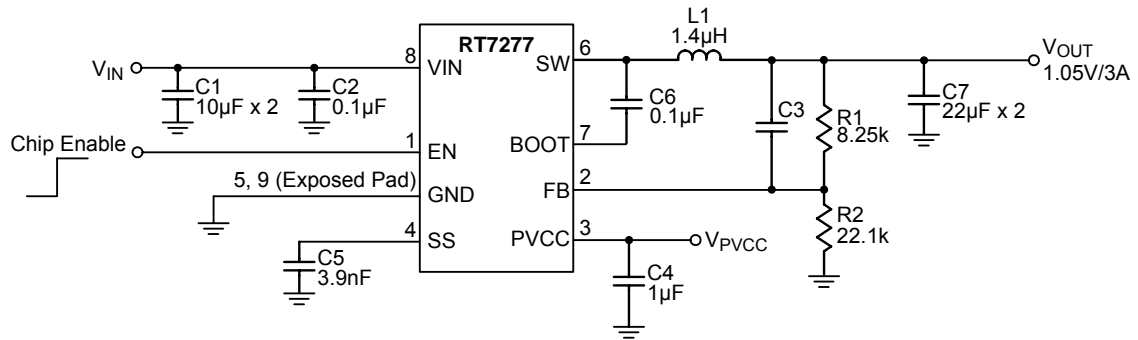
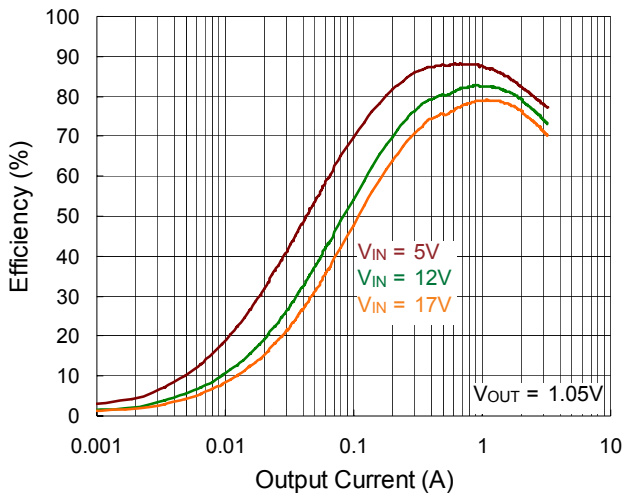


Table 1. Suggested Component Values

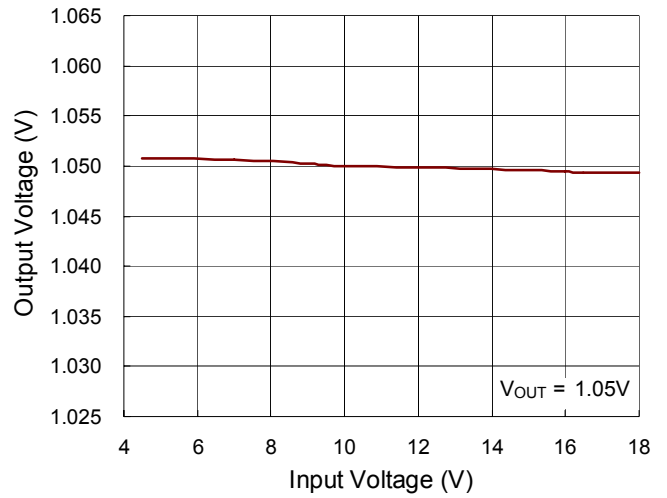
V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)	C3 (pF)	L1 (µH)	C7 (µF)
1	6.81	22.1	--	1.4	22 to 68
1.05	8.25	22.1	--	1.4	22 to 68
1.2	12.7	22.1	--	1.4	22 to 68
1.8	30.1	22.1	5 to 22	2	22 to 68
2.5	49.9	22.1	5 to 22	2	22 to 68
3.3	73.2	22.1	5 to 22	2	22 to 68
5	124	22.1	5 to 22	3.3	22 to 68
7	180	22.1	5 to 22	3.3	22 to 68

**Typical Operating Characteristics**

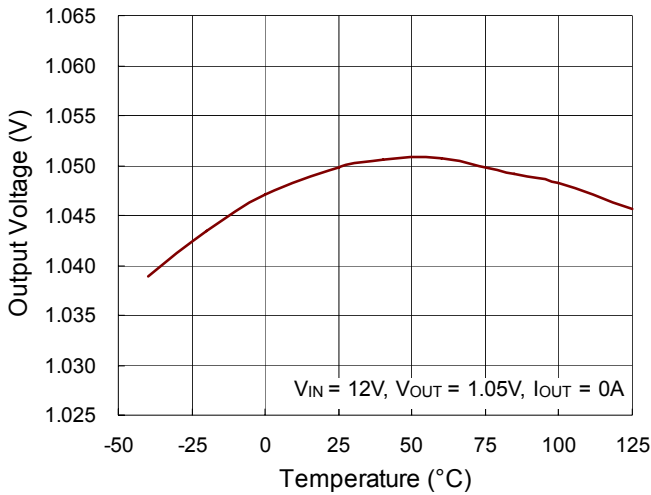
**Efficiency vs. Output Current**



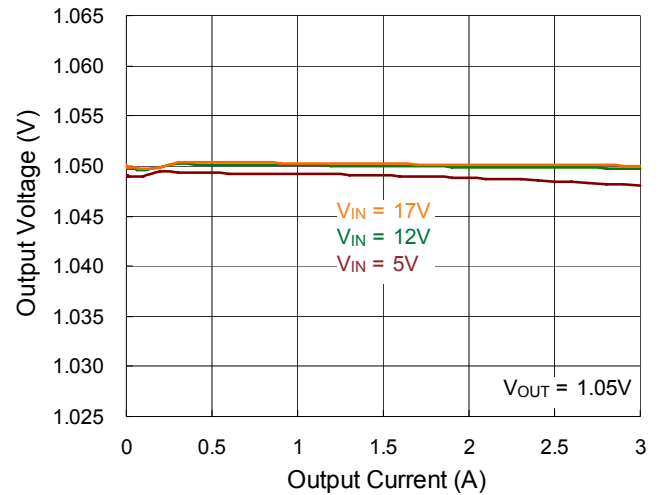
**Output Voltage vs. Input Voltage**



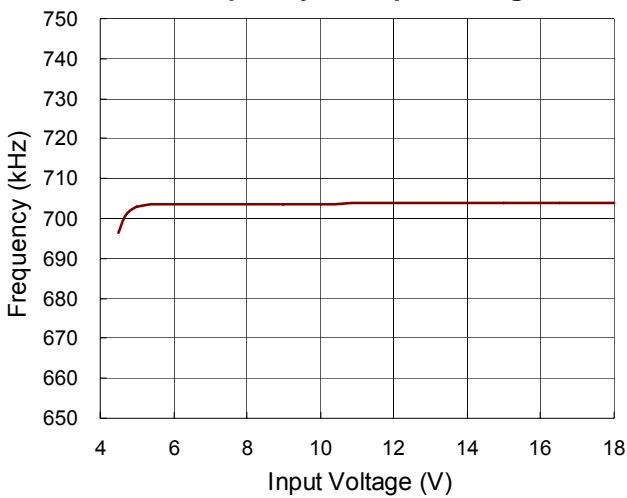
**Output Voltage vs. Temperature**



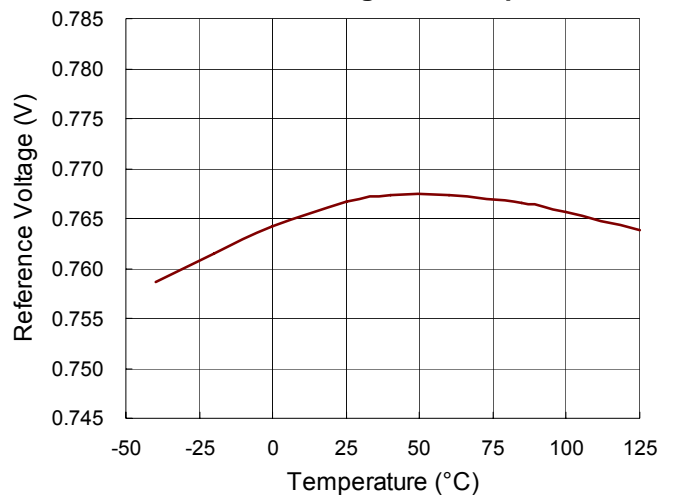
**Output Voltage vs. Output Current**



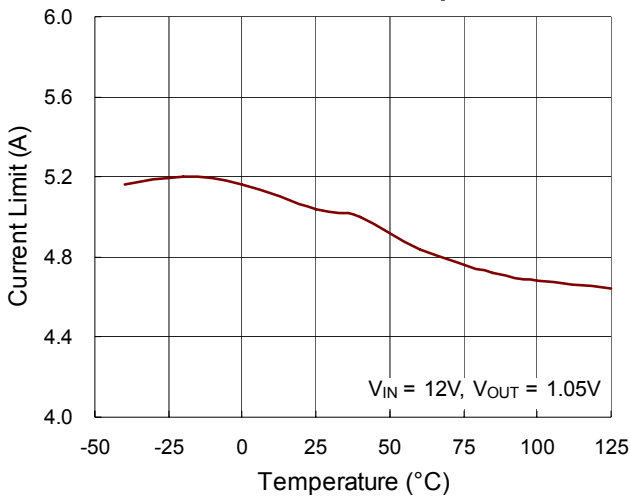
**Frequency vs. Input Voltage**



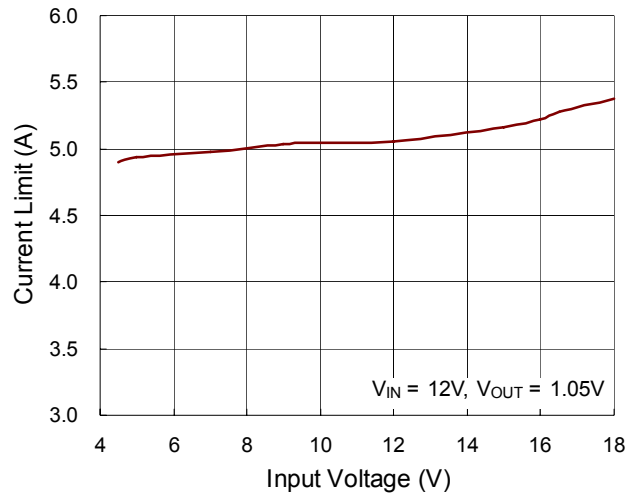
**Reference Voltage vs. Temperature**



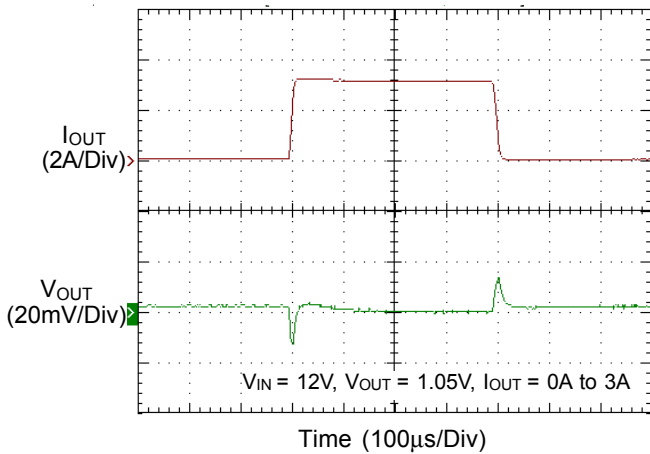
Current Limit vs. Temperature



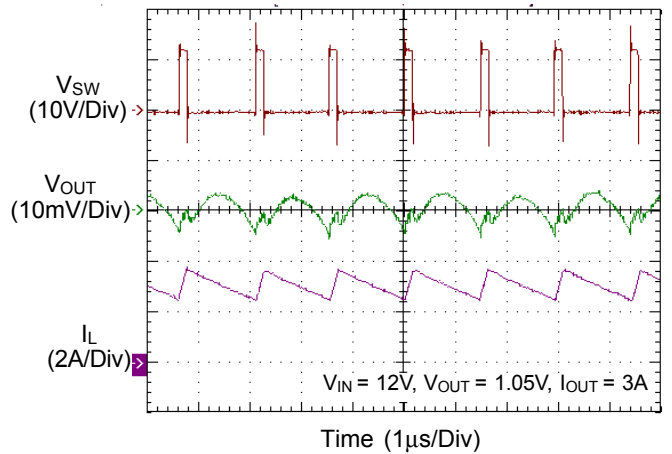
Current Limit vs. Input Voltage



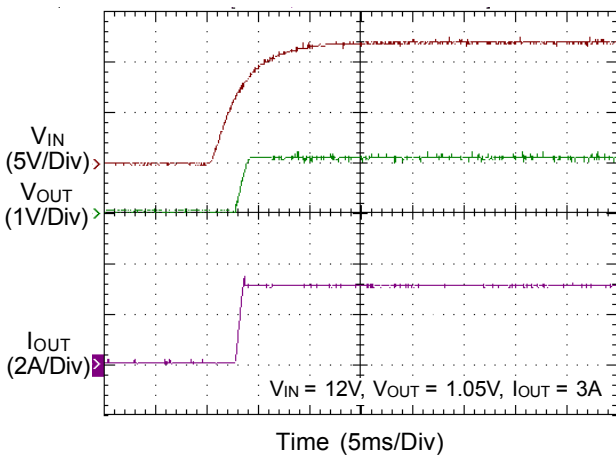
Load Transient Response



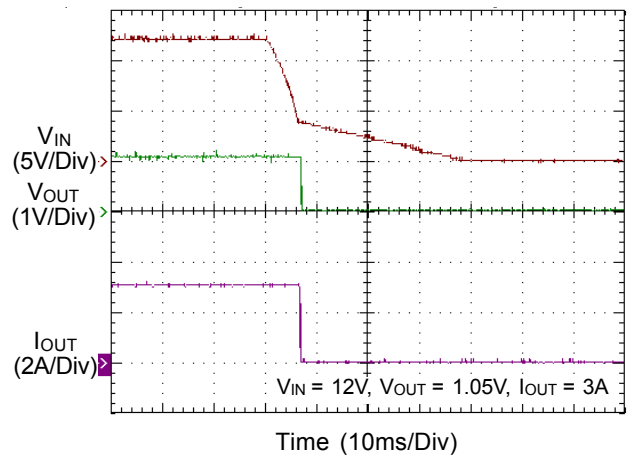
Switching



Power On from VIN

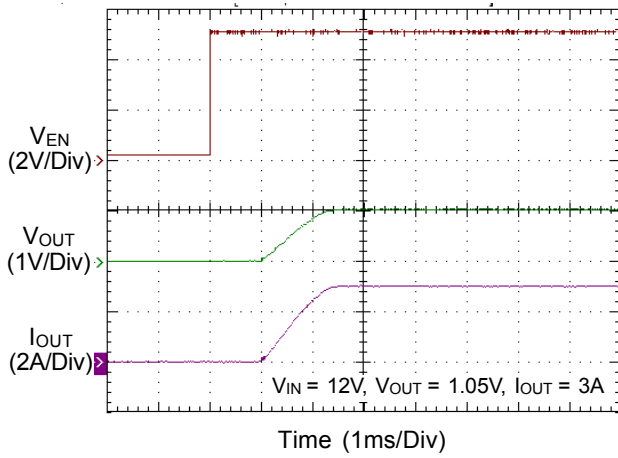


Power Off from VIN

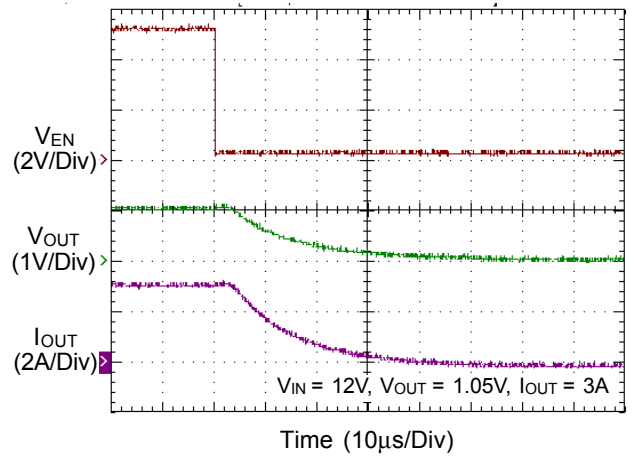




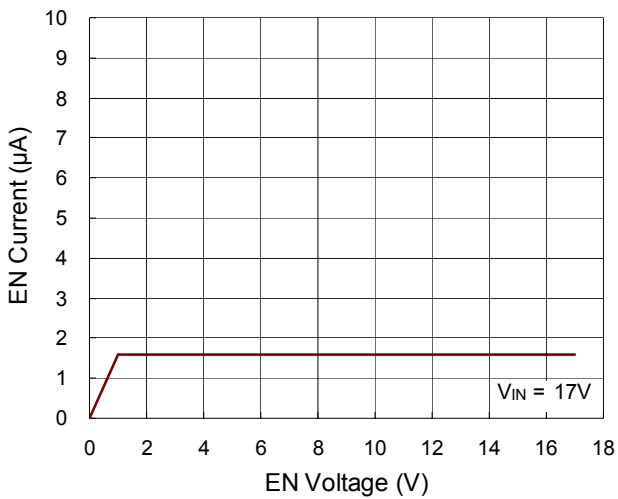
**Power On from EN**



**Power Off from EN**



**EN Current vs. EN Voltage**



### Application Information

The RT7277 is a synchronous high voltage Buck converter that can support the input voltage range from 4.5V to 18V and the output current up to 3A. It adopts ACOT™ mode control to provide a very fast transient response with few external compensation components.

#### PWM Operation

It is suitable for low external component count configuration with appropriate amount of Equivalent Series Resistance (ESR) capacitors at the output. The output ripple valley voltage is monitored at a feedback point voltage. The synchronous high side MOSFET is turned on at the beginning of each cycle. After the internal on-time timer expires, the MOSFET is turned off. The pulse width of this on-time is determined by the converter's input and output voltages to keep the frequency fairly constant over the entire input voltage range.

#### Advanced Constant On-Time Control

The RT7277 has a unique circuit which sets the on-time by monitoring the input voltage and SW signal. The circuit ensures the switching frequency operating at 700kHz over input voltage range and loading range.

#### Soft-Start

The RT7277 contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing can be programmed by the external capacitor between SS pin and GND. The chip provides a 2μA charge current for the external capacitor. If a 3.9nF capacitor is used, the soft-start will be 2.6ms (typ.). The available capacitance range is from 2.7nF to 220nF.

$$t_{SS} \text{ (ms)} = \frac{C_5 \text{ (nF)} \times 1.365}{I_{SS} \text{ (}\mu\text{A)}}$$

#### Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the RT7277 quiescent current drops to lower than 10μA. Driving the EN pin high (>2V, <18V) will turn on the

device again. For external timing control, the EN pin can also be externally pulled high by adding a R<sub>EN</sub> resistor and C<sub>EN</sub> capacitor from the V<sub>IN</sub> pin (see Figure 1).

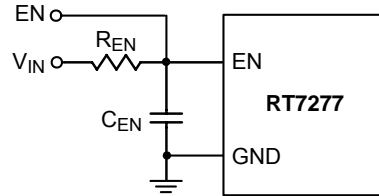


Figure 1. External Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2V is available, as shown in Figure 2. In this case, a 100kΩ pull-up resistor, R<sub>EN</sub>, is connected between V<sub>IN</sub> and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

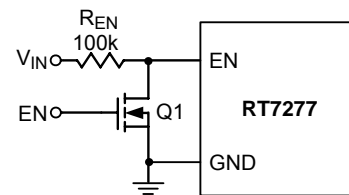


Figure 2. Digital Enable Control Circuit

To prevent enabling circuit when V<sub>IN</sub> is smaller than the V<sub>OUT</sub> target value, a resistive voltage divider can be placed between the input voltage and ground and connected to the EN pin to adjust IC lockout threshold, as shown in Figure 3. For example, if an 8V output voltage is regulated from a 12V input voltage, the resistor R<sub>EN2</sub> can be selected to set input lockout threshold larger than 8V.

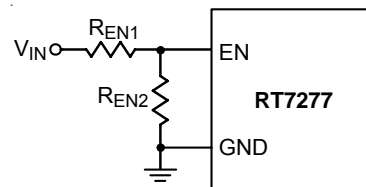


Figure 3. Resistor Divider for Lockout Threshold Setting

**Output Voltage Setting**

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 4.

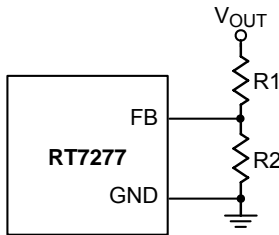


Figure 4. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation. It is recommended to use 1% tolerance or better divider resistors.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right)$$

**Under Voltage Lockout Protection**

The RT7277 has Under Voltage Lockout Protection (UVLO) that monitors the voltage of PVCC pin. When the V<sub>PVCC</sub> voltage is lower than UVLO threshold voltage, the RT7277 will be turned off in this state. This is non-latch protection.

**Over Temperature Protection**

The RT7277 equips an Over Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C the main converter will resume operation. To keep operating at maximum, the junction temperature should be prevented from rising above 150°C.

**Inductor Selection**

The inductor value and operating frequency determine the ripple current according to a specific input and an output voltage. The ripple current Δ<sub>I<sub>L</sub></sub> increases with higher V<sub>IN</sub> and decreases with higher inductance.

$$\Delta I_L = \left[ \frac{V_{OUT}}{f \times L} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large

inductor to achieve this goal. For the ripple current selection, the value of Δ<sub>I<sub>L</sub></sub> = 0.2(I<sub>MAX</sub>) will be a reasonable starting point. The largest ripple current occurs at the highest V<sub>IN</sub>. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[ \frac{V_{OUT}}{f \times \Delta I_L(MAX)} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

**Input and Output Capacitors Selection**

The input capacitance, C<sub>IN</sub>, is needed to filter the trapezoidal current at the source of the high side MOSFET. A low ESR input capacitor with larger ripple current rating should be used for the maximum RMS current. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V<sub>IN</sub> = 2V<sub>OUT</sub>, where I<sub>RMS</sub> = I<sub>OUT</sub> / 2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, two 10μF and 0.1μF low ESR ceramic capacitors are recommended.

The selection of C<sub>OUT</sub> is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C<sub>OUT</sub> selection to ensure that the control loop is stable. The output ripple, ΔV<sub>OUT</sub>, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since Δ<sub>I<sub>L</sub></sub> increases with input voltage. Multiple capacitors placed in parallel may need to meet the ESR and RMS current handling requirements.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and

output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input,  $V_{IN}$ . A sudden inrush of current through the long wires can potentially cause a voltage spike at  $V_{IN}$  large enough to damage the part.

### External Bootstrap Diode

Connect a 0.1 $\mu$ F low ESR ceramic capacitor between the BOOT and SW pins. This capacitor provides the gate driver voltage for the high side MOSFET. It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65%. The bootstrap diode can be a low cost one such as 1N4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT7277. Note that the external boot voltage must be lower than 5.5V

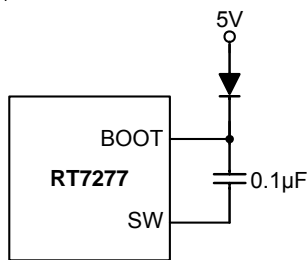


Figure 5. External Bootstrap Diode

### PVCC Capacitor Selection

Decouple with a 1 $\mu$ F ceramic capacitor. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.

### Over Current Protection

When the output shorts to ground, the inductor current decays very slowly during a single switching cycle. An over current detector is used to monitor inductor current to prevent current runaway. The over current detector monitors the voltage between SW and GND during the low side MOS turn-on state. This is cycle-by-cycle protection. The over current detector also supports temperature compensated.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance,  $\theta_{JA}$ , is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formulas :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (49^\circ\text{C/W}) = 2.041\text{W for SOP-8 (Exposed Pad) package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 6 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

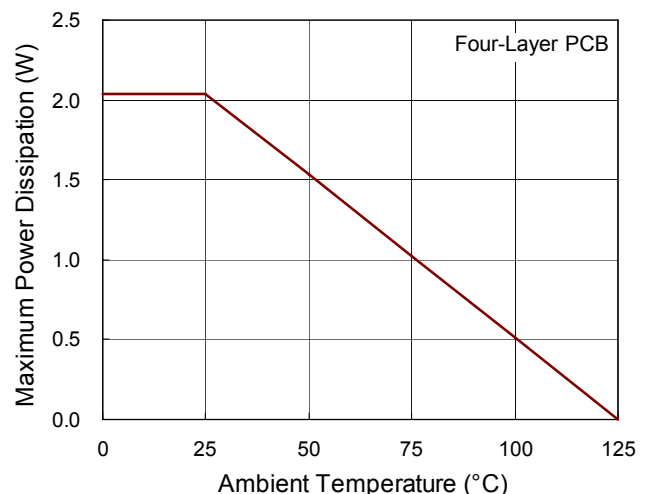


Figure 6. Derating Curve of Maximum Power Dissipation

**Layout Consideration**

Follow the PCB layout guidelines for optimal performance of the RT7277

- ▶ Keep the traces of the main current paths as short and wide as possible.
- ▶ Put the input capacitor as close as possible to the device pins (VIN and GND).

- ▶ SW node is with high frequency voltage swing and should be kept at small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pickup.
- ▶ Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT7277 feedback pin.
- ▶ The GND and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

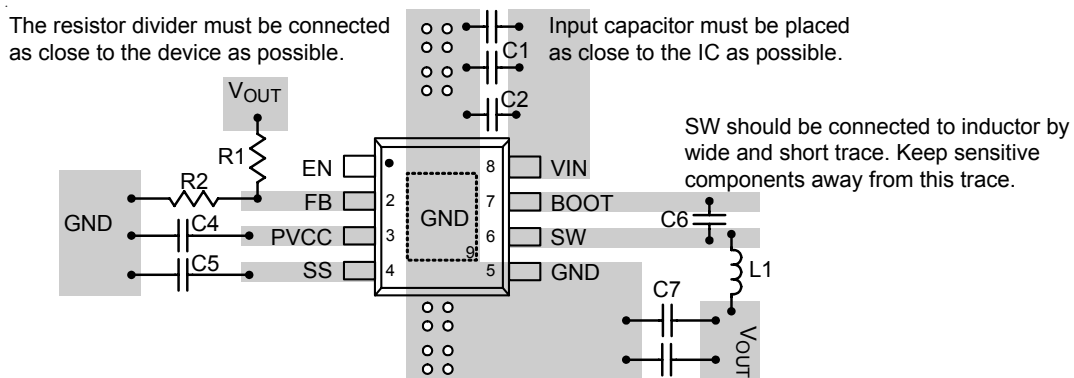
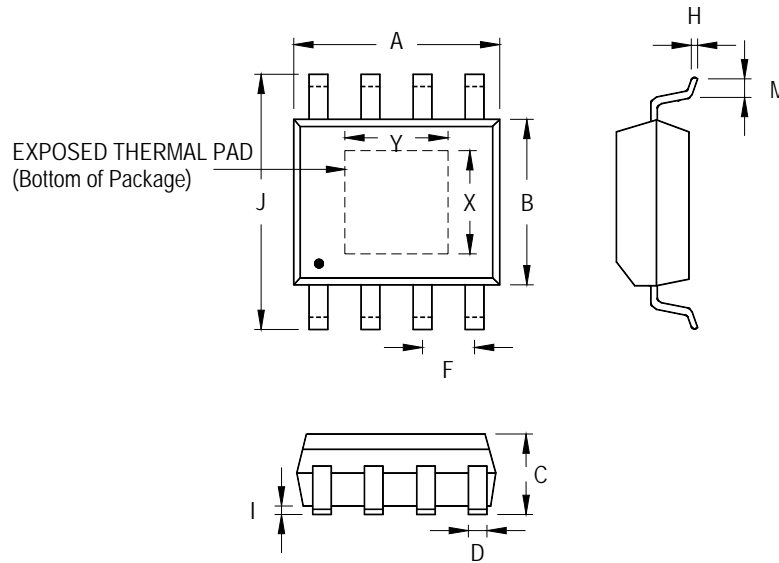


Figure 7. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	4.801	5.004	0.189	0.197	
B	3.810	4.000	0.150	0.157	
C	1.346	1.753	0.053	0.069	
D	0.330	0.510	0.013	0.020	
F	1.194	1.346	0.047	0.053	
H	0.170	0.254	0.007	0.010	
I	0.000	0.152	0.000	0.006	
J	5.791	6.200	0.228	0.244	
M	0.406	1.270	0.016	0.050	
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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