Power Management IC with Single Cell Li-Battery Switching Charger Integrated Power Path Controller

General Description

The RT5036 is a highly integrated smart power management IC which includes: switch-mode single cell Li-Ion/Li-Polymer battery charger, LDO, synchronize Buck regulator, Load Switch, and RTC-OSC for portable applications. The RT5036 also features USB On-The-Go (OTG) support.

The RT5036 optimizes the charging task by using a control algorithm to vary the charge rate via different modes, including pre-charge mode, fast charge mode, and constant voltage mode. The key charge parameters can be programmed via the I^2C interface. The RT5036 resumes the charge cycle whenever the battery voltage falls below an internal threshold and automatically enters sleep mode when the input power supply is removed.

Four integrated Synchronize Buck Regulators are designed to provide MAX 1.6/1.6/1.2/1.2A application with high efficiency.

Four integrated LDOs are designed to provide MAX 0.35/0.35/0.35/0.35A application.

Two Load Switches are integrated with load Ron. And a Real Time Clock (RTC) includes time counter and a 32768Hz oscillator for portable applications.

The RT5036 also provides rich protection functions : Over Current Protection, Under Voltage Protection, Over Voltage Protection, Over Temperature Protection, and Over Load Protection.

Ordering Information

RT5036□□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

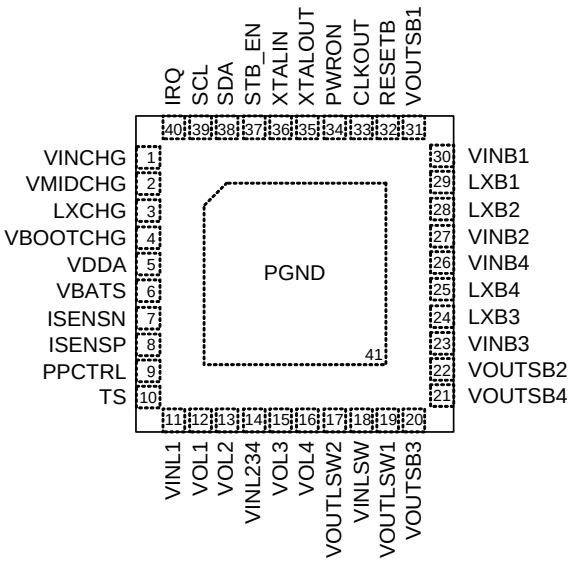
- **Battery Charger**
  - **High Accuracy Voltage/Current Regulation**
  - **Average Input Current Regulation(AICR) : 0.1/0.5/0.7/0.9/1/1.5/2A**
  - **Minimum Input Voltage Regulation(MIVR) : 4.2V to 4.8V**
  - **Charge Voltage Regulation: 3.65V to 4.4V**
  - **Charge Current Regulation: 0.5A to 2A**
  - **Synchronous 0.75/1.5MHz Fixed Frequency PWM Controller With Up To 95% Duty Cycle**
  - **Reverse Leakage Protection To Prevent Battery Drainage**
  - **Thermal Regulation**
  - **IRQ Output For Communication With I^2C**
  - **Battery Temperature Detection**
  - **Reverse Boost to Support OTG 1A**
- **4 LDOs**
  - **MAX Output Current 0.35/0.35/0.35/0.35A**
  - **I^2C Programmable Output Level**
- **4 LV Buck Regulators**
  - **MAX Output Current 1.6/1.6/1.2/1.2A**
  - **I^2C Programmable Output Level**
  - **No Schottky Barrier Diode Required**
  - **1.5M/3MHz Fixed Frequency Operation**
  - **Auto Discharge Function**
- **RTC Timer and Oscillator**
- **2 Load Switches**

Applications

- Cellular Telephones
- Personal Information Appliances
- Tablet PC, Power Bank
- Portable Instruments

Pin Configurations

(TOP VIEW)



WQFN-40L 5x5

Marking Information

RT5036GQW : Product Number

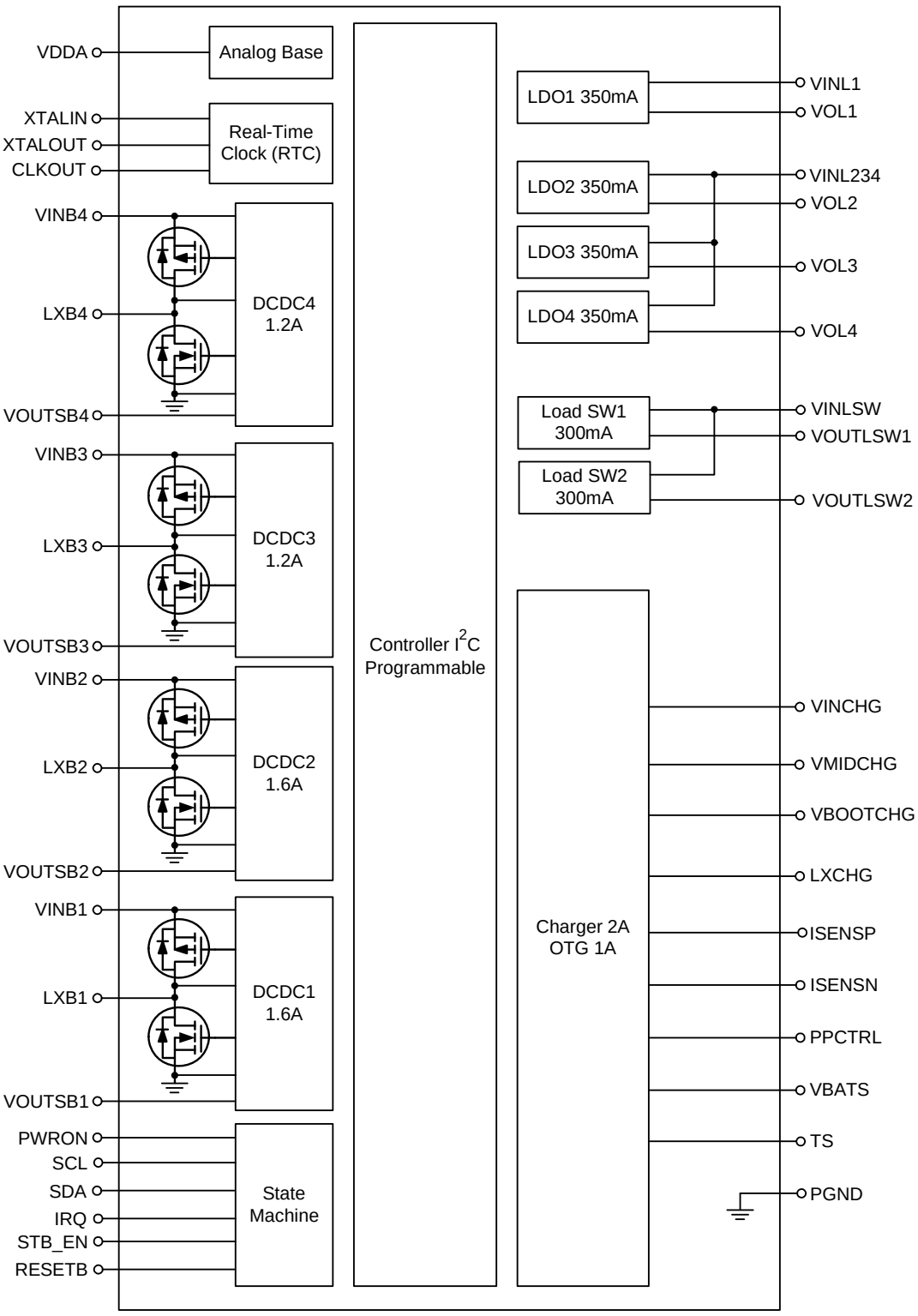
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VINCHG	Charger Input Voltage For Adaptor/USB Power Source.
2	VMIDCHG	Connection Point Between Reverse Blocking and High Side MOSFET.
3	LXCHG	Internal Switch Node To Output Inductor Connection of Switching Charger
4	VBOOTCHG	Bootstrap Power Node For Switching Charger
5	VDDA	Internal Power For Analog Blocks, Put 1μF To GND.
6	VBATS	Battery Voltage Regulation Node for Charger.
7	ISENSN	Charging Current Sensing Negative Node.
8	ISENSP	Charging Current Sensing Positive Node
9	PPCTRL	External Power Path Control. Used to control external power P-MOSFET to achieve power path operation.
10	TS	Battery Temperature Detection.
11	VINL1	Input Power for LDO1.
12	VOL1	Output Voltage Regulation Node for LDO1.
14	VINL234	Input Power for LDO2, LDO3, LDO 4.
13	VOL2	Output Voltage Regulation Node for LDO2.
15	VOL3	Output Voltage Regulation Node for LDO3.
16	VOL4	Output Voltage Regulation Node for LDO4.
17	VOUTLSW2	Output Pin for Load Switch 2.
18	VINLSW	Input Pin for Load Switches GOOD.

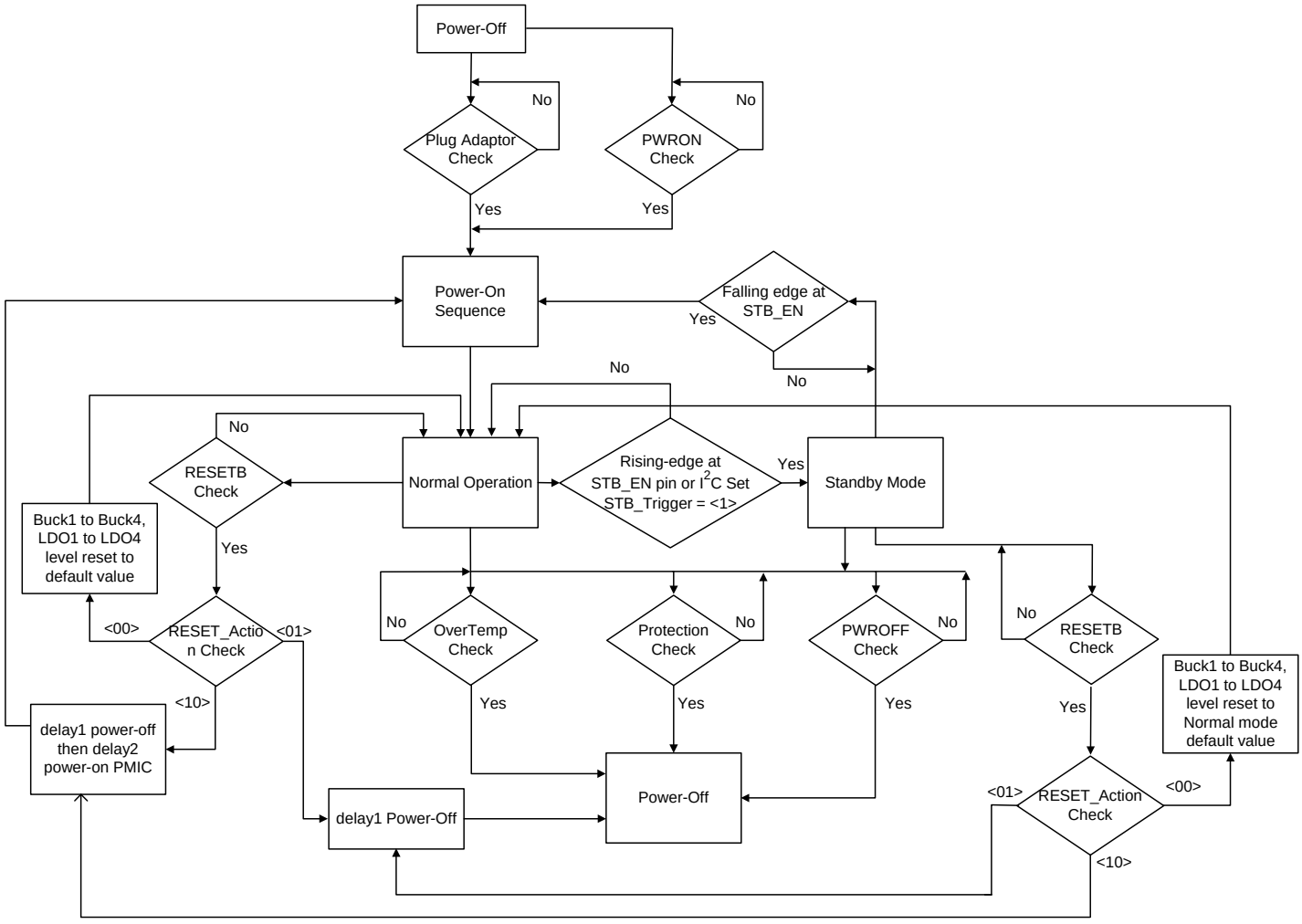
Pin No.	Pin Name	Pin Function
19	VOUTLSW1	Output Pin for Load Switch 1.
20	VOUTSB3	Output Voltage Regulation Node for Buck3.
21	VOUTSB4	Output Voltage Regulation Node for Buck4.
22	VOUTSB2	Output Voltage Regulation Node for Buck2.
23	VINB3	Input Power for Buck3.
24	LXB3	Internal Switch Node to Output Inductor Connection for Buck3.
25	LXB4	Internal Switch Node to Output Inductor Connection for Buck4.
26	VINB4	Input Power for Buck4.
27	VINB2	Input Power for Buck2.
28	LXB2	Internal Switch Node to Output Inductor Connection for Buck2.
29	LXB1	Internal Switch Node to Output Inductor Connection for Buck1.
30	VINB1	Input Power for Buck1.
31	VOUTSB1	Output Voltage Regulation Node for Buck1.
32	RESETB	Power-On Reset Output and Reset Key Input. Open drain, Connect A Pull-Up Resister. The pin is high impedance after RT5036 booting completely, otherwise, the pin is short to GND. Low pulse to triggers soft reset event.
33	CLKOUT	RTC 32768Hz Clock Output. Open drain.
34	PWRON	Power On Key Input. Low pulse to triggers power-on event.
35	XTALOUT	Crystal Output. This pin's parasitic capacitance should be kept as low as possible. Noise interference should also be avoided.
36	XTALIN	Crystal Input. This pin's parasitic capacitance should be kept as low as possible. Noise interference should also be avoided.
37	STB_EN	Standby Mode control pin. From low to high will trigger standby mode and from high to low will leave standby mode.
38	SDA	Data Input For I^2C. Open Drain, Connect A Pull-Up Resister.
39	SCL	Clock Input For I^2C. Open Drain, Connect A Pull-Up Resister
40	IRQ	IRQ Output Node. Open drain.
41 (Exposed Pad)	PGND	The exposed pad must be soldered to a large PCB and connected to PGND for maximum thermal dissipation and current flow.

Function Block Diagram



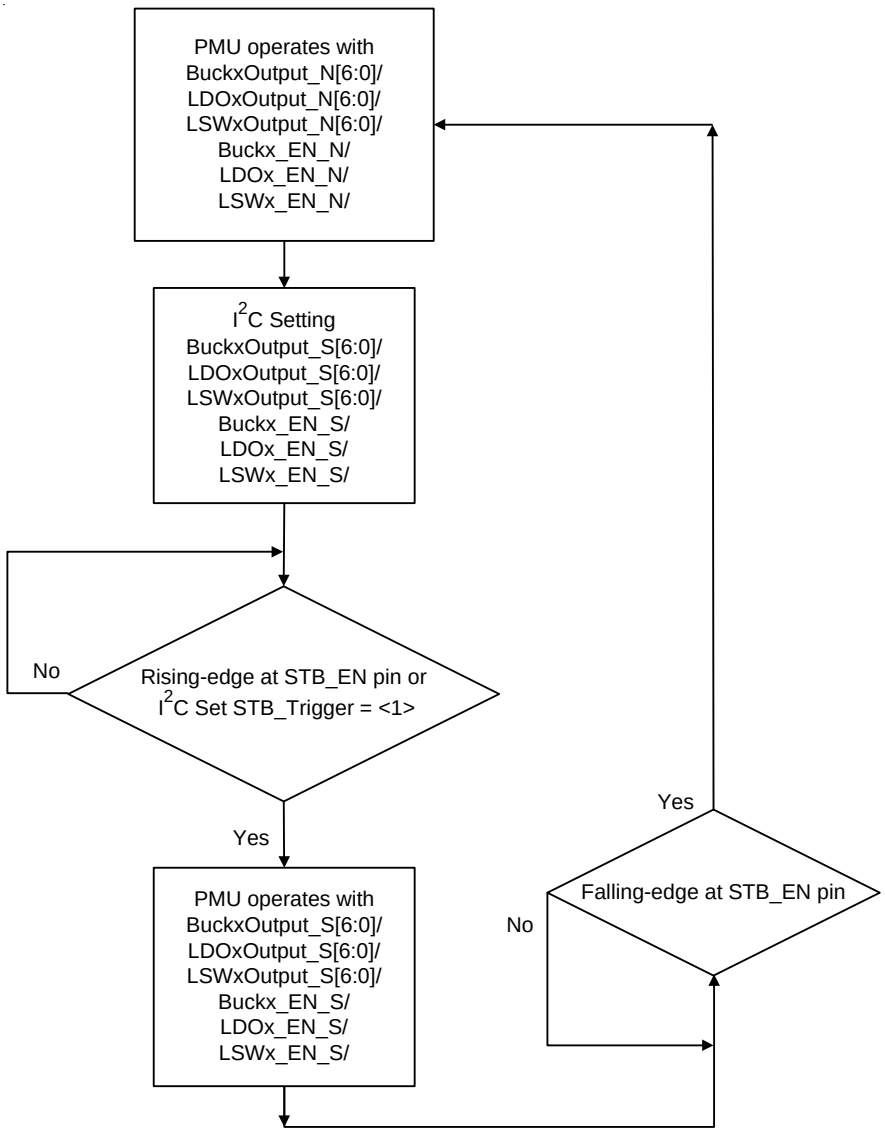
Flow Chart

Power Channel Flow Chart

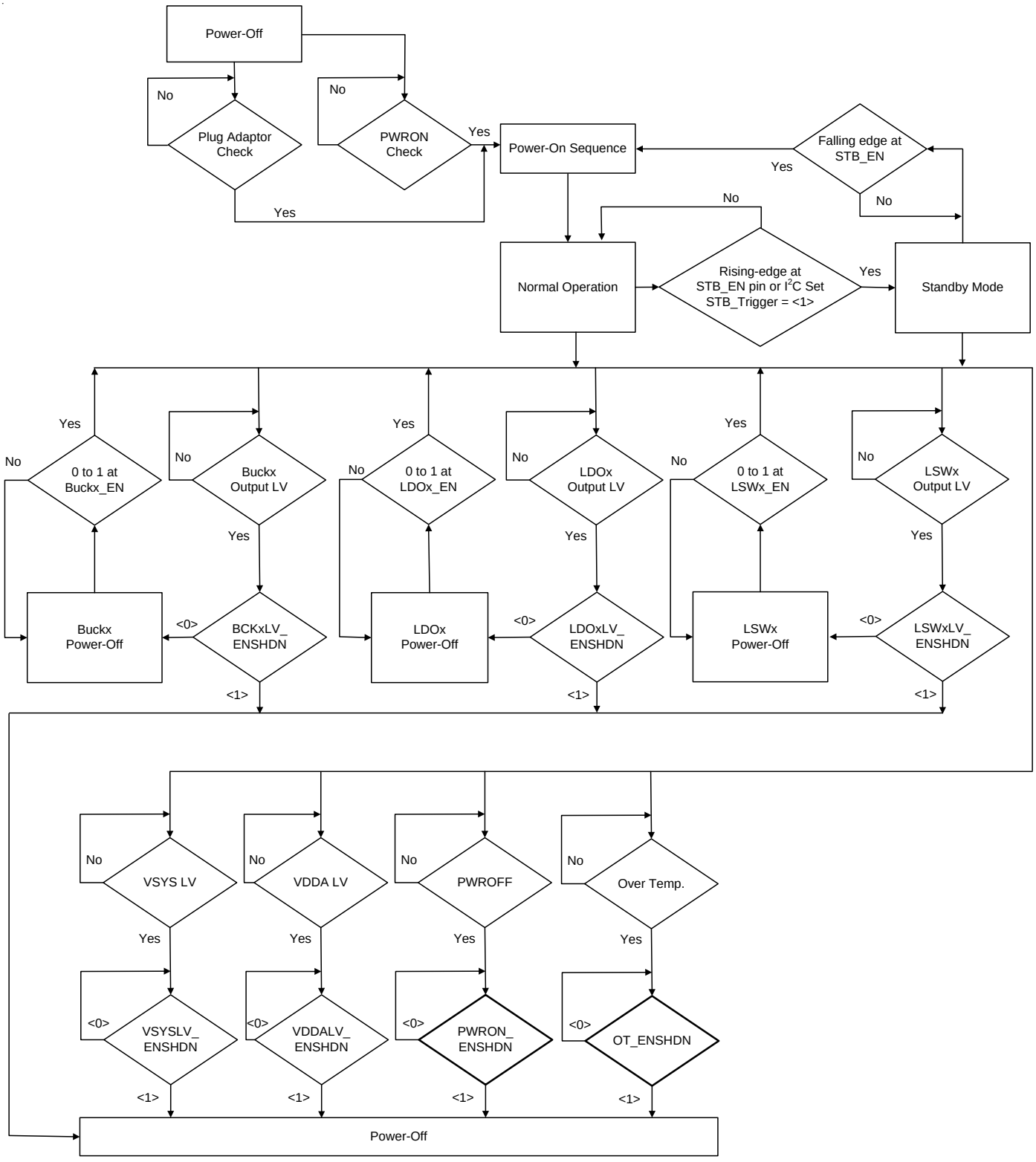


Note : RESETB Check : From "LOW" to "HIGH" rising input into RESETB pin with 100ms debouncing time

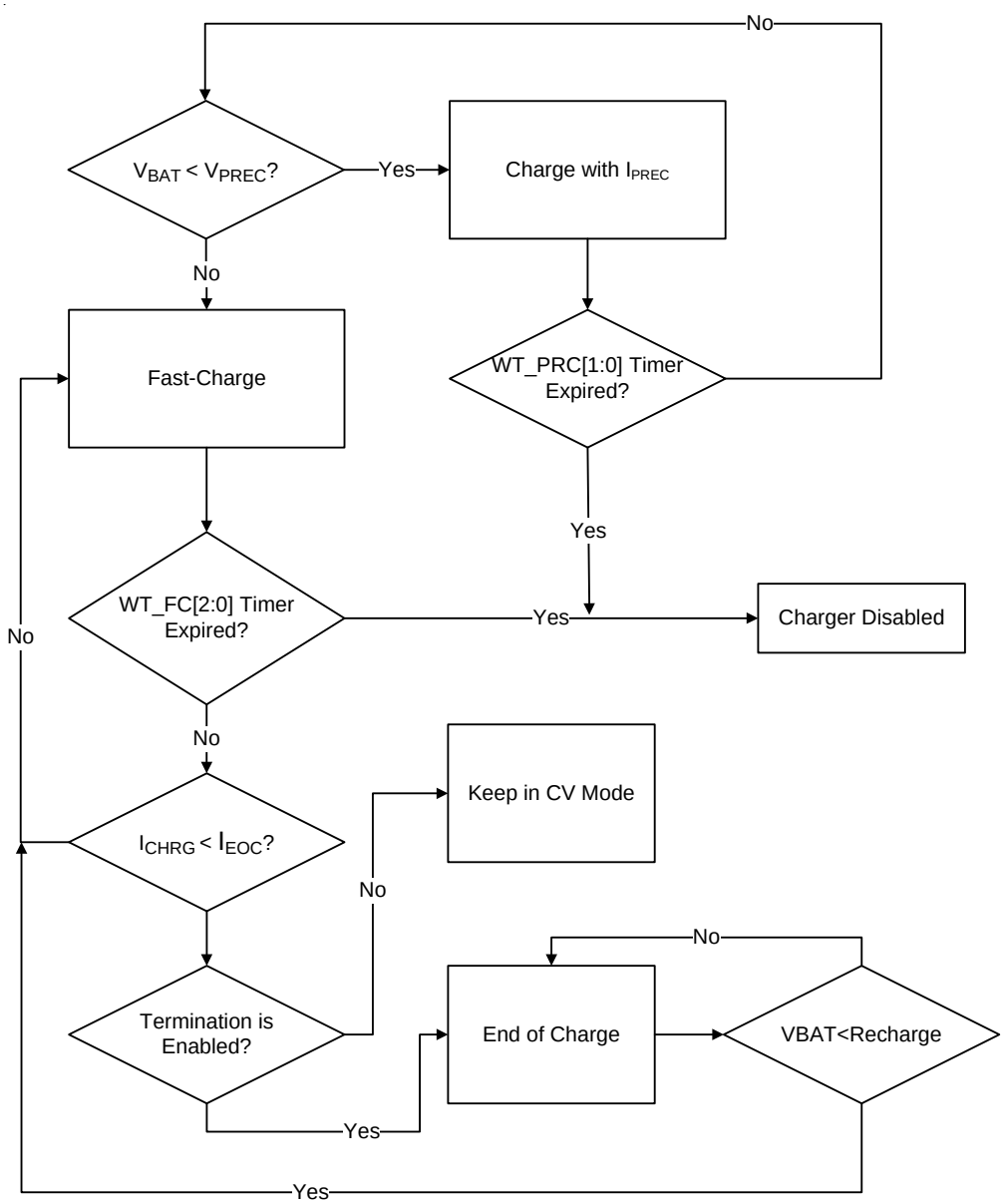
Stand-By and Wake-Up Flow Chart



Protection Flow Chart



Charger Flow Chart



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 10V
- VMIDCHG, VBOOTCHG ---------- –0.3V to 10V
- LXCHG ---------- –0.3V to 6V
- VMIDCHG – VINCHG, VBOOTCHG – LXCHG ---------- –0.3V to 6V
- Others ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 5x5 ---------- 3.63W
- Package Thermal Resistance (Note 2)
  WQFN-40L 5x5, θ_{JA} ---------- 27.5°C/W
  WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4.3V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(VINCHG = 5V, V_{ISENSN} = 4.2V, L = 1µH, C_{VINCHG} = 4.7µF, C_{VBATS} = 4.7µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Source						
VINCHG Operation Range			4.3	--	5.5	V
VINCHG Supply Current		Charger is switching, ICHG = 0, Buck loading = 0, LDOs loading = 0	--	10	--	mA
VINCHG Supply Current		Charger is not switching, ICHG = 0, Bucks loading = 0, LDOs loading = 0	--	--	5	mA
Leakage Current from Battery		VISENSN = 3.8V, VINCHG = 0V, Charger, Bucks and LDOs and LSWs are OFF. SCL = SDA = 0V.	--	--	50	µA
Protection						
VINCHG OVP Threshold Voltage			5.6	5.75	5.9	V
VINCHG OVP Hysteresis			--	100	--	mV
ISENSN OVP			110	117	124	%
ISENSN OVP Hysteresis			--	10	--	%
Over Temperature Protection		(Note 4)	--	165	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OTP Hysteresis			--	10	--	°C
Thermal Regulation Threshold		Charge Current Begins To Reduce (Note 4)	--	120	--	°C
Input Power Source Detection						
Poor Source Detect Threshold		Bad Voltage Source Detection	3.6	3.8	4	V
Poor Source Detect Deglitch			--	30	--	ms
Poor Source Detect Hysteresis		VINCHG Rising	100	--	200	mV
Current Sink to GND		During Poor Source Detection	--	45	--	mA
Detection Interval		Input Power Source Detection	--	2	--	s
Sleep Mode Comparator						
Sleep-Mode Entry Threshold VINCHG – ISENSN	V_{SLP}	3V < ISENSN < V_{BATREG}, VINCHG Falling	0	0.04	0.1	V
Sleep-Mode Exit Hysteresis VINCHG - ISENSN	$V_{SLPEXIT}$	3V < ISENSN < V_{BATREG}, VINCHG Rising	40	120	200	mV
Sleep-Mode Deglitch Time	t_{SLP}	VINCHG Rising Above V_{SLP} + $V_{SLPEXIT}$	--	128	--	ms
Under Voltage Lockout (UVLO) Threshold for VINCHG						
Charger Active Threshold Voltage		VINCHG Rising,	3.05	3.3	3.45	V
Charger Active Hysteresis		VINCHG Falling	--	150	--	mV
Minimum Input Voltage Regulation (MIVR)						
Minimum Input Voltage Regulation	V_{MIVR}	I^2C per 0.1V	4.2	--	4.8	V
V_{MIVR} Accuracy			–5	--	5	%
Average Input Current Regulation (AICR) Accuracy	I_{AICR}	I_{AICR} = 100mA	80	90	100	mA
		I_{AICR} = 500mA	400	450	500	
		I_{AICR} = 1000mA	800	900	1000	
VDDA Regulator						
VDDA Voltage		V_{VINCHG} > 4.5V	--	4.5	--	V
		V_{VINCHG} < V_{ISENSN}	--	V_{ISENSN}	--	V
VDDA UVLO		VDDA Falling	2.4	2.5	2.6	V
VDDA UVLO Hysteresis		VDDA Rising	--	0.2	--	
Battery Voltage Regulation						
Battery Voltage Regulation	V_{BATREG}	I^2C Programmable Per 25mV	3.65	--	4.4	V
V_{BATREG} Accuracy		0 to 85°C	–1	--	1	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Re-Charge Threshold	(V_{BATREG} – V_{REC})	V_{VBATS} Falling, (V_{BATREG} – V_{REC}) = programmable	100	--	300	mV
Re-Charge Deglitch	t_{REC}		--	128	--	ms
Charging Current Regulation						
Output Charging Current	I_{CHG}	I^2C Per 0.1A, R_{SENSE} = 20mΩ	0.7	--	2	A
I_{CHG} Accuracy		R_{SENSE} = 20mΩ	-100	--	100	mA
Pre-Charge Threshold	V_{PREC}	I^2C Per 0.1V, rising threshold	2.3	--	3.8	V
V_{PREC} Accuracy			–5	--	5	%
Pre-Charge Current	I_{PREC}	I^2C Per 100mA, from VBATS U100 mode : I_{PREC} will fix 50mA	150	--	450	mA
I_{PREC} Accuracy			–20	--	20	%
Charge Termination Detection						
End of Charge Current	I_{EOC}	I^2C per 50mA, R_{SENSE} = 20mΩ U100 mode : IEOC will fix 50mA	150	--	600	mA
I_{EOC} Accuracy		R_{SENSE} = 20mΩ	–100	--	100	mA
Deglitch Time for EOC	t_{EOC}	I_{CHG} < I_{EOC}, V_{ISENSN} > V_{REC} I^2C 32/64/128/256us	32	--	256	µs
Charger Timer Protection						
FastCharge Timer		I^2C per 2 Hrs	4	--	16	Hrs
PreCharge Timer		I^2C 0.5/1/2/4 Hrs	0.5	--	4	Hrs
Battery Detection Current	I_{BATDET}	As RNTC is disable, after EOC Done	--	0.5	--	mA
Battery Detection Time	t_{BATDET}	As RNTC is disable, after EOC Done	--	256	--	ms
NTC Monitor						
HOT Threshold	V_{VTS_HOT}	VTS falling, the ratio of VOL1, VINCHG > $V_{IN(MIN)}$	--	28	--	%VOL1
WARM Threshold	V_{VTS_WARM}	VTS falling, the ratio of VOL1, VINCHG > $V_{IN(MIN)}$	--	34	--	%VOL1
COOL Threshold	V_{VTS_COOL}	VTS rising, the ratio of VOL1, VINCHG > $V_{IN(MIN)}$	--	64	--	%VOL1
COLD Threshold	V_{VTS_COLD}	VTS rising, the ratio of VOL1, VINCHG > $V_{IN(MIN)}$	--	74	--	%VOL1
Accuracy of VTS			–2	--	2	%VOL1
Low Temperature Hysteresis	ΔV_{VTS}		--	1	--	%VPTS
Disable Threshold	V_{VTS_OFF}	TS function disable	--	--	5	%VPTS
Battery Absent Detection	V_{BAT_ABS}	VTS rising, the ratio of VPTS, VINCHG > $V_{IN(MIN)}$	--	90	--	%VPTS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Switching Charger						
Reverse Block On-Resistance	RREV	From VINCHG to VMIDCHG, as I_{AICR} disable or I_{AICR} = 2A	--	90	--	mΩ
High-Side On-Resistance	R_{HS}	From VMIDCHG to LXCHG	--	200	--	mΩ
Low-Side On-Resistance	R_{LS}	From CHGLX to PGND	--	90	--	mΩ
Charging Efficiency		V_{VINCHG} = 5V, V_{ISENSN} = 4V, and I_{CHG} = 1.5A,	--	85	--	%
Oscillator Frequency	f_{OSC}	I^2C for 0.75/1.5 MHz	--	1.5	--	MHz
Frequency Accuracy			–10	--	10	%
Maximum Duty Cycle		At Minimum Voltage Input	--	95	--	%
Minimum Duty Cycle			0	--	--	%
Peak OCP as Charger Mode			2.4	3	3.6	A
Reverse Boost Mode Operation						
Output Voltage Level		To VMIDCHG, I^2C per 25mV VMIDCHG setting ≧ V_{VBATS} + 0.4	3.625	--	5.2	V
Output Voltage Accuracy			–3	--	3	%
Efficiency		VMIDCHG = 5V, V_{ISENSN} = 4V, and Loading = 1A,	--	85	--	%
MAX Output Current for VINCHG		As V_{ISENSN} > 3.5V	1	--	--	A
Peak Over Current Protection			2.4	3.0	3.6	A
VMIDCHG OVP as Reverse Boost			--	5.5	--	V
VMIDCHG OVP Hysteresis			--	200	--	mV
Minimum Battery Voltage for Boost.	V_{BATMIN}	As Boost Start-Up. I^2C programmable Per 0.1V	2.9	--	3.6	V
I^2C Characteristics						
Output Low Voltage	V_{OL}	I_{DS} = 10mA	--	--	0.4	V
SCL /SDA Input Threshold Voltage	V_{IH}	Logic High Threshold	1.4	--	--	V
	V_{IL}	Logic Low Threshold	--	--	0.4	V
SCL Clock			--	--	400	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Control I/O Pin						
Output Low Voltage (IRQ, RESETB)	V_{OL}	I_{DS} = 10mA	--	--	0.4	V
Logic Input Threshold Voltage (PWRON)	V_{IH}	Logic High Threshold	1.4	--	--	V
	V_{IL}	Logic Low Threshold	--	--	0.4	V
LDO1 to LDO4, LSW1, LSW2						
VINL1,VINL234 Input Voltage Range	$V_{VINL1,234}$		2.7	--	5.5	V
LDO1 to LDO4 Adjustable Output Range		I^2C per 25mV	0.8	--	3.3	V
PSRR		$V_{VINL1, 234}$ = 4V, F = 1kHz, $C_{VOL1\ to\ 4}$ = 1µF	--	60	--	dB
LDO1 to LDO4 MAX Current			350	--	--	mA
Output Current Limit for LDO1 to LDO4			500	--	--	mA
Drop Out Voltage		$V_{VINL1, 234}$ = 3V, I_{OUT} = 150mA	--	--	150	mV
Internal Off Discharge			--	1	--	kΩ
VINLSW1, VINLSW2			2.7	--	5.5	V
LSW Drop Out Voltage		$V_{VINLSW1, 2}$ = 3.3V, I_{OUT} = 500mA	--	0.2	--	V
Output Current Limit for LSW1, LSW2			600	--	--	mA
Synchronize Buck Regulator1 to Buck Regulator4						
VINB1 to VINB4 Input Voltage Range	$V_{BUCKVIN}$		2.7	--	5.5	V
Quiescent Current from VINB1 to VINB4		Loading = 0mA, no switch, Each one	--	25	40	µA
Shutdown Current from VINB1 to VINB4		Each one	--	0.1	1	µA
Buck1 to Buck4 Adjustable Output Range	$V_{VOUTSB1\ to\ 4}$	I^2C per 25mV	0.8	--	3.3	V
Output Voltage Accuracy		$V_{VINB1\ to\ 4}$ = 2.7V to 5.5V, V_{OUT} > 1V	–3	--	3	%
Output Voltage Accuracy		$V_{VINB1\ to\ 4}$ = 2.7V to 5.5V, $V_{OUT} \leq$ 1V	–30	--	30	mV
High-Side On-Resistance		$V_{VINB1\ to\ 4}$ = 3.6V	--	0.20	--	Ω
Low -Side On-Resistance		$V_{VINB1\ to\ 4}$ = 3.6V	--	0.20	--	Ω
Buck 1, 2 Output Current capability		DC	1.6	--	--	A
Buck 1, 2 Output Current capability		Peak	2	--	--	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Accuracy		$V_{VINL1\ to\ 4}$ = 2.7V to 5.5V, V_{OUT} > 1V	–3		3	%
Output Voltage Accuracy		$V_{VINL1\ to\ 4}$ = 2.7V to 5.5V, $V_{OUT} \leq$ 1V	–30		30	mV
Buck 3, 4 Output Current capability		DC	1.2	--	--	A
Buck 3, 4 Output Current capability		Peak	1.5	--	--	A
Oscillator Frequency		$V_{VINB1\ to\ 4}$ = 3.6V, Loading = 200mA	--	1.5	--	MHz
Maximum Duty Cycle			100	--	--	%
Soft-Start Time	T_{SS}		--	150	--	μs
Discharge Time		C_{OUT} of Buck = 10μF, (Note 5)	--	--	10	ms
Line Regulation				0.1	--	%/V
RTC						
RTC Operation Voltage			2.4	--	4.5	V
RTC Quiescent Current		RTCPWR > UVLO Threshold, XIN = XOUT = 14pF	--	--	3	μA
RTC Clock			--	32.768	--	kHz
RTC Clock Accuracy		RTC Operation Voltage = 1.6V to 3.3V	–10	--	10	ppm
RTC Clock Output High		Pin C32K Source Out 0.1mA	VDDA –0.3	--	--	V
RTC Clock Output Low		Pin C32K Sink 0.1mA	--	--	0.3	V
RTC OSC Startup Time			--	0.5	1	s

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

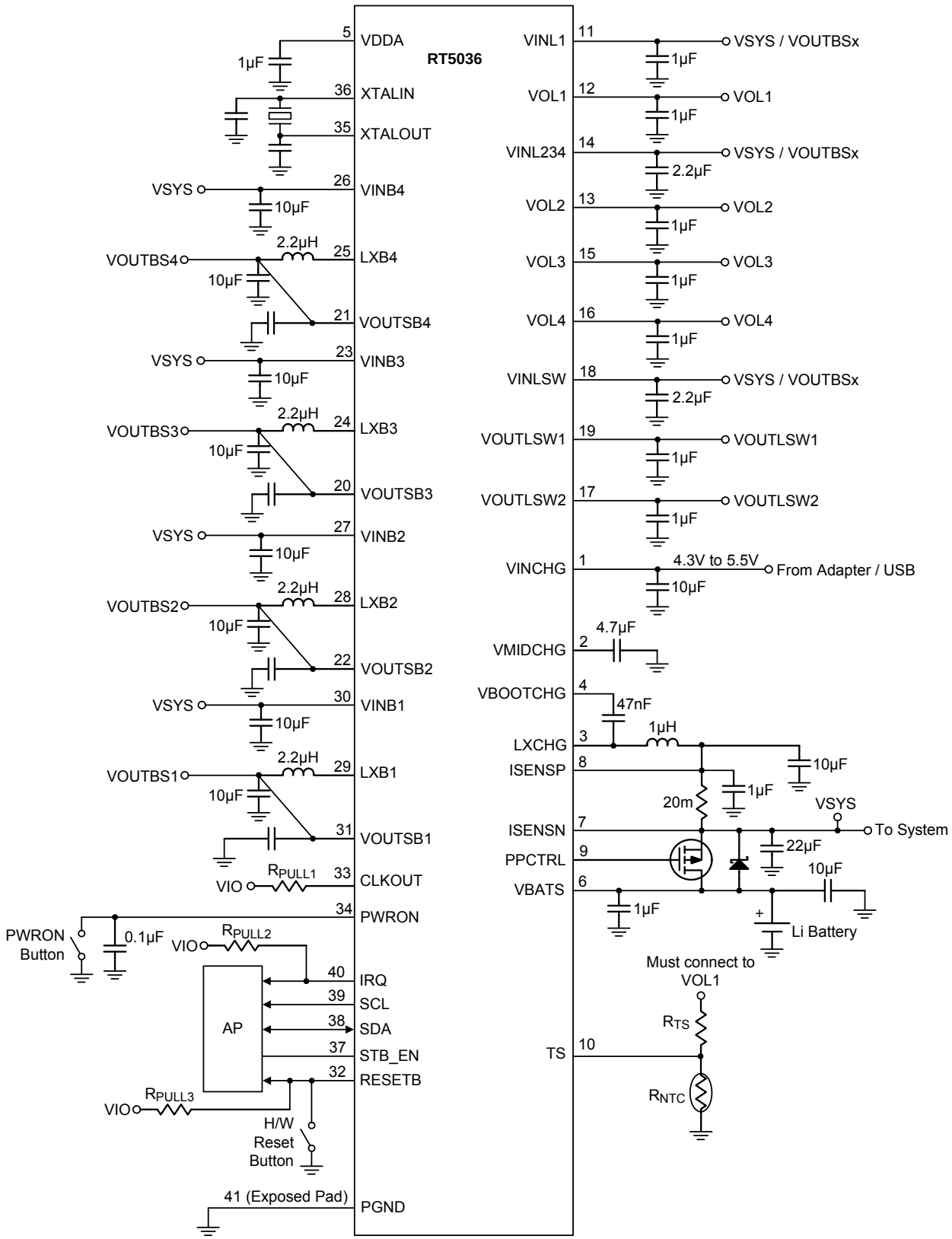
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee By Design.

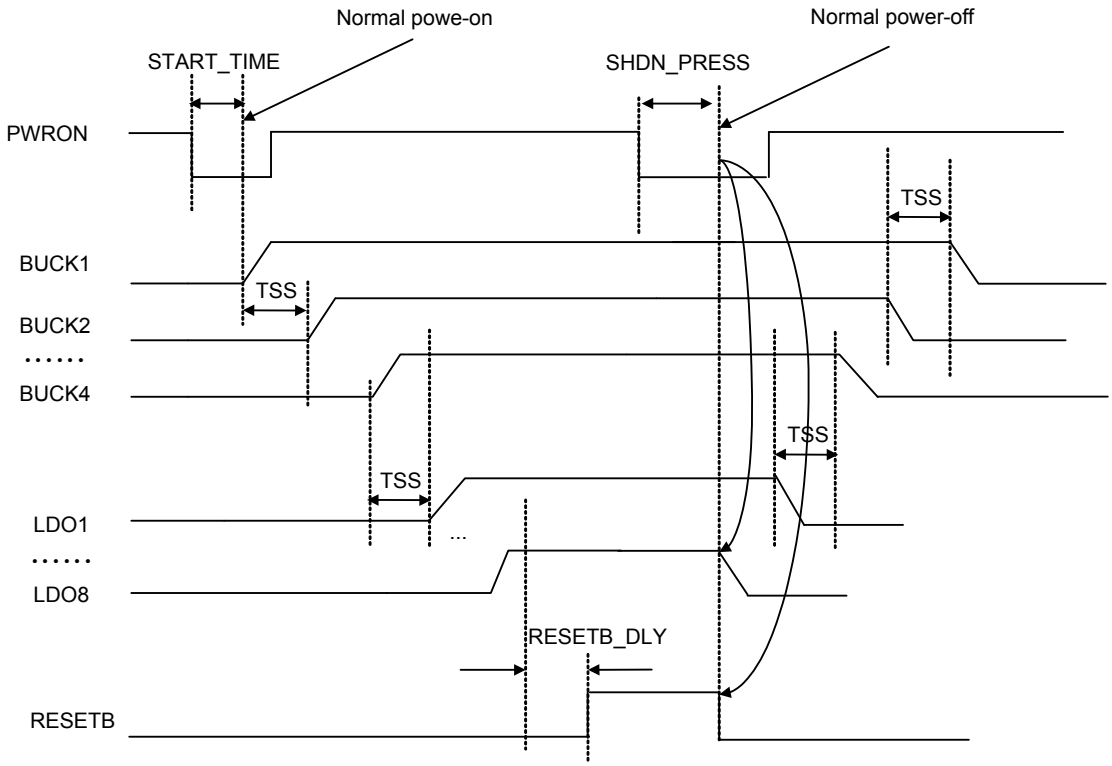
Typical Application Circuit



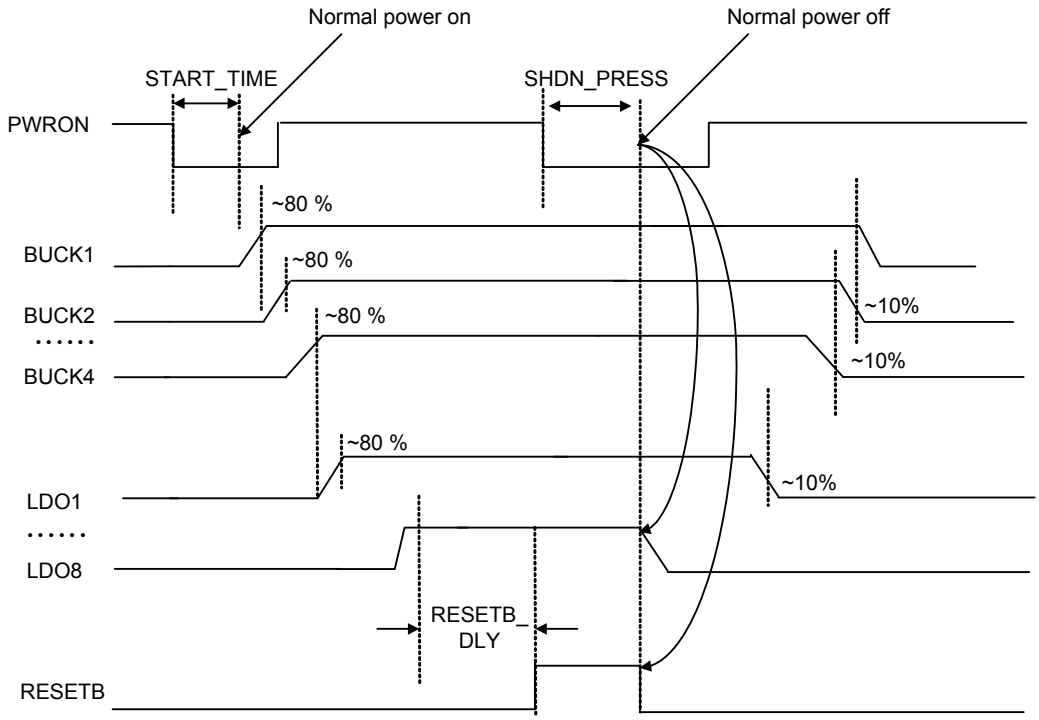
Timing Diagram

PMIC - POWER On/Off DIAGRAM

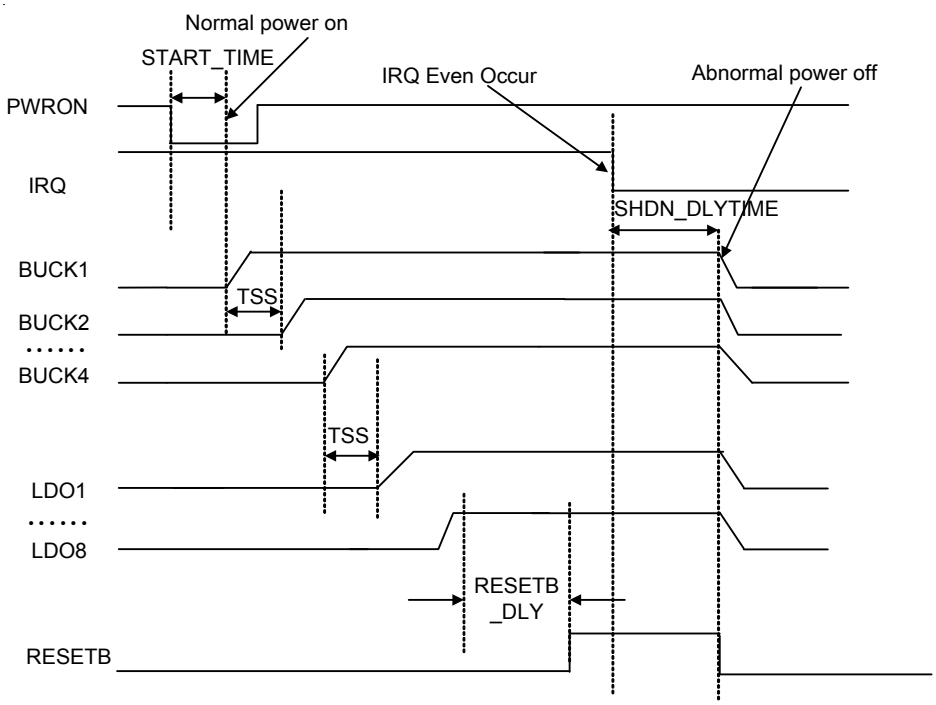
Timing Based On/Off Sequence



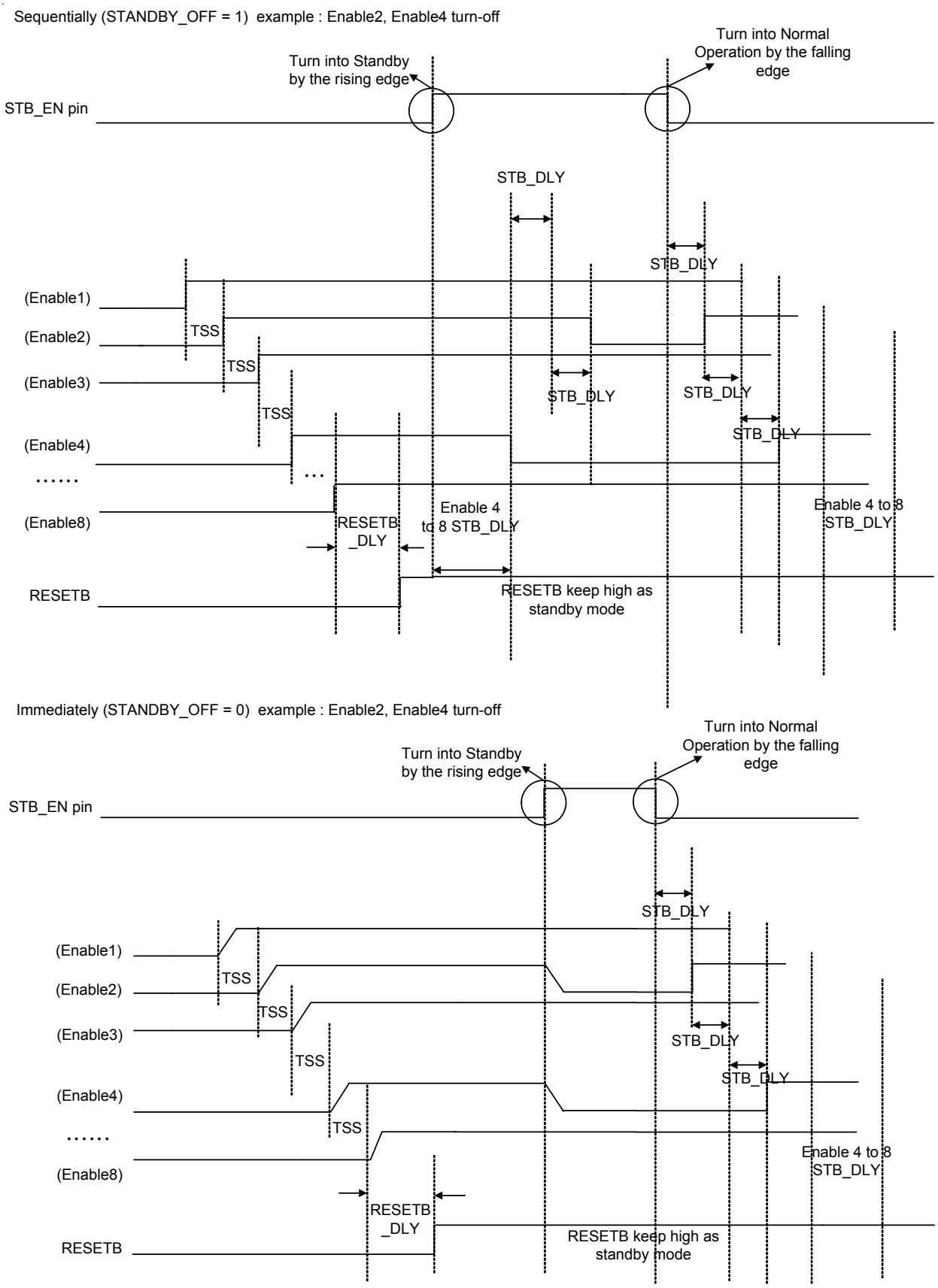
Level Based On/Off Sequence



Abnormal Off

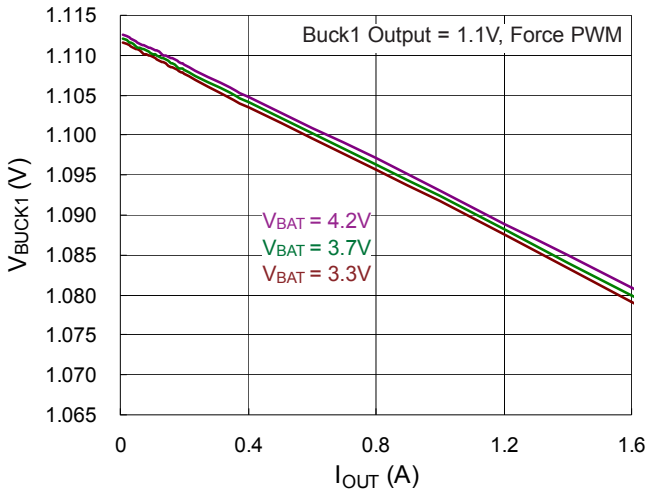


Standby mode and wake up by power-on

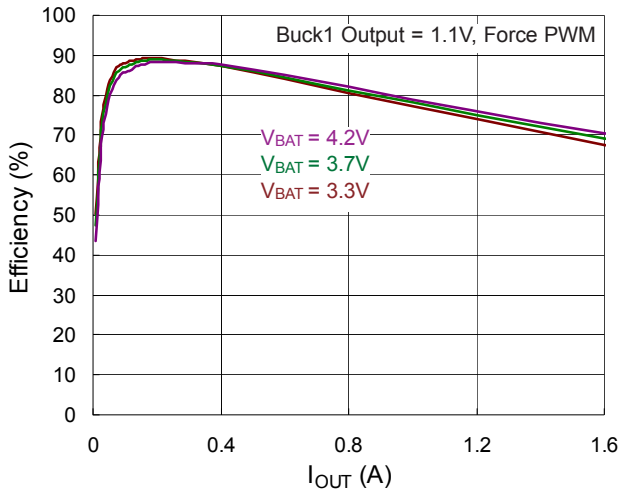


Typical Operating Characteristics

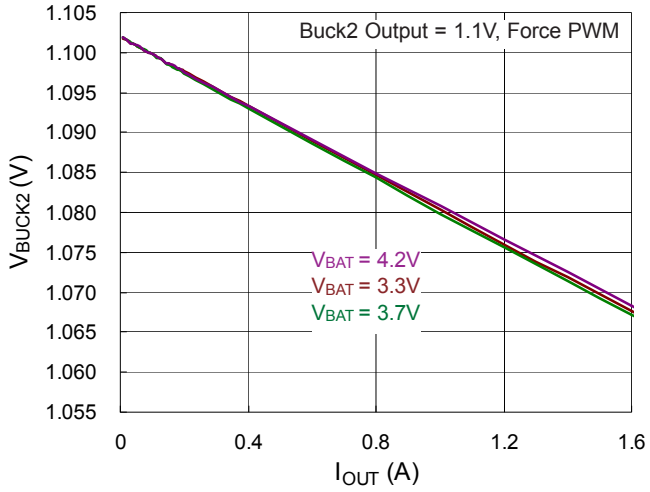
Buck1 Load Regulation



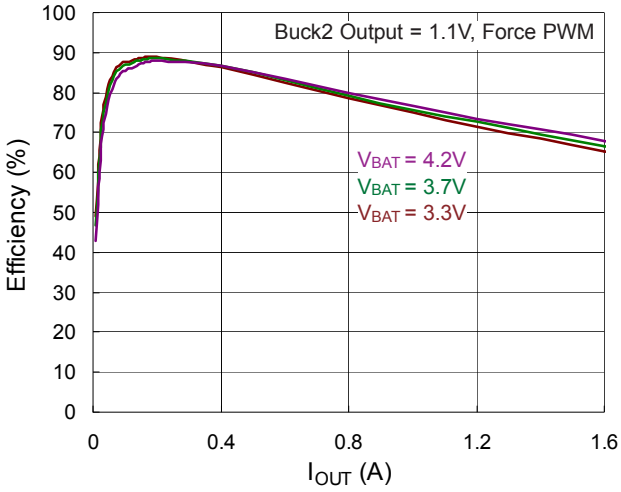
Buck1 Efficiency



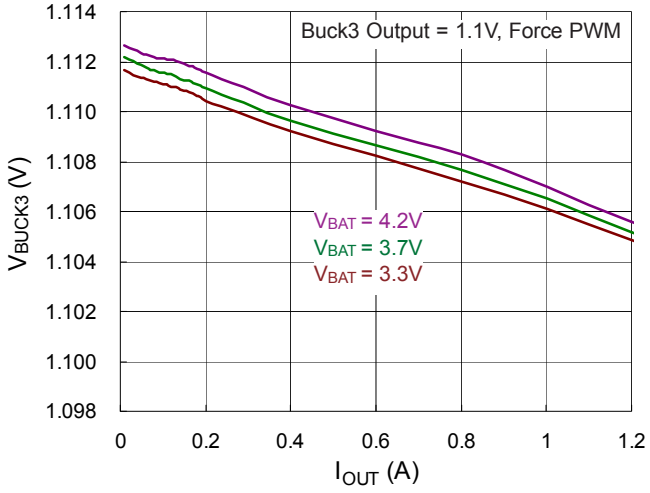
Buck2 Load Regulation



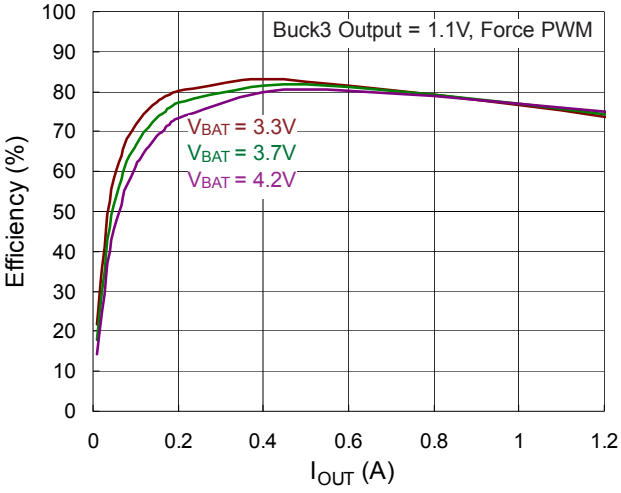
Buck2 Efficiency



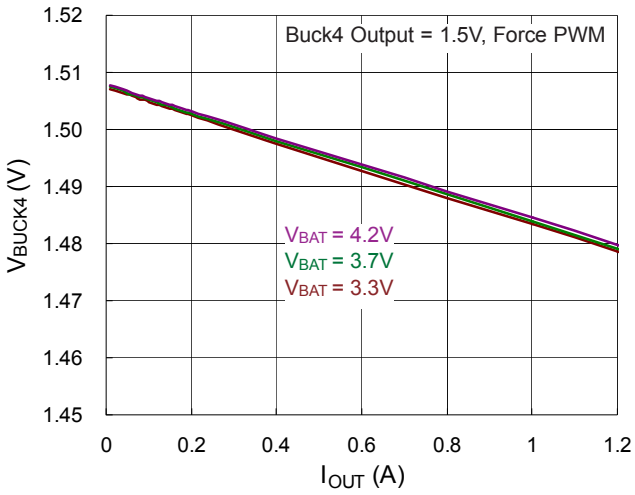
Buck3 Load Regulation



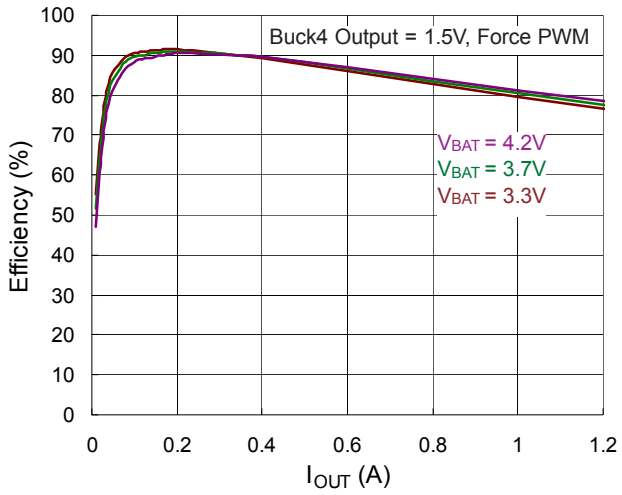
Buck3 Efficiency



Buck4 Load Regulation



Buck4 Efficiency



Application Information

Switching Charger

The switching charger integrates a synchronous PWM controller with power MOSFETs to provide Minimum Input Voltage Regulation (MIVR), Average Input Current Regulation (AICR), high accuracy current and voltage regulation, and charge termination. The charger also features OTG-Boost (On-The-Go).

The switching charger has two operation modes: charge mode, and boost mode (OTG-Boost). In charge mode, the switching charger supports a precision charging system for single cell. In boost mode, the switching charger works as the boost converter and boosts the voltage from battery to VINCHG pin for sourcing the OTG devices.

Notice that the switching charger does not integrate input power source (AC adapter or USB input) charging detection. Thus, the switching charger does not set the charge current automatically. The charge current needs to be set via I^2C interface by the host. The switching charger application mechanism and I^2C compatible interface are introduced in later sections.

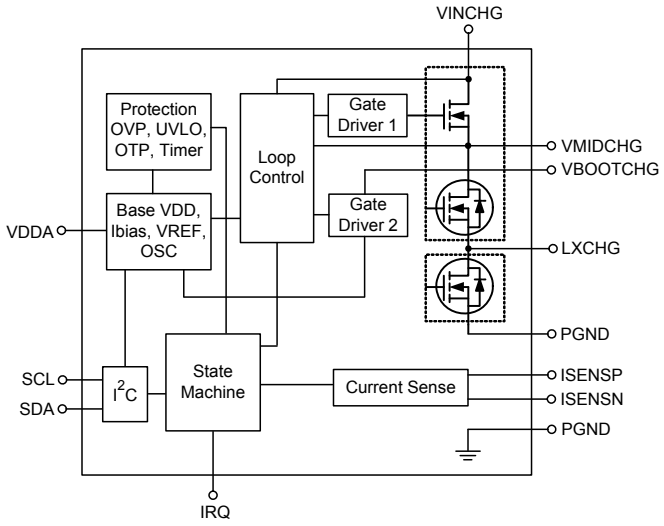


Figure 1. Switching Charger Function Block Diagram

Charge Mode Operation

Minimum Input Voltage Regulation (MIVR)

The switching charger features Minimum Input Voltage Regulation function to prevent input voltage drop due to insufficient current provided by the adaptor or USB input. If MIVR function is enabled, the input voltage decreases when the over current of the input power source occurs. VINCHG is regulated at a predetermined voltage level which can be set as 4.2V to 4.8V per 0.1V by I^2C interface. At this time, the current drawn by the switching charger equals to the maximum current value that the input power can provide at the predetermined voltage level, instead of the set value.

Table 1. MIVR Register Setting Table

MIVR[2:0]	V_{MIVR}
000	Disable
001	4.2V
010	4.3V
011	4.4V
100	4.5V (default)
101	4.6V
110	4.7V
111	4.8V

Charge Profile

The switching charger provides a precision Li-ion or Li-polymer charging solution for single-cell applications. Input current limit, charge current, termination current, charge voltage and input voltage MIVR are all programmable via the I^2C interface. In charge mode, the switching charger has five control loops to regulate input current, charge current, charge voltage, input voltage MIVR and device junction temperature. During the charging process, all five loops (if MIVR is enabled) are enabled and the dominant one will take over the control.

For normal charging process, the Li-ion or Li-polymer battery is charged in three charging modes depending on the battery voltage. At the beginning of the charging process, the switching charger is in pre-charge mode. When the battery voltage rises above pre-charge threshold

voltage (V_{PREC}), the switching charger enters fast-charge mode. Once the battery voltage is close to the regulation voltage (V_{BATREG}), the switching charger enters constant voltage mode.

Pre-Charge Mode

For life-cycle consideration, the battery cannot be charged with large current under low battery condition. When the VBATS pin voltage is below pre-charge threshold voltage (V_{PREC}), the charger is in pre-charge mode with a weak charge current witch equals to the pre-charge current (I_{PREC}). In pre-charge mode, the charger basically works as a Linear Charger. The pre-charge current also acts as the current limit when the VBATS pin is shorted.

The Pre-Charge current levels are 150mA to 450mA programmed by I^2C per 100mA.

Table 2. VPREC Register Setting Table

VPREC[2:0]	Pre-Charge Threshold
0000	2.3V
0001	2.4V
0010	2.5V
0011	2.6V
0100	2.7V
0101	2.8V
0110	2.9V
0111	3V
1000	3.1V
1001	3.2V
1010	3.3V
1011	3.4V
1100	3.5V (Default)
1101	3.6V
1110	3.7V
1111	3.8V

Table 3. IPREC Register Setting Table

IPREC[1:0]	Pre-Charge Current
00	150mA (Default)
01	250mA
10	350mA
11	450mA

Fast-Charge Mode and Settings

As the VBATS pin rises above V_{PREC}, the charger enters fast-charge mode and starts switching. Notice that the switching charger does not integrate input power source (AC adapter or USB input) detection. Thus, the switching charger does not set the charge current automatically. Unlike the linear charger (LDO), the switching charger (Buck converter) is a current amplifier. The current drawn by the switching charger is different from the current into the battery. The user can set the Average Input Current Regulation (AICR) and output charge current (I_{CHRG}) respectively.

Cycle-by-Cycle Current Limit

The charger of the switching charger has an embedded cycle-by-cycle current limit for inductor. Once the inductor current touches the threshold, the charger stops charging immediately to prevent over current from damaging the device. Notice that, the mechanism cannot be disabled by any way.

Average Input Current Regulation (AICR)

The AICR setting is controlled by I^2C. The AICR100 mode limits the input current to 100mA. The AICR500 mode limits the input current to 500mA.. If the application does not need input current limit, it can be disabled also.

The AICR levels are as below table and programmed by I^2C and suitable for USB port and several TA types (5V/ 0.7A, 5V/1A, 5V/2A).

Table 4. AICR Register Setting Table

AICR[2:0]	I_{AICR}
000	Disable
001	0.1A
010	0.5A
011	0.7A
100	0.9A (Default)
101	1A
110	1.5A
111	2A

Charge Current (I_{CHRG})

The charge current into the battery is determined by the sense resistor (R_{SENSE}) and ICC setting by I^2C. The voltage between the ISENSP and ISENSN pins is regulated to the voltage control by ICC setting.

As the R_{SENSE} is 20mΩ, the Fast-Charge currents are 700mA to 2A programmed by I^2C per 100mA.

Table 5. ICHG Register Setting Table

ICHG[3:0]	VCC	ICHG R_{SENSE} is 20mΩ
0000	10mV	0.5A
0001	12mV	0.6A
0010	14mV	0.7A
0011	16mV	0.8A
0100	18mV	0.9A
0101	20mV	1A
0110	22mV	1.1A
0111	24mV	1.2A
1000	26mV	1.3A
1001	28mV	1.4A
1010	30mV	1.5A (Default)
1011	32mV	1.6A
1100	34mV	1.7A
1101	36mV	1.8A
1110	38mV	1.9A
1111	40mV	2A

Constant Voltage Mode and Settings

The switching charger enters constant voltage mode when the ISENSN voltage is close to the output-charge voltage (V_{BATREG}). Once in this mode, the charge current begins to decrease. For default settings (charge current termination is disabled), the switching charger does not turn off and always regulates the battery voltage at V_{BATREG}. However, once the charge current termination is enabled, the charger terminates if the charge current is below termination current (I_{EOC}) in constant-voltage mode. The charge current termination function is controlled by the I^2C interface. After termination, a new charge cycle restarts when one of the following conditions is detected :

- The VBATS pin voltage falls below the VBATREG as V_{REC} threshold.
- VINCHG Power-On Reset (POR).
- Charge or Termination Enable bit toggle or Charger reset (via I^2C interface).

Output Charge Voltage (VBATREG)

The output-charge voltage is set by the I^2C interface. Its range is from 3.65V to 4.4V per 25mV.

Termination Current (IEOC)

If the charger current termination is enabled (TE bit = "1"), the end-of-charge current is determined by both the termination current sense voltage (V_{EOC}) and sense resistor (R_{SENSE}). As R_{SENSE} is 20mΩ, I_{EOC} is set by the I^2C interface from 150mA to 600mA per 50mA.

Table 6. EOC Register Setting Table

EOC[2:0]	VEOC	IEOC R_{SENSE} is 20mΩ
000	Disable	Disable
001	3mV	150mA
010	4mV	200mA
011	5mV	250mA (default)
100	6mV	300mA
101	8mV	400mA
110	10mV	500mA
111	12mV	600mA

Input Voltage Protection in Charge Mode

During charge mode, there are two protection mechanisms against if input power source capability is less than the charging current setting. One is AICR and the other is minimum input voltage regulation. A suitable level of AICR can prevent VINCHG drop by the insufficient capability. As the AICR setting is not suitable, MIVR will regulate the VINCHG in the setting level and sink the maximum current of power source.

Sleep Mode (V_{VINCHG} – V_{VBATS} < V_{SLP})

The switching charger enters sleep mode if the voltage drop between the VINCHG and VBATS pins falls below VSLP. In sleep mode, the reverse blocking switch and PWM are all turned off. This function prevents battery drain during poor or no input power source.

Input Over Voltage Protection

When VINCHG rises above the input over voltage threshold, the switching charger stops charging and then sets fault status bits. The condition is released when VINCHG falls below OVP threshold. The switching charger then resumes charging operation.

Reverse Boost Mode Operation (OTG)

Trigger and Operation

The switching charger features OTG-Boost support. When OTG function is enabled, the synchronous boost control loop takes over the power MOSFETs and reverses the power flow from the battery to the VINCHG pin. In normal boost mode, the VMIDCHG pin is regulated to 5V (typ.) to support other OTG devices connected to the USB connector.

Output Over-Voltage Protection

In boost mode, the output over voltage protection is triggered when the VMIDCHG voltage is above the output OVP threshold. When OVP occurs, the boost converter stops switching and turns off immediately.

Battery Protection

Battery Over-Voltage Protection in Charge Mode

The switching charger monitors the ISENSN voltage for output over voltage protection. In charge mode, if the ISENSN voltage rises above V_{OVP_BAT} x V_{BATREG}, such as when the battery is suddenly removed, the switching charger stops charging and then sets fault status bits and sends out fault pulse at the STAT pin. The condition is released when the ISENSN voltage falls below (V_{OVP_BAT} – ΔV_{OVP_BAT}) x V_{OVP_BAT}. The switching charger then resumes charging process with default settings and the fault is cleared.

Bucks

The RT5036 includes a synchronous step-down DC/DC converter that can support the input voltage range from 2.7V to 5.5V. The output current is up to 600mA. The output voltage can be programmable by I^2C. Following shows the function block of the RT5036 buck.

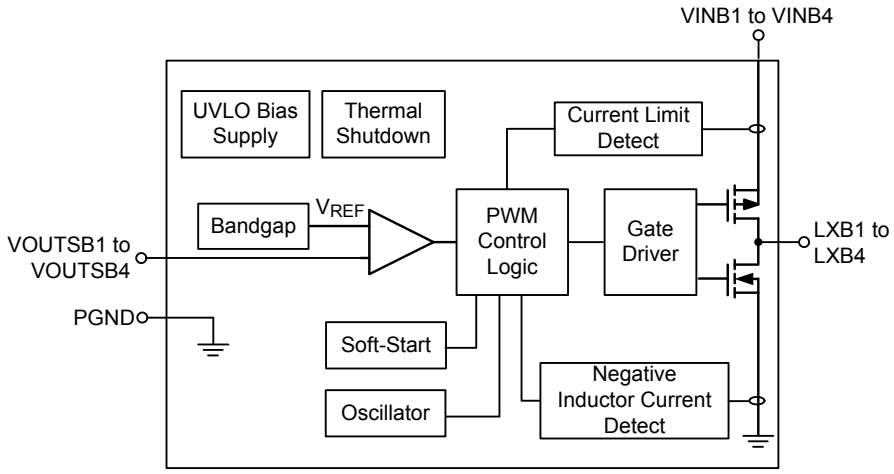


Figure 2. Buck Function Block Diagram

Normally, the high-side MOSFET is turned on by the PWM control logic block which drives the gate driver block when VOUTSB1 to VOUTSB4 is lower than the internal reference voltage. After VOUTSB1 to VOUTSB4 is higher than the internal reference voltage, the high side MOSFET will be turned off. While the high side MOSFET is turned off, the low side MOSFET is turned on until the current of the inductor is around zero by the negative inductor current detection block.

When the current of high side MOSFET is over the rating current, the high side MOSFET is turned off. When the temperature is over the rating temperature, the high side MOSFET is turned off until the temperature is dropped by the thermal shutdown block. After the thermal shutdown is released, VOUTSB1 to VOUTSB4 will be soft-started again.

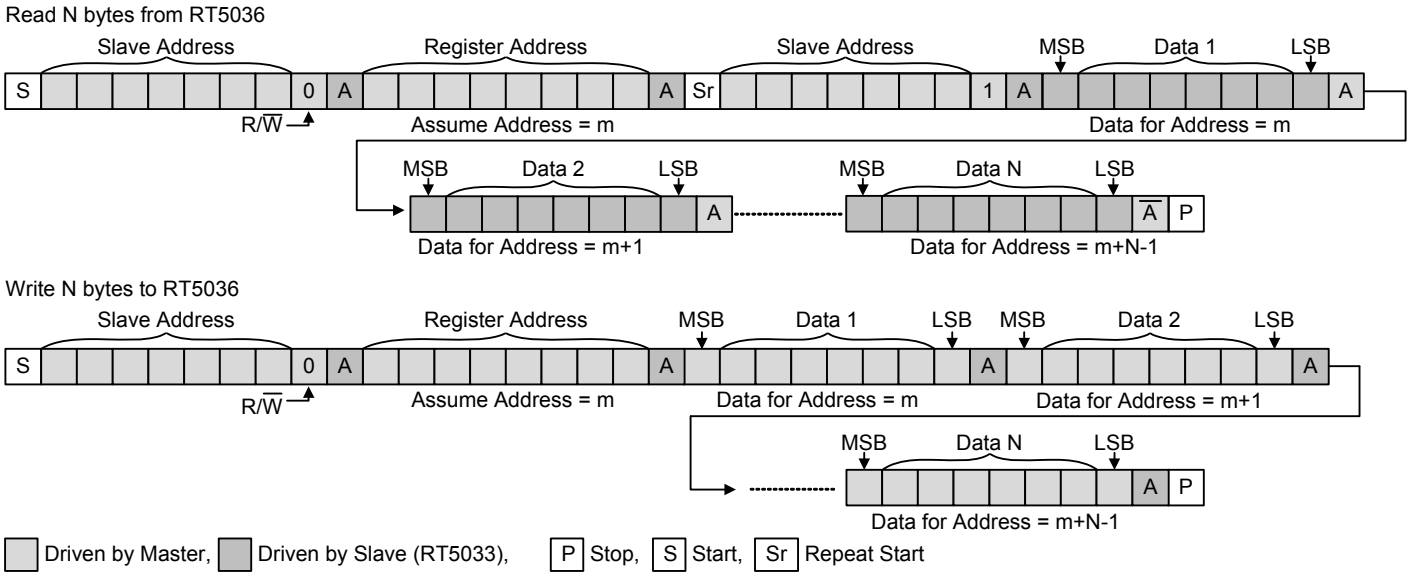
IRQ Operation

RT5036 summarize all IRQ items in the register table. All IRQ_status registers are implemented as reset after read. And IRQ pin is released only after IRQ_PRez bit is set. If IRQ Mask bit is High, the IRQ_status bit will not update status. IRQ_enable will mask IRQ_status to trigger IRQ Low, so the system can decide which interrupt is necessary.

I²C Interface

RT5036 I²C slave address = 7'b0111000.

I²C interface support fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :



I²C Registers Table

Switching Charger Parts

Name		Function	Addr	Reset
ID		ID	0x00	0x36
Bit	**Mode**	**name**	**Reset Value**	**Description**
[7:4]	R	VENDOR_ID	0011	Vendor Identification
[3:0]	R	CHIP_REV_ID	0110	CHIP_REV_ID

Name		Function	Addr	Reset
CHGControl1		Charger Control1	0x01	0x90
Bit	**Mode**	**name**	**Reset Value**	**Description**
[7:5]	R/W	IAICR[2:0]	100	AICR setting : 000 - Disable 001 - 0.1A 010 - 0.5A 011 - 0.7A 100 - 0.9A (default) 101 - 1.0A 110 - 1.5A 111 - 2A
4	R/W	Higher_OCP	1	The OCP level of buck mode selection bit 0 - OCP = 3A, 1 - OCP = 4A
3	R/W	TE	0	Termination enable 1 - Enable charge current termination, 0 - Disable charge current termination
2	R/W	Sel_SWFreq	0	The switching frequency selection bit (Charger/OTG) 0 - the switching frequency is 1.5MHz, 1 - the switching frequency is 0.75MHz
1	R/W	HZ	0	1-High impedance mode, 0-Not high impedance mode (default 0)
0	R/W	OPA_MODE	0	1 - Boost mode for OTG 0 - Charger mode (default 0)

Name		Function	Addr	Reset
CHGControl2		Charger Control2	0x02	0x58
Bit	**Mode**	**name**	**Reset Value**	**Description**
[7:2]	R/W	CV[5:0]	010110	Battery regulation voltage. The delta-V of the Battery regulation voltage is 25mV. 00 0000 - CHG: 3.65V, OTG: 3.625V 00 0001 - CHG: 3.675V, OTG: 3.65V 00 0010 - CHG: 3.7V, OTG : 3.675V 00 1101 - CHG: 3.975V, OTG: 3.95V ... 00 1110 - CHG: 4V, OTG: 3.975V 00 1111 - CHG: 4.025V, OTG: 4V ... 01 0110 - CHG: 4.2V, OTG: 4.175V (default) 01 1010 - CHG: 4.3V, OTG: 4.275V … 01 1011 - CHG: 4.325V, OTG: 4.3V 01 1100 - CHG: 4.350V, OTG: 4.325V 01 1101 - CHG: 4.375V, OTG: 4.35V 01 1110 - CHG: 4.4V, OTG: 4.375V … 11 0111 - CHG: 4.4V, OTG: 5.0V … 11 1110 - CHG: 4.4V, OTG: 5.175V 11 1111 - CHG: 4.4V, OTG: 5.2V
[1:0]	R/W	Reserved	00	Reserved

Name		Function	Addr	Reset
CHGControl3		Charger Control3	0x04	0xFF
Bit	**Mode**	**name**	**Reset Value**	**Description**
7	R/W	PP_BCK_SEL	1	EOC termination behavior selection. It's only works when SW_HW_CTRL = 1 0 : Disable Buck and supply power from power path PMOS. 1 : Disable Power Path MOS (Power supplied from Buck). (Default)
6	R/W	CHGOTG_EN	1	Charger OTG enable 0 – Charger and OTG mode are disabled, 1 – Charger and OTG mode can be enabled
[5:3]	R/W	WT_FC[2:0]	111	Fast charge Timer 000 – 4hrs 001 – 6hrs 010 – 8hrs 011 – 10hrs

Bit	Mode	name	Reset Value	Description
[5:3]	R/W	WT_FC[2:0]	111	100 – 12hrs 101 – 14hrs 110 – 16hrs 111 – 16hrs
[2:1]	R/W	WT_PRC[1:0]	11	Pre-charge charge Timer 00 – 0.5 hrs 01 – 1hrs 10 – 2hrs 11 – 4hrs
0	R/W	EN_TMR	1	0 - Disable internal timer function, 1 - Enable internal timer function (default 1)

Name		Function	Addr	Reset
CHGControl4		Charger Control4	0x05	0x83
Bit	**Mode**	**name**	**Reset Value**	**Description**
[7:5]	R/W	MIVR[2:0]	100	VMIVR 000 - Disable 001 - 4.2V 010 - 4.3V … 100 – 4.5V (default) 101 - 4.6V 110 - 4.7V 111 - 4.8V
[4:3]	R/W	IPREC[1:0]	00	Pre-Charge Current 00 - 150mA (default) 01 - 250mA 10 - 350mA 11 - 450mA
[2:0]	R/W	EOC[2:0]	011	Termination Current (IEOC RSENSE is 20mΩ) 000 - Disable 001 - 150mA 010 - 200mA 011 - 250mA (default) 100 - 300mA 101 - 400mA 110 - 500mA 111 - 600mA

Name		Function	Addr	Reset
CHGControl5		Charger Control5	0x06	0xAC
Bit	**Mode**	**name**	**Reset Value**	**Description**
[7:4]	R/W	ICHG[3:0]	1010	Charging regulation current External Sensing R : Charge current sense voltage (current equivalent for 20mΩ sense resistor) 0000 - 10mV (0.5A) 0001 - 12mV (0.6A) 0010 - 14mV (0.7A) 0011 - 16mV (0.8A) …… 1010 - 30mV (1.5A) (default) …… 1100 - 34mV (1.7A) 1101 - 36mV (1.8A) 1110 - 38mV (1.9A) 1111 - 40mV (2A)
[3:0]	R/W	VPREC[3:0]	1100	Pre-Charge Threshold (Rising threshold with hysteresis of 200mV) 0000 - 2.3V 0001 - 2.4V … 0100 - 2.7V 0101 - 2.8V … 1100 – 3.5 (default) 1101 – 3.6V 1110 – 3.7V 1111 - 3.8V

Name		Function	Addr	Reset
CHGControl6		Charger Control6	0x07	0xBC
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reserved	1	Reserved
6	R/W	TMR_PAUSE	0	0 – Internal timer keeps counting (default) 1 – Internal timer stops counting
5	R/W	Reverse Block ON/OFF	1	0 – Turn Off Reverse Block as OTG mode 1 – Turn On Reverse Block as OTG mode
[4:3]	R/W	Reserved	11	Reserved
[2:0]	R/W	BATLV	100	Low battery voltage threshold (Falling threshold with hysteresis of 400mV) 000 : 2.5V 001 : 2.6V 010 : 2.7V 011 : 2.8V (default) 100 : 2.9V 101 : 3V 110 : 3.1V 111 : 3.2V

Name		Function	Addr	Reset
CHGControl7		Charger Control7	0x08	0x01
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	CC_JEITA	0	Charging current setting bit for JEITA 1 – I_{CHG} / 2, 0 – I_{CHG},
6	R/W	OTG_OLP_BLK	0	When OTG OLP occurs, 0 : Enter HZ mode (Default) 1 : Disable UUG only and reverse boost keeps working.
[5:4]	R/W	Reserved	00	Reserved
[3:2]	R/W	VRECHG	00	Re-Charge Level 00 – CV-0.1V 01 – CV-0.2V. 10 – CV-0.3V. 11 – CV-0.3V.
1	R/W	Reserved	0	Reserved
0	R/W	TS_EN	1	TS shutdown ENABLE for TSHOT and TSCOLD. 0 : Disable TS shutdown function. 1 : Enable TS shutdown function. (Default)

Name		Function	Addr	Reset
RESET of CHG		RESET of CHG	0x09	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	CHG_RST	0	Write this bit to reset charger related registers 1 – Charger in reset mode, 0 – No effect, Read : always get “0”
[6:0]	R/W	Reserved	0000000	Reserved

Name		Function	Addr	Reset
CHG_IRQ1		Charger IRQ1	0x10	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	Reversed	0	Reversed
6	R	VINOVPI	0	CHGVIN over voltage protection. Set when CHGVIN > VIN_OVP is detected
5	R	IEOCI	0	Charging is terminated. It would not be triggered if TE bit is low.
4	R	PPBATLVI	0	BAT is in low level (power path need to be turned off)
3	R	VINCHG_Plugin	0	1 : VINCHG connected, 0 : Not connected
2	R	VINCHG_Plugout	0	1 : VINCHG removed, 0 : Not removed
1	R	CHBADADPI	0	Charger fault. Bad VIN source (Input source detect)
0	R	BAT_Absence	0	Detection result of battery absence detection 0 : Battery exists 1 : Detected battery-absence from battery detection of either one : a. TS > 90%*VPTS b. Battery detection when EOC c. Battery absence when adapter plug-in

Name		Function	Addr	Reset
CHG_IRQ2		Charger IRQ2	0x11	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	CHRVPI	0	Charger fault. Reverse protection fault (VIN < BATS + VSLP)
6	R	Reserved	0	Reserved
5	R	CHBATOVI	0	Charger fault. Battery OVP
4	R	CHTERMI	0	The charging current is lower than end-of-charge current. The charger keeps charging.
3	R	CHRCHGI	0	Re-Charge request.
2	R	CHTMRFI	0	Charger fault. Time-out (fault)
[1:0]	R	Reserved	00	Reserved

Name		Function	Addr	Reset
CHG_IRQ3		Charger IRQ3	0x12	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	BSTVMIDOVP	0	Boost fault. VMID OVP
5	R	CHBSTLOWVI	0	Charge or Boost fault. Battery voltage is too low
[4:1]	R	Reserved	0000	Reserved
0	R	CHG_STAT2 _ALT	0	Any Event in CHG_STAT2 changes, IRQ indicator.

Name		Function	Addr	Reset
CHG_IRQ1_MASK		Charger IRQ1 Mask	0x13	0x0C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
6	R/W	VINOVPIM	0	CHGVIN OVP fault interrupt mask 0 – interrupt is not masked, 1 – interrupt is masked
5	R/W	IEOCM	0	Charge terminated interrupt mask 0 – Interrupt is not masked 1 – Interrupt is masked
4	R/W	PPBATLVM	0	BAT is in low level (power path need to be turned off) 0 – Interrupt is not masked 1 – Interrupt is masked
3	R/W	VINCHG_PluginM	1	VINCHG connected, IRQ interrupt mask (UVP detects VINCHG > UVLO) 0 – Interrupt is not masked 1 – Interrupt is masked
2	R/W	VINCHG_PlugoutM	1	VINCHG removed, IRQ interrupt mask (UVP detects VINCHG < UVLO) 0 – Interrupt is not masked 1 – Interrupt is masked
1	R/W	Reversed	0	Reversed
0	R/W	BAT_Absence	0	BAT absence interrupt mask. 0 – Interrupt is not masked 1 – Interrupt is masked

Name		Function	Addr	Reset
CHG_IRQ2_ MASK		Charger IRQ2 Mask	0x14	0x80
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	CHRVPIM	1	Charger reverse protection interrupt mask 0 – Interrupt is not masked 1 – Interrupt is masked
6	R/W	Reserved	0	Reserved
5	R/W	CHBATOVIM	0	Charger battery over voltage interrupt mask 0 – Interrupt is not masked 1 – Interrupt is masked
4	R/W	CHTERMIM	0	Charge current is lower than EOC current interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
3	R/W	CHRCHGIM	0	Charger Re-Charge request interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
2	R/W	CHTMRFIM	0	Charger timeout interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
[1:0]	R/W	Reserved	00	Reserved

Name		Function	Addr	Reset
CHG_IRQ3_ MASK		Charger IRQ3 Mask	0x15	0x0F
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	BSTVMIDOVPM	0	Boost VMID over voltage interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
5	R/W	BSTLOWVIM	0	Boost mode low battery voltage interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
4	R/W	Reserved	0	Reserved
0	R/W	CHG_STAT2 _ALTM	0	Any Event in CHG_STAT2 changes, interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked

Name		Function	Addr	Reset
CHG_STAT		Charger status	0x16	0x02
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	EXT_PMOS_CTRL	0	Control external PPC PMOS on/off 0 - Disable PMOS 1 - Enable PMOS
6	R	VBAT_VL	0	Battery voltage level: 0: Battery voltage is lower than pre-charge level 1: Battery voltage is higher than pre-charge level
[5:4]	R	CHG_STAT	00	Charging Status 00：Ready to charge 01：Charge in progress 10：Charge Done 11：Charge Fault
3	R	BOOST_STAT	0	1 : Boost mode, 0 : Not in Boost mode
2	R	Reserved	0	Reserved
1	R/W	SW_HW_CTRL	1	Power path control by SW or HW 0 - Software decide 1 - Hardware decide
0	R/W	CHG_ENB	0	Charge Disable 1 - charger is disabled, 0 - charger is enabled

Name		Function	Addr	Reset
CHG_STAT2		Charger STAT2	0x17	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	PWR_RDY	0	Power status bit 0 : CHGVIN > VOVP or CHGVIN < ISENSN + VSLP (Power Fault) 1 : CHGVIN < VOVP & CHGVIN > ISENSN + VSLP (Power Ready)
6	R	CHTREGI	0	Charger warning. 0 - Thermal regulation loop inactive. 1 - Thermal regulation loop active.
5	R	CHMIVRI	0	Charger warning. 0 - MIVR regulation loop inactive. 1 – MIVR regulation loop active.
4	R	CHGAICRI	0	Charger warning. AICR regulation loop active. 0 - AICR regulation loop inactive. 1 - AICR regulation loop active.
3	R	TSHOT	0	Battery HOT Fault 0 –TS not in HOT region 1 – TS in HOT region, and charger disabled automatically.

Bit	Mode	Name	Reset Value	Description
2	R	TSWAR	0	Battery WARM Fault 0 –TS not in WARM region 1 – TS in WARM region
1	R	TSCOOL	0	Battery COOL Fault 0 –TS not in COOL region 1 – TS in COOL region
0	R	TSCOLD	0	Battery COLD Fault 0 – TS not in COLD region 1 – TS in COLD region, and charger disabled automatically.

Name		Function	Addr	Reset
CHG_STAT2_MASK		Charger STAT2_MASK	0x18	0x70
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	PWR_RDYM	0	Charger Power ON Ready, interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
6	R/W	CHTREGIM	1	Charger warning. Thermal regulation loop active, interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
5	R/W	CHMIVRIM	1	Charger warning. Input voltage MIVR loop active, interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
4	R/W	CHGAICRIM	1	Charger warning. AICR regulation loop active, interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
3	R/W	TSHOTM	0	Battery HOT Fault, , interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
2	R/W	TSWARMM	0	Battery WARM Fault, interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
1	R/W	TSCOOLM	0	Battery COOL Fault, interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked
0	R/W	TSCOLDM	0	Battery COLD Fault, interrupt mask 0 – Interrupt is not masked, 1 – Interrupt is masked

PMIC Parts

Name		Function	Addr	Reset
BUCK1 Control Normal		BUCK1 Output Control	0x41	0x0C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	IRQ_PRez	0	IRQ pin reset trigger. From low to high will reset IRQ pin and keep it in low within Tmsk, and after Tmsk expired. IRQ_PRez will be set to “0”
[6:0]	R/W	Buck1 Output_N[6:0]	0001100	Buck1 output voltage regulation (default by OTP 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111111 – 3.3V

Name		Function	Addr	Reset
BUCK1 Control Standby		BUCK1 Output Control	0x71	0x0C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	Buck1 Output_S [6:0]	0001100	Buck1 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111111 – 3.3V

Name		Function	Addr	Reset
BUCK2 Control Normal		BUCK2 Output Control	0x42	0x0C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	Buck2 Output_N [6:0]	0001100	Buck2 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V -- 1100101 – 3.3V 1111111 – 3.3V

Name		Function	Addr	Reset
BUCK2 Control Standby		BUCK2 Output Control	0x72	0x0C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	Buck2 Output_S [6:0]	0001100	Buck2 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111111 – 3.3V

Name		Function	Addr	Reset
BUCK3 Control Normal		BUCK3 Output Control	0x43	0x64
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	Buck3 Output_N [6:0]	1100100	Buck3 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111111 – 3.3V

Name		Function	Addr	Reset
BUCK3 Control Standby		BUCK3 Output Control	0x73	0x58
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	Buck3 Output_S [6:0]	1011000	Buck3 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111111 – 3.3V

Name		Function	Addr	Reset
BUCK4 Control Normal		BUCK4 Output Control	0x44	0x1C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	Buck4 Output_N [6:0]	0011100	Buck4 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111111 – 3.3V

Name		Function	Addr	Reset
BUCK4 Control Standby		BUCK4 Output Control	0x74	0x10
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	Buck4 Output_S[6:0]	0010000	Buck4 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111111 – 3.3V

Name		Function	Addr	Reset
BUCK VRC Control Normal		BUCK VRC Control	0x45	Option
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Buck1 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs,11 – 100mV/10μs,
[5:4]	R/W	Buck2 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs,11 – 100mV/10μs,
[3:2]	R/W	Buck3 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10uS, 10 – 75mV/10μs,11 – 100mV/10μs,
[1:0]	R/W	Buck4 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs,11 – 100mV/10μs,

Name		Function	Addr	Reset
BUCK VRC Control Standby		BUCK VRC Control	0x75	Option
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Buck1 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[5:4]	R/W	Buck2 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[3:2]	R/W	Buck3 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[1:0]	R/W	Buck4 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,

Name		Function	Addr	Reset
BUCK VRC Enable Normal		BUCK VRC Enable	0x46	0xF0
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Buck1VRC_EN_N	1	Buck1 VRC Normal 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
6	R/W	Buck2VRC_EN_N	1	Buck2 VRC Normal 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
5	R/W	Buck3VRC_EN_N	1	Buck3 VRC Normal 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
4	R/W	Buck4VRC_EN_N	1	Buck4 VRC Normal 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
[3:0]	R/W	Reversed	0000	Reversed

Name		Function	Addr	Reset
BUCK VRC Enable Standby		BUCK VRC Enable	0x76	0xF0
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Buck1VRC_EN_S	1	Buck1 VRC Normal 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
6	R/W	Buck2VRC_EN_S	1	Buck2 VRC Normal 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
5	R/W	Buck3VRC_EN_S	1	Buck3 VRC Normal 0 – Disable – voltage ramps up to target voltage with one time 1 – enable – voltage ramps up to target voltage with slope control
4	R/W	Buck4VRC_EN_S	1	Buck4 VRC Normal 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
[3:0]	R/W	Reversed	0000	Reversed

Name		Function	Addr	Reset
BUCK Mode		BUCK Mode	0x47	0x0F
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Buck1mode	0	Buck1 mode 0 – Force PWM 1 – Auto Mode (PSM/PWM)
6	R/W	Buck2mode	0	Buck2 mode 0 – Force PWM 1 – Auto Mode (PSM/PWM)
5	R/W	Buck3mode	0	Buck3 mode 0 – Force PWM 1 – Auto Mode (PSM/PWM)
4	R/W	Buck4mode	0	Buck4 mode 0 – Force PWM 1 – Auto Mode (PSM/PWM)
3	R/W	Buck1oms	1	Buck1 output off mode state 0 – floating 1 – Ground-discharged

Bit	Mode	Name	Reset Value	Description
2	R/W	Buck2oms	1	Buck2 output off mode state 0 – Floating 1 – Ground-discharged
1	R/W	Buck3oms	1	Buck3 output off mode state 0 – Floating 1 – Ground-discharged
0	R/W	Buck4oms	1	Buck4 output off mode state 0 – Floating 1 – Ground-discharged

Name		Function	Addr	Reset
LDO1Control Normal		LDO1 Output Control	0x48	0x64
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LDO1 Output_N[6:0]	1100100	LDO1 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 – Full On

Name		Function	Addr	Reset
LDO1Control Standby		LDO1 Output Control	0x78	0x58
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LDO1 Output_S [6:0]	1011000	LDO1 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 – Full On

Name		Function	Addr	Reset
LDO2 Control Normal		LDO2 Output Control	0x49	0x0C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LDO2 Output_N [6:0]	0001100	LDO2 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 –Full On

Name		Function	Addr	Reset
LDO2 Control Standby		LDO2 Output Control	0x79	0x0C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LDO2 Output_S [6:0]	0001100	LDO2 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 –Full On

Name		Function	Addr	Reset
LDO3 Control Normal		LDO3 Output Control	0x4A	0x50
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LDO3 Output_N [6:0]	1010000	LDO3 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 – Full On

Name		Function	Addr	Reset
LDO3 Control Standby		LDO3 Output Control	0x7A	0x28
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LDO3 Output_S [6:0]	0101000	LDO3 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 – Full On

Name		Function	Addr	Reset
LDO4 Control Normal		LDO4 Output Control	0x4B	0x28
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LDO4 Output_N[6:0]	0101000	LDO4 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 – Full On

Name		Function	Addr	Reset
LDO4 Control Standby		LDO4 Output Control	0x7B	0x28
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LDO4 Output_S[6:0]	0101000	LDO4 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 –Full On

Name		Function	Addr	Reset
LDO VRC Control Normal		LDO VRC Control	0x4C	Option
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	LDO1 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[5:4]	R/W	LDO2 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[3:2]	R/W	LDO3 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[1:0]	R/W	LDO4 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,

Name		Function	Addr	Reset
LDO VRC Control Standby		LDO VRC Control	0x7C	Option
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	LDO1 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[5:4]	R/W	LDO2 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[3:2]	R/W	LDO3 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[1:0]	R/W	LDO4 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,

Name		Function	Addr	Reset
LDO VRC Enable Normal		LDO VRC Enable	0x4D	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	LDO1VRC_EN_N	0	LDO1 VRC 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
6	R/W	LDO2VRC_EN_N	0	LDO2 VRC 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
5	R/W	LDO3VRC_EN_N	0	LDO3 VRC 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
4	R/W	LDO4VRC_EN_N	0	LDO4 VRC 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
[3:0]	R/W	Reserved	0000	Reserved

Name		Function	Addr	Reset
LDO VRC Enable Standby		LDO VRC Enable	0x7D	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	LDO1VRC_EN_S	0	LDO1 VRC 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
6	R/W	LDO2VRC_EN_S	0	LDO2 VRC 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
5	R/W	LDO3VRC_EN_S	0	LDO3 VRC 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control

Bit	Mode	Name	Reset Value	Description
4	R/W	LDO4VRC_EN_S	0	LDO4 VRC 0 – Disable – voltage ramps up to target voltage with one time 1 – Enable – voltage ramps up to target voltage with slope control
[3:0]	R/W	Reserved	0000	Reserved

Name		Function	Addr	Reset
LDOs/LSW Mode		LDOs/LSW Off Mode	0x4E	0XF3
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	LDO1oms	1	LDO1 output off mode state 0 – Floating 1 – Ground-discharged
6	R/W	LDO2oms	1	LDO2 output off mode state 0 – Floating 1 – Ground-discharged
5	R/W	LDO3oms	1	LDO3 output off mode state 0 – Floating 1 – Ground-discharged
4	R/W	LDO4oms	1	LDO4 output off mode state 0 – Floating 1 – Ground-discharged
[3:2]	R/W	Reserved	00	Reserved
1	R/W	LSW2oms	1	LSW2 output off mode state 0 – Floating 1 – Ground-discharged
0	R/W	LSW1oms	1	LSW1 output off mode state 0 – Floating 1 – Ground-discharged

Name		Function	Addr	Reset
Bucks/LDOs On/Off Normal		Bucks/LDOs On/Off	0x4F	Option
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	LDO1_EN_N	0	LDO1 Enable Control Bit. 0 – OFF 1 – ON
6	R/W	LDO2_EN_N	0	LDO2 Enable Control Bit. 0 – OFF 1 – ON
5	R/W	LDO3_EN_N	0	LDO3 Enable Control Bit. 0 – OFF 1 – ON

Bit	Mode	Name	Reset Value	Description
4	R/W	LDO4_EN_N	0	LDO4 Enable Control Bit. 0 – OFF 1 – ON
3	R/W	Buck1_EN_N	0	Buck1 Enable Control Bit. 0 – OFF 1 – ON
2	R/W	Buck2_EN_N	0	Buck2 Enable Control Bit. 0 – OFF 1 – ON
1	R/W	Buck3_EN_N	0	Buck3 Enable Control Bit. 0 – OFF 1 – ON
0	R/W	Buck4_EN_N	0	Buck4 Enable Control Bit. 0 – OFF 1 – ON

Name		Function	Addr	Reset
Bucks/LDOs On/Off Standby		Bucks/LDOs On/Off standby	0x7F	Option
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	LDO1_EN_S	0	LDO1 Enable Control Bit. 0 – OFF 1 – ON
6	R/W	LDO2_EN_S	0	LDO2 Enable Control Bit. 0 – OFF 1 – ON
5	R/W	LDO3_EN_S	0	LDO3 Enable Control Bit. 0 – OFF 1 – ON
4	R/W	LDO4_EN_S	0	LDO4 Enable Control Bit. 0 – OFF 1 – ON
3	R/W	Buck1_EN_S	0	Buck1 Enable Control Bit. 0 – OFF 1 – ON
2	R/W	Buck2_EN_S	0	Buck2 Enable Control Bit. 0 – OFF 1 – ON
1	R/W	Buck3_EN_S	0	Buck3 Enable Control Bit. 0 – OFF 1 – ON
0	R/W	Buck4_EN_S	0	Buck4 Enable Control Bit. 0 – OFF 1 – ON

Name		Function	Addr	Reset
LSWs On/Off		LSWs On/Off	0x50	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	WK_CTRL	0	Wake-up Control 0 –Adapter Plug-in or RTC Count Down to 0 or PWRON Reboot can't wake-up from standby mode 1 – Adapter Plug-in or RTC Count Down to 0 or PWRON Reboot can wake-up from standby mode
[6:4]	R/W	Reserved	000	Reserved
3	R/W	LSW2_EN_S	0	LSW2 Enable Control Bit. Standby 0 – OFF 1 – ON
2	R/W	LSW1_EN_S	0	LSW1 Enable Control Bit. Standby 0 – OFF 1 – ON
1	R/W	LSW2_EN_N	0	LSW2 Enable Control Bit. Normal 0 – OFF 1 – ON
0	R/W	LSW1_EN_N	0	LSW1 Enable Control Bit. Normal 0 – OFF 1 – ON

Name		Function	Addr	Reset
REBOOT/StandBy Ctrl		REBOOT/StandBy Ctrl	0x51	0xA0
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Delay2[1:0]	10	Delay2 setting00 : 100ms 01 : 500ms 10 : 1s 11 : 2s
[5:4]	R/W	Delay1[1:0]	10	Delay1 setting 00 : 100ms 01 : 500ms 10 : 1s 11 : 2s
[3:2]	R/W	RESET Action	10	00 : Reset BUCK1 to BUCK4 and LDO1 to LDO4 output level to default 01 : delay1 power-off PMIC 10 : delay1 power-off then delay2 power-on PMIC 11 : reserved
[1:0]	R/W	Reserved	00	Reserved

Name		Function	Addr	Reset
PWRON/RESETB Time Setting		PWRON/RESETB Time Setting	0x52	0X16
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Reserved	00	Reserved
[5:4]	R/W	L_PRESS_TIME[1:0]	01	Long-press time setting (after Power-On) 00 : 1s 01 : 1.5s 10 : 2s 11 : 2.5s Sending short/long-press IRQ to CPU Ex : 1.5s = low time < 1.5s (short IRQ) = low time > 1.5s but < 6s (shutdown time) (long IRQ) = low time > 6s (shutdown time) (shutdown)
[3:2]	R/W	SHDN_PRESS	01	Key-press forced shutdown time setting 00 : 4s (pressing time-low level) 01 : 6s 10 : 8s 11 : 10s
[1:0]	R/W	RESETB_DLY	Option	RESETB signal delay after the last power startup is done 00 : 100ms 01 : 200ms 10 : 400ms 11 : 800ms

Name		Function	Addr	Reset
SHDN/standby Control		Shutdown/standby Control	0x53	0X48
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	SHDN_CTRL	0	Power Off is set by CPU. 100ms delay to power off after setting. 0 : Normal operation 1 : Disable the PMIC output
6	R/W	SHDN_TIMING	1	Disable Buck/LDO only for normal power off (SHDN_CTRL = 1) 0 : disable at the same time 1 : contrary to the startup timing (first_on-last_off)
[5:4]	R/W	SHDN_DLYTIME	00	Shutdown delay time after send the PWRON key-press-forced-shutdown IRQ (when IRQ is disable, there is no delay) 00: 0ms (default) 01 : 100ms 10 : 500ms 11 : 1s

Bit	Mode	Name	Reset Value	Description
3	R/W	STANDBY_OFF	1	Standby off control (0 : off at the same time, 1 : off sequentially)
[2:1]	R/W	StandBy_EN [1:0]	00	Standby En/Disable and each power re-startup interval time 00 : standby mode disable 01 : enable and 1ms 10 : enable and 2ms 11 : enable and 4ms
0	R/W	STB_Trigger	0	0 : normal operation 1 : Standby Mode control. From low to high will trigger standby mode and from high to low will leave standby mode.

Name		Function	Addr	Reset
SHDN Off Enable Setting1		SHDN Off Enable Setting1	0x54	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	BCK1LV_ENSHDN	0	Buck1 output voltage low SHDN 0 : disable this event. 1 : enable this event.
6	R/W	BCK2LV_ENSHDN	0	Buck2 output voltage low SHDN 0 : disable this event. 1 : enable this event.
5	R/W	BCK3LV_ENSHDN	0	Buck3 output voltage low SHDN 0 : disable this event. 1 : enable this event.
4	R/W	BCK4LV_ENSHDN	0	Buck3 output voltage low SHDN 0 : disable this event. 1 : enable this event.
3	R/W	LDO1LV_ENSHDN	0	LDO1 output voltage low SHDN 0 : disable this event. 1 : enable this event.
2	R/W	LDO2LV_ENSHDN	0	LDO2 output voltage low SHDN 0 : disable this event. 1 : enable this event.
1	R/W	LDO3LV_ENSHDN	0	LDO3 output voltage low SHDN 0 : disable this event. 1 : enable this event.
0	R/W	LDO4LV_ENSHDN	0	LDO4 output voltage low SHDN 0 : disable this event. 1 : enable this event.

Name		Function	Addr	Reset
SHDN Off Enable Setting2		SHDN Off Enable Setting2	0x55	0X06
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	LSW2LV_ENSHDN	0	LSW2 output voltage low SHDN 0 : disable this event. 1 : enable this event.
6	R/W	LSW1LV_ENSHDN	0	LSW1 output voltage low SHDN 0 : disable this event. 1 : enable this event.
5	R/W	VSYSLV_ENSHDN	0	VSYS low SHDN 0 : disable this event. 1 : enable this event.
[4:3]	R/W	Reserved	00	Reserved
2	R/W	PWRON_ENSHDN	1	PWRON key-pressed forced SHDN 0 : disable this event. 1 : enable this event.
1	R/W	OT_ENSHDN	1	Over temperature SHDN 0 : disable this event. 1 : enable this event.
0	R/W	VDDALV_ENSHDN	0	VDDA voltage low SHDN 0 : disable this event. 1 : enable this event.

Name		Function	Addr	Reset
OFF/ON Event		OFF/ON Event	0x56	0XF0
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:4]	R	OFF_Event	1111	Powered off because of (Only shows last power-off event) 0000 : VDDA voltage low (VOFF) (Set by reg) 0001 : Buck1 output voltage low 0010 : Buck2 output voltage low 0011 : Buck3 output voltage low 0100 : Buck4 output voltage low 0101 : PWRON key-pressed forced shutdown 0110 : Power Off register setting 0111 : Over temperature event 1000 : from RESETB pin event or PMIC booting unsuccessfully 1001: LDO1 output voltage low 1010: LDO2 output voltage low 1011: LDO3 output voltage low 1100: LDO4 output voltage low 1101: LSW2 output voltage low 1110: LSW1 output voltage low 1111 : SYSLV

Bit	Mode	Name	Reset Value	Description
3	R	Reserved	0	Reserved
2	R	Standby Status	0	Show Standby Status : 0 : PMIC is not in standby mode 1: PMIC is in standby mode
[1:0]	R	ON_Event	00	Powered on because of (Only shows last power-on event) 00 : VIN Plug-in 01 : PWRON key 10 : RESET Delay1 OFF then Delay2 Power-on 11 : Reserved

Name		Function	Addr	Reset
Bucks/LDOs_IRQ		Bucks/LDOs_IRQ	0x57	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	BCK1LV_IRQ	0	Buck1 output voltage is lower than 66%, IRQ indicator.
6	R	BCK2LV_IRQ	0	Buck2 output voltage is lower than 66%, IRQ indicator.
5	R	BCK3LV_IRQ	0	Buck3 output voltage is lower than 66%, IRQ indicator.
4	R	BCK4LV_IRQ	0	Buck4 output voltage is lower than 66%, IRQ indicator.
3	R	LDO1LV_IRQ	0	LDO1 output voltage is lower than 50%, IRQ indicator.
2	R	LDO2LV_IRQ	0	LDO2 output voltage is lower than 50%, IRQ indicator.
1	R	LDO3LV_IRQ	0	LDO3 output voltage is lower than 50%, IRQ indicator.
0	R	LDO4LV_IRQ	0	LDO4 output voltage is lower than 50%, IRQ indicator.

Name		Function	Addr	Reset
LSWs/BASE_IRQ		LSWs/BASE_IRQ	0x58	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	LSW2LV_IRQ	0	LSW2 output voltage is lower than 66%, IRQ indicator.
6	R	LSW1LV_IRQ	0	LSW1 output voltage is lower than 66%, IRQ indicator.
5	R	PMICSYSLV_IRQ	0	PMIC VSYS voltage is lower than SYSLV setting, IRQ indicator.
[4:2]	R	Reversed	000	Reversed
1	R	OT_IRQ	0	Charger thermal shutdown fault. Set when the die temperature exceeds thermal shutdown threshold or PMIC Internal over-temperature was triggered, IRQ indicator.
0	R	VDDALV_IRQ	0	VDDA voltage is lower VDDAUVLO, IRQ indicator.

Name		Function	Addr	Reset
POWER_KEY_IRQ		POWER_KEY_IRQ	0x59	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	KPSHDN_IRQ	0	PWRON Key-press forced shutdown, IRQ indicator.
6	R	PWRONR_IRQ	0	PWRON Key-press rising edge, IRQ indicator.
5	R	PWRONF_IRQ	0	PWRON Key-press falling edge, IRQ indicator.
4	R	PWRONSP_IRQ	0	PWRON key short press, IRQ enable (32μs deglitch time)
3	R	PWRONLP_IRQ	0	PWRON key long press, IRQ enable (32μs deglitch time)
[2:0]	R	Reversed	000	Reversed

Name		Function	Addr	Reset
Bucks/LDOs _IRQ_Mask		Bucks/LDOs _IRQ_Mask	0x5A	0XFF
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	BCK1LVM	1	Buck1 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
6	R/W	BCK2LVM	1	Buck2 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
5	R/W	BCK3LVM	1	Buck3 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
4	R/W	BCK4LVM	1	Buck4 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
3	R/W	LDO1LVM	1	LDO1 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
2	R/W	LDO2LVM	1	LDO2 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
1	R/W	LDO3LVM	1	LDO3 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
0	R/W	LDO4LVM	1	LDO4 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.

Name		Function	Addr	Reset
LSWs/BASE _IRQ_Mask		Bucks/LDOs _IRQ_Mask	0x5B	0XE0
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	LSW2LVM	1	LSW2 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
6	R/W	LSW1LVM	1	LSW1 low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
5	R/W	PMICSYSLVM	1	PMIC VSYS low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
[4:2]	R/W	Reversed	000	Reversed
1	R/W	OTM	0	Over Temperature protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
0	R/W	VDDALVM	0	VDDA low voltage protection interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.

Name		Function	Addr	Reset
POWER_KEY _IRQ_Mask		POWER_KEY _IRQ_Mask	0x5C	0X78
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	KPSHDN _IRQM	0	PWRON Key-press forced shutdown interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
6	R/W	PWRONR _IRQM	1	PWRON Key-press rising edge, IRQ interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
5	R/W	PWRONF _IRQM	1	PWRON Key-press falling edge, IRQ interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
4	R/W	PWRONSP _IRQM	1	PWRON key short press, IRQ interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
3	R/W	PWRONLP _IRQM	1	PWRON key long press, IRQ interrupt mask. 0 – Interrupt is not masked. 1 – Interrupt is masked.
[2:0]	R/W	Reversed	000	Reversed

Name		Function	Addr	Reset
Buck Syn-Clock Syn-Clock Frequency Control		Buck Syn-Clock Syn-Clock Frequency Control	0x65	0x40
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:5]	R/W	VSYSUVLO[2:0]	010	VSYS UVLO 2.8~3.5V per 0.1V (Falling threshold with hysteresis of 300mV) 000 – 2.8V 001 – 2.9V 010 – 3.0V (default) 011 – 3.1V 100 – 3.2V 101 – 3.3V 110 – 3.4V 110 – 3.5V
[4:1]	R/W	Reversed	0000	Reversed
0	R/W	1.5/3.0MHz	0	Select Buck Syn-Clock Syn-Clock Frequency 0:1.5MHz 1:30MHz

Name		Function	Addr	Reset
LSW2 control Normal		LSW2 Output Control	0x80	0x64
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LSW2 Output_N[6:0]	1100100	LSW2 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 – Full On

Name		Function	Addr	Reset
LSW2 control Standby		LSW2 Output Control	0x82	0x58
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LSW2 Output_S [6:0]	1011000	LSW2 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 – Full On

Name		Function	Addr	Reset
LSW1 control Normal		LSW1 Output Control	0x81	0x64
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LSW1 Output_N[6:0]	1100100	LSW1 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 – Full On

Name		Function	Addr	Reset
LSW1 control Standby		LSW1 Output Control	0x83	0x7F
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	Reversed	0	Reversed
[6:0]	R/W	LSW1 Output_S [6:0]	1111111	LSW1 output voltage regulation (default by OTP) 0000000 – 0.8V, 25mV per step 0000001 – 0.825V -- 0010000 – 1.2V -- 0011100 – 1.5V. -- 1100101 – 3.3V 1111110 – 3.3V 1111111 – Full On

Name		Function	Addr	Reset
LSW VRC Control		LSW VRC Control	0x84	Option
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	LSW2 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[5:4]	R/W	LSW1 VRC_N[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[3:2]	R/W	LSW2 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,
[1:0]	R/W	LSW1 VRC_S[1:0]	00	VRC Setting 00 – 25mV/10μs, 01 – 50mV/10μs, 10 – 75mV/10μs, 11 – 100mV/10μs,

Name		Function	Addr	Reset
LSW VRC Enable		LSW VRC Enable	0x85	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	LSW2VRC_EN_N	0	LSW2 VRC in Normal Mode 0 – disable – voltage ramps up to target voltage with one time 1 – enable – voltage ramps up to target voltage with slope control
6	R/W	LSW1VRC_EN_N	0	LSW1 VRC in Normal Mode 0 – disable – voltage ramps up to target voltage with one time 1 – enable – voltage ramps up to target voltage with slope control
[5:4]	R/W	Reserved	00	Reserved
3	R/W	LSW2VRC_EN_S	0	LSW2 VRC in Standby Mode 0 – disable – voltage ramps up to target voltage with one time 1 – enable – voltage ramps up to target voltage with slope control
2	R/W	LSW1VRC_EN_S	0	LSW1 VRC in Standby Mode 0 – disable – voltage ramps up to target voltage with one time 1 – enable – voltage ramps up to target voltage with slope control
[1:0]	R/W	Reserved	00	Reserved

Name		Function	Addr	Reset
RTCADJ		RTC Frequency Adjust	0x90	0XBC
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	RTC_EN	1	Enable RTC 0 – RTC disabled 1 – RTC enabled
[6:0]	R/W	RTCADJ[6:0]	0111100	finely tune the RTC time counting Frequency by adjusting (RTCAJ - ? 60)/2 ppm. Hence, the tuning range is - 30ppm to 33ppm.

Name		Function	Addr	Reset
RTCT_SEC		RTC Timing_SEC	0x91	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	BUSY	0	1 : RTC is busy, and the writing access is not allowed
6	R	Reversed	0	Reversed
[5:0]	R/W	RTCT_SEC[5:0]	00000	Stores the SECOND field of RTC time. That is 0 to 59.

Name		Function	Addr	Reset
RTCT_MINUTE		RTC Timing_MINUTE	0x92	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Reversed	00	Reversed
[5:0]	R/W	RTCT_MIN[5:0]	00000	Stores the MINUTE field of RTC time. That is 0 to 59.

Name		Function	Addr	Reset
RTCT_HOUR		RTC Timing_HOUR	0x93	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	12/24hours	0	12hours/24hours selection. 0 – 24hours. 1 – 12 hours.
6	R/W	AM/PM	0	AM/PM selection. 0 – AM 1 –PM If the 24hours is selected, user can't set this bit.
5	R/W	Reversed	0	
[4:0]	R/W	RTCT_HOUR[4:0]	00000	Stores the HOUR field of RTC time. That is 0 to 23 (24hour format).

Name		Function	Addr	Reset
RTCT_YEAR		RTC YEAR	0x94	0X0D
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Reversed	00	Reversed
[5:0]	R/W	RTCT_ YEAR [5:0]	0001101	Stores the YEAR field of RTC time. That is 0 to 63. RTCT_ YEAR [5:0] = 0 means 2000.

Name		Function	Addr	Reset
RTCT_MONTH		RTCT_MONTH	0x95	0X01
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:4]	R/W	Reversed	0000	Reversed
[3:0]	R/W	RTCT_MON[3:0]	0001	Stores the MONTH field of RTC time. That is 1 to 12. RTCT_MON = 1 means January.

Name		Function	Addr	Reset
RTC DATE/WEEK		RTC DATE/WEEK	0x96	0X41
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:5]	R/W	RTCT_WEEK[2:0]	010	Stores the DAY-of-WEEK field of RTC time. That is 0 to 6. RTCT_WEK = 0 means Sunday. RTCT_WEK = 1 means Monday. RT5036 cannot calculate automatically the field based on other fields. (YEAR, MONTH,DATE).
[4:0]	R/W	RTCT_DAY[4:0]	00001	Stores the DATE field of RTC time. That is 1 to 31.

Name		Function	Addr	Reset
STB Mode_Setting		Standby(STB) Mode Setting	0x97	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:1]	R/W	Reversed	0000000	Reversed
0	R/W	STB_CTRL	0	STB_CTRL = 0 means count down (CD) mode. STB_CTRL = 1 means clock alarm (Alarm) mode.

Name		Function	Addr	Reset
STB_Alarm_SEC		STB_Alarm_SEC	0x98	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Reversed	00	Reversed
[5:0]	R/W	STB_Alarm_ SEC[5:0]	00000	Stores the SECOND field of standby alarm time. That is 0 to 59.

Name		Function	Addr	Reset
STB_Alarm _MINUTE		STB_Alarm_MINUTE	0x99	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Reversed	00	Reversed
[5:0]	R/W	STB_Alarm_MIN[5:0]	00000	Stores the MINUTE field of standby alarm time. That is 0 to 59.

Name		Function	Addr	Reset
STB_Alarm_HOUR		STB_Alarm_HOUR	0x9A	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	STB_Alarm_12/24hours	0	12hours/24hours selection. 0 – 24hours. 1 – 12 hours.
6	R/W	STB_Alarm_AM/PM	0	AM/PM selection. 0 – AM 1 –PM If the 24hours is selected, user can't set this bit.
5	R/W	Reversed	0	Reversed.
[4:0]	R/W	STB_Alarm_HOUR[4:0]	0000	Stores the HOUR field of standby alarm time. That is 0 to 23 (24hour format).

Name		Function	Addr	Reset
STB_Alarm_YEAR		STB_Alarm_ YEAR	0x9B	0X0D
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Reversed	00	Reversed
[5:0]	R/W	STB_Alarm_YEAR[5:0]	001101	Stores the YEAR field of standby alarm time. That is 0 to 63. STB_Alarm_YEAR = 0 means the year 2000. Hence, RT5036 can setting maximum year is 2063.

Name		Function	Addr	Reset
STB_Alarm_MONTH		STB_Alarm_MONTH	0x9C	0X01
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:4]	R/W	Reversed	0000	Reversed
[3:0]	R/W	STB_Alarm_MON[3:0]	0001	Stores the MONTH field of standby alarm time. That is 1 to 12. STB_Alarm_MON = 1 means January.

Name		Function	Addr	Reset
STB_Alarm_DAY		STB_Alarm_ DAY	0x9D	0X01
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:5]	R	Reversed	00	Reversed
[4:0]	R/W	STB_Alarm_DAY[4:0]	0001	Stores the DATE field of standby alarm time. That is 1 to 31, depending on the month. STB_Alarm_DAY [4:0] = 1 means 1st day of each month. RT5036 supports leap year counting.

Name		Function	Addr	Reset
STB_CD_SEC		STB_CD_SEC	0x9E	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Reversed	00	Reversed
[5:0]	R/W	STB_CD_SEC[5:0]	00000	Stores the SECOND field of standby count down time. That is 0 to 59.

Name		Function	Addr	Reset
STB_CD_MINUTE		STB_CD_MINUTE	0x9F	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:6]	R/W	Reversed	00	Reversed
[5:0]	R/W	STB_CD_MIN[5:0]	00000	Stores the MINUTE field of standby count down time. That is 0 to 59.

Name		Function	Addr	Reset
STB_CD_HOUR		STB_CD_HOUR	0xA0	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	STB_CD_12/24hours	0	12hours/24hours selection. 0 – 24hours. 1 – 12 hours.
6	R/W	STB_CD_AM/PM	0	AM/PM selection. 0 – AM 1 –PM If the 24hours is selected, user can't set this bit.
5	R/W	Reversed	0	Reversed
[4:0]	R/W	STB_CD_HOUR[4:0]	0000	Stores the HOUR field of standby count down time. That is 0 to 23 (24hour format).

Name		Function	Addr	Reset
STB_CD_DATE_L		STB_CD_DATE_L	0xA1	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:0]	R/W	STB_CD_DAY[7:0]	00000000	The low byte of day down counter

Name		Function	Addr	Reset
STB_CD_DAY_H		STB_CD_DAY_H	0xA2	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:4]	R/W	Reversed	0000	Reversed
[3:0]	R/W	STB_CD_ DAY [11:8]	0000	The high byte of day down counter

Name		Function	Addr	Reset
STB_WKUP_IRQ		Standby WakeUp_IRQ	0xA4	0X00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:2]	R	Reversed	000000	Reversed
1	R	CD_IRQ	0	Standby mode wakes up by count down (CD) IRQ indicator.
0	R	CA_IRQ	0	Standby mode wakes up by clock alarm (CA) IRQ indicator.

Name		Function	Addr	Reset
STB_WKUP_Mask		Standby WakeUp _IRQ _Mask	0xA5	0X03
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:2]	R/W	Reversed	000000	Reversed
1	R/W	CDM	1	Standby mode wakes up by count down interrupt mask. 0 – interrupt is not masked. 1 – Interrupt is masked.
0	R/W	CAM	1	Standby mode wakes up by clock alarm interrupt mask. 0 – interrupt is not masked. 1 – Interrupt is masked.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.5°C/W) = 3.63W for WQFN-40L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

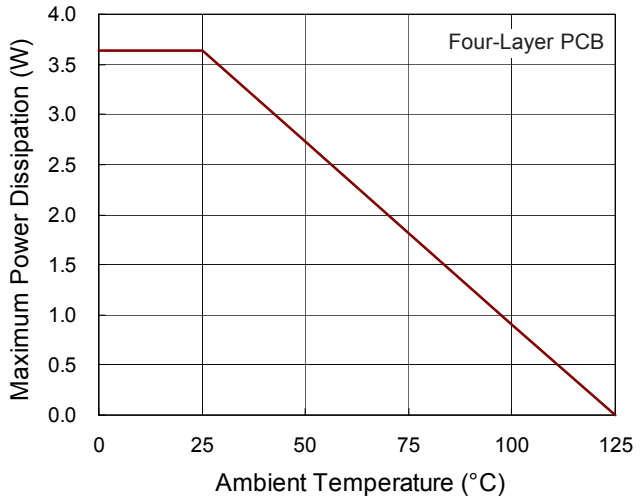


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

Some PCB layout guidelines for optimal performance of RT5036 list as following. Following figure shows the real PCB layout considerations and it is based on the real component size whose unit is millimeter (mm).

- Place the input and output capacitors as close to the input and output pins as possible.
- Keep the main power traces as wide and short as possible.
- The output inductor and bootstrap capacitor should be placed close to the chip and LXCHG pins.
- The battery voltage sensing point should be placed after the output capacitor, and kept wide for maximum pre-charge current.
- To optimize current sense accuracy, connect the traces to RSENSE with Kelvin sense connection.
- Put the input capacitor as close as possible to the device pins.
- LXB1 to LXB4 node is with high frequency voltage swing and should be kept small area. Keep analog components away from LXB1 to LXB4 node to prevent stray capacitive noise pick-up.
- Connect VOUTSB1 to VOUTSB4 pin network behind the output capacitors.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.

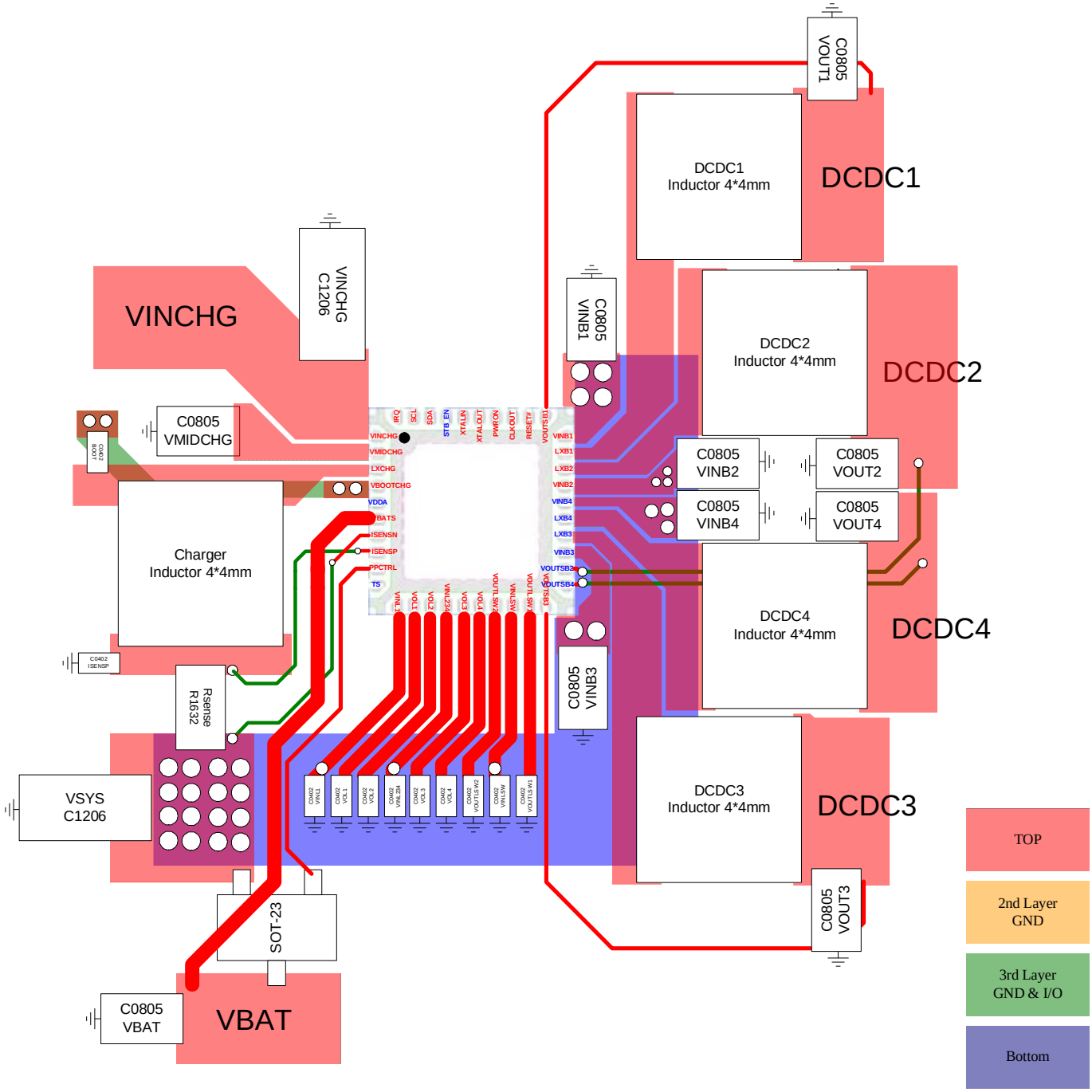
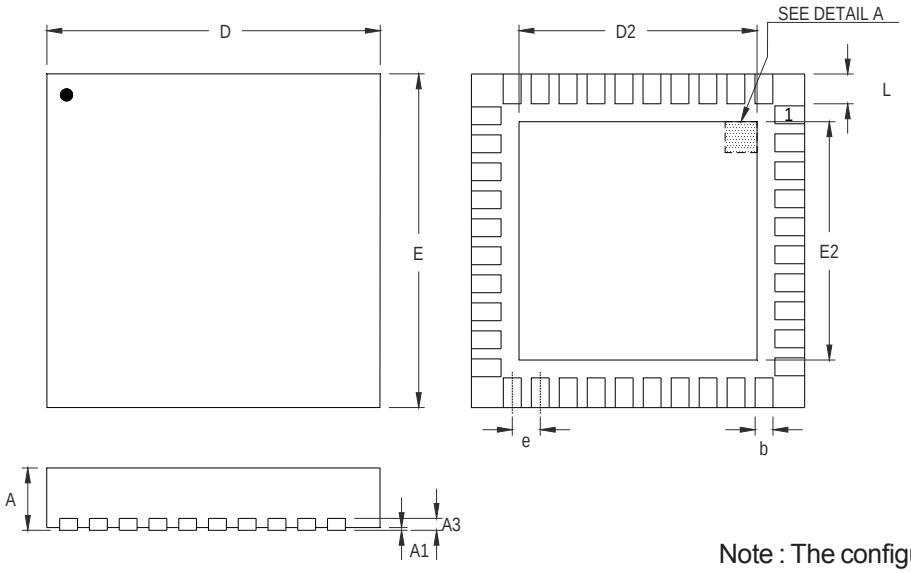
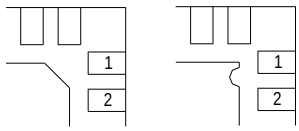


Figure 4. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

Datasheet Revision History

Version	Date	Item	Description
P00	2014/1/21		First Edition
P01	2014/3/6	Functional Pin Description Typical Application Circuit Application Information I²C Registers Table	Modify
P02	2014/3/25	I²C Registers Table	Modify
P03	2014/6/9	General Description Features Power Channel Flow Chart Electrical Characteristics Typical Application Circuit I²C Registers Table	Modify
P04	2014/7/31	Features Electrical Characteristics Application Information	Modify
P05	2014/8/14	I²C Registers Table	
P06	2015/1/6	Typical Operating Characteristics	Modify Add Typical Operating Characteristics (from RT5037_RK-P01)

单击下面可查看定价，库存，交付和生命周期等信息

>>Richtek(台湾立锜)