

1.5MHz, 1A, High Efficiency PWM Step-Down DC/DC Converter

General Description

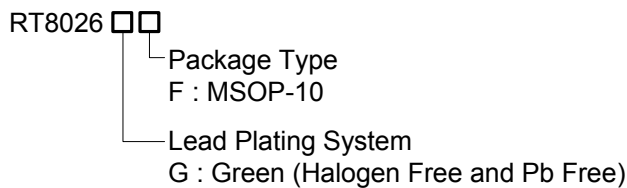
The RT8026 is a high-efficiency Pulse-Width-Modulated (PWM) step-down DC/DC converter. Capable of delivering 1A output current over a wide input voltage range from 2.7V to 5.5V, the RT8026 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources such as cellular phones, PDAs and hand-held devices.

Two operating modes are available including : PWM/Low-Dropout autoswitch and shut-down modes. The Internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical application.

The RT8026 enters Low-Dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper P-MOSFET. The RT8026 enter shut-down mode and consumes less than 0.1 μ A when the EN pin is pulled low.

The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operating frequency of 1.5MHz. This along with small MSOP-10 package provides small PCB area application. Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

Ordering Information



Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

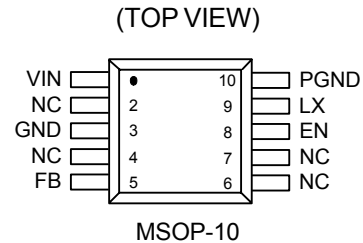
Features

- Input Voltage Range : 2.7V to 5.5V
- Adjustable Output Voltage : 1V to V_{IN}
- Output Current : 1A
- High Efficiency : up to 95%
- No Schottky Diode Required
- 1.5MHz Fixed Frequency PWM Operation
- Current Limiting Protection
- Thermal Shutdown Protection
- Small MSOP-10 Package
- RoHS Compliant and Halogen Free

Applications

- Mobile Phones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Portable Instruments

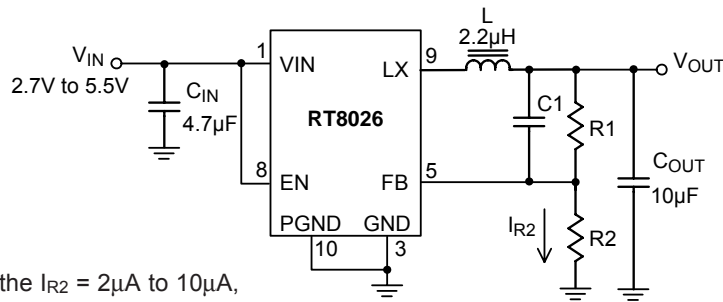
Pin Configurations



Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Typical Application Circuit



$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

with R2 = 300kΩ to 60kΩ so the IR2 = 2µA to 10µA,

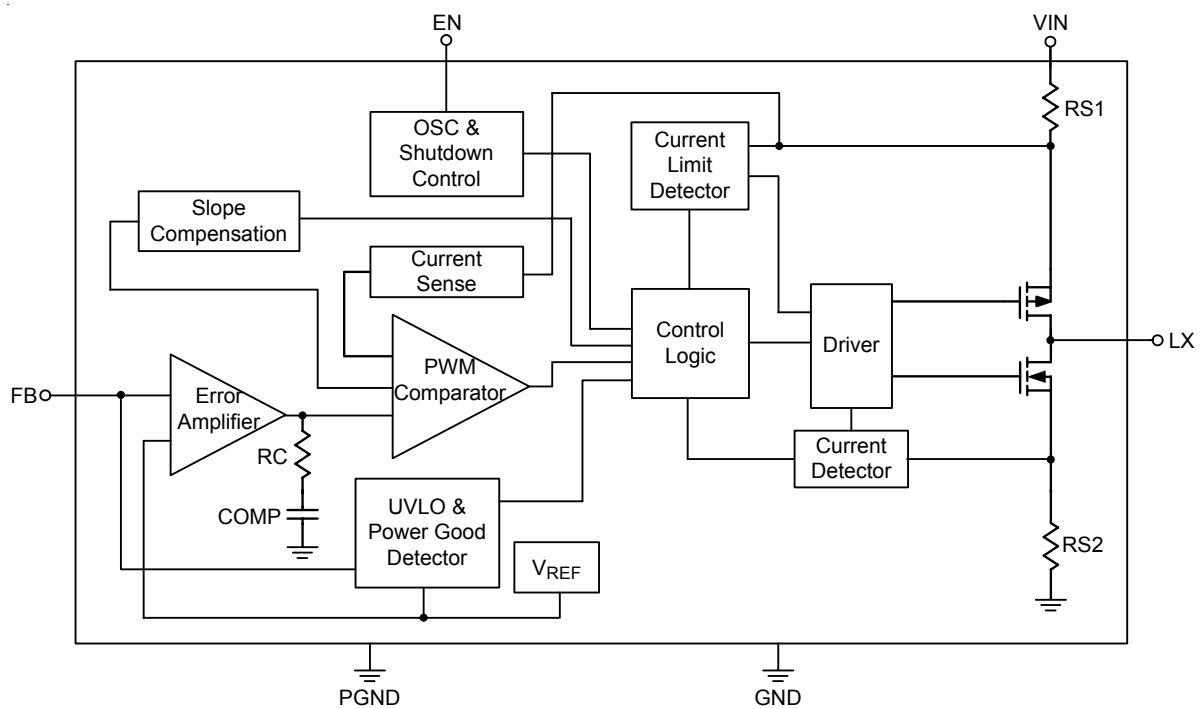
and (R1 x C1) should be in the range between 3x10⁻⁶ and 6x10⁻⁶ for component selection.

Figure 1. Typical Application Circuit for RT8026

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Power Input.
2, 4, 6, 7	NC	No Internal Connection.
3	GND	Ground Pin.
5	FB	Feedback Input Pin. Receives the feedback voltage from a resistive divider connected across the output.
8	EN	Chip Enable (Active High). It is recommended to add a 100kΩ resistor between EN and GND pin.
9	LX	Pin for Switching. Connect this pin to the inductor.
10	PGND	Power Ground Pin.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ----- 6.5V
- EN, FB Pin Voltage ----- -0.3V to V_{IN}
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 MSOP-10 ----- 833mW
- Package Thermal Resistance (Note 2)
 MSOP-10, θ_{JA} ----- 120°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- Junction Temperature ----- 150°C
- ESD Susceptibility (Note 3)
 HBM (Human Body Mode) ----- 2kV
 MM (Machine Mode) ----- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ----- 2.7V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{IN} = 3.6\text{V}$, $V_{OUT} = 2.5\text{V}$, $V_{REF} = 0.6\text{V}$, $L = 2.2\mu\text{H}$, $C_{IN} = 4.7\mu\text{F}$, $C_{OUT} = 10\mu\text{F}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current	I_Q	$I_{OUT} = 0\text{mA}$, $V_{FB} = V_{REF} + 5\%$	–	50	70	μA
Shutdown Current	I_{SHDN}	EN = GND	–	0.1	1	μA
Reference Voltage	V_{REF}	For Adjustable Output Voltage	0.588	0.6	0.612	V
Adjustable Output Range	V_{OUT}	(Note 6)	1	--	$V_{IN} - 0.2\text{V}$	V
Output Voltage Accuracy	ΔV_{OUT}	$V_{IN} = V_{OUT} + \Delta V$ to 5.5V $0\text{A} < I_{OUT} < 1\text{A}$ (Note 5)	-3	--	+3	%
FB Input Current	I_{FB}	$V_{FB} = V_{IN}$	-50	--	50	nA
PMOSFET R_{ON}	$R_{DS(ON)_P}$	$I_{OUT} = 200\text{mA}$, $V_{IN} = 3.6\text{V}$	–	0.28	--	Ω
NMOSFET R_{ON}	$R_{DS(ON)_N}$	$I_{OUT} = 200\text{mA}$, $V_{IN} = 3.6\text{V}$	–	0.25	--	Ω
P-Channel Current Limit	I_{LIM_P}	$V_{IN} = 2.7\text{V}$ to 5.5 V	1.2	1.5	--	A
EN High-Level Input Voltage	V_{EN_H}	$V_{IN} = 2.7\text{V}$ to 5.5V	1.5	--	--	V
EN Low-Level Input Voltage	V_{EN_L}	$V_{IN} = 2.7\text{V}$ to 5.5V	–	--	0.4	V
Under Voltage Lock Out threshold	UVLO		–	1.8	--	V
UVLO Hysteresis			–	0.1	--	V
Oscillator Frequency	f_{OSC}	$V_{IN} = 3.6\text{V}$, $I_{OUT} = 100\text{mA}$	1.2	1.5	1.8	MHz
Thermal Shutdown Temperature	TSD		–	160	--	$^\circ\text{C}$
Max. Duty Cycle			100	--	--	%

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

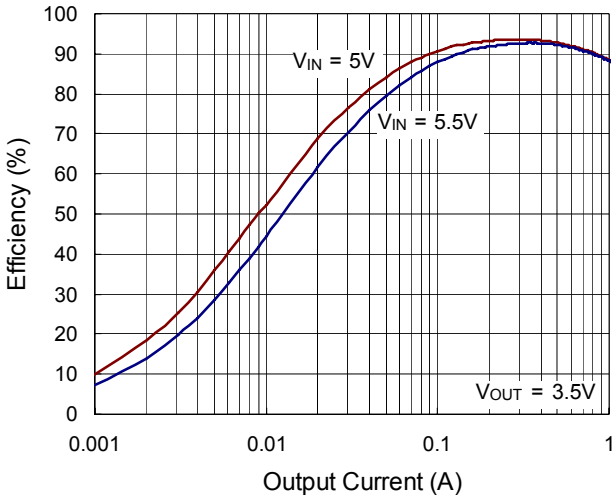
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. $\Delta V = I_{OUT} \times P_{RDS(ON)}$

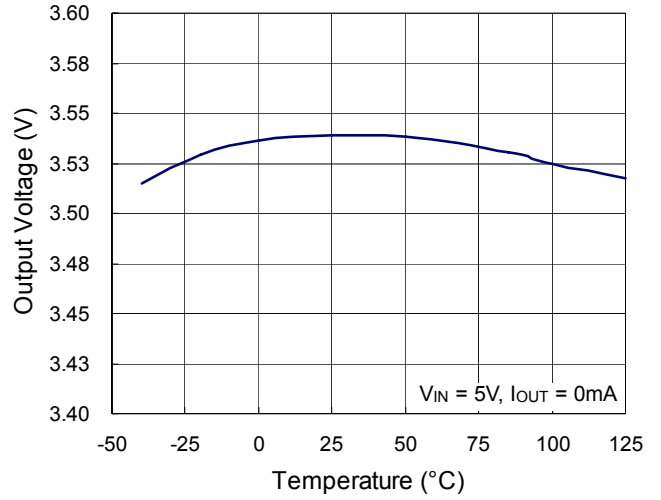
Note 6. Guarantee by design.

Typical Operating Characteristics

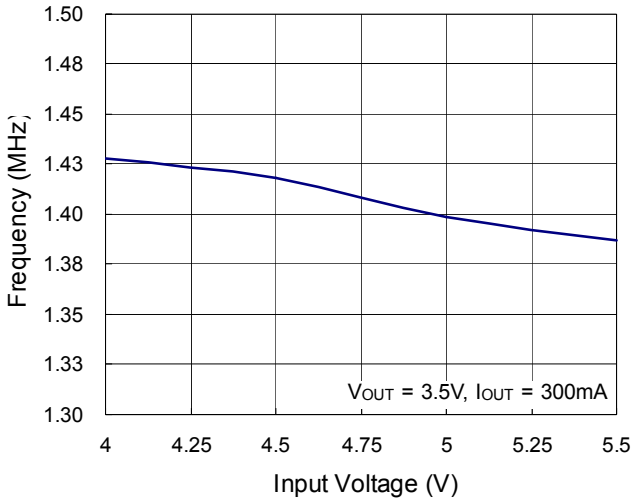
Efficiency vs. Output Current



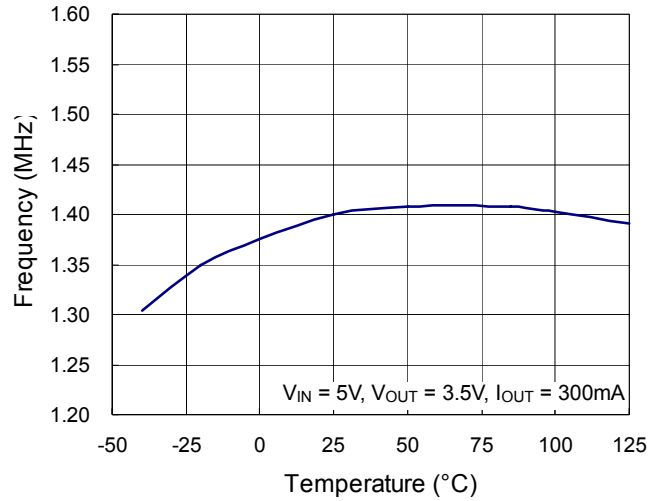
Output Voltage vs. Temperature



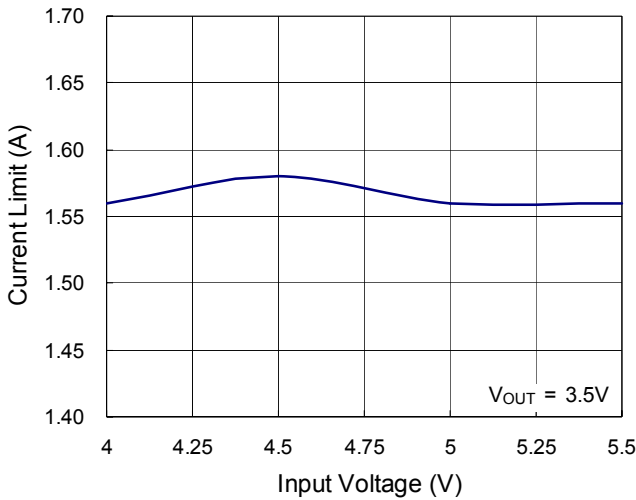
Frequency vs. Input Voltage



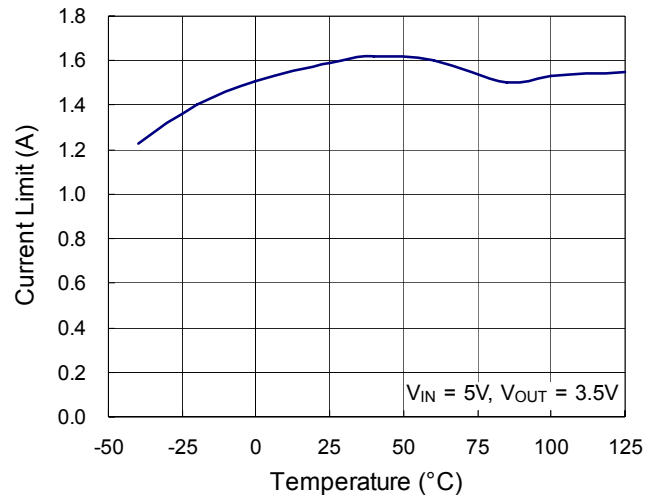
Frequency vs. Temperature



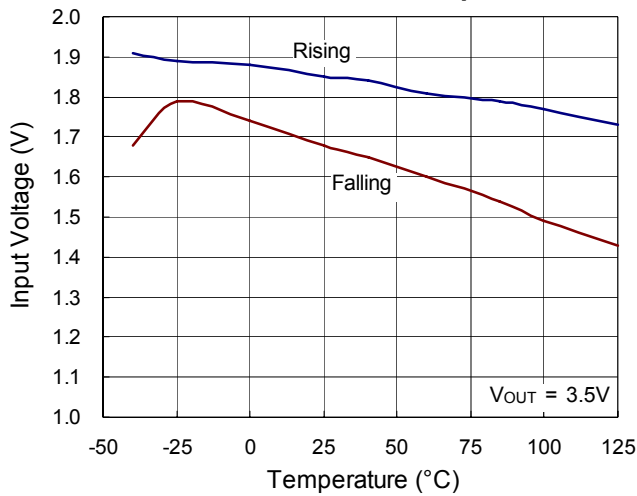
Current Limit vs. Input Voltage



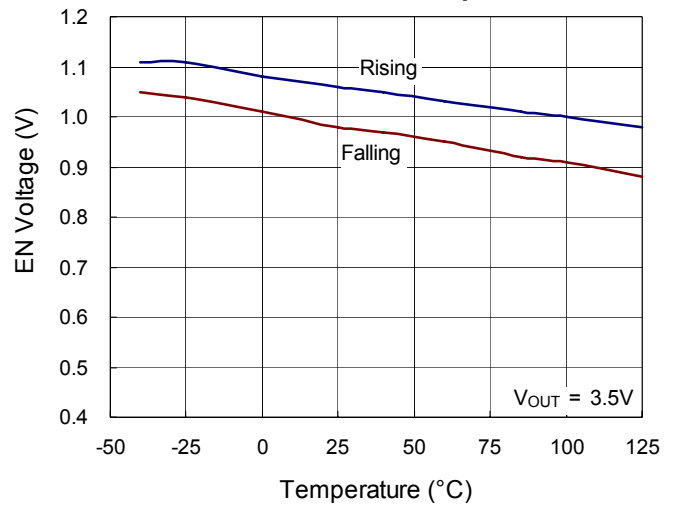
Current Limit vs. Temperature



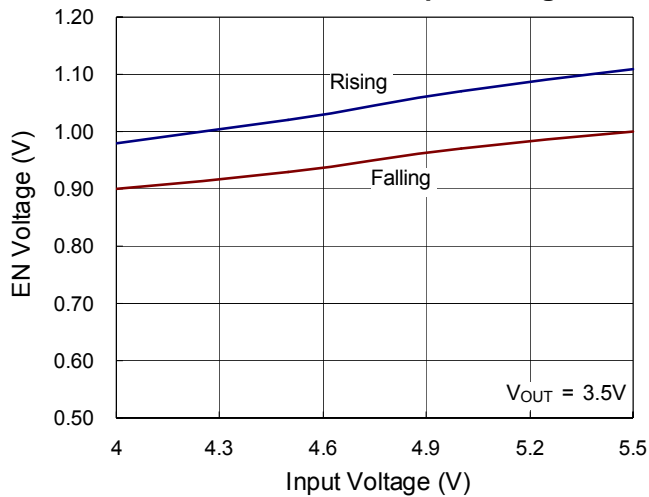
UVLO Threshold vs. Temperature



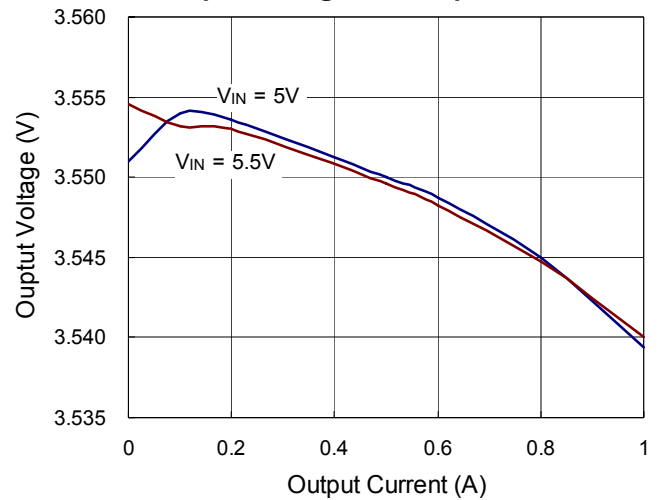
EN Threshold vs. Temperature



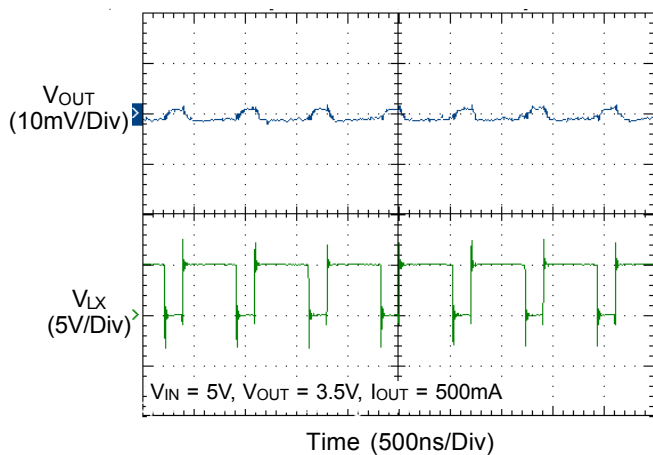
EN Threshold vs. Input Voltage



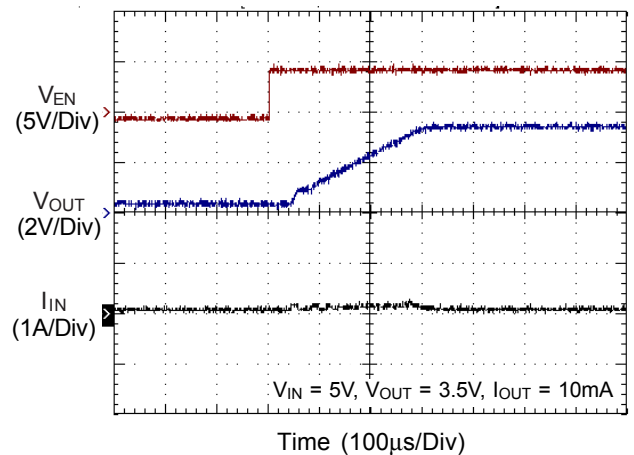
Output Voltage vs. Output Current



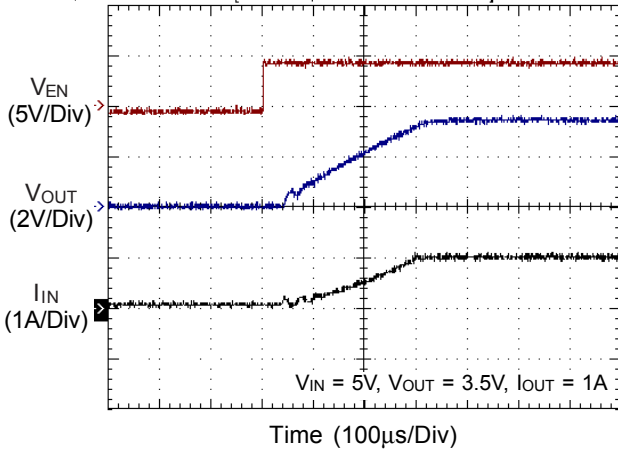
Output Ripple



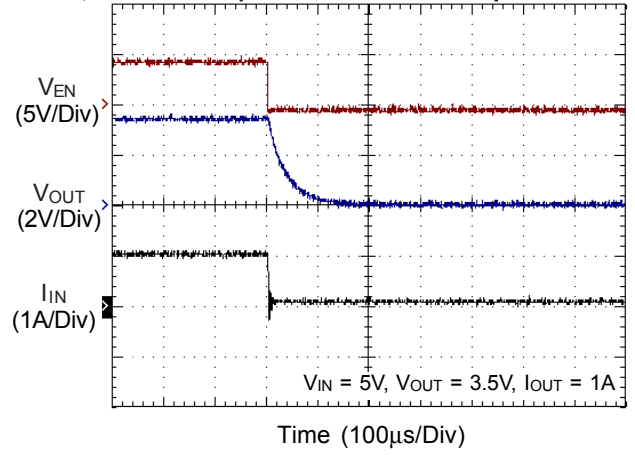
Power On from EN



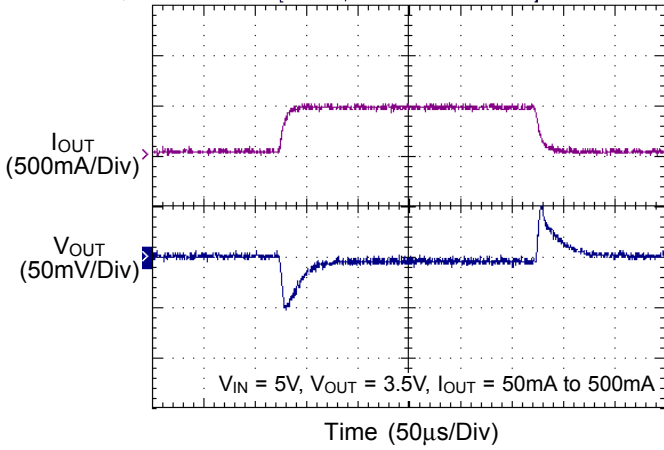
Power On from EN



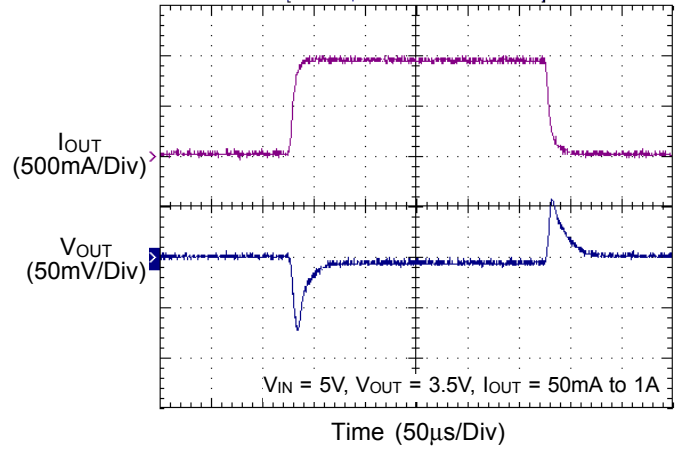
Power Off from EN



Load Transient Response



Load Transient Response



Applications Information

The basic RT8026 application circuit is shown in the Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT} .

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L} \right] \left[1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN} . To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_L(MAX)} \right] \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in

inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs. size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN} , is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT} , is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance

density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The resistive divider allows the V_{FB} pin to sense a fraction of the output voltage as shown in Figure 2.

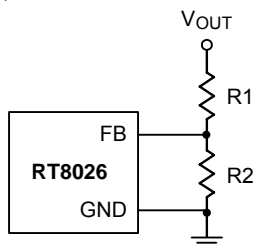


Figure 2. Setting the Output Voltage

For adjustable output voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \left(1 + \frac{R1}{R2} \right)$$

where V_{REF} is the feedback reference voltage (0.6V typ.).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as :

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$$

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses : V_{IN} quiescent current and I²R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I²R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current is due to two components : the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{IN} to ground.

The resulting ΔQ/Δt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode,

$$I_{GATECHG} = f(Q_T + Q_B)$$

where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge

losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L . In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows :

$$R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8026, the maximum junction temperature is 125°C . The junction to ambient thermal resistance θ_{JA} is layout dependent. For MSOP-10 packages, the thermal resistance θ_{JA} is 120°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (120^\circ\text{C/W}) = 0.833\text{W for MSOP-10 packages}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} . For RT8026 packages, the Figure 3 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

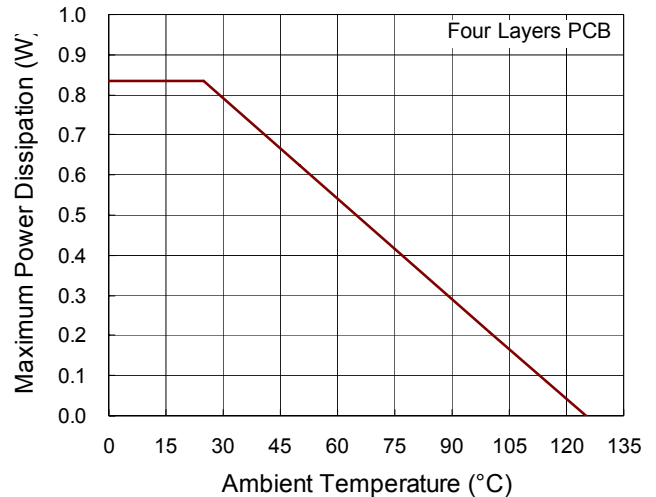
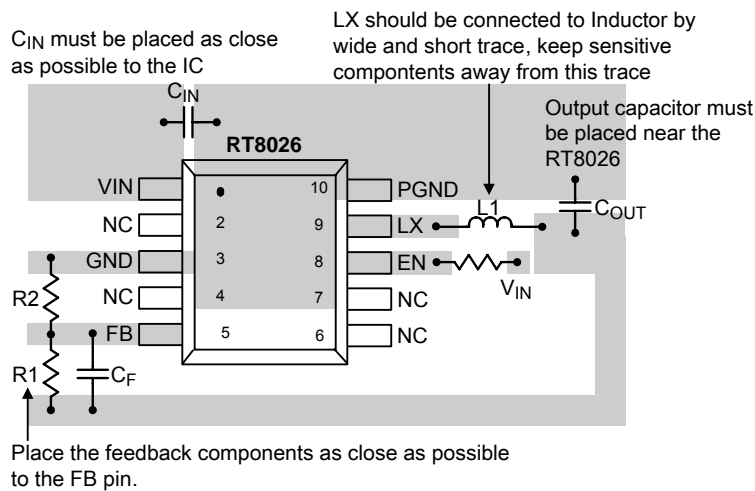


Figure 3. Derating Curves for RT8026 Packages

Layout Considerations

For the best performance of the RT8026, the following guidelines must be strictly followed.

- ▶ The input capacitor should be placed as close as possible to the device pins (V_{IN} and GND).
- ▶ The LX node is with high frequency voltage swing. It should be kept at a small area.
- ▶ Place the feedback components as close as possible to the IC and keep away from the noisy devices.
- ▶ The GND and PGND should be connected to a strong ground plane for heat sinking and noise protection.



Layout note:

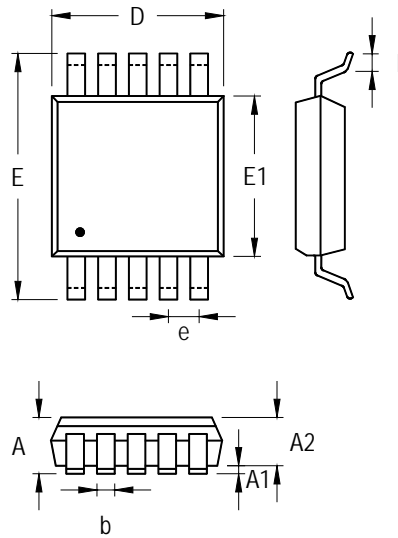
1. The distance that C_{IN} connects to V_{IN} is as close as possible (Under 2mm).
2. C_{OUT} should be placed near the RT8026.

Figure 4. Layout Guide

Table 1. Recommended Components for Different Output Voltage Application

Component Supplier	L1 (μH)	C_{OUT} (μF)	R1 ($\text{k}\Omega$)	R2 ($\text{k}\Omega$)	V_{OUT} (V)
TAIYO YUDEN	10	10	300	62	3.5
TAIYO YUDEN	10	10	120	27	3.3
GOTREND	2.2	10	200	62	2.5
GOTREND	2.2	10	150	75	1.8
GOTREND	2.2	10	100	100	1.2

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.810	1.100	0.032	0.043
A1	0.000	0.150	0.000	0.006
A2	0.750	0.950	0.030	0.037
b	0.170	0.270	0.007	0.011
D	2.900	3.100	0.114	0.122
e	0.500		0.020	
E	4.800	5.000	0.189	0.197
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031

10-Lead MSOP Plastic Package

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