Single Synchronous Buck PWM Controller with LDO Regulator

General Description

The RT8234A is a cost effective synchronous buck controller with an integrated 3A linear regulator. The PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage supplies in notebook computers.

The constant on-time PWM control scheme handles wide input/output voltage ratios with ease and provides "instant-on" response to load transients while maintaining a relatively constant switching frequency. The Ultra Sonic Mode (USM) setting maintains the switching frequency above 30kHz, which eliminates noise in audio applications.

The RT8234A is intended for CPU core, chipset, DRAM, or other low voltage supplies as low as 0.75V at a reduced cost without the need for a current sense resistor.

The 3A LDO regulator maintains fast transient response, only requiring a 20µF ceramic output capacitor. In addition, the LDO supply input is provided by an external power source to significantly reduce the total power loss. The RT8234A is available in a WQFN-16L 3x3 package.

Ordering Information

RT8234A□□

- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)

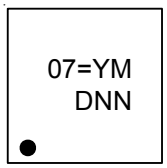
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

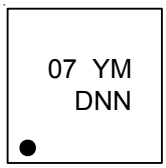
Marking Information

RT8234AGQW



07=: Product Code
YMDNN : Date Code

RT8234AZQW



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Features

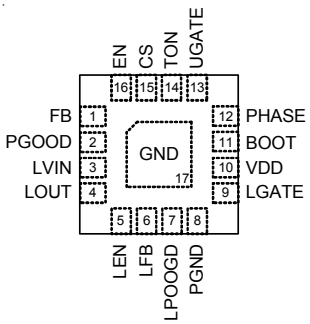
- **PWM Controller**
  - **Wide Input Voltage Range : 4.5V to 26V**
  - **Adjustable Output Voltage Range : 0. 75V to 3.3V**
  - **Resistor Programmable Current Limit**
  - **Quick Load Step Response within 100ns**
  - **1% V_{OUT} Accuracy Over Line and Load**
  - **Resistor Programmable Frequency**
  - **Over/Under Voltage Protection**
  - **Linear Current Limit Soft-Start**
  - **Drives Large Synchronous Rectifier FETs**
  - **Power Good Indicator**
- **LDO Regulator**
  - **Output Current Up to 3A**
  - **1% Accuracy Over Line and Load**
  - **Adjustable Output Voltage Down to 0.75V**
  - **Independent Enable and Power Good Indicator**
- **RoHS Compliant and 100% Halogen Free**

Applications

- Notebook Computers
- CPU Core Supply
- Chipset/RAM Supply as Low as 0.75V

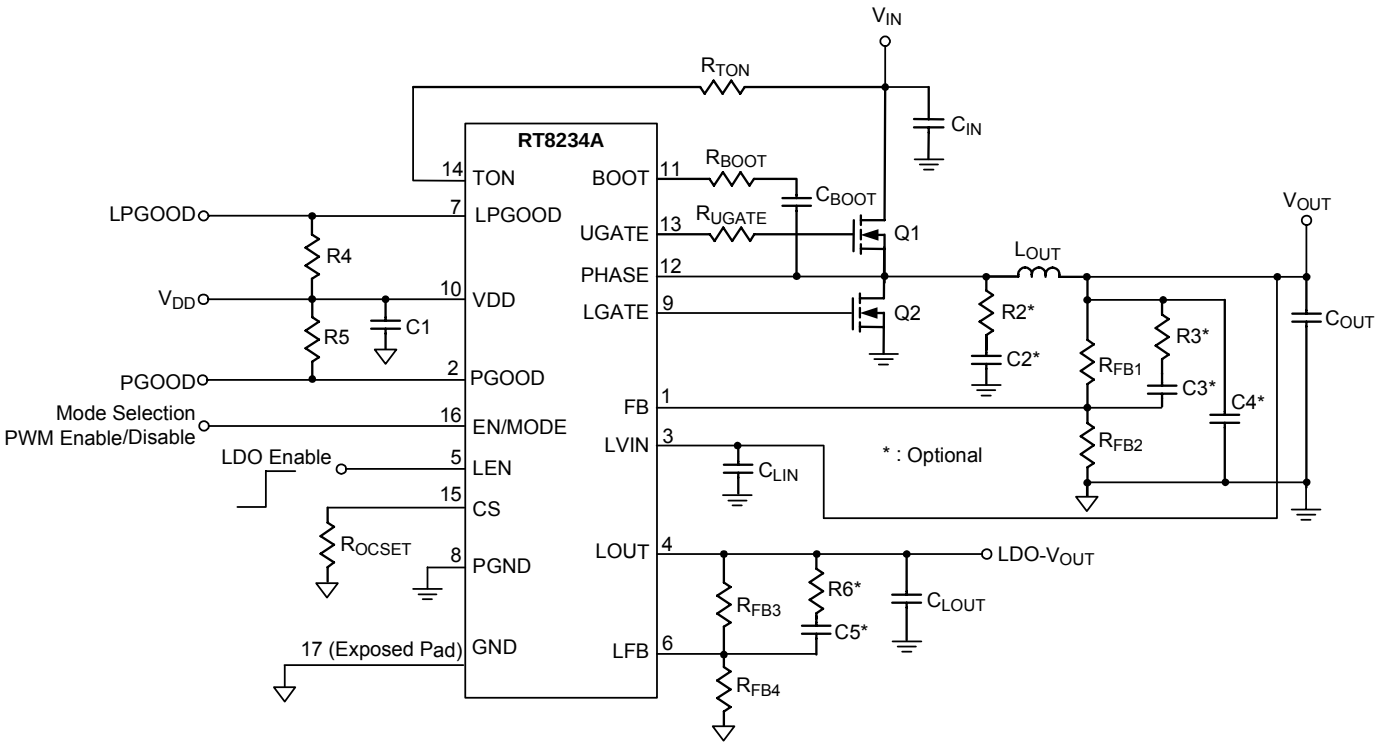
Pin Configurations

TOP VIEW

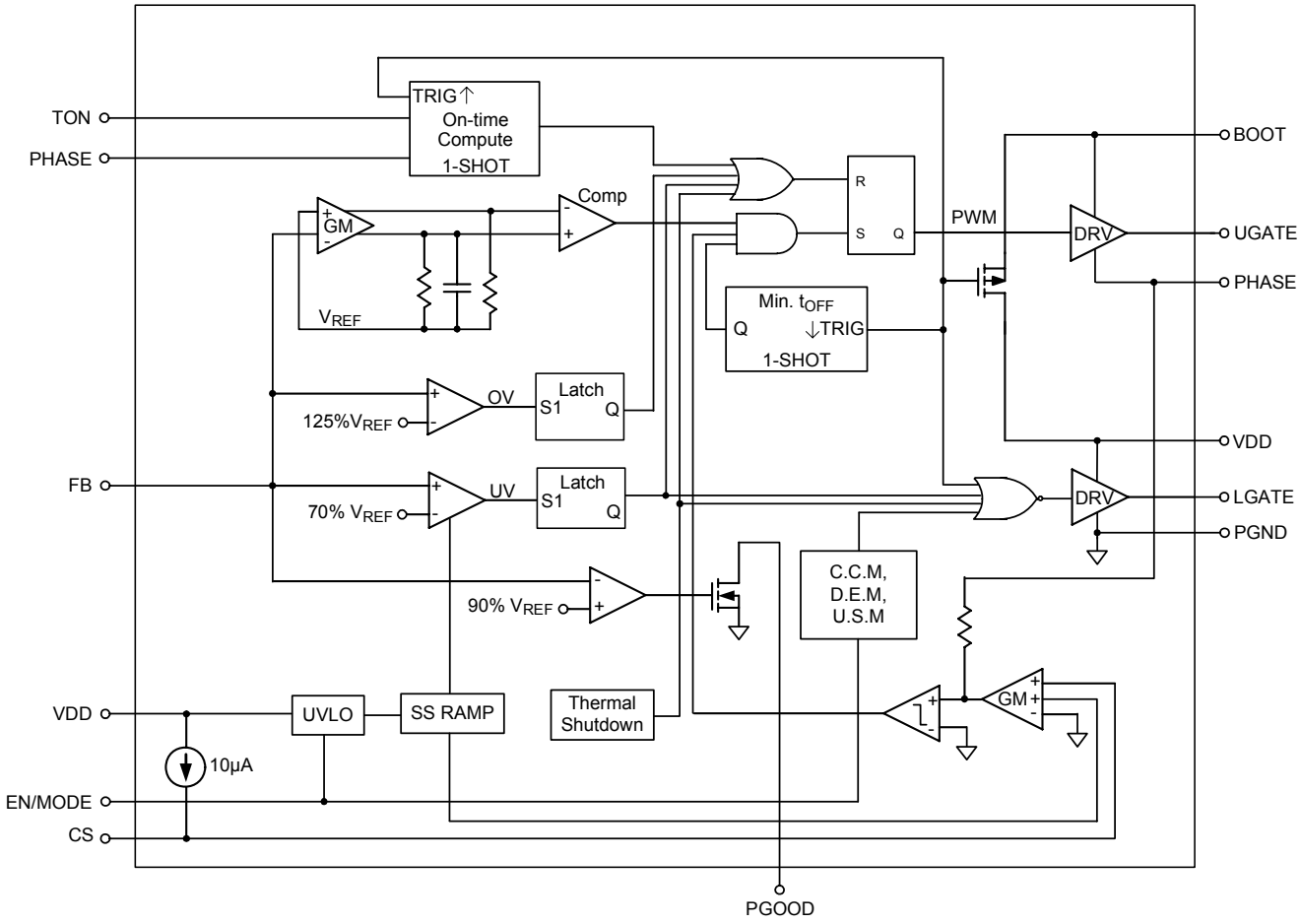


WQFN-16L 3x3

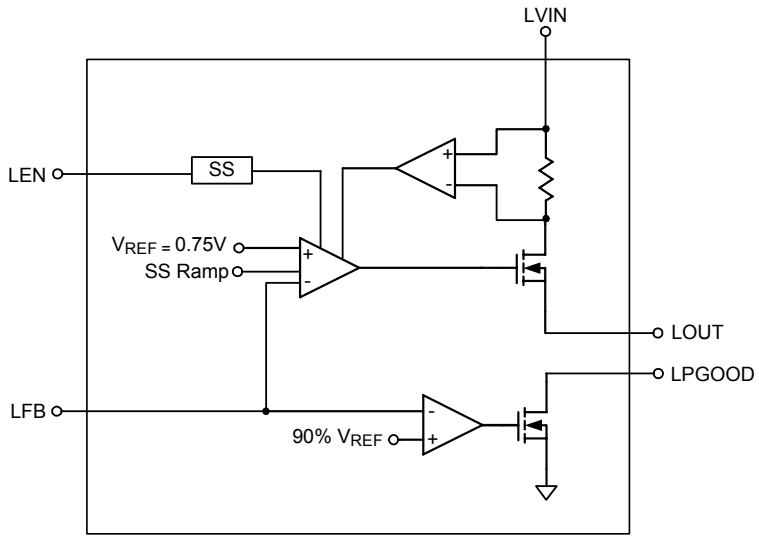
Typical Application Circuit



Function Block Diagram



PWM Controller



LDO Regulator

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB	V_{OUT} Feedback Input. Connect FB to a resistor voltage divider from V_{OUT} to GND to adjust the output from 0.75V to 3.3V.
2	PGOOD	Power Good Indicator. It is an open drain output of the internal switch. This pin will be pulled high when the output voltage is within the target range.
3	LVIN	Supply Input Pin for LDO.
4	LOUT	Output Terminal of the LDO.
5	LEN	Enable Input Pin for LDO with Internal Pull Low Resistor. LDO is enabled if LEN is greater than the ON level and disabled if LEN is less than the OFF level.
6	LFB	LDO Feedback Input. Connect LFB to a resistive voltage divider from LOUT to GND to adjust the output voltage from 0.75V to 3V.
7	LPGOOD	Power Good Indicator. It is an open drain output of LDO regulator. This pin will be pulled high when the output voltage is within the target range.
8	PGND	Power Ground.
9	LGATE	Low Side N-MOSFET Gate Drive Output for PWM. This pin swings between PGND and VDD.
10	VDD	Supply Input Pin. Gate driver supply for external MOSFETS and analog supply for the device. Bypass to PGND with a 1μF ceramic capacitor.
11	BOOT	Bootstrap Power Pin. This pin powers the high side MOSFET driver. Connect a bootstrap capacitor between this pin and phase.
12	PHASE	Switch Node. This pin is not only the current sense input, but also the high side gate driver return.
13	UGATE	High Side N-MOSFET Gate Driver Output for PWM. This pin swings between PHASE and BOOT.
14	TON	On-Time Setting Pin. Connect to VIN through a resistor. TON is an input of the PWM controller.
15	CS	Over Current Set Input. Connect resistor from this pin to signal ground to set the current limit threshold.
16	EN/MODE	PWM enable, disable and mode selection input. Connect this pin to VDD for CCM mode, connect this pin to 3.3V for diode-emulation mode, connect this pin to 2V for ultra sonic mode and connect this pin to GND for shutdown mode.
17 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, TON to GND ---------- –0.3V to 32V
- BOOT to PHASE ---------- –0.3V to 6V
- PHASE to GND
  - DC ---------- –1V to 32V
  - <20ns ---------- –8V to 38V
- VDD, FB, PGOOD, EN, CS ---------- –0.3V to 6V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-16L 3x3 ---------- 1.471W
- Package Thermal Resistance (Note 2)
  - WQFN-16L 3x3, θ_{JA} ---------- 68°C/W
  - WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 4.5V to 26V
- Control Voltage, V_{DD} ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 5V, V_{IN} = 15V, R_{CS} = 100kΩ, R_{TON} = 500kΩ, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
Quiescent Supply Current		FB forced above the regulation point, V_{CS} = 1V	--	0.5	1.25	mA
TON Operating Current		R_{TON} = 500k	--	30	--	μA
Shutdown Current	I_{SHDN}	V_{DD} (V_{EN} = 0V, V_{LEN} = 0V)	--	3	15	μA
		TON	--	1	5	
		V_{EN} = 0V	--	0	--	
FB Error Comparator Threshold (0.75V)		V_{DD} = 4.5 to 5.5V DEM	–1	--	1	%
FB Input Bias Current		V_{FB} = 0.75V	–1	0.1	1	μA
Output Voltage Range	V_{OUT}		0.75	--	3.3	V
On-Time, V_{IN} = 15V		V_{PHASE} = 1.25V, DEM, R_{TON} = 500k	267	334	401	ns
Minimum Off-Time		V_{FB} = 0.6V	250	400	550	ns
Minimum On-Time			60	--	--	ns
Current Sensing Threshold						
OCSET Source Current			9	10	11	μA
Source Current Temperature Coefficient		In Comparison with 25°C	--	4700	--	ppm/°C
CS Pin Setting Range			0.5	--	2	V
Zero Crossing Threshold		PHASE – GND	–13	–3	7	mV
USM Frequency		R_{TON} to PHASE	22	30	--	kHz
Fault Protection						
Current Limit	I_{LIM}	GND – PHASE, V_{CS} = 2V	180	200	220	mV
Output UV Threshold		Falling edge	60	70	80	%
Output UV Hysteresis			--	5	--	%
OVP Threshold		Rising edge	120	125	130	%
OV Fault Delay		FB forced above OV threshold	--	5	--	μs
Under Voltage Lockout Threshold		Falling edge, hysteresis = 300mV, PWM and LDO disabled below this level	3.7	3.9	4.1	V
Under Voltage Lockout Hysteresis			--	300	--	mV
Ramp Current Limit at Soft-Start		From EN high to Current Limit threshold reaches 100mV	--	1.75	--	ms
UV Blank Time		From EN signal going high	--	5	--	ms
Thermal Shutdown	T_{SD}		--	155	--	°C
Driver On-Resistance						
UGATE Driver Source	$R_{UGATEsr}$	BOOT – PHASE forced to 5V, UGATE High State	--	2	4	Ω
UGATE Driver Sink	$R_{UGATEsk}$	BOOT – PHASE forced to 5V, UGATE, 10W State	--	1	2	Ω
LGATE Driver Source	$R_{LGATEsr}$	LGATE, Low State	--	1	2	Ω

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LGATE Driver Sink	$R_{LGATEsk}$	LGATE, Low State	--	0.7	1.5	Ω
Dead Time		LGATE Rising (V_{PHASE} = 1.5V)	--	30	--	ns
		UGATE Rising	--	30	--	
Internal Boost Charging Switch On Resistance		VDD to BOOT, 10mA	--	--	80	Ω
EN Logic Voltage Threshold						
EN Threshold Voltage		PWM Off	--	--	0.8	V
		PWM On, USM Mode	1.7	2	2.3	
		PWM On, DEM Mode	2.9	3.3	3.7	
		PWM On, CCM Mode	4.4	--	--	
PGOOD (upper side threshold decide by OV threshold)						
Trip Threshold (falling)		Measured at FB, with respect to reference, No Load	87	90	93	%
Trip Hysteresis			--	3	--	
Fault Propagation Delay		Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage		I_{SINK} = 1mA	--	--	0.4	V
Leakage Current	I_{LEAK}	High State, forced to 5V	--	--	1	μA
LDO Regulator						
LDO Quiescent Current	I_Q	PWM off, LDO on, I_{OUT} = 0mA	--	--	400	μA
LDO Current Limit	I_{LDOOC}	V_{LVIN} = 1.8V, V_{LOUT} = 1.05V, V_{LFB} = 0.7V	3.1	4.5	--	A
Fold Back Short Current		V_{LVIN} = 1.8V, V_{LFB} < 0.375V	--	1.8	--	A
Soft-Start Time	t_{SS}	From LEN high to internal V_{REF} reaches 0.71V	--	3	--	ms
LDO PGOOD Delay Time		From LEN High to LPGOOD High	--	6	--	ms
LDO Feedback			0.7425	0.75	0.7575	V
Dropout Voltage	V_{DROP}	I_{OUT} = 2A, V_{LOUT} = 1.05V	--	--	300	mV
Load Regulation	ΔV_{LOAD}	0A < I_{LDO} < 3A, V_{DD} = 5V, V_{LVIN} = V_{LOUT} + 1V	--	--	1	%
Line Regulation	ΔV_{LINE_IN}	V_{DD} = 5V, V_{LVIN} = V_{LOUT} + 1V to 5V, I_{LDO} = 1mA	--	--	0.6	%
LDO discharge resistance	$I_{LDODischg}$	V_{LEN} = 0V, V_{LOUT} = 0.5V	--	--	50	Ω
LEN Threshold Voltage — Logic-High	V_{LEN_H}	LDO On	2	--	--	V
LEN Threshold Voltage — Logic-Low	V_{LEN_L}	LDO Off	--	--	0.8	
LEN Input Current	I_{LEN}	V_{LEN} = 5V (internal pull low)	--	--	10	μA
LFB Input Current	I_{LFB}		–1	--	1	μA
LPGOOD Threshold		Measured at LFB, with respect to reference, no load.	87	90	93	%
LPGOOD Hysteresis			--	3	--	%
LPGOOD Propagation Delay			--	2.5	--	μs
LPGOOD Low Voltage		I_{SINK} = 1mA	--	--	0.4	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings, Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

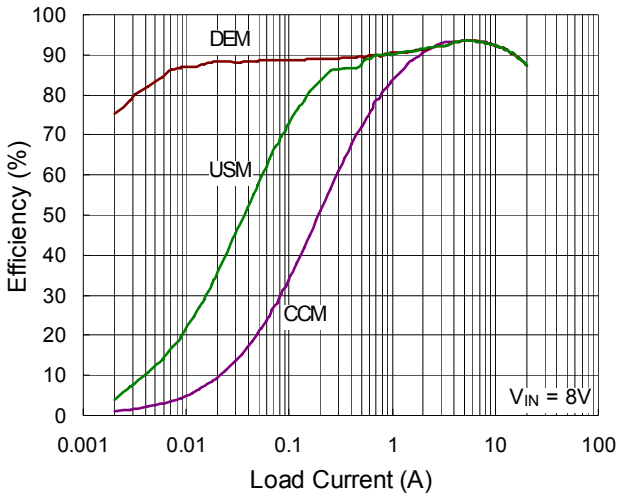
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

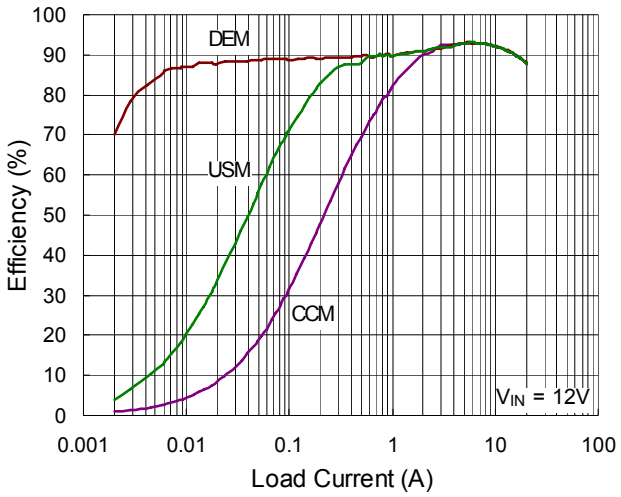
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

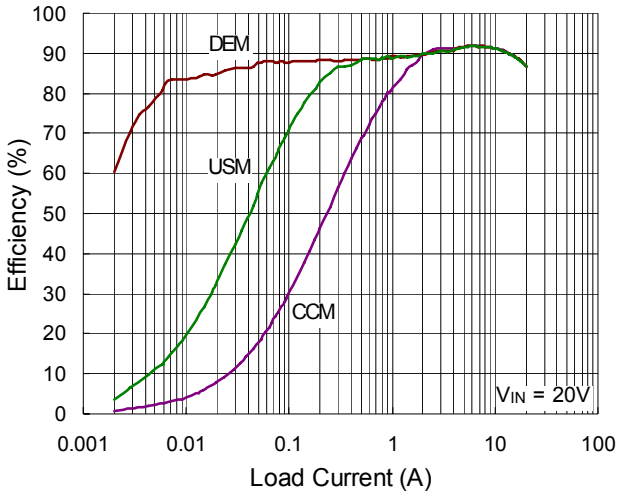
Efficiency vs. Load Current



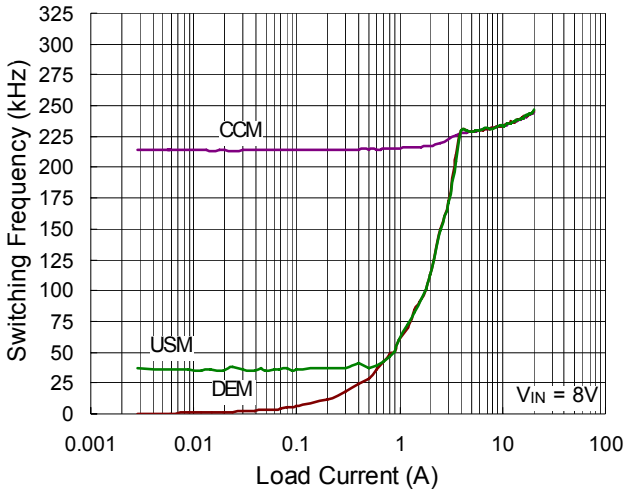
Efficiency vs. Load Current



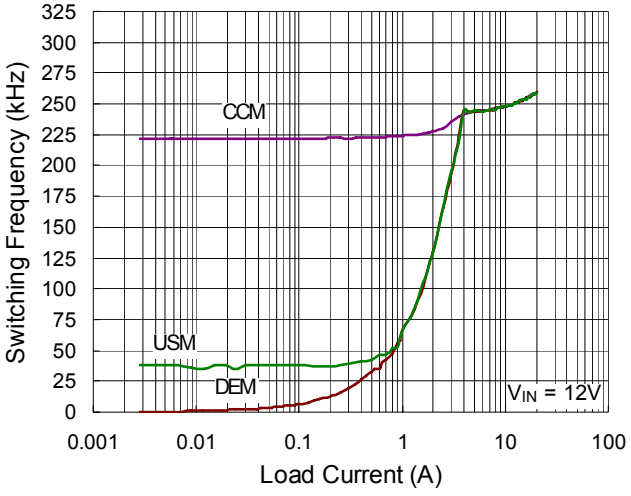
Efficiency vs. Load Current



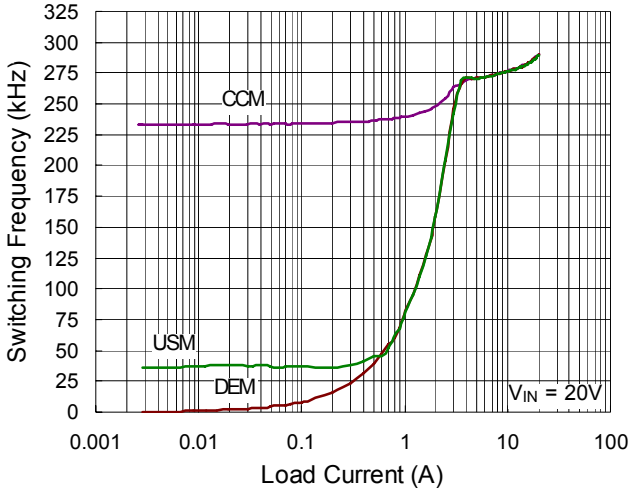
Switching Frequency vs. Load Current



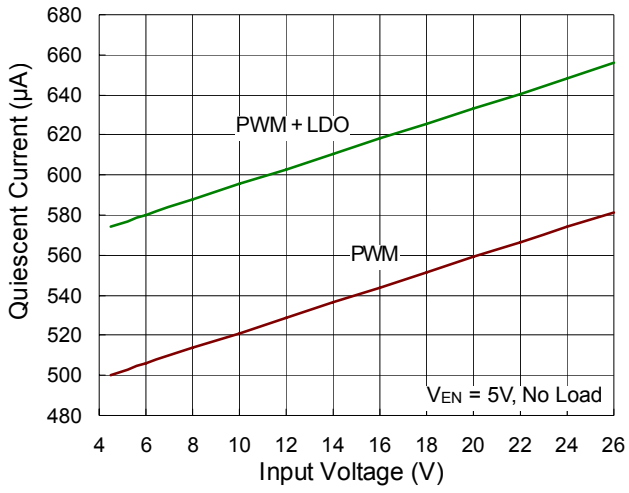
Switching Frequency vs. Load Current



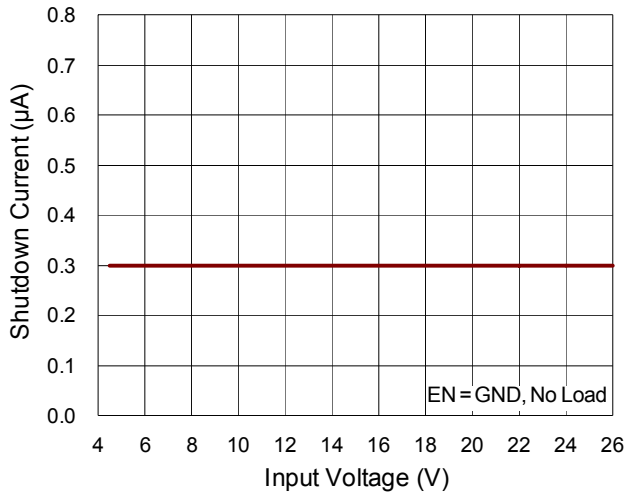
Switching Frequency vs. Load Current



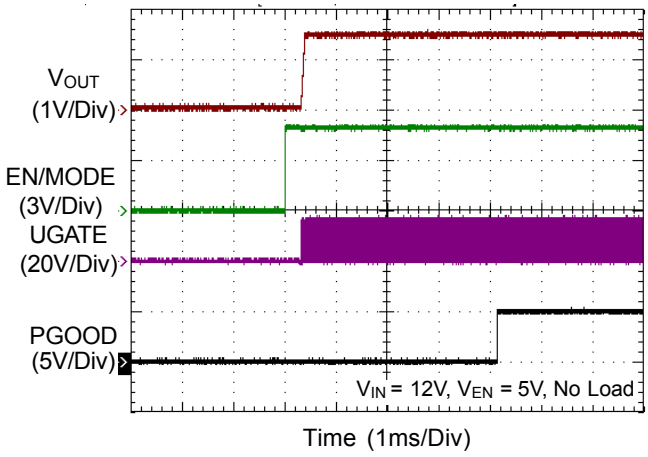
Quiescent Current vs. Input Voltage



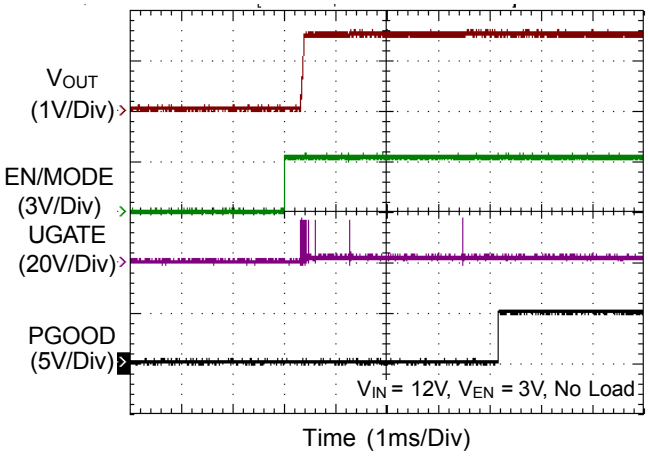
Shutdown Current vs. Input Voltage



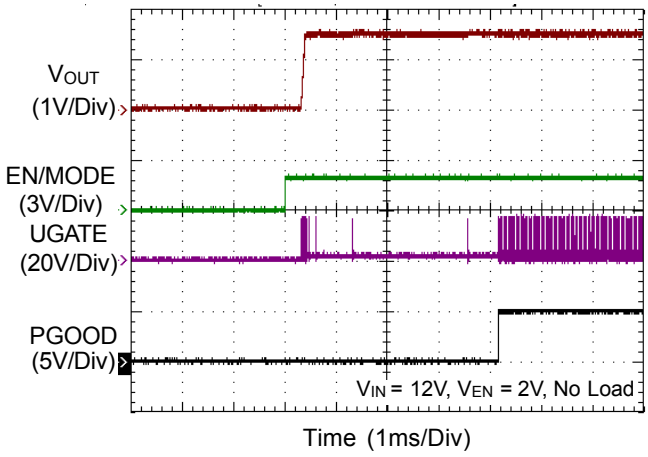
Power On from EN/MODE (CCM)



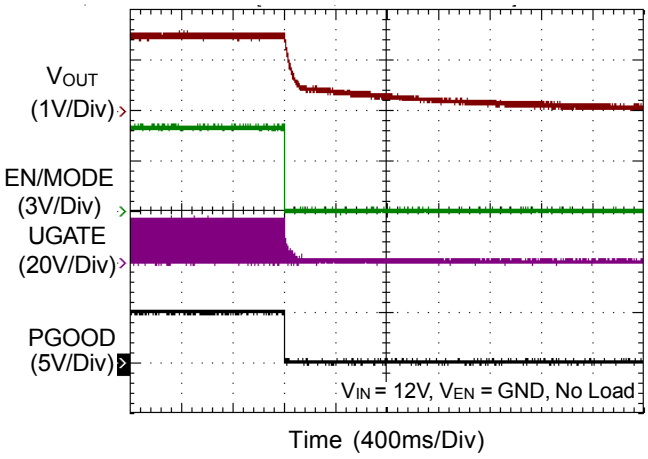
Power On from EN/MODE (DEM)



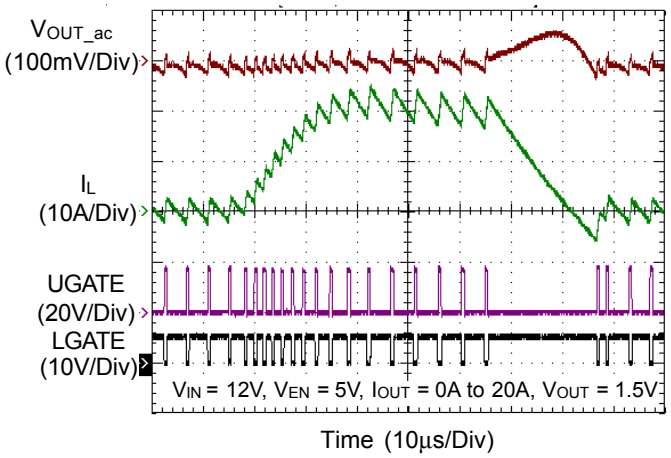
Power On from EN/MODE (USM)



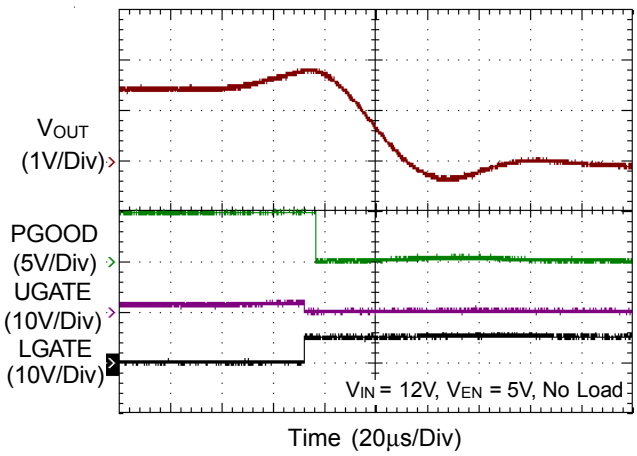
Power Off from EN/MODE (CCM)



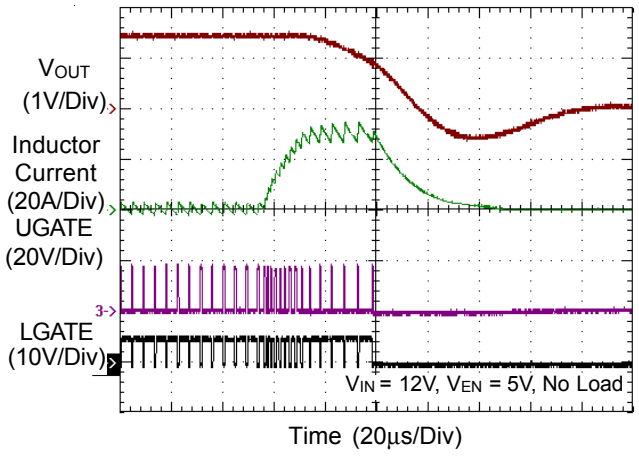
VOUT Load Transient Response



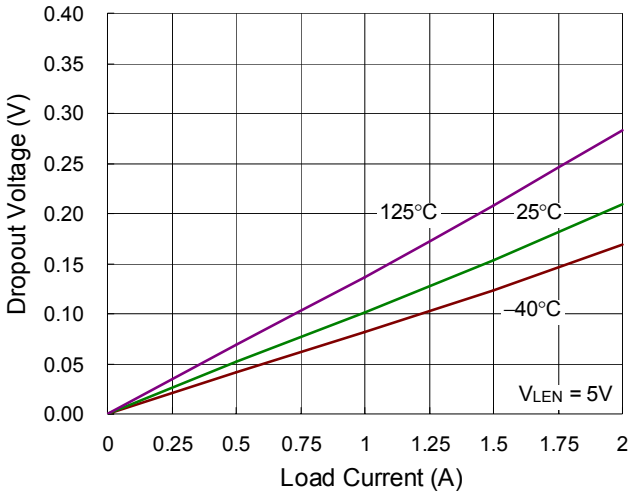
OVP



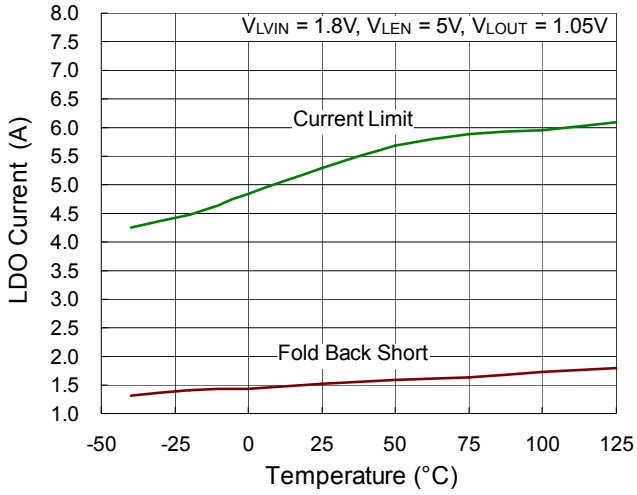
UVP



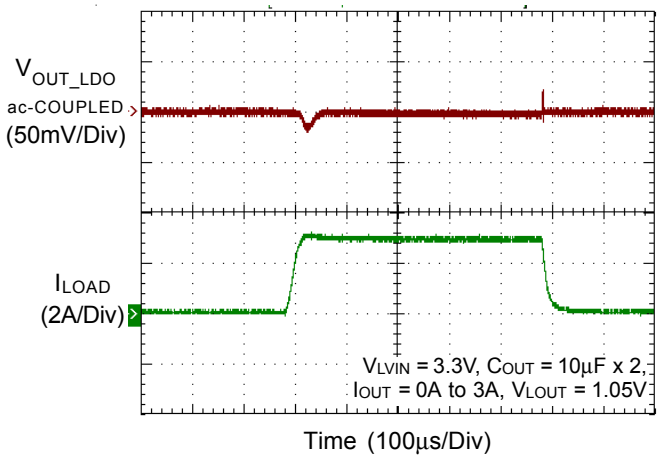
LDO Dropout Voltage vs. Load Current



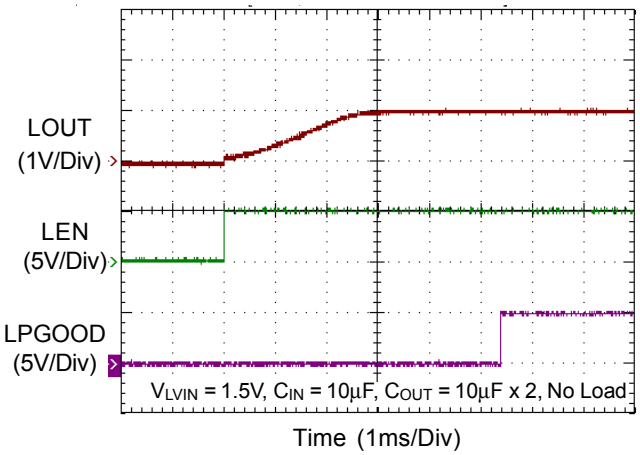
LDO Current vs. Temperature



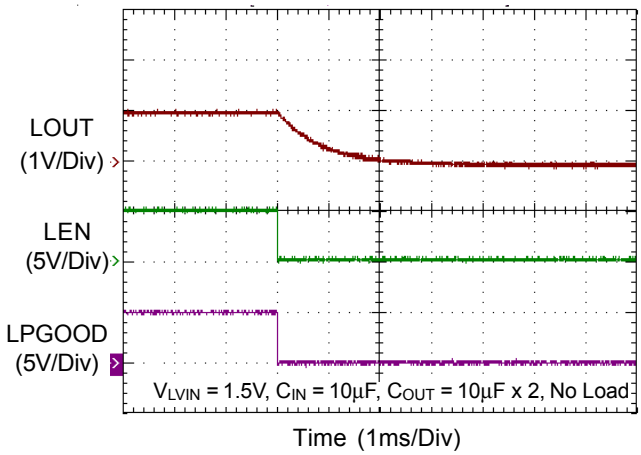
LDO Load Transient Response



LDO Power On from LEN



LDO Power Off from LEN



Application Information

Overview

The RT8234A PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers. Richtek Mach Response™ technology is specifically designed for providing 100ns "Rinstant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages.

The topology circumvents the poor load transient timing problems of fixed-frequency current-mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

PWM Operation

The output ripple valley voltage is monitored at a feedback point voltage. Refer to the function diagrams of RT8234A, the synchronous high side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET is turned off. The pulse width of this one shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

On-Time Control

The on-time one-shot comparator has two inputs. One input monitors the output voltage from the PHASE pin, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high side switch directly proportional to the output voltage and inversely proportional to the input voltage. This implementation results in a nearly constant switching frequency without the need for a clock generator.

The on-time is set according to below equation :

t_{ON} = [V_O x 3.53 / (V_{IN} – 0.9)] x R_{TON} x 2 + 33ns; R_{TON} connects to V_{IN}

And the switching frequency is :

f = V_{OUT} / (V_{IN} x t_{ON})

There is a minimum on-time about 60ns to ensure that the output voltage can start up from 0V.

Enable and Disable

The EN/MODE pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT8234A remains in shutdown if the EN pin is lower than 800mV. When EN/MODE pin rises above the V_{EN} trip point, the RT8234A will begin a new initialization and soft-start cycle.

POR, UVLO and Soft-Start

Power On Reset (POR) occurs when VDD rises above to approximately 4.2V, the RT8234A will reset the fault latch and prepare the PWM for operation. Below 3.7V (MIN), the VDD Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low. A built-in soft-start is used to prevent surge current from power supply input after PWM is enabled. A ramping up current limit threshold can eliminate the V_{OUT} folded-back while in the soft-start duration.

Mode Selection (EN/MODE) Operation

Operation mode is set according to the enable voltage level. When V_{EN} is set from 4.4V to 5.5V, the controller operates in CCM. When V_{EN} is set from 2.9V to 3.7V, the controller operates in diode emulation mode. Finally, when V_{EN} is from 1.7V to 2.3V, the controller operates in ultrasonic mode.

Ultrasonic Mode (V_{EN} from 1.7V to 2.3V)

The RT8234A activates a unique Diode-Emulation Mode with a minimum switching frequency of 30kHz, called the Ultrasonic Mode. The Ultrasonic Mode avoids audio frequency modulation that would otherwise be present when a lightly loaded controller automatically skips

pulses. In Ultrasonic Mode, the high side switch gate driver signal is OR with an internal oscillator (>30kHz). Once the internal oscillator is triggered, the controller enters constant off-time control. When output voltage reaches the setting peak threshold, the controller turns on the low side MOSFET until the controller detects that the inductor current has dropped below the zero crossing threshold. The internal circuitry provides a constant off-time control, and it is effective to regulate the output voltage under light load condition.

Diode-Emulation Mode (V_{EN} from 2.9V to 3.7V)

When V_{EN} is set from 2.9V to 3.7V, the controller operates in diode-emulation mode. In diode-emulation mode, the RT8234A automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly without increasing VOUT ripple or load regulation. As the output current decreases from heavy-load condition, the inductor current is also reduced and eventually reaches the point where its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial negative current when the inductor freewheeling current reaches negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level that requires the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light load operation can be calculated as follows (Figure 1) :

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

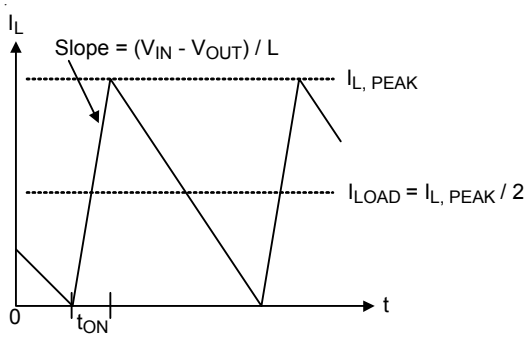


Figure 1. Boundary Condition of CCM/DCM

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

Forced-CCM Mode (V_{EN} from 4.4V to 5.5V)

The low noise, forced-CCM mode (V_{EN} from 4.4V to 5.5V) disables the zero-crossing comparator, which controls the low side switch on-time. This causes the low side gate drive waveform to become the complement of the high side gate drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio VOUT/VIN. The benefit of forced-CCM mode is maintenance of a fairly constant switching frequency, but it comes at a cost. The no load battery current can be anywhere from 10mA to 40mA, depending on the external MOSFETs.

Current Limit Setting (CS)

The RT8234A has cycle-by-cycle current limiting control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current-sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 2). In order to provide both good accuracy and a cost effective solution, the RT8234A supports temperature compensated MOSFET $R_{DS(ON)}$ sensing.

The current limit threshold is equal to 1/10 of the voltage at this pin.

Choose a current limit resistor by following below equation:

R_{OCSET} = (I_{ILIMT} x $R_{DS(ON)}$) x 10 / 10μA

The inductor current is monitored by the voltage between the GND pin and the PHASE pin, so the PHASE pin should be connected to the drain terminal of the low side MOSFET. I_{OCSET} has a temperature coefficient to compensate the temperature dependency of the $R_{DS(ON)}$. GND is used as the positive current sensing node so GND should be connected to the source terminal of the bottom MOSFET.

As the comparison is being done during the OFF state, V_{ILIMT} (current limit threshold) sets the valley level of the inductor current. Thus, the load current at over current threshold, I_{ILIMP}, can be calculated as follows :

$$I_{ILIMP} = \frac{V_{ILIMT}}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

$$= \frac{V_{ILIMT}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

In an over current condition, the current to the load exceeds the current to the output capacitor. Thus, the output voltage tends to fall. Eventually it crosses the under voltage protection threshold and shuts down.

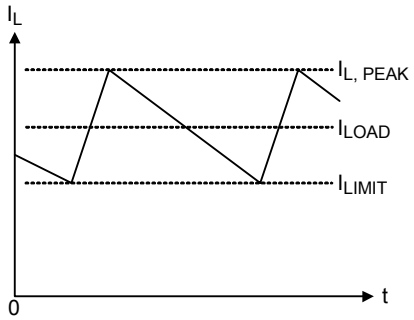


Figure 2. "Valley" Current Limit

MOSFET Gate Driver

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the VDD supply. The average drive current is proportional to the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOT and PHASE pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on. The low side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). The internal pull-down transistor that drives LGATE low is robust, with a 0.7Ω typical on-resistance. A 5V bias voltage is delivered from the VDD supply. The instantaneous drive current is supplied by the flying capacitor between VDD and GND.

For high current applications, some combinations of high and low side MOSFETs that will cause excessive gate-drain coupling may be encountered, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high side MOSFET without degrading the turn-off time (Figure 3).

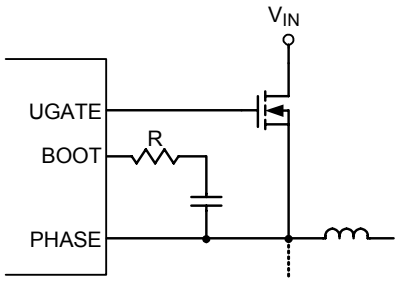


Figure 3. Reducing the UGATE Rise Time

Power Good Output (PGOOD)

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 25% above or 10% below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. During soft-start, PGOOD is actively held low and only allowed to transition high when soft-start is over and the output reaches 90% of its set voltage. There is a 2.5μs delay built into the PGOOD circuitry to prevent false transition.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage protection. When the output voltage exceeds 25% of its set voltage threshold, over voltage protection is triggered and the low side MOSFET is latched on. This activates the low side MOSFET to discharge the output capacitor. The RT8234A is latched once OVP is triggered and can only be released by VDD or EN power on reset. There is a 5μs delay built into the over voltage protection circuit to prevent false transitions.

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When the output voltage is less than 70% of its set voltage threshold, under voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. In order to remove the residual charge on the output capacitor during the under voltage period, if PHASE is greater than 0.75V, LGATE is forced high until PHASE is lower than 0.75V. There is a 2.5µs delay built into the under voltage protection circuit to prevent false transitions. During soft-start, the UVP blanking time is 5ms.

Output Voltage Setting (FB)

The output voltage can be adjusted from 0.75V to 3.3V by setting the feedback resistors, R1 and R2 (Figure 4). Choose R2 to be approximately 10kΩ, and solve for R1 using the below equation :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{FB} is 0.75V.

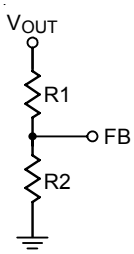


Figure 4. Setting V_{OUT} with a Resistive Voltage Divider

Inductor Selection

The inductor plays an important role in step-down converters because the energy from the input power rail is stored in it and then released to the load. From the viewpoint of efficiency, the DC Resistance (DCR) of inductor should be as small as possible to minimize the conduction loss. In addition, because the inductor takes up most of the board space, its size is also important. Low profile inductors can save board space especially when the height has limitation. However, low DCR and low profile inductors are usually cost ineffective.

Additionally, larger inductance results in lower ripple current, which means lower power loss. However, the inductor current rising time increases with inductance value.

This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, the inductance is designed such that the ripple current ranges between 20% to 40% of full load current. The inductance can be calculated using the following equation :

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_rated}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between inductor ripple current and rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters when selecting input capacitor. Generally, the input capacitor should have a voltage rating 1.5 times greater than the maximum input voltage to be considered a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is selecting a proper capacitor for RMS current rating. Using more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Besides, placing ceramic capacitor close to the drain of the high side MOSFET is helpful in reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output filter capacitor must have ESR low enough to meet output ripple and load-transient requirement, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transient, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain at an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{L_{IR} \times I_{LOAD(MAX)}}$$

Organic semiconductor capacitors or specially polymer capacitors are recommended.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high-value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic and unstable operation. However, it is easy to add sufficient series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting V_{OUT} or FB divider close to the inductor.

There are two related but distinct ways including double-pulsing and feedback loop instability to identify the unstable operation.

Double-pulsing occurs due to noise on the output or because the ESR is too low that there is not enough voltage ramp in the output voltage signal. The "fools" the error comparator into triggering a new cycle immediately after 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillation at the output after line or load perturbations that can trip the over voltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for stability checking is to apply a very zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with AC probe. Do not allow more than one ringing cycle after the initial step-response under- or over-shoot.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the high side MOSFET is small. Therefore, the switching loss of the high side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application.

However, the small duty cycle means that the low side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve overall efficiency, MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low side MOSFET driver capability and the budget.

LDO Normal Operation

The RT8234A includes a built-in N-MOSFET LDO. It provides current up to 3A, from a 1.5V to 3.3V LDO input. VDD powers the LDO internal circuitry. Like any low-dropout regulator, the device requires input and output decoupling capacitors. Please note that linear regulators with a low dropout voltage have high internal loop gains which require care in guarding against oscillation caused by insufficient decoupling capacitance.

LDO Input and Output Capacitor Selection

Like any low-dropout regulator, the external capacitors used with the built-in LDO must be carefully selected for regulator stability and performance. Use a capacitor with value >10μF on the LDO input and the amount of capacitance can be increased. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic can be used for this capacitor. A capacitor with larger value and lower ESR (Equivalent Series Resistance) will provide better line transient response.

The RT8234A LDO is designed specifically to work with ceramic output capacitor in space saving and performance consideration. Using a ceramic capacitor with value of at least 20μF on the LDO output will ensure stability. Output

capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located at not more than 0.5 inch from the LOUT pin of the RT8234A and returned to a clean analog ground.

LDO Output Voltage Setting

The LFB pin connects directly to the inverting input of the error amplifier and the output voltage is set using external resistors, R3 and R4 (Figure 5). The following equation is for adjusting the output voltage.

$$V_{LOUT} = V_{LFB} \times \left(1 + \frac{R3}{R4}\right)$$

where V_{LFB} is 0.75V (typ.).

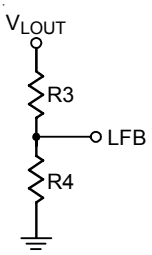


Figure 5. Setting V_{LOUT} with a Resistive Voltage Divider

LDO Enable

The RT8234A LDO is shut down by pulling the LEN pin lower than 800mV and turned on by pulling the LEN pin above the V_{LEN_H} trip point. If the shutdown feature is not required, the LEN pin should be tied to LVIN to keep the regulator on at all times (the LEN pin MUST NOT be left floating).

LDO Power Good Output (LPGOOD)

The power good output is an open-drain output and requires a pull-up resistor. When the LDO output voltage is 25% above or 10% below its set voltage, LPGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. During soft-start, LPGOOD is actively held low and allowed to transition high only after soft-start is over and the output reaches 90% of its set voltage. There is a 2.5µs delay built into LPGOOD circuitry to prevent false transition.

LDO Current Limit

The RT8234A continuously monitors the LDO output current for over current protection. In the event of output over current or short circuit, over current protection function will activate and override the voltage regulation function to limit the output current at 4.5A (typical). If over current or short circuit is not removed, large power dissipation at this condition may also cause chip temperature to rise and trigger the over temperature protection.

Package Power Dissipation

The device implements an internal thermal shutdown feature to protect itself if junction temperature exceeds 155°C. When the junction temperature exceeds the thermal shutdown threshold, the OTP function will be triggered and the RT8234A will shut down and entrer Latch-Off Mode. In Latch-Off Mode, the RT8234A can only be reset by EN/LEN or power input VDD.

The RT8234A is a synchronous buck controller with 3A linear regulator. The main source of power dissipation on the package is the MOSFET driver and the LDO. The total power dissipation must not exceed the maximum allowable power dissipation for the WQFN-16L package. Calculating the power dissipation for both driver and LDO is crucial to ensure a safe operation of the controller. Exceeding the maximum allowable power dissipation will cause the IC to be operated beyond the recommended maximum junction temperature of 125°C.

The maximum power dissipation for the WQFN-16L package is approximately equal to 1.47W at room temperature. The following equations provide the estimation of power dissipation of the integrated drivers and LDO.

$$P_D = \left(N_{HS} \times C_{UGATE} \times V_{BOOT-PHASE}^2 \times f_{SW}\right) + \left(N_{LS} \times C_{LGATE} \times V_{CC} \times f_{SW}\right) + (V_{LVIN} - V_{LVOUT}) \times LDOI_{OUT}$$

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where N_{HS} and N_{LS} are the number of high side MOSFET and the low side MOSFET. C_{UGATE} and C_{LGATE} represent C_{ISS} of the high side MOSFET and the low side MOSFET, respectively. V_{LVIN} is the LDO input voltage and V_{LVOUT} is the LDO output voltage.

From above equations, it is clear that the junction temperature is directly proportional to the total C_{ISS} of all the external MOSFETs and LDO power dissipation.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8234A, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-16L 3x3 packages, the thermal resistance, θ_{JA}, is 68°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)} = (125°C - 25°C) / (68°C/W) = 1.471W$ for

WQFN-16L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J\ (MAX)}$ and thermal resistance, θ_{JA}. For the RT8234A package, the derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

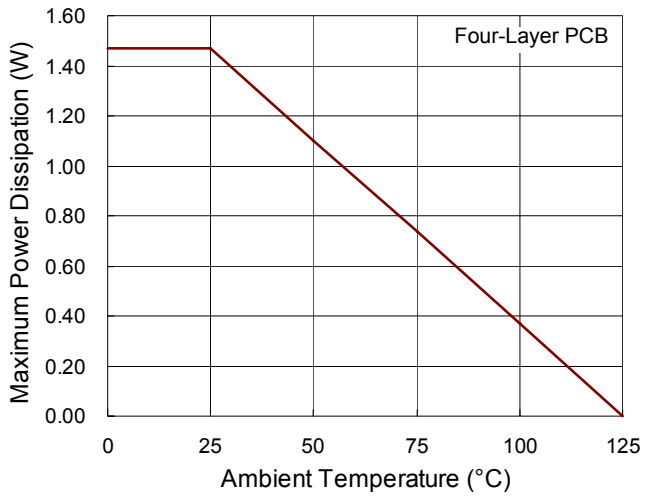


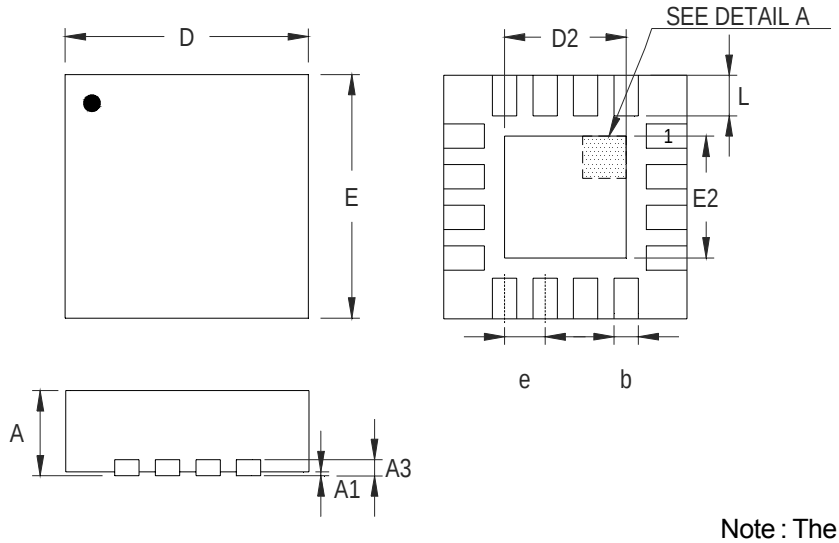
Figure 6. Derating Curve for the RT8234A Package

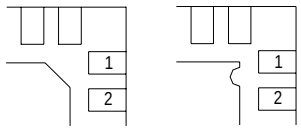
Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to converter instability. Certain points must be considered before starting a layout for the RT8234A.

- Connecting capacitors to VDD, LVIN, LOUT are recommended. Place these capacitors close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as FB, LFB, GND, PGND, EN, LEN, CS, PGOOD, LPGOOD, VDD, and TON should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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