Smart Cap Divider Charger

General Description

The RT9759 is a high efficiency and high charge current charger. The efficiency is up to 97.8% when VBAT = 4.2V, IBAT = 2.5A and the maximum charge current is up to 8A. The device integrates smart cap divider topology, external over-voltage protection control, an input reverse blocking NFET and 2-way regulation, a dual-phase charge pump core, 15-way protection, 7-way system alarm and 9-Channel high speed analog-to-digital converter. The high speed analog-to-digital converter provides input and output voltage, current and temperature information for the host. The host can monitor the information by I^2C serial interface.

Applications

- Smart Phones
- Tablet
- PC

Ordering Information

RT9759 □

└Package Type
WSC : WL-CSP-56B 3.35x3.35 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **External OVP Control and Regulation**
  - **High Absolute Maximum Rating of 40V**
  - **Fast Reaction Time 100ns and Fast Turn Off Time 100ns**
  - **VBAT Voltage Regulation (VBAT REG)**
  - **IBAT Current Regulation (IBAT REG)**
- **Input Reverse Blocking NFET**
  - **Block the Reverse Current**
- **Dual-Phase Charge Pump Core**
  - **8A Output Current Capability**
  - **Efficiency Up to 97.8% when VBAT = 4.2V, IBAT = 2.5A**
  - **250kHz to 750kHz Variable Switching Frequency Stay Out of Audio Band**
  - **Spread Spectrum Technology for EMI Reduction**
- **4-Error Charge Pump Switch Protection**
  - **VBUS Voltage Too High Error Protection before Switch (VBUS_HIGH_ERR)**
  - **VBUS Voltage Too Low Error Protection before Switch (VBUS_LOW_ERR)**
  - **CFLY Short Error Protection Before Switch (CFLY_DIAG)**
  - **NFET Over-Current Error Protection During Switch (CON_OCP)**
- **10-Way System Protection**
  - **VBUS Over-Voltage Protection (VBUS_OVP)**
  - **IBUS Over-Current Protection (IBUS_OCP)**
  - **IBUS Under-Current Protection (IBUS_UCP)**
  - **VOUT Over-Voltage Protection (VOUT_OVP)**
  - **VBAT Over-Voltage Protection (VBAT_OVP)**
  - **IBAT Over-Current Protection (IBAT_OCP)**
  - **Dropout Over-Voltage Protection (VDR_OVP)**
  - **TSBUS Over-Temperature Protection (TBUS_OTP)**
  - **TSBAT Over-Temperature Protection (TBAT_OTP)**
  - **Junction Over-Temperature Protection (TDIE_OTP)**
- **7-Way System Alarm**
  - **VBUS Over-Voltage Alarm (VBUS_OVP_ALM)**
  - **IBUS Over-Current Alarm (IBUS_OCP_ALM)**

- VBAT Over-Voltage Alarm (VBAT_OVP_ALM)
- IBAT Over-Current Alarm (IBAT_OCP_ALM)
- IBAT Under-Current Alarm (IBAT_UCP-ALM)
- TSBUS and TSBAT Over-Temperature Alarm (TBUS_TSBAT_OTP_ALM)
- TDIE Over-Temperature Alarm (TDIE_OTP_ALM)

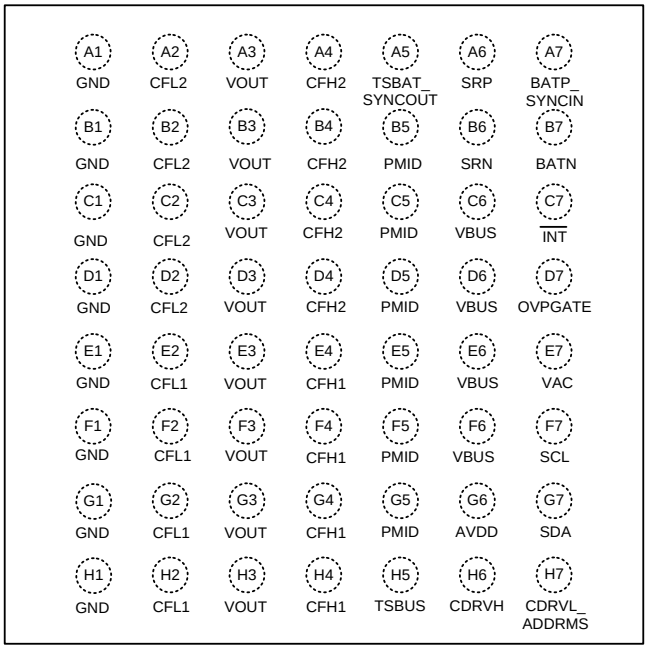
- 9-Channel 12-bit ADC
  - High Speed Data Rate for 128 Times Average Per Channel
  - VBUS, IBUS, VOUT, VBAT, IBAT, TSBUS, TSBAT, TDIE, VAC 9-Channel for Voltage/Current Measurement

Marking Information

RT9759WSC : Product Number
YMDNN : Date Code
$: Random Code

Pin Configuration

(TOP VIEW)



WL-CSP-56B 3.35x3.35 (BSC)

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
A1, B1, C1, D1, E1, F1, G1, H1	GND	P	Power ground.
A2, B2, C2, D2	CFL2	P	Flying capacitor negative node. Three 22μF capacitors must be connected to CFL2 and CFH2 and placed as close as possible to the device. These pins must be connected together on the PCB.
E2, F2, G2, H2	CFL1	P	Flying capacitor negative node. Three 22μF capacitors must be connected to CFL1 and CFH1 and placed as close as possible to the device. These pins must be connected together on the PCB.
A3, B3, C3, D3, E3, F3, G3, H3	VOUT	P	Power supply. Connect to positive terminal of the battery pack. Must be connected together on the PCB. Two 10μF capacitors must be connected to VOUT and GND.
A4, B4, C4, D4	CFH2	P	Flying capacitor positive node. Three 22μF capacitors must be connected to CFL2 and CFH2 and placed as close as possible to the device. These pins must be connected together on the PCB.
A5	TSBAT_ SYNCOUT	AI	Battery temperature qualification voltage input. Requires external resistor divider and voltage reference. In parallel configuration, connect this pin to BATP_SYNCIN of slave.
A6	SRP	AI	Positive input for battery current sensing. Place 5mΩ or 2mΩ between SRN and SRP.
A7	BATP_ SYNCIN	AI	Positive input for battery voltage sensing. Connect 100Ω in series with positive terminal of battery pack. In parallel configuration, connect this pin to TSBAT_SYNCOUT of master.

Pin No.	Pin Name	I/O	Pin Function
B5, C5, D5, E5, F5, G5	PMID	P	Connected to the drain of the reverse blocking NFET. One 10μF capacitors must be connected to PMID and PGND.
B6	SRN	AI	Negative input for battery current sensing. Place 5mΩ or 2mΩ between SRN and SRP.
B7	BATN	AI	Negative input for battery voltage sensing. Connect 100Ω in series with negative terminal of battery pack.
C6, D6, E6, F6	VBUS	P	These pins are the input power supply and must be connected together on the PCB. One 1μF capacitor must be connected to VBUS and GND.
C7	$\overline{INT}$	DO	Open drain interrupt output. Connect to pull-up voltage via 10kΩ pull-up resistor. Normally high, when event happen, INT pin sends a 256μs low pulse to system.
D7	OVPGATE	AO	External N-FET control pin, connect to gate of external N-FET.
E4, F4, G4, H4	CFH1	P	Flying capacitor positive node. Three 22μF capacitors must be connected to CFL1 and CFH1 and placed as close as possible to the device. These pins must be connected together on the PCB.
E7	VAC	AI	Input voltage sense pin, connect to drain of external N-FET
F7	SCL	DI	I^2C serial clock line. Connect to pull-up voltage via 10kΩ pull-up resistor.
G6	AVDD	AO	Analog power supply. This pin is the internal power supply. It is recommended to connect a 4.7μF capacitor from AVDD to the GND plane, and placed as close as possible to the device. Do not use this pin for other function.
G7	SDA	DIO	I^2C serial data line. Connect to pull-up voltage via 10kΩ pull-up resistor.
H5	TSBUS	AI	BUS temperature qualification voltage input. Requires external resistor divider and voltage reference.
H6	CDRVH	AIO	Charge pump for gate drive. Connect a 0.22μF capacitor between CDRVH and CDRVL_ADDRMS.
H7	CDRVL_ ADDRMS	AIO	Charge pump for gate drive. Connect a 0.22μF capacitor between CDRVH and CDRVL_ADDRMS. Place different resistance between CDRVL_ADDRMS and GND to assign the address of device and the mode of device as Standalone, Master or Slave.

Typical Application Circuit

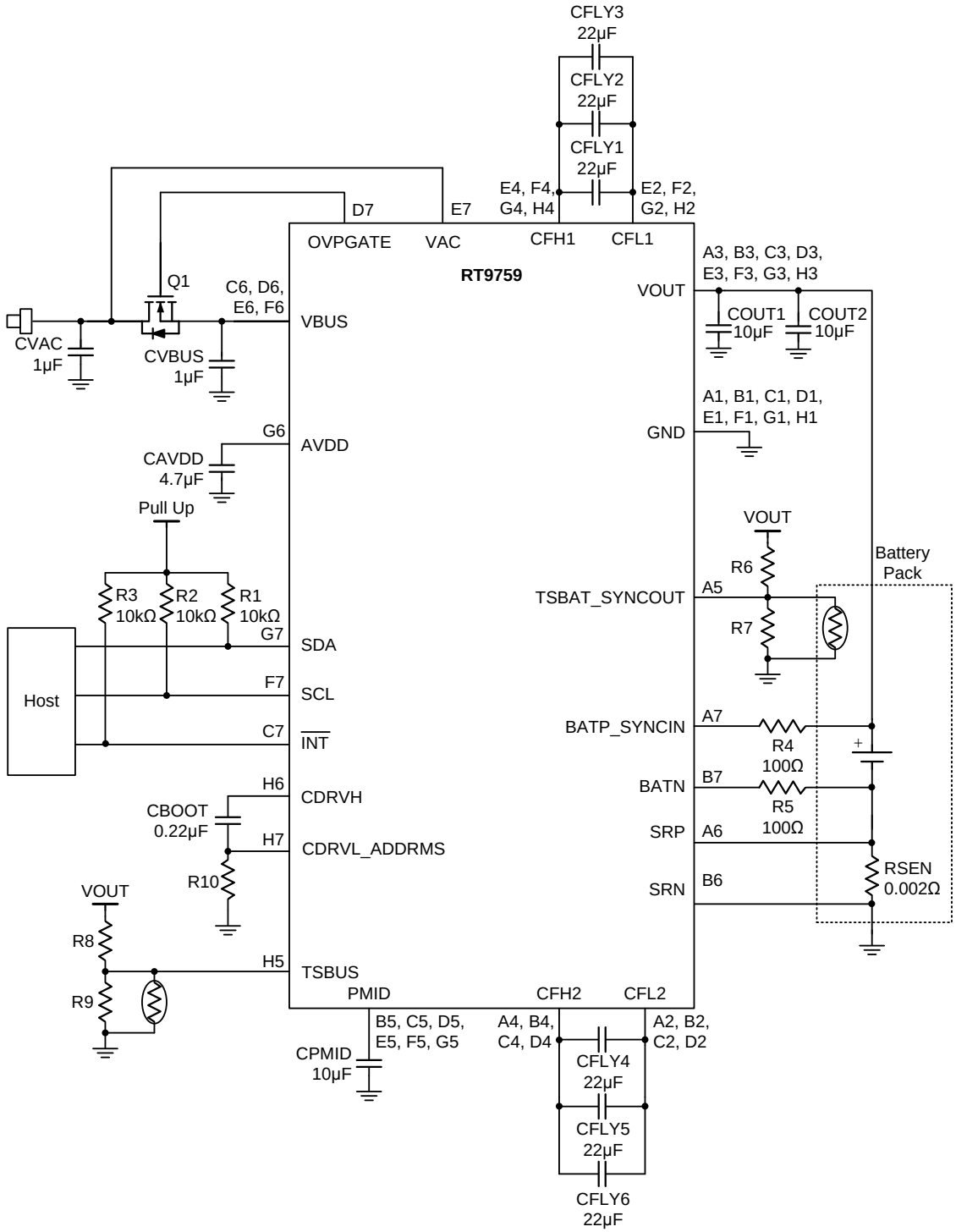
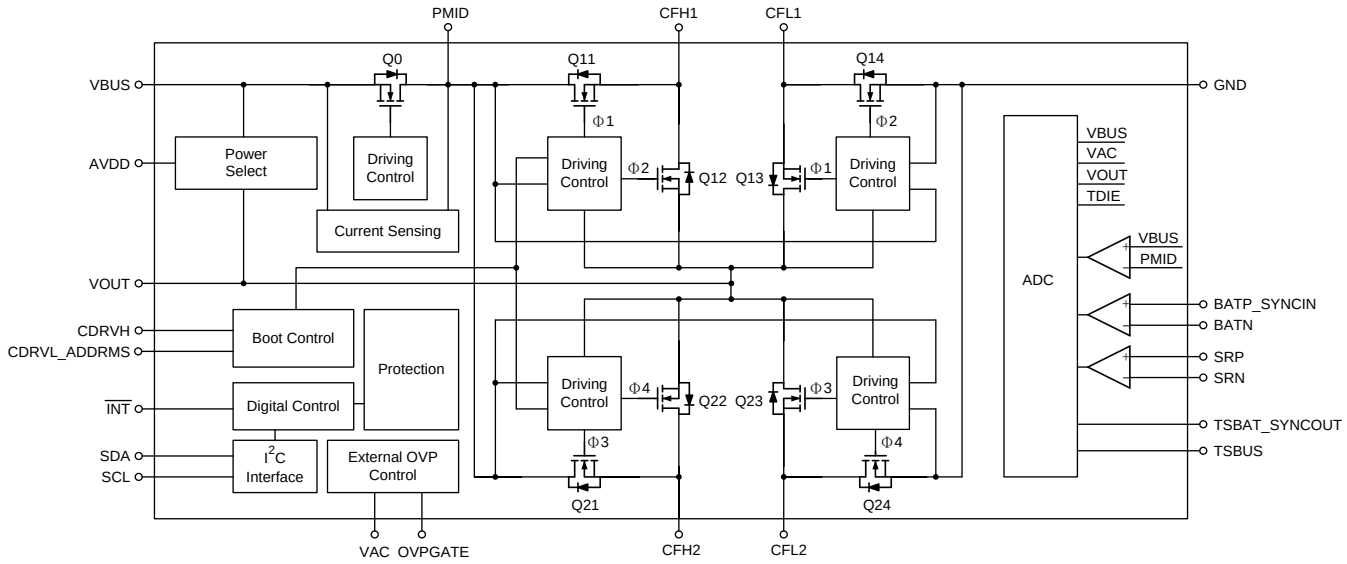


Table 1. BOM List

Name	Part Number	Description	Package	Manufacturer
CVAC	GRM188R61H105KAAL	CAP, CERM, 1µF, 50V, ±10%, X5R	0603	MuRata
CVBUS	GRM188R61E105KA12D	CAP, CERM, 1µF, 25V, ±10%, X5R	0603	MuRata

Name	Part Number	Description	Package	Manufacturer
Q1	PSMN2R4-30MLD	N-Channel 30V, 2.4mΩ logic level MOSFET in LFPAK33, using NextPowerS3 Technology	LFPAK33	Nexperia
CFLY1, CFLY2, CFLY3, CFLY4, CFLY5, CFLY6	GRM188R61A226ME15D	CAP, CERM, 22μF, 10V, ±20%, X5R	0603	MuRata
COUT1, COUT2	GRM185R60J106ME15	CAP, CERM, 10μF, 6.3V, ±20%, X5R	0603	MuRata
CPMID	GRM188R61E106MA73	CAP, CERM, 10μF, 25V, ±20%, X5R	0603	MuRata
CBOOT	GRM033R61C224KE14	CAP, CERM, 0.22μF, 16V, ±10%, X5R	0201	MuRata
CAVDD	GRM155R61A475MEAAD	CAP, CERM, 4.7μF, 10V, ±20%, X5R	0402	MuRata
R1, R2, R3	CRCW040210K0JNED	RES, 10k, 5%, 0.063W	0402	Vishay-Dale
R4, R5	ERJ-2RKF1000X	RES, 100Ω, 1%, 0.1W, 0402	0402	Panasonic
RSEN	CSNL1206FT2L00	RES, 0.002, 1%, 1W	1206	Stackpole Electronics Inc

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Pin Voltage, VAC ---------- –2V to 40V
- Supply Pin Voltage, VBUS ---------- –2V to 22V
- Supply Pin Voltage, VOUT ---------- –0.7V to 6V
- Control Pin Voltage, OVPGATE ---------- –0.3V to 40V
- Terminal Pin Voltage, PMID ---------- –0.3V to 22V
- Terminal Pin Voltage, CDRVH ---------- –0.3V to 18V
- Terminal Pin Voltage, CFH1, CFH2 ---------- –0.3V to 12V
- Terminal Pin Voltage, CFL1, CFL2 ---------- –0.3V to 6V
- Terminal Pin Voltage, $\overline{INT}$, SDA, SCL, CDRVL_ADDRMS, AVDD ---------- –0.3V to 6V
- Terminal Pin Voltage, SRP, SRN ---------- –0.3V to 6V
- Terminal Pin Voltage, BATP_SYNCIN, BATN ---------- –0.3V to 6V
- Terminal Pin Voltage, TSBUS, TSBAT_SYNCOUT ---------- –0.3V to 6V
- Terminal Pin Current, $\overline{INT}$ ---------- 0mA to 6mA
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-56B 3.35x3.35 (BSC) ---------- 4.16W
- Package Thermal Resistance (Note 2)

  WL-CSP-56B 3.35x3.35 (BSC), θ_{JA} ---------- 24°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model), per ANSI/ESDA/JEDEC JS-001 ---------- ±2kV

  CDM (Charged Device Model), per JEDEC specification JESD22-C101 ---------- ±500V

Recommended Operating Conditions (Note 4)

- Supply Pin Voltage, VAC ---------- 2.8V to 17V
- Supply Input Voltage Range, VBUS, PMID ---------- 2.8V to 11V
- Ouput Voltage Range, VOUT ---------- 2.8V to 5V
- Analog Sense Voltage Range, BATP_SYNCIN, BATN ---------- 0V to 5V
- Analog Sense Voltage Range, SRP, SRN ---------- 0V to 0.2V
- Temperature Sense Voltage Range, TSBUS, TSBAT_SYNCOUT ---------- 0V to 2.25V
- Positive flying capacitor Voltage Range, CFH1, CFH2 ---------- 0V to 11V
- Negative flying capacitor Voltage Range, CFL1, CFL2 ---------- 0V to 5V
- I/O Control Voltage Range, SDA, SCL, $\overline{INT}$ ---------- 0V to 5V
- Charger Current Range, IBAT ---------- 0A to 8A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 150°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
External OVP Control						
OVPGATE Voltage	$V_{OVPGATE}$	Operation voltage OVPGATE – VBUS, VAC = 6V to 9V	9	10	11	V
VAC_INSERT Threshold	$V_{AC\_INSERT\_TH}$	V_{AC} rising threshold to turn on external MOS	2.6	2.8	3	V
VAC_INSERT Hysteresis	$V_{AC\_INSERT\_HY}$	V_{AC} falling hysteresis to turn off external MOS	250	500	750	mV
VAC_INSERT Deglitch Time	$t_{VAC\_INSERT\_DEG}$	Deglitch time between VAC higher than $V_{AC\_INSERT\_TH}$ and turn on external MOS	18	20	22	ms
VAC Insert Threshold Rising Deglitch Time	$V_{AC\_INSERT\_RIS\_DEG}$	Deglitch between VAC over $V_{AC\_INSERT\_TH}$ and sent an INT.	--	1	--	ms
VAC OVP Range	$V_{AC\_OVP\_RAN}$	I^2C programmable, 3-bit DAC, 6.5V, 11V to 17V	6.5	--	17	V
VAC OVP Accuracy	$V_{AC\_OVP\_ACC}$	VAC_OVP Threshold accuracy	–2	--	2	%
VAC OVP Hysteresis	$V_{AC\_OVP\_HY}$	V_{AC} falling to turn on external MOS after VAC OVP happen	250	500	750	mV
OVPGATE Turn-Off Time	$t_{VAC\_OVP\_OFF}$	Duration between OVPGATE start to turn off external MOS and the external MOS be fully turn off, C_{GS} = 4nF	--	100	--	ns
OVPGATE Reaction Time	$t_{VAC\_OVP\_RE}$	Duration between V_{AC} over VAC_OVP threshold and OVPGATE start to turn off external MOS, C_{GS} = 4nF	--	100	--	ns
VBAT Regulation Range	$V_{BAT\_REG\_RAN}$	VBAT_OVP – Register 0x2C[5:4] setting	3.5	--	5.075	V
VBAT Regulation Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT} = 4.2V to 4.65V	–20	--	20	mV
IBAT Regulation Range	$I_{BAT\_REG\_RAN}$	IBAT_OCP – Register 0x2C[7:6] setting	2	--	10	A
IBAT Regulation Accuracy	$I_{BAT\_REG\_ACC}$	I_{BAT} = 2A to 5A, RSEN = 0.002Ω	–200	--	200	mA
Regulation Time Out	$t_{REG\_TIMEOUT}$	If device in regulation and no VDR_OVP for this time, the device will stop charge.	585	650	715	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Select and Source						
VBUS Quiescent Current	I_{BUS_IQ}	ADC disable, charge disable, OVP MOS no used, VBUS and VAC are open. VOUT no present. Measure quiescent current on VBUS.	--	55	95	μA
VAC Quiescent Current	I_{AC_IQ}	ADC disable, charge disable, OVP MOS used, VOUT no present, no VAC_OVP happen. Measure quiescent current on VAC. VAC = 3.5V to 12V.	--	315	395	μA
		ADC enable, charge disable, OVP MOS used, VOUT no present. Measure quiescent current on VAC.	--	3	4	mA
VOUT Quiescent Current	I_{OUT_IQ}	ADC disable, charge disable, VAC no present. VOUT falling from 4.5V to 0V, Measure quiescent current on VOUT.	--	10	16	μA
		ADC enable, charge disable, VAC no present. Measure quiescent current on VOUT.	--	2	3	mA
VDDA UVLO Threshold	$V_{DDA\_UVLO\_TH}$	V_{DDA} rising	2.6	2.8	3	V
VDDA UVLO Hysteresis	$V_{DDA\_UVLO\_HY}$	V_{DDA} falling	--	0.8	--	V
Device Start Up Time	t_{VDDA_START}	Duration time between VDDA > $V_{DDA\_UVLO\_TH}$ and device can start I^2C communicate	--	--	64	ms
Soft-Start Time	t_{SOFT_START}	Duration time between the device start switching and CHG_EN = 1	--	--	50	ms
VOUT Insert Threshold	$V_{OUT\_INSERT\_TH}$	VOUT rising	2.65	2.8	2.95	V
VOUT Insert Threshold Rising Deglitch Time	$V_{OUT\_INSERT\_RIS\_DEG}$		--	17	--	μs
VOUT Insert Hysteresis	$V_{OUT\_INSERT\_HY}$	VOUT falling	50	150	250	mV
Cap Divider Charger						
Q0 RON	R_{Q0}	VBUS = 9V, VOUT = 4.5V charge enable	--	6	8	mΩ
Q11, Q21 RON	R_{Q11}, R_{Q21}	VBUS = 9V, VOUT = 4.5V, charge enable	--	14	19	mΩ
Q12, Q22 RON	R_{Q12}, R_{Q22}	VBUS = 9V, VOUT = 4.5V charge enable	--	9.5	13	mΩ
Q13, Q23 RON	R_{Q13}, R_{Q23}	VBUS = 9V, VOUT = 4.5V charge enable	--	8	12.5	mΩ
Q14, Q24 RON	R_{Q14}, R_{Q24}	VBUS = 9V, VOUT = 4.5V Charge enable	--	9	12.5	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Charge Switch Frequency	f_{SW}	Select by register 0x0B[6:5] = 11	675	750	825	kHz
		Select by register 0x0B[6:5] = 10, default	450	500	550	
		Select by register 0x0B[6:5] = 01	337	375	412	
		Select by register 0x0B[6:5] = 00	225	250	275	
Protection						
VBAT OVP Range	$V_{BAT\_OVP\_RAN}$	Rising	3.5	--	5.075	V
VBAT OVP Step Size	$V_{BAT\_OVP\_SIZE}$		--	25	--	mV
VBAT OVP Accuracy	$V_{BAT\_OVP\_ACC}$	VBAT_OVP = 4.2V to 4.65V	–20	--	20	mV
VBAT OVP Deglitch time	$t_{VBAT\_OVP\_DEG}$		—	3	--	µs
IBAT_OCP Range	$I_{BAT\_OCP\_RAN}$	Rising	2	--	10	A
IBAT_OCP Step Size	$I_{BAT\_OCP\_SIZE}$		--	100	--	mA
IBAT_OCP Accuracy	$I_{BAT\_OCP\_ACC}$	IBAT_OCP = 3A to 8A, RSEN = 0.002Ω	–200	--	200	mA
IBAT OCP Deglitch time	$t_{IBAT\_OCP\_DEG}$		--	50	--	µs
VBUS OVP Range	$V_{BUS\_OVP\_RAN}$	Rising	6	--	12.35	V
VBUS OVP Step Size	$V_{BUS\_OVP\_SIZE}$		--	50	--	mV
VBUS OVP Accuracy	$V_{BUS\_OVP\_ACC}$		–35	--	35	mV
VBUS OVP Deglitch Time	$t_{VBUS\_OVP\_DEG}$		--	3	--	µs
IBUS_OCP Range	$I_{BUS\_OCP\_RAN}$	Rising	1	--	4.75	A
IBUS_OCP Step Size	$I_{BUS\_OCP\_SIZE}$		--	250	--	mA
IBUS_OCP Accuracy	$I_{BUS\_OCP\_ACC}$		–250	--	250	mA
IBUS_OCP Deglitch	$t_{IBUS\_OCP\_DEG}$		--	50	--	µs
IBUS_UCP_RISE Accuracy	$I_{BUS\_UCP\_RISE\_ACC}$	Rising, IBUS_UCP_RISE = 300mA, set by Register 0x2B[2] = 0	200	300	400	mA
	$I_{BUS\_UCP\_RISE\_ACC}$	Rising, IBUS_UCP_RISE = 500mA, set by Register 0x2B[2] = 1	400	500	600	mA
IBUS_UCP_RISE Deglitch Time	$t_{IBUS\_UCP\_RISE\_DEG}$		--	22	--	µs
IBUS_UCP_FALL Accuracy	$I_{BUS\_UCP\_FALL\_ACC}$	Falling, IBUS_UCP_FALL = 150mA, set by Register 0x2B[2] = 0	10	150	290	mA
	$I_{BUS\_UCP\_FALL\_ACC}$	Falling, IBUS_UCP_FALL = 250mA, set by Register 0x2B[2] = 1	110	250	390	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBUS_UCP_FALL Deglitch Time	$t_{IBUS\_UCP\_FALL\_DEG}$	$t_{IBUS\_UCP\_FALL\_DEG}$ = 10μs, set by Register 0x2E[3] = 0	--	22	--	μs
		$t_{IBUS\_UCP\_FALL\_DEG}$ = 5ms, set by Register 0x2E[3] = 1	--	5	--	ms
IBUS UCP Time Out	$t_{IBUS\_UCP\_TIMEOUT}$	$t_{BUS\_UCP\_TIMEOUT}$ = 12.5ms, set by Register 0x2B[7:5] = 001	11.25	12.5	13.75	ms
		$t_{BUS\_UCP\_TIMEOUT}$ = 25ms, set by Register 0x2B[7:5] = 010	22.5	25	27.5	ms
		$t_{BUS\_UCP\_TIMEOUT}$ = 50ms, set by Register 0x2B[7:5] = 011	45	50	55	ms
		$t_{BUS\_UCP\_TIMEOUT}$ = 100ms, set by Register 0x2B[7:5] = 100	90	100	110	ms
		$t_{BUS\_UCP\_TIMEOUT}$ = 400ms, set by Register 0x2B[7:5] = 101	360	400	440	ms
		$t_{BUS\_UCP\_TIMEOUT}$ = 1.5s, set by Register 0x2B[7:5] = 110	1.35	1.5	1.65	sec
		$t_{BUS\_UCP\_TIMEOUT}$ = 100s, set by Register 0x2B[7:5] = 111	90	100	110	sec
VDR OVP Accuracy	$V_{DR\_OVP\_ACC}$	Rising, VDR_OVP = 300mV, set by Register 0x05[4] = 0	245	300	355	mV
		Rising, VDR_OVP = 400mV, set by Register 0x05[4] = 1	345	400	455	
VDR OVP Deglitch time	$t_{VDR\_OVP\_DEG}$	VDR OVP Deglitch = 8μs, set by Register 0x05[3] = 0	--	8	--	μs
		VDR OVP Deglitch = 10ms, set by Register 0x05[3] = 1	--	5	--	ms
VOUT OVP Accuracy	$V_{OUT\_OVP\_ACC}$	Rising, VOUT_OVP = 4.9V	4.8	4.9	5	V
VOUT OVP Deglitch Time	$t_{VOUT\_OVP\_DEG}$		--	3	--	μs
TSBAT OTP Range	$T_{SBAT\_OTP\_RAN}$	Falling, TSBAT_OTP = TSBAT/VOUT, (VOUT<4.6V)	0	--	50	%
TSBAT OTP Step Size	$T_{SBAT\_OTP\_SIZE}$	Falling, TSBAT_OTP = TSBAT/VOUT, (VOUT < 4.6V)	--	0.1953	--	%
TSBAT OTP Accuracy	$T_{SBAT\_OTP\_ACC}$	Falling, TSBAT_OTP = TSBAT/VOUT, (VOUT < 4.6V)	–1	--	1	%
TSBUS OTP Range	$T_{SBUS\_OTP\_RAN}$	Falling, TSBUS _OTP = TSBUS /VOUT, (VOUT < 4.6V)	0	--	50	%
TSBUS OTP Step Size	$T_{SBUS\_OTP\_SIZE}$	Falling, TSBUS_OTP = TSBUS /VOUT, (VOUT < 4.6V)	--	0.1953	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TSBUS OTP Accuracy	$T_{SBUS\_OTP\_ACC}$	Falling, TSBUS _OTP = TSBUS /VOUT, (VOUT < 4.6V)	–1	--	1	%
Thermal Shutdown Threshold	$T_{DIE\_OTP\_TH}$		--	130	--	°C
Thermal Shutdown Deglitch Time	t_{TDIE_DEG}		--	3	--	µs
VBUS_HIGH_ERR Accuracy	$V_{BUS\_HIGH\_ERR\_ACC}$	Rising, VBUS_HIGH_ERR = VBUS/VOUT	2.328	2.4	2.472	V/V
VBUS_HIGH_ERR Deglitch	$t_{VBUS\_HIGH\_ERR\_DEG}$		--	32	--	µs
VBUS_LOW_ERR Accuracy	$V_{BUS\_LOW\_ERR\_ACC}$	Falling, VBUS_LOW_ERR = VBUS/VOUT	2	2.04	2.08	V/V
VBUS_LOW_ERR Deglitch	$t_{VBUS\_LOW\_ERR\_DEG}$	Set by Register 0x2E[4] = 0	--	10	--	µs
		Set by Register 0x2E[4] = 1	--	10	--	ms
Converter OCP Threshold	$I_{CON\_OCP\_TH}$	Rising, VOUT = 4V	--	16	--	A
CFLY Short Detect Level	R_{CFLY_DIAG}	If device detect the short resistance of flying capacitor smaller than this level while soft-start duration, the device will stop charging.	--	--	30	Ω
Alarm						
VBAT_OVP_ALM Range	$V_{BAT\_OVP\_ALM\_RAN}$	Rising	3.5	--	5.075	V
VBAT_OVP_ALM Step Size	$V_{BAT\_OVP\_ALM\_SIZE}$		--	25	--	mV
VBAT_OVP_ALM Hysteresis	$V_{BAT\_OVP\_ALM\_HY}$	Falling	--	50	--	mV
VBAT_OVP_ALM Accuracy	$V_{BAT\_OVP\_ALM\_ACC}$	VBAT_OVP_ALM = 3.5V to 4.5V	–20	--	20	mV
IBAT_OCP_ALM Range	$I_{BAT\_OCP\_ALM\_RAN}$	Rising	2	--	10	A
IBAT_OCP_ALM Step Size	$I_{BAT\_OCP\_ALM\_SIZE}$		--	100	--	mA
IBAT_OCP_ALM Hysteresis	$I_{BAT\_OCP\_ALM\_HY}$	Falling	--	100	--	mA
IBAT_OCP_ALM Accuracy	$I_{BAT\_OCP\_ALM\_ACC}$	IBAT_OCP_ALM = 3A to 8A	–200	--	200	mA
IBAT_UCP_ALM Range	$I_{BAT\_UCP\_ALM\_RAN}$	Falling	0	--	6.35	A
IBAT_UCP_ALM Step Size	$I_{BAT\_UCP\_ALM\_SIZE}$		--	50	--	mA
IBAT_UCP_ALM Hysteresis	$I_{BAT\_UCP\_ALM\_HY}$	Falling	--	50	--	mA
IBAT_UCP_ALM Accuracy	$I_{BAT\_UCP\_ALM\_ACC}$	IBAT_UCP_ALM = 3A	–200	--	200	mA
VBUS_OVP_ALM Range	$V_{BUS\_OVP\_ALM\_RAN}$	Rising	6	--	12.35	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS_OVP_ALM Step Size	$V_{BUS\_OVP\_ALM\_SIZE}$		--	50	--	mV
VBUS_OVP_ALM Hysteresis	$V_{BUS\_OVP\_ALM\_HY}$	Falling	--	50	--	mV
VBUS_OVP_ALM Accuracy	$V_{BUS\_OVP\_ALM\_ACC}$	VBAT_OVP_ALM = 6V to 9V	–35	--	35	mV
IBUS_OCP_ALM Range	$I_{BUS\_OCP\_ALM\_RAN}$	Rising	0	--	5	A
IBUS_OCP_ALM Step Size	$I_{BUS\_OCP\_ALM\_SIZE}$		--	50	--	mA
IBUS_OCP_ALM Hysteresis	$I_{BUS\_OCP\_ALM\_HY}$	Falling	--	50	--	mA
IBUS_OCP_ALM Accuracy	$I_{BUS\_OCP\_ALM\_ACC}$	IBUS_OCP = 1.5A to 4A	–250	--	250	mA
TSBAT_TSBUS_ALM Range	$T_{S\_OTP\_ALM\_RAN}$	Falling, TSBAT_TSBUS_ALM_Threshold = TSBAT_OTP + 5% or TSBAT_TSBUS_ALM_Threshold = TSBUS_OTP + 5%	0	--	50	%
TSBAT_TSBUS_ALM Hysteresis	$T_{S\_OTP\_ALM\_ALM\_HY}$	Rising	--	4	--	%
TSBAT_TSBUS_ALM Accuracy	$T_{S\_OTP\_ALM\_ACC}$		–1	--	1	%
TDIE_OTP_ALM Range	$T_{DIE\_OTP\_ALM\_RAN}$	Rising	0	--	152.5	°C
TDIE_OTP_ALM Step Size	$T_{DIE\_OTP\_ALM\_SIZE}$		--	0.5	--	°C
TDIE_OTP_ALM Hysteresis	$T_{DIE\_OTP\_ALM\_HY}$	Falling	--	10	--	°C
TDIE_OTP_ALM Accuracy	$T_{DIE\_OTP\_ALM\_ACC}$		–4	--	4	°C
ADC Specification						
ADC Sample Rate	f_{SAMPLE_RATE}	(Note 5)	1800	2000	2200	kHz
ADC Data Rate	t_{DATA_ADC}	12bit, 128 averages Report data for each channel (Note 5)	--	1.2	--	ms
VBUS ADC Range	$V_{BUS\_ADC\_RAN}$		0	--	14	V
VBUS ADC Accuracy	$V_{BUS\_ADC\_ACC}$	VBUS = 6V to 9V	–35	--	35	mV
IBUS ADC Range	$I_{BUS\_ADC\_RAN}$		0	--	5	A
IBUS ADC Accuracy	$I_{BUS\_ADC\_ACC}$	IBUS = 0A to 4A (0°C to 85°C)	–150	--	150	mA
VAC ADC Range	$V_{AC\_ADC\_RAN}$		0	--	14	V
VAC ADC Accuracy	$V_{AC\_ADC\_ACC}$	VAC = 6V to 9V	–35	--	35	mV
VOUT ADC Range	$V_{OUT\_ADC\_RAN}$		0	--	5	V
VOUT ADC Accuracy	$V_{OUT\_ADC\_ACC}$	VOUT = 3V to 4.5V	–20	--	20	mV
VBAT ADC Range	$V_{BAT\_ADC\_RAN}$		0	--	5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBAT ADC Accuracy	$V_{BAT\_ADC\_ACC}$	VBAT = 3V to 4.5V	–20	--	20	mV
IBAT ADC Range	$I_{BAT\_ADC\_RAN}$		0	--	10	A
IBAT ADC Accuracy	$I_{BAT\_ADC\_ACC}$	IBAT = 3A to 8A, RSEN = 0.002Ω	–200	--	200	mA
TDIE ADC Range	$T_{DIE\_ADC\_RAN}$		0	--	150	°C
TDIE ADC Accuracy	$T_{DIE\_ADC\_ACC}$		–4	--	4	°C
TSBUS ADC Range	$T_{SBUS\_ADC\_RAN}$		0	--	50	%
TSBUS ADC Accuracy	$T_{SBUS\_ADC\_ACC}$	TSBUS pin voltage = 0.2V to 2V	–1	--	1	%
TSBAT ADC Range	$T_{SBAT\_ADC\_RAN}$		0	--	50	%
TSBAT ADC Accuracy	$T_{BAT\_ADC\_ACC}$	TSBAT pin voltage = 0.2V to 2V	–1	--	1	%
Pull Down						
VAC Pull Down Resistor	R_{VAC_PD}		100	125	150	Ω
VAC Pull Down Time Out	t_{VAC_PD}		360	400	440	ms
VBUS Pull Down Resistor	R_{VBUS_PD}		0.6	1	1.4	kΩ
Watch Dog Time Out						
Watch Dog Time Out	WDT	No I^2C communication for 0.5s, set by Register 0x0b[1:0] = 00	0.475	0.5	0.525	sec
		No I^2C communication for 1s, set by Register 0x0b[1:0] = 01	0.95	1	1.05	
		No I^2C communication for 5s, set by Register 0x0b[1:0] = 10	4.75	5	5.25	
		No I^2C communication for 30s, set by Register 0x0b[1:0] = 11	27	30	33	
CDRVL Pull Low Resistance Setting						
Slave address = 0x66 (Standalone1)	R_{CDRVL}	CDRVL Pull low resistance to setting slave address	142.5	150	--	kΩ
Slave address = 0x65 (Standalone2)			71.25	75	78.75	
Slave address = 0x66 (Slave)			37.05	39	40.95	
Slave address = 0x65 (Master)			--	18	18.9	

I²C Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		1.5	--	--	V
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
SCL Clock Frequency	f_{CLK}	Standard-mode	--	--	100	kHz
		Fast-mode	--	--	400	
		Fast-mode Plus	--	--	1000	
		High-speed mode Cb = 400pF	--	--	1.7	MHz
		High-speed mode Cb = 100pF	--	--	3.4	
Bus Free Time between Stop and Start Condition	t_{BUF}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode Plus	0.5	--	--	
(Repeated) Start Hold Time	$t_{HD;STA}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
		High-speed mode Cb = 400pF	160	--	--	
		High-speed mode Cb = 100pF	160	--	--	
(Repeated) Start Setup Time	$t_{SU;STA}$	Standard-mode	4.7	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
		High-speed mode Cb = 400 pF	160	--	--	ns
		High-speed mode Cb = 100 pF	160	--	--	
STOP Condition Setup Time	$t_{SU;STO}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
		High-speed mode Cb = 400pF	160	--	--	ns
		High-speed mode Cb = 100pF	160	--	--	
SDA Data Hold Time	$t_{HD;DAT}$	Standard-mode	0.1	--	--	ns
		Fast-mode	0.1	--	--	
		Fast-mode Plus	0.1	--	--	
		High-speed mode Cb = 400pF	0.1	--	150	
		High-speed mode Cb = 100pF	0.1	--	70	
SDA Valid Acknowledge Time	$t_{VD;ACK}$	Standard-mode	--	--	3.45	µs
		Fast-mode	--	--	0.9	
		Fast-mode Plus	--	--	0.45	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA Setup Time	$t_{SU;DAT}$	Standard-mode	250	--	--	ns
		Fast-mode	100	--	--	
		Fast-mode Plus	50	--	--	
		High-speed mode Cb = 400pF	10	--	--	
		High-speed mode Cb = 100pF	10	--	--	
SCL Clock Low Time	t_{LOW}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode Plus	0.5	--	--	
		High-speed mode Cb = 400pF	320	--	--	ns
		High-speed mode Cb = 100pF	160	--	--	
SCL Clock High Time	t_{HIGH}	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
		High-speed mode Cb = 400pF	120	--	--	ns
		High-speed mode Cb = 100pF	60	--	--	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

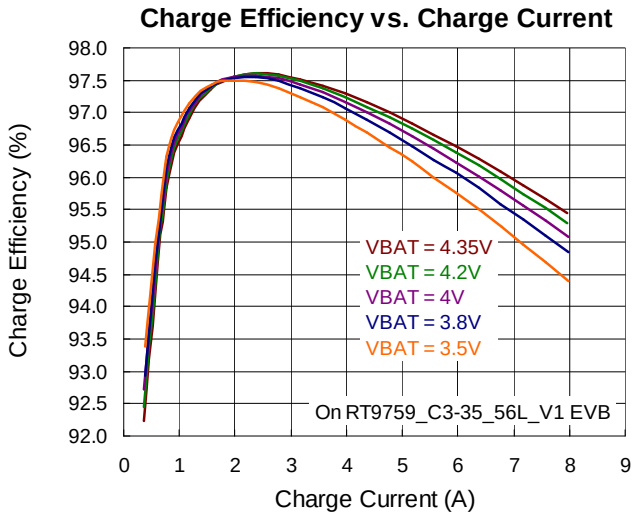
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

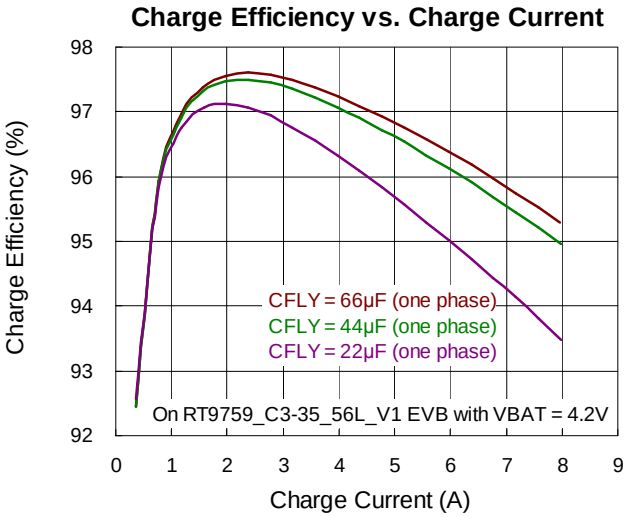
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

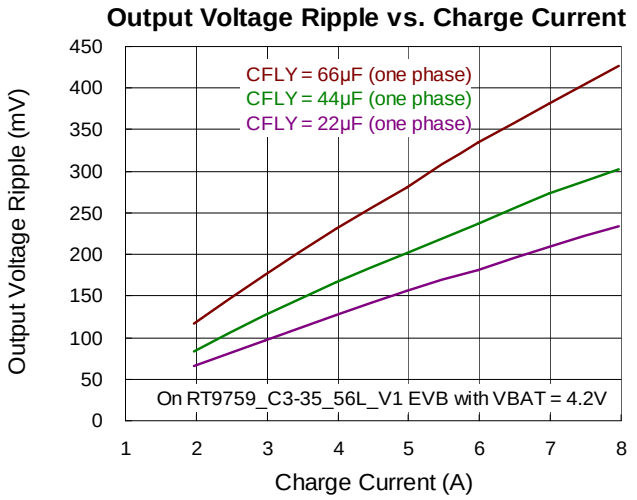
Note 4. The device is not guaranteed to function outside its operating conditions.

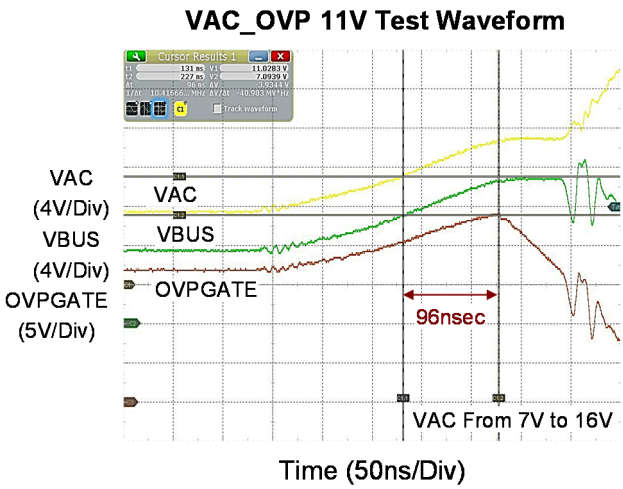
Note 5. Specification is guaranteed by design and/or correlation with statistical process control.

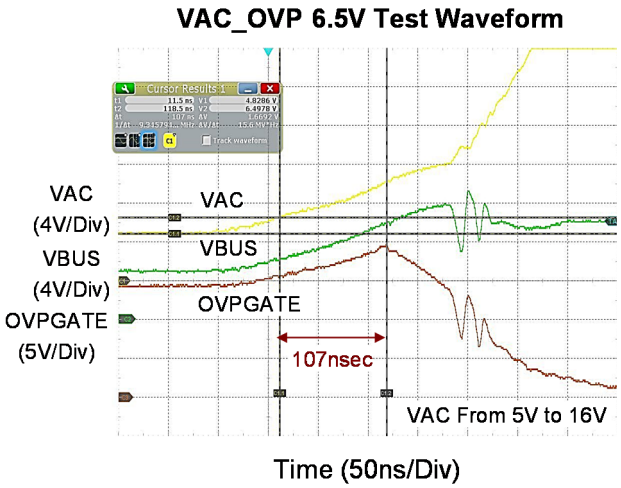
Typical Operating Characteristics











Register Descriptions

Register Map

Function Name	STAT	FLAG	MASK	Threshold	Enable	Deglitch
VBAT_OVP	0x10[7]	0x11[7]	0x12[7]	0x00[5:0]	0x00[7]	--
IBAT_OCP	0x10[6]	0x11[6]	0x12[6]	0x02[6:0]	0x02[7]	--
VAC_OVP	0x05[7]	0x05[6]	0x05[5]	0x05[2:0]	--	--
VDR_OVP	0x2C[1]	0x2D[5]	0x2D[1]	0x05[4]	--	0x05[3]
VBUS_OVP	0x10[5]	0x11[5]	0x12[5]	0x06[6:0]	--	--
IBUS_OCP	0x10[4]	0x11[4]	0x12[4]	0x08[3:0]	0x08[7]	--
IBUS_UCP_RISE	--	0x08[6]	0x08[5]	0x2B[2]	--	--
IBUS_UCP_FALL	--	0x08[4]	--	0x2B[2]	--	0x2E[3]
TDIE_OTP	0x0A[6]	0x0A[7]	--	--	0x0C[0]	--
VBUS_LOW_ERR	0x0A[5]	--	--	--	--	0x2E[4]
VBUS_HIGH_ERR	0x0A[4]	--	--	--	--	--
CFLY_DIAG_FLAG	--	0x0A[0]	--	--	--	--
VOUT_OVP	0x2C[0]	0x2D[4]	0x2D[0]	--	0x2B[3]	--
CON_OCP	--	0x0A[1]	--	--	--	--
IBUS_UCP_TIMEOUT	--	0x0A[3]	--	0x2B[7:5]	0x2B[7:5]	--
VAC_INSERT_STAT	0x0D[2]	0x0E[2]	0x0F[2]	--	--	--
VOUT_INSERT_STAT	0x0D[1]	0x0E[1]	0x0F[1]	--	--	--
WDT	--	0x0B[3]	--	0x0B[1:0]	0x0B[2]	--
ADC_DONE	0x0D[0]	0x0E[0]	0x0F[0]	--	--	--
VBUS_PD	--	--	--	--	0x06[7]	--
VAC_PD	--	--	--	--	0x2B[0]	--
CON_SWITCHING	0x0A[2]	--	--	--	--	--
TSBUS_OTP	0x10[1]	0x11[1]	0x12[1]	0x28[7:0]	0x0C[2]	--
TSBAT_OTP	0x10[2]	0x11[2]	0x12[2]	0x29[7:0]	0x0C[1]	--
VBAT_OVP_ALM	0x0D[7]	0x0E[7]	0x0F[7]	0x01[5:0]	0x01[7]	--
IBAT_OCP_ALM	0x0D[6]	0x0E[6]	0x0F[6]	0x03[6:0]	0x03[7]	--
IBAT_UCP_ALM	0x0D[3]	0x0E[3]	0x0F[3]	0x04[6:0]	0x04[7]	--
VBUS_OVP_ALM	0x0D[5]	0x0E[5]	0x0F[5]	0x07[6:0]	0x07[7]	--
TDIE_ALM	0x10[0]	0x11[0]	0x12[0]	0x2A[7:0]	--	--
IBUS_OCP_ALM	0x0D[4]	0x0E[4]	0x0F[4]	0x09[6:0]	0x09[7]	--
TSBUS_TSBAT_ALM_STAT	0x10[3]	0x11[3]	0x12[3]	--	--	--
IBAT_REG	0x2B[2]	0x2D bit6	0x2D[2]	0x2C[7:6]	--	--
VBAT_REG	0x2B[3]	0x2D bit7	0x2D[3]	0x2C[5:4]	--	--
Enable Regulation	--	--	--	--	0x2B[4]	--

Register Default Value

I²C Slave Address is 0x66 (Standalone1)

I²C Slave Address is 0x65 (Standalone2)

I²C Slave Address is 0x66 (Slave)

I²C Slave Address is 0x65 (Master)

Register (Hex)	standalone1 (Hex)	standalone2 (Hex)	Slave (Hex)	Master (Hex)
0x00	0x22	0x22	0xA2	0x22
0x01	0x1C	0x1C	0x9C	0x1C
0x02	0x3D	0x3D	0xBD	0x3D
0x03	0x3C	0x3C	0xBC	0x3C
0x04	0x28	0x28	0xA8	0x28
0x05	0x07	0x00	0x00	0x07
0x06	0x3A	0x3A	0x3A	0x3A
0x07	0x38	0x38	0xB8	0x38
0x08	0x0D	0x0D	0x0D	0x0D
0x09	0x50	0x50	0x50	0x50
0x0A	0x00	0x00	0x00	0x00
0x0B	0x40	0x40	0x40	0x40
0x0C	0x00	0x00	0x20	0x46
0x0D	0x00	0x00	0x00	0x00
0x0E	0x00	0x00	0x00	0x00
0x0F	0x00	0x00	0x00	0x00
0x10	0x00	0x00	0x00	0x00
0x11	0x00	0x00	0x00	0x00
0x12	0x00	0x00	0x00	0x00
0x13	0x00	0x00	0x00	0x00
0x14	0x00	0x00	0x00	0x00
0x15	0x00	0x00	0xF8	0x06
0x16	0x00	0x00	0x00	0x00
0x17	0x00	0x00	0x00	0x00
0x18	0x00	0x00	0x00	0x00
0x19	0x00	0x00	0x00	0x00
0x1A	0x00	0x00	0x00	0x00
0x1B	0x00	0x00	0x00	0x00
0x1C	0x00	0x00	0x00	0x00
0x1D	0x00	0x00	0x00	0x00
0x1E	0x00	0x00	0x00	0x00
0x1F	0x00	0x00	0x00	0x00
0x20	0x00	0x00	0x00	0x00
0x21	0x00	0x00	0x00	0x00

Register (Hex)	standalone1 (Hex)	standalone2 (Hex)	Slave (Hex)	Master (Hex)
0x22	0x00	0x00	0x00	0x00
0x23	0x00	0x00	0x00	0x00
0x24	0x00	0x00	0x00	0x00
0x25	0x00	0x00	0x00	0x00
0x26	0x00	0x00	0x00	0x00
0x27	0x00	0x00	0x00	0x00
0x28	0x15	0x15	0x15	0x15
0x29	0x15	0x15	0x15	0x15
0x2A	0xC8	0xC8	0xC8	0xC8
0x2B	0xE0	0xE0	0xE0	0xE0
0x2C	0x00	0x00	0x00	0x00
0x2D	0x00	0x00	0x00	0x00
0x2E	0x00	0x00	0x00	0x00

Default Reset for standalone1

R : Read only

R/W : Read and write

Register Address : 0x00, Register Name : VBAT_OVP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_DIS	0	N	Y	R/W	Battery over-voltage protection control. 0 : Enable (Default) 1 : Disable Default for slave = 1
6	Reversed	0	NA	NA	NA	Reversed
5:0	VBAT_OVP	100010	N	Y	R/W	Battery over-voltage protection threshold. VBAT_OVP = 3.5V + REG[5:0] x LSB LSB = 25mV Default = 4.35V

Register Address : 0x01, Register Name : VBAT_OVP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_ALM_DIS	0	N	Y	R/W	Battery over-voltage alarm control. 0 : Enable (Default) 1 : Disable Default for slave= 1
6	Reversed	0	NA	NA	NA	Reversed
5:0	VBAT_OVP_ALM	011100	N	Y	R/W	Battery over-voltage alam threshold. VBAT_OVP_ALM = 3.5V + REG[5:0] x LSB LSB = 25mV Default = 4.2V

Register Address : 0x02, Register Name : IBAT_OCP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBAT_OCP_DIS	0	N	Y	R/W	Battery over-current protection control. 0 : Enable (Default) 1 : Disable Default for slave = 1
6:0	IBAT_OCP	0111101	N	Y	R/W	Battery over-current protection threshold IBAT_OCP = 2A + REG[6:0] x LSB LSB = 100mA Default = 8.1A Any setting over 10A is set to 10A.

Register Address : 0x03, Register Name : IBAT_OCP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBAT_OCP_ALM_DIS	0	N	Y	R/W	Battery over-current alarm control. 0 : Enable (Default) 1 : Disable Default for slave = 1
6:0	IBAT_OCP_ALM	0111100	N	Y	R/W	Battery over-current alarm threshold IBAT_OCP_ALM = 2A + REG[6:0] x LSB LSB = 100mA Default = 8A

Register Address : 0x04, Register Name : IBAT_UCP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBAT_UCP_ALM_DIS	0	N	Y	R/W	IBAT_UCP_ALM disable bit 0 : Enable (Default) 1 : Disable Default for slave = 1
6:0	IBAT_UCP_ALM	0101000	N	Y	R/W	Battery under-current alarm threshold IBAT_UCP_ALM = REG[6:0] x LSB LSB = 50mA Default = 2A

Register Address : 0x05, Register Name : AC_PROTECTION

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VAC_OVP_STAT	0	N	N	R	Set 1 when a VAC_OVP event occurs. Persists until condition is no longer valid. 0 : No VAC_OVP Fault 1 : VAC_OVP Fault is occurring
6	VAC_OVP_FLAG	0	N	N	R	Set 1 when a VAC_OVP event occurs. Cleared upon read. 0 : No VAC_OVP Fault 1 : VAC_OVP Fault has occurred
5	VAC_OVP_MASK	0	N	Y	R/W	Mask VAC_OVP event to send $\overline{INT}$. 0 : Not masked (Default) 1 : Masked
4	VDR_OVP_THRESHOLD_SET	0	N	N	R/W	This is the voltage difference between VAC and VBUS that will cause the device to stop switching. 0 : 300mV (Default) 1 : 400mV
3	VDR_OVP_DEGLITCH_SET	0	N	Y	R/W	This is the deglitch time after the device reaches the VDR_OVP threshold before the part stops switching. 0 : 8μs (Default) 1 : 5ms
2:0	VAC_OVP	111	N	Y	R/W	000-110 setting is determined by VAC_OVP = 11V + VAC_OVP[3:0] x 1V Writing all 1 to these bits set the VAC_OVP to 6.5V. Default for slave = 000. Default for standalone2 = 000

Register Address : 0x06, Register Name : VBUS_OVP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBUS_PD_EN	0	N	Y	R/W	VBUS pull down resistor enable bit. 0 : Pull down disable (Default) 1 : Pull down enable
6:0	VBUS_OVP	0111010	N	Y	R/W	VBUS over-voltage protection threshold. VBUS_OVP = 6V + VBUS_OVP[6:0] x 50mV, Default = 8.9V

Register Address : 0x07, Register Name : VBUS_OVP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBUS_OVP_ALM_DIS	0	N	Y	R/W	VBUS over-voltage alarm disable bit. 0 : Enable (Default) 1 : Disable Default for slave = 1
6:0	VBUS_OVP_ALM	0111000	N	Y	R/W	VBUS over-voltage alarm threshold. VBUS_OVP_ALM = 6V + VBUS_OVP_ALM[6:0] x 50mV, Default : 8.8V

Register Address : 0x08, Register Name : IBUS_OCP_UCP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBUS_OCP_DIS	0	N	Y	R/W	IBUS_OCP_ALM disable bit 0 : Enable (Default) 1 : Disable
6	IBUS_UCP_RISE_FLAG	0	N	N	R	Set 1 and send an $\overline{\text{INT}}$ when IBUS current larger than IBUS_UCP_RISE threshold. Clear upon read. 0 : No IBUS_UCP_RISE 1 : IBUS_UCP_RISE event has occurred
5	IBUS_UCP_RISE_MASK	0	N	Y	R/W	Masks an IBUS_UCP_RISE event to send an $\overline{\text{INT}}$ 0 : Not masked (Default) 1 : Masked
4	IBUS_UCP_FALL_FLAG	0	N	N	R	Set 1 and send an $\overline{\text{INT}}$ when IBUS current smaller than IBUS_UCP_FALL threshold. Clear upon read. 0 : No IBUS_UCP_FALL 1 : IBUS_UCP_FALL event has occurred
3:0	IBUS_OCP	1101	N	Y	R/W	IBUS over-current protection threshold. IBUS_OCP = 1A + IBUS_OCP[3:0] x 250mA, Default : 4.25A

Register Address : 0x09, Register Name : IBUS_OCP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBUS_OCP_ALM_DIS	0	N	Y	R/W	IBUS_OCP_ALM disable bit. 0 : Enable (Default) 1 : Disable
6:0	IBUS_OCP_ALM	1010000	N	Y	R/W	IBUS over-current alarm threshold. IBUS_OCP_ALM[6:0] x 50mA Writing all 0's is 0A Default : 4A

Register Address : 0x0A, Register Name : CONVERTER_STATE

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	TDIE_OTP_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when die temperature higher than TDIE threshold. Clear upon read. 0 : Normal 1 : TDIE_OTP has occurred
6	TDIE_OTP_STAT	0	N	N	R	Set 1 when die temperature higher than TDIE threshold. Persists until condition is no longer valid. 0 : Normal 1 : TDIE_OTP is occurring
5	VBUS_LOW_ERR_STAT	0	N	N	R	Set 1 when VBUS voltage lower than VBUS_LOW_ERR threshold. Persists until condition is no longer valid. This status only active before switching. 0 : Normal 1 : VBUS_LOW_ERR is occurring
4	VBUS_HIGH_ERR_STAT	0	N	N	R	Set 1 when VBUS is higher than VBUS_HIGH_ERR threshold. Persists until condition is no longer valid. This status only active before switching. 0 : Normal 1 : VBUS_HGIH_ERR is occurring
3	IBUS_UCP_TIMEOUT_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when IBUS is not ramped to the IBUS_UCP_RISE threshold in IBUS_UCP_TIMEOUT time after CHG_EN = 1, Cleared upon read. 0 : Normal 1 : IBUS_UCP_TIMEOUT has occurred
2	SWITCHING_STAT	0	N	N	R	Set 1 and send an $\overline{INT}$ when the converter start switching and IBUS_UCP_TIMEOUT timer start. Only one $\overline{INT}$ is sent when switching starts. Persists until condition is no longer valid. 0 : Normal 1 : SWITCHING is occurring
1	CON_OCP_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when converter current larger than CON_OCP threshold. Clear upon read. 0 : Normal 1 : CON_OCP has occurred
0	CFLY_DIAG_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when CFLY short during converter soft-start. Clear upon read. 0 : Normal 1 : CFLY_DIG has occurred

Register Address : 0x0B, Register Name : CHG_CTL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	REG_RST	0	N	Y	R/W	Register reset 0 : No register reset (Default) 1 : Reset registers
6:5	FSW_SET	10	N	N	R/W	Set the switching frequency 00 : 250kHz 01 : 375kHz 10 : 500kHz (Default) 11 : 750kHz
4	Reserved	0	NA	NA	NA	Reserved
3	WDT_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when watchdog time out happen. Clear upon read. 0 : Normal 1 : WDT has occurred
2	WDT_DIS	0	N	Y	R/W	Watchdog disable 0 : Enabled (Default) 1 : Disabled
1:0	WDT_TIMER	00	N	Y	R/W	Watchdog timer setting. 00 : 0.5s (Default) 01 : 1s 10 : 5s 11 : 30s

Register Address : 0x0C, Register Name : CHG_CTL1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_EN	0	Y	Y	R/W	Charger control bit 0 : Charger disable (Default) 1 : Charge enable
6:5	MS	00	N	N	R	Master, Slave, or Standalone operation. 00 : Standalone 01 : Slave 1X : Master
4:3	CHG_FSHIFT	00	N	Y	R/W	Adjust switching frequency for EMI 00 : Nominal frequency (Default) 01 : Nominal frequency + 10% 10 : Nominal frequency - 10% 11 : Spread spectrum
2	TSBUS_OTP_DIS	0	N	Y	R/W	TSBUS over-temperature protection disable bit. 0 : Enable (Default) 1 : Disable Default for master = 1
1	TSBAT_OTP_DIS	0	N	Y	R/W	TSBAT over-temperature protection disable bit. 0 : Enable (Default) 1 : Disable Default for master = 1
0	TDIE_OTP_DIS	0	N	Y	R/W	TDIE over-temperature protection disable bit. 0 : Enable (Default) 1 : Disable

Register Address : 0x0D, Register Name : INT_STAT

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_ ALM_STAT	0	N	N	R	Set 1 when VBAT is higher than VBAT_OVP_ALM threshold. Persists until condition is no longer valid. 0 : Normal 1 : VBAT_OVP_ALM is occurring
6	IBAT_OCP_ ALM_STAT	0	N	N	R	Set 1 when IBAT is larger than IBAT_OCP_ALM threshold. Persists until condition is no longer valid. 0 : Normal 1 : IBAT_OCP_ALM is occurring
5	VBUS_OVP_ ALM_STAT	0	N	N	R	Set 1 when VBUS is higher than VBUS_OVP_ALM threshold. Persists until condition is no longer valid. 0 : Normal 1 : VBUS_OVP_ALM is occurring
4	IBUS_OCP_ ALM_STAT	0	N	N	R	Set 1 when IBUS is larger than IBUS_OCP_ALM threshold. Persists until condition is no longer valid. 0 : Normal 1 : IBUS_OCP_ALM is occurring
3	IBAT_UCP_ ALM_STAT	0	N	N	R	Set 1 when IBAT is smaller than IBAT_UCP_ALM threshold. Persists until condition is no longer valid. 0 : Normal 1 : IBAT_UCP_ALM is occurring
2	VAC_INSERT_ STAT	0	N	N	R	Set 1 when VAC voltage above the VAC_INSERT threshold 0 : Normal 1 : VAC_INSERT is occurring
1	VOUT_ INSERT_STAT	0	N	N	R	Set 1 when VOUT voltage above the VOUT_INSERT threshold 0 : Normal 1 : VOUT_INSERT is occurring
0	ADC_DONE_ STAT	0	N	N	R	Set 1 when the ADC conversion is completed in 1-shot mode. This bit will change to '0' when an ADC conversion is requested in 1-shot mode, and it will change back to '1' when the conversion is complete. During continuous conversion mode, this bit will be '0' 0 : Conversion not complete 1 : Conversion complete

Register Address : 0x0E, Register Name : INT_FLAG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP _ALM_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when VBAT higher than VBAT_OVP_ALM threshold. Clear upon read. 0 : Normal 1 : VBAT_OVP_ALM has occurred
6	IBAT_OCP_ ALM_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when IBAT larger than IBAT_OCP_ALM threshold. Clear upon read. 0 : Normal 1 : IBAT_OCP_ALM has occurred
5	VBUS_OVP_ ALM_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when VBUS higher than VBUS_OVP_ALM threshold. Clear upon read. 0 : Normal 1 : VBUS_OVP_ALM has occurred
4	IBUS_OCP_ ALM_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when IBUS larger than IBUS_OCP_ALM threshold. Clear upon read. 0 : Normal 1 : IBUS_OCP_ALM has occurred
3	IBAT_UCP_ ALM_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when IBAT smaller than IBAT_UCP_ALM threshold. Clear upon read. 0 : Normal 1 : IBAT_UCP_ALM has occurred
2	VAC_ INSERT_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when VAC higher than VAC_INSERT threshold. Clear upon read. 0 : Normal 1 : VAC_INSERT has occurred
1	VOUT_ INSERT_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when VOUT higher than VOUT_INSERT threshold. Clear upon read. 0 : Normal 1 : VOUT_INSERT has occurred
0	ADC_DONE _FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when ADC conversion is completed in 1-shot mode. Clear upon read. 0 : Normal 1 : Conversion completed

Register Address : 0x0F, Register Name : INT_MASK

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_ ALM_MASK	0	N	Y	R/W	VBAT_OVP_ALM mask. 0 : Not masked (Default) 1 : Masked
6	IBAT_OCP_ ALM_MASK	0	N	Y	R/W	IBAT_OCP_ALM mask. 0 : Not masked (Default) 1 : Masked
5	VBUS_OVP_ ALM_MASK	0	N	Y	R/W	VBUS_OVP_ALM mask. 0 : Not masked (Default) 1 : Masked
4	IBUS_OCP_ ALM_MASK	0	N	Y	R/W	IBUS_OCP_ALM mask. 0 : Not masked (Default) 1 : Masked
3	IBAT_UCP_ ALM_MASK	0	N	Y	R/W	IBAT_UCP_ALM mask. 0 : Not masked (Default) 1 : Masked
2	VAC_INSERT_ MASK	0	N	Y	R/W	VAC_INSERT mask. 0 : Not masked (Default) 1 : Masked
1	VOUT_ INSERT _MASK	0	N	Y	R/W	VOUT_INSERT mask. 0 : Not masked (Default) 1 : Masked
0	ADC_DONE_ MASK	0	N	Y	R/W	ADC_DONE mask. 0 : Not masked (Default) 1 : Masked

Register Address : 0x10, Register Name : FLT_STAT

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_STAT	0	N	N	R	Set 1 when VBAT is higher than VBAT_OVP threshold. Persists until condition is no longer valid. 0 : Normal 1 : VBAT_OVP is occurring
6	IBAT_OCP_STAT	0	N	N	R	Set 1 when IBAT is larger than IBAT_OCP threshold. Persists until condition is no longer valid. 0 : Normal 1 : IBAT_OCP is occurring
5	VBUS_OVP_STAT	0	N	N	R	Set 1 and send an $\overline{INT}$ when VBUS is higher than VBUS_OVP threshold. Persists until condition is no longer valid. 0 : Normal 1 : VBUS_OVP has occurred
4	IBUS_OCP_STAT	0	N	N	R	Set 1 when IBUS is larger than IBUS_OCP threshold. Persists until condition is no longer valid. 0 : Normal 1 : IBUS_OCP is occurring
3	TSBUS_TSBAT_OTP_ALM_STAT	0	N	N	R	Set 1 when the TSBUS or TSBAT threshold has been within 5% of the TSBUS_OTP or TSBAT_OTP set threshold. 0 : Normal 1 : TSBUS_TSBAT_OTP_ALM is occurring
2	TSBAT_OTP_STAT	0	N	N	R	Set 1 when the TSBAT lower than TSBUS_OTP set threshold 0 : Normal 1 : TSBUS_OTP is occurring
1	TSBUS_OTP_STAT	0	N	N	R	Set 1 when the TSBUS lower than TSBUS_OTP set threshold 0 : Normal 1 : TSBUS_OTP is occurring
0	TDIE_OTP_ALM_STAT	0	N	N	R	Set 1 when die temperature over TDIE_OTP_ALM threshold. Persists until condition is no longer valid. 0 : Normal 1 : TDIE_OTP_ALM is occurring

Register Address : 0x11, Register Name : FLT_FLAG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when VBAT is higher than VBAT_OVP threshold. Clear upon read. 0 : Normal 1 : VBAT_OVP has occurred
6	IBAT_OCP_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when IBAT is larger than IBAT_OCP threshold. Clear upon read. 0 : Normal 1 : IBAT_OCP has occurred
5	VBUS_OVP_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when VBUS is higher than VBUS_OVP threshold. Clear upon read. 0 : Normal 1 : VBUS_OVP has occurred
4	IBUS_OCP_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when IBUS is larger than IBUS_OCP threshold. Clear upon read. 0 : Normal 1 : IBUS_OCP has occurred
3	TSBUS_TSBAT_OTP_ALM_FLAG	0	N	N	R	Set 1 when the TSBUS or TSBAT threshold has been within 5% of the TSBUS_OTP or TSBAT_OTP set threshold. Clear upon read. 0 : Normal 1 : TSBUS_TSBAT_OTP_ALM has occurred
2	TSBAT_OTP_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when TSBAT lower than TSBAT_OTP threshold. Clear upon read. 0 : Normal 1 : TSBAT_OTP has occurred
1	TSBUS_OTP_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when TSBUS lower than TSBUS_OTP threshold. Clear upon read. 0 : Normal 1 : TSBUS_OTP has occurred
0	TDIE_OTP_ALM_FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when TDIE is higher than TDIE_OTP_ALM threshold. Clear upon read. 0 : Normal 1 : TDIE_OTP_ALM has occurred

Register Address : 0x12, Register Name : FLT_MASK

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_ MASK	0	N	Y	R/W	Masks a VBAT_OVP event to send an $\overline{INT}$. 0 : Not masked (Default) 1 : Masked
6	IBAT_OCP_ MASK	0	N	Y	R/W	Masks an IBAT_OCP event to send an $\overline{INT}$. 0 : Not masked (Default) 1 : Masked
5	VBUS_OVP_ MASK	0	N	Y	R/W	Masks a VBUS_OVP event to send an $\overline{INT}$. 0 : Not masked (Default) 1 : Masked
4	IBUS_OCP_ MASK	0	N	Y	R/W	Masks an IBUS_OCP event to send an $\overline{INT}$. 0 : Not masked (Default) 1 : Masked
3	TSBUS_ TSBAT_OTP_ ALM_MASK	0	N	Y	R/W	Masks a TSBUS_TSBAT_OTP_ALM event to send an INT. 0 : Not masked (Default) 1 : Masked
2	TSBAT_OTP_ MASK	0	N	Y	R/W	Masks a TSBAT_OTP event to send an $\overline{INT}$ 0 : Not masked (Default) 1 : Masked
1	TSBUS_OTP_ MASK	0	N	Y	R/W	Masks a TSBUS_OTP event to send an $\overline{INT}$ 0 : Not masked (Default) 1 : Masked
0	TDIE_OTP_ ALM_MASK	0	N	Y	R/W	Masks a TDIE_ALM_OTP event to send an $\overline{INT}$. 0 : Not masked (Default) 1 : Masked

Register Address : 0x13, Register Name : DEVICE_INFO

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	Device Revision	0000	N	N	R	Device Revision
3:0	Device ID	1000	N	N	R	Device ID 1000 = RT9759

Register Address : 0x14, Register Name : ADC_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ADC_EN	0	Y	Y	R/W	ADC control 0 : Disable (Default) 1 : Enable
6	ADC_RATE	0	N	Y	R/W	ADC conversion rate control 0 : Continuous mode (Default) 1 : 1-shot mode
5:1	Reversed	00000	NA	NA	NA	Reversed
0	IBUS_ADC_DIS	0	N	Y	R/W	IBUS_ADC control 0 : Enable conversion (Default) 1 : Disable conversion Default for slave = 1

Register Address : 0x15, Register Name : ADC_EN

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBUS_ADC_DIS	0	N	Y	R/W	VBUS ADC control bit. 0 : Enable (Default) 1 : Disable Default for slave = 1
6	VAC_ADC_DIS	0	N	Y	R/W	VBAT_ADC control bit. 0 : Enable (Default) 1 : Disable Default for slave = 1
5	VOUT_ADC_DIS	0	N	Y	R/W	VOUT ADC control bit. 0 : Enable (Default) 1 : Disable Default for slave = 1
4	VBAT_ADC_DIS	0	N	Y	R/W	VBAT ADC control bit. 0 : Enable (Default) 1 : Disable Default for slave = 1
3	IBAT_ADC_DIS	0	N	Y	R/W	IBAT_ADC control bit. 0 : Enable (Default) 1 : Disable Default for slave= 1
2	TSBUS_ADC_DIS	0	N	Y	R/W	TSBUS_ADC control bit. 0 : Enable (Default) 1 : Disable Default for Master = 1
1	TSBAT_ADC_DIS	0	N	Y	R/W	TSBAT_ADC control bit. 0 : Enable (Default) 1 : Disable Default for Master = 1
0	TDIE_ADC_DIS	0	N	Y	R/W	TDIE_ADC control bit. 0 : Enable (Default) 1 : Disable

Register Address : 0x16, Register Name : IBUS_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	NA	Reserved
6:0	IBUS_ADC1	0000000	N	N	R	IBUS ADC high byte HSB<6:0> : 16384mA, 8192mA, 4096mA, 2048mA, 1024mA, 512mA, 256mA

Register Address : 0x17, Register Name : IBUS_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	IBUS_ADC0	00000000	N	N	R	IBUS ADC low byte LSB<7:0> : 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA

Register Address : 0x18, Register Name : VBUS_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	NA	Reserved
6:0	VBUS_ADC1	0000000	N	N	R	VBUS ADC high byte HSB<6:0> : 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

Register Address : 0x19, Register Name : VBUS_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	VBUS_ADC0	00000000	N	N	R	VBUS ADC low byte LSB<7:0> : 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV

Register Address : 0x1A, Register Name : VAC_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	NA	Reserved
6:0	VAC_ADC1	0000000	N	N	R	VAC ADC high byte HSB<6:0> : 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

Register Address : 0x1B, Register Name : VAC_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	VAC_ADC0	00000000	N	N	R	VAC ADC low byte LSB<7:0> : 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV

Register Address : 0x1C, Register Name : VOUT_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	NA	Reserved
6:0	VOUT_ADC1	0000000	N	N	R	VOUT ADC high byte HSB<6:0> : 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

Register Address : 0x1D, Register Name : VOUT_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	VOUT_ADC0	00000000	N	N	R	VOUT ADC low byte LSB<7:0> : 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV

Register Address : 0x1E, Register Name : VBAT_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	NA	Reserved
6:0	VBAT_ADC1	0000000	N	N	R	VBAT ADC high byte HSB<6:0> : 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

Register Address : 0x1F, Register Name : VBAT_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	VBAT_ADC0	00000000	N	N	R	VBAT ADC low byte LSB<7:0> : 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV

Register Address : 0x20, Register Name : IBAT_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	NA	Reserved
6:0	IBAT_ADC1	0000000	N	N	R	IBAT ADC high byte HSB<6:0> : 16384mA, 8192mA, 4096mA, 2048mA, 1024mA, 512mA, 256mA

Register Address : 0x21, Register Name : IBAT_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	IBAT_ADC0	00000000	N	N	R	IBAT ADC low byte LSB<7:0> : 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA

Register Address : 0x22, Register Name : TSBUS_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:2	Reserved	000000	NA	NA	NA	Reserved
1:0	TSBUS_ADC1	00	N	N	R	TSBUS ADC high byte HSB<1:0> : 50%, 25%

Register Address : 0x23, Register Name : TSBUS_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	TSBUS_ADC0	00000000	N	N	R	TSBUS ADC low byte LSB<7:0> : 12.5%, 6.25%, 3.125%, 1.5625%, 0.78125%, 0.39063%, 0.19531%, 0.09766%

Register Address : 0x24, Register Name : TSBAT_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:2	Reserved	000000	NA	NA	NA	Reserved
1:0	TSBAT_ADC1	00	N	N	R	TSBAT ADC high byte HSB<1:0> : 50%, 25%

Register Address : 0x25, Register Name : TSBAT_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	TSBAT_ADC0	00000000	N	N	R	TSBAT ADC low byte LSB<7:0> : 12.5%, 6.25%, 3.125%, 1.5625%, 0.78125%, 0.39063%, 0.19531%, 0.09766%

Register Address : 0x26 Register Name : TDIE_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:1	Reserved	0000000	NA	NA	NA	Reserved
0	TDIE_ADC1	0	N	N	R	TDIE ADC high byte HSB<0> : 128°C

Register Address : 0x27 Register Name : TDIE_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	TDIE_ADC0	00000000	N	N	R	TDIE ADC low byte LSB<7:0> : 64°C, 32°C, 16°C, 8°C, 4°C, 2°C, 1°C, 0.5°C

Register Address : 0x28 Register Name : TSBUS_OTP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	TSBUS_OTP	00010101	N	Y	R/W	TSBUS Percentage Fault Threshold TSBUS_FLT = TSBUS_FLT[7:0] x 0.19531% Default = 4.1%

Register Address : 0x29 Register Name : TSBAT_OTP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	TSBAT_OTP	00010101	N	Y	R/W	TSBAT Percentage Fault Threshold TSBAT_FLT = TSBAT_FLT[7:0] x 0.19531% Default = 4.1%

Register Address : 0x2A Register Name : TDIE_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	TDIE_ALM	11001000	N	Y	R/W	TDIE alarm fault threshold setting TDIE_ALM = 25°C + REG[7:0] x 0.5°C Default = 125°C

Register Address : 0x2B, Register Name : REG_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	IBUS_UCP_ TIMEOUT	111	N	N	R/W	Adjustable timeout for IBUS to rise to IBUS_UCP_RISE threshold. 000 : Timeout disabled 001 : 12.5ms 010 : 25ms 011 : 50ms 100 : 100ms 101 : 400ms 110 : 1.5s 111 : 100s (Default)
4	REG_EN	0	N	N	R/W	Enables the device to regulate the output based on VBAT_OVP and IBAT_OCP thresholds. 0 : Disable (Default) 1 : Enable
3	VOUT_OVP_ DIS	0	N	N	R/W	VOUT over-voltage control bit. 0 : Enable (Default) 1 : Disable
2	IBUS_UCP_ RISE_ THRESH	0	N	N	R/W	This bit is set the threshold IBUS_UCP_RISE threshold. The system should control the IBUS current rise to IBUS_UCP_RISE within the IBUS_UCP_TIMEOUT. 0 : 300mA rising, 150mA falling (Default) 1 : 500mA rising, 250mA falling
1	IBAT_RSEN	0	N	N	R/W	This bit selects the external battery current sense resistor value. 0 : 2mΩ (Default) 1 : 5mΩ
0	VAC_PD_EN	0	N	N	R/W	VAC pull down resistor control bit. 0 : Disable (Default) 1 : Enable

Register Address : 0x2C, Register Name : REG_THRESHOLD

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	IBAT_REG	00	N	N	R/W	These two bits set the threshold below IBAT_OCP where the part starts regulation. 00 : 200mA below IBAT_OCP setting (Default) 01 : 300mA below IBAT_OCP setting 10 : 400mA below IBAT_OCP setting 11 : 500mA below IBAT_OCP setting
5:4	VBAT_REG	00	N	N	R/W	These two bits set the threshold below VBAT_OVP where the part starts regulation. 00 : 50mV below VBAT_OVP setting (Default) 01 : 100mV below VBAT_OVP setting 10 : 150mV below VBAT_OVP setting 11 : 200mV below VBAT_OVP setting
3	VBAT_REG_STAT	0	N	N	R	Set 1 when VBAT_REG is active. Persists until condition is no longer valid. 0 : Normal 1 : VBAT_REG is occurring
2	IBAT_REG_STAT	0	N	N	R	Set 1 when IBAT_REG is active. Persists until condition is no longer valid. 0 : Normal 1 : IBAT_REG is occurring
1	VDR_OVP_STAT	0	N	N	R	Set 1 when the voltage difference between VAC and VBUS is higher than VDR_OVP threshold. Persists until condition is no longer valid. 0 : Normal 1 : VDR_OVP is occurring
0	VOUT_OVP_STAT	0	N	N	R	Set 1 when the VOUT is higher than VOUT_OVP threshold. Persists until condition is no longer valid. 0 : Normal 1 : VOUT_OVP is occurring

Register Address : 0x2D, Register Name : REG_FLAG_MASK

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_REG_ FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when VBAT_REG has been active. Clear upon read. 0 : Normal 1 : VBAT_REG has occurred
6	IBAT_REG_ FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when IBAT_REG has been active. Clear upon read. 0 : Normal 1 : IBAT_REG has occurred
5	VDR_OVP_ FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when VDR_OVP has occurred. Clear upon read. 0 : Normal 1 : VDR_OVP has occurred
4	VOUT_OVP_ FLAG	0	N	N	R	Set 1 and send an $\overline{INT}$ when VOUT_OVP has occurred. Clear upon read. 0 : Normal 1 : VOUT_OVP has occurred
3	VBAT_REG_ MASK	0	N	Y	R/W	Masks an VBAT_REG event to send an $\overline{INT}$ 0 : Not masked (Default) 1 : Masked
2	IBAT_REG_ MASK	0	N	Y	R/W	Masks an IBAT_REG event to send an $\overline{INT}$ 0 : Not masked (Default) 1 : Masked
1	VDR_OVP_ MASK	0	N	Y	R/W	Masks an VDR_OVP event to send an $\overline{INT}$ 0 : Not masked (Default) 1 : Masked
0	VOUT_OVP_ MASK	0	N	Y	R/W	Masks an VOUT_OVP event to send an $\overline{INT}$ 0 : Not masked (Default) 1 : Masked

Register Address : 0x2E, Register Name : REG_STAT_FLAG_MASK

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	Reversed	000	NA	NA	NA	Reversed
4	VBUS_LOW_ ERR_DEGLIT CH_SET	0	N	Y	R/W	This bit sets the deglitch time for VBUS_LOW_ERR 0 : 10μs (Default) 1 : 10ms
3	IBUS_UCP_ FALL_DEGLTI CH_SET	0	N	Y	R/W	This bit sets the deglitch time for VBUS_UCP_FALL 0 : 10μs (Default) 1 : 5ms
2:0	Reversed	000	NA	NA	R/W	Reversed

Application Information

Operation Principle

The cap divider topology relies on a smart wall adapter to control the voltage and current of input in order to charge. Based on the cap divider topology, the 4 MOSFETs (Q1 to Q4) are used to charge and discharge flying capacitor (CFLY) alternately. The simplified circuit of cap divider is shown in Figure 1.

In period 1: When Q1 and Q3 are turned on and Q2 and Q4 are turned off, the CFLY and BAT are in series with VBUS. The BUS current is supplied to COUT and BAT directly. During this period, the voltage of CFLY can be expressed as equation 1 :

VCFLY = VBUS - VBAT ---- (1)

In period 2 : When Q1 and Q3 are turned off and Q2 and Q4 are turned on, the CFLY and BAT are in parallel. The current of BAT is only supplied by CFLY. During this period, the voltage of CFLY can be expressed as equation 2 :

VCFLY = VBAT ---- (2)

If the equation 2 is substituted into equation 1, the equation 1 can be expressed as equation 3 :

VBAT = VBUS / 2 ---- (3)

If the power dissipation of topology is ignored, the output power can be expressed as equation 4 :

VBAT x IBAT = VBUS x IBUS --- (4)

If the equation 3 is substituted into equation 4, the IBAT can be expressed as equation 5 :

IBAT = 2 x IBUS --- (5)

According to the equations above, the battery voltage is half of the input voltage and the current flow into the battery is twice the input current in cap divider topology. For the efficiency and output ripple improvement in application, the dual phase cap divider topology with phase shift 180-degree between phases are built in the RT9759.

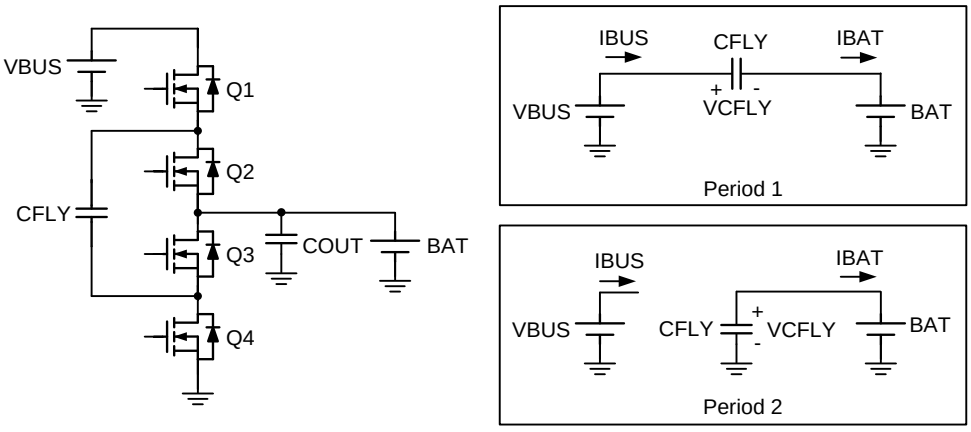


Figure 1. Simplified Circuit of Cap Divider

Charge System Introduction

The RT9759 is a smart cap divider charger used in slave charger application. The RT9759 generates high output current with cap divider topology. Before enabling the RT9759, the host set up all of protection and alarm functions and disable main charger in power solution. The host must monitor the alarms that set up in RT9759 during high current charging period and communicate with the smart wall adapter to control the charging current flow into the battery.

The Figure 2 is the simplified charge system block. In this charge system, the switching charger is used to detect USB BC1.2 of adapter and the PD controller is used to communicate with adapter by PD protocol. Once the smart wall adapter is detected, the AP will control the switching charger and smart cap divider charger to achieve high current charging period. These devices can communicate with each other through I^2C serial interface.

The charge profile of high capacity battery using switching charger and cap divider charger is shown in Figure 3. In order to achieve the charge profile, the switching charger is required to dominate pre-charge, fast charge when battery voltage is lower than system startup voltage, constant voltage and termination periods, respectively. The cap divider charger is used to achieve fast charge period. To shorten the constant voltage period, the cap divider charger is controlled to reduce the charge current by ramp step when battery voltage triggers the BAT_OVP_ALM.

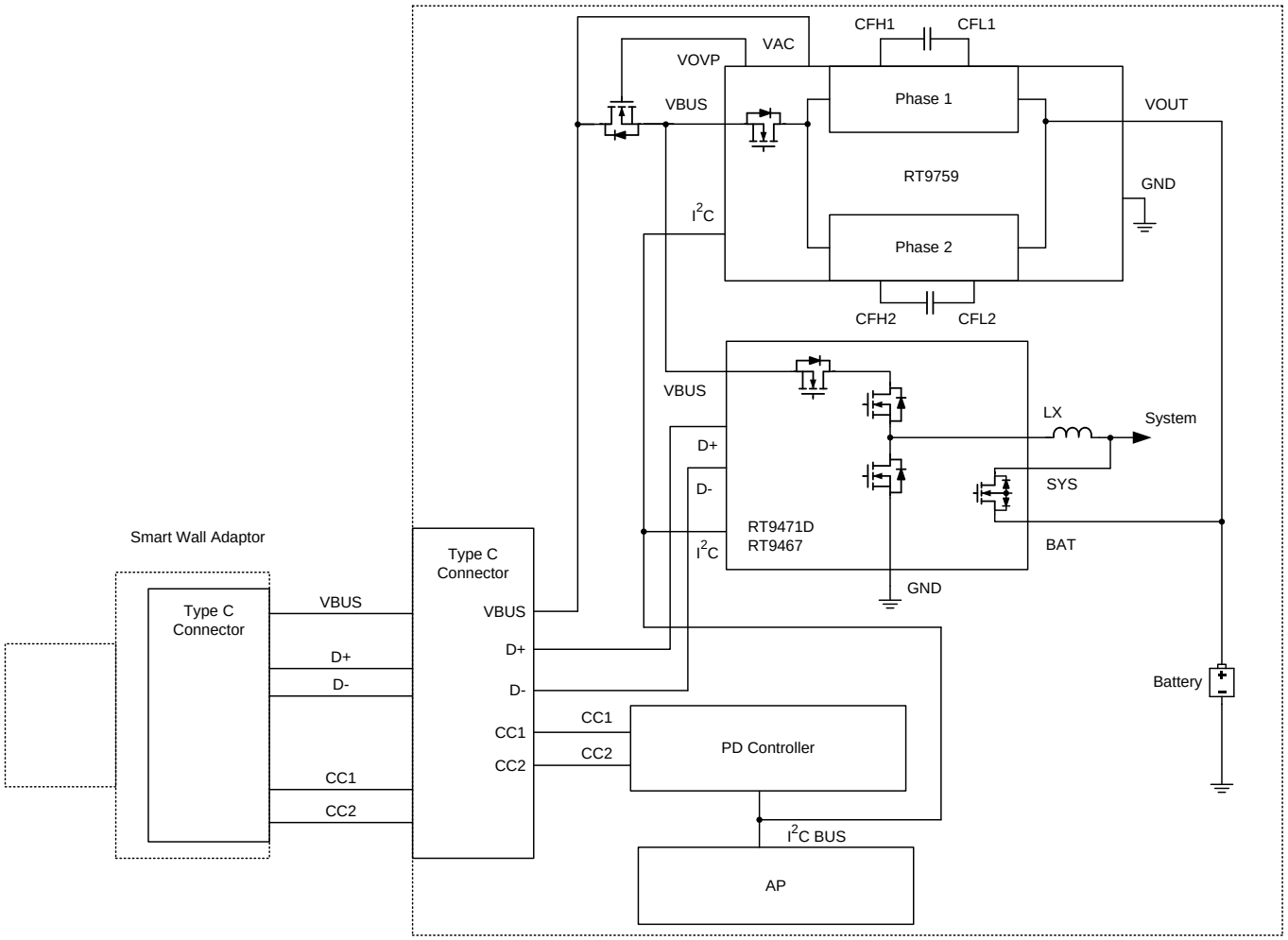


Figure 2. Simplified Charge System

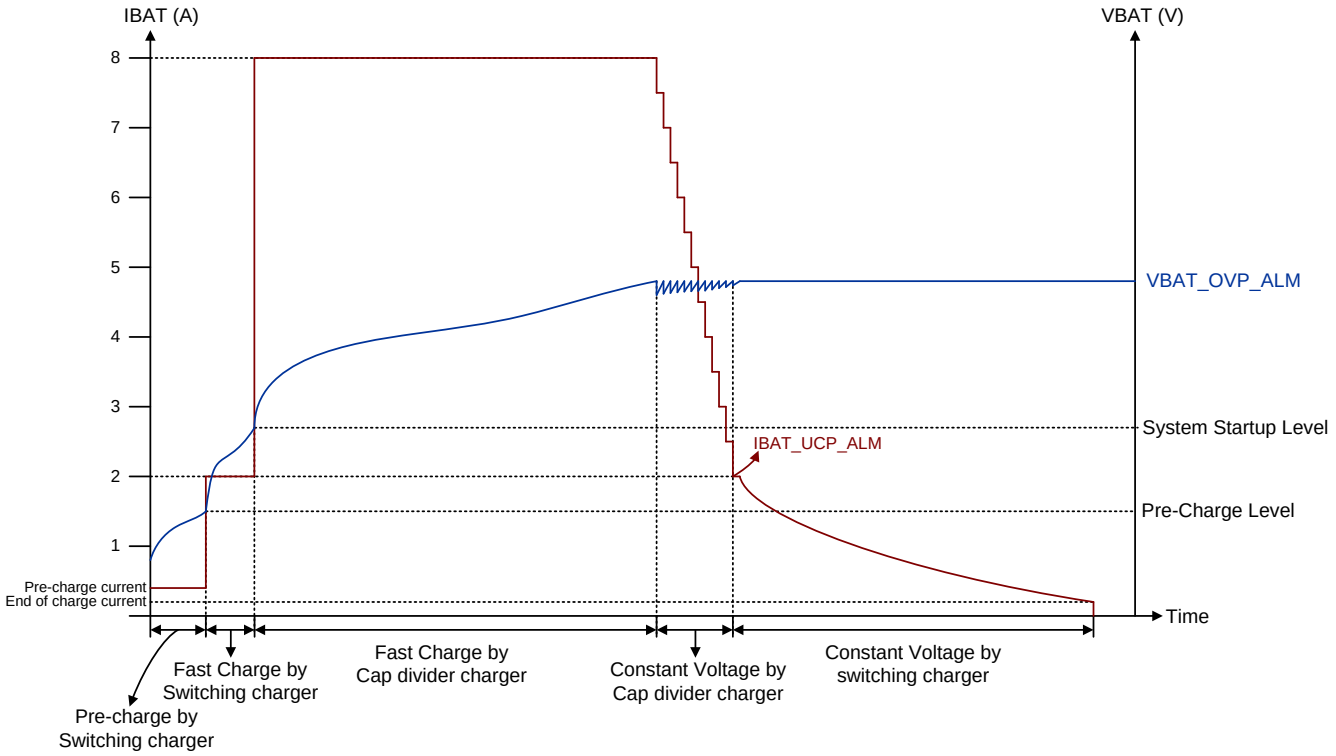


Figure 3. Charge Profile using Switching Charger and Cap Divider Charger

While the RT9759 is charging, host needs to communicate with smart wall adapter to control the charging current provided by the RT9759. The communication flow between smart wall adapter and charge system is shown in Figure 4. In order to prevent abnormal events when charging, the RT9759 is established with many adjustable protections and alarm functions. All alarms and protections are activated in specific operation condition that are shown in Table 2 and Table 4, respectively.

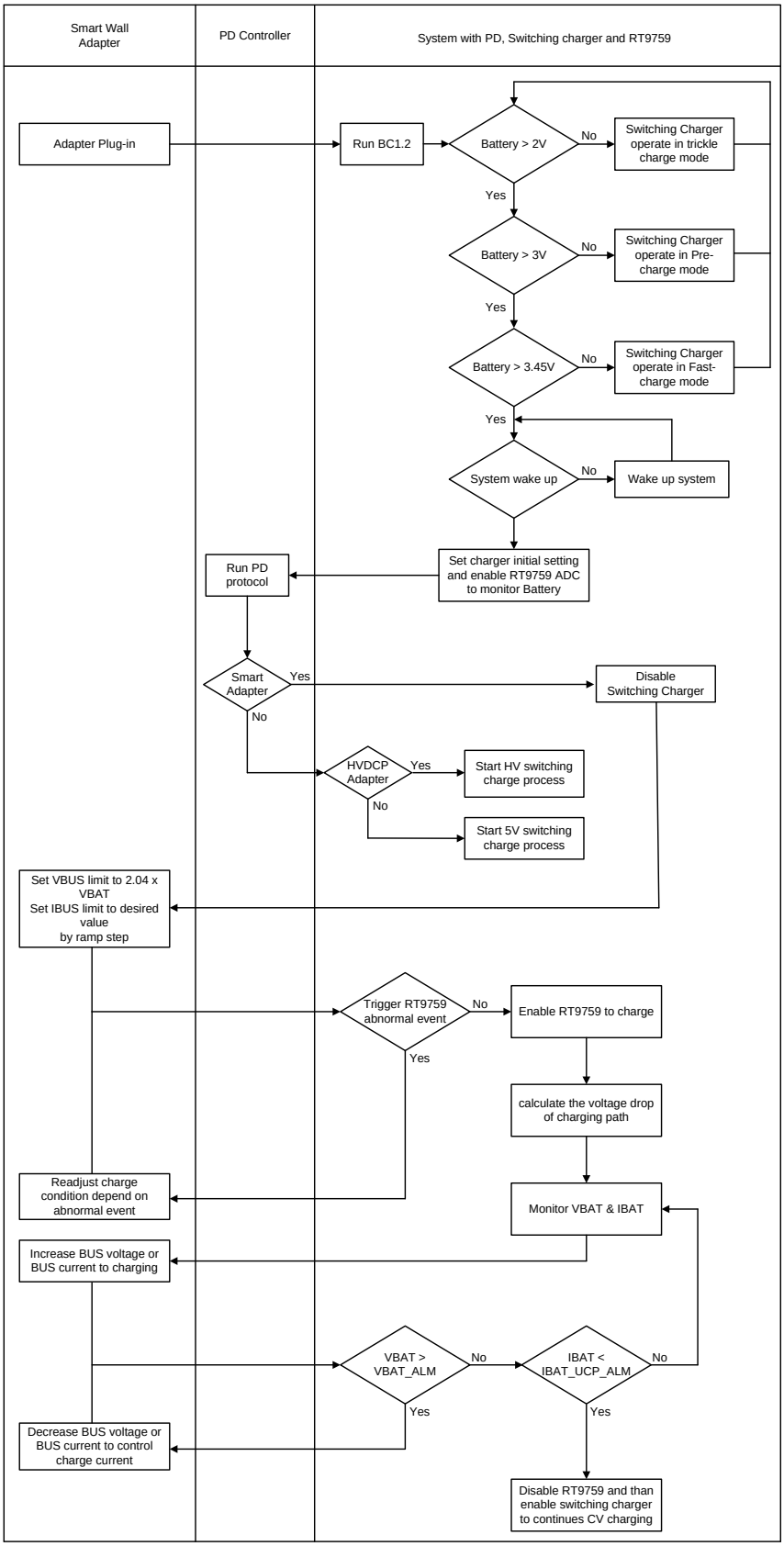


Figure 4. System Control Flow Chart

Device Power Up

The device is powered by VDDA. When VDDA voltage is higher than VDDA_UVLO Threshold, the device will start working. The VDDA voltage can be powered by either VBUS or VOUT and that is dominated by the higher voltage level.

Once the RT9759 is powered, the device will active the address detection mechanism to assign the slave address of device and configuration mode. The slave address of device and configuration mode are determined by resistance between CDRVL_ ADDRMS pin and GND. The criteria of CDRVL pull low resistance (R_{CDRVL}) is shown in electrical characteristics list. After address detection is finished, the host can communicate with the RT9759 by I^2C serial interface. Furthermore, the reaction time during VDDA > VDDA_UVLO to I^2C release (t_{VDDA_START}) is around 64 msec.

The RT9759 includes a watch dog timer that is enabled by default. If the device is not read or written before watch dog timer timeout, only the ADC_EN and CHG_EN will be set to default value. Moreover, the watchdog timeout flag and /INT pulse will be triggered to inform the host.

If the VOUT is not higher than VOUT_INSERT rising threshold, the charge can't be enabled. Once VOUT exceeds VOUT_INSERT rising threshold, the minimum allowable VOUT for enable charge is VOUT_INSERT falling threshold. Before charge enable, the RT9759 can report ADC information while the ADC is enabled. After charge enable, the RT9759 still can report ADC information whether the ADC is enabled or not.

In order to reduce quiescent current, most of sensing circuit inside the RT9759 will be turned off after address detection is finished and ADC_EN and CHG_EN are disabled for 500ms. In other words, part of protections and insert function are still activated before disabling device sensing circuit. The Figure 5 shows the device power on flow with protections and insert function activation list in each state. The VBAT_OVP, VOUT_OVP, VBUS_OVP, TDIE_OTP, VBUS_HIGH _ERR, VBUS_LOW_ERR, VOUT_INSERT and VAC_ INSERT function are still active before sensing circuits are turned off. When the device disable sensing circuit, all of protections and VOUT_INSERT are disabled except VAC_INSERT. Because the VAC_OVP function is independent circuit inside the RT9759, the activation state about VAC_OVP is excluded in Figure 5 and the detail about VAC_OVP will be described in protection feature section.

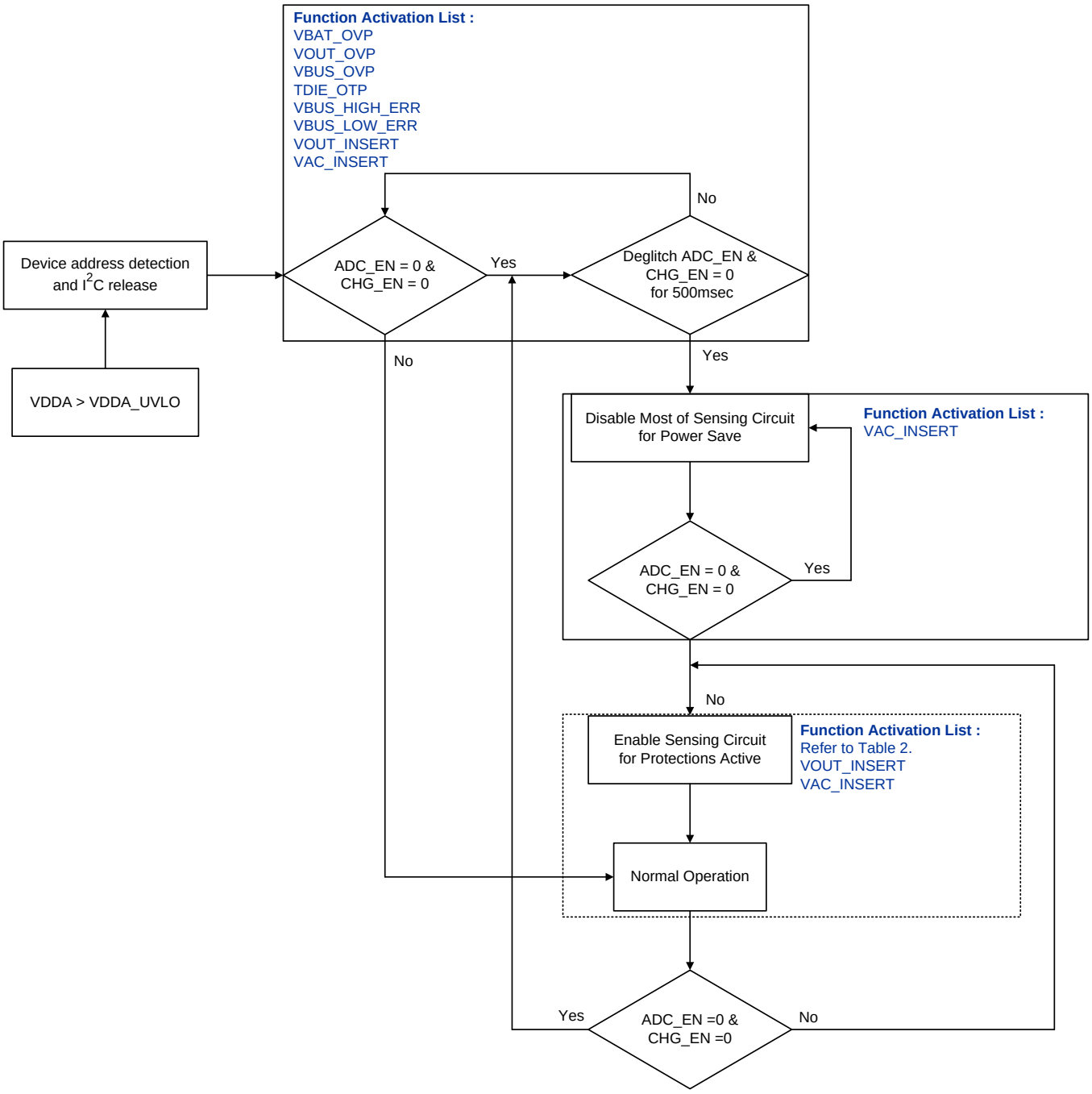


Figure 5. Device Power On Flow with Protections and Insert Function Activation List

9-Channel Analog to Digital Converter

The RT9759 integrates 9-Cannel ADC conversion for users to monitor input and output status of the device. The ADC function is allowed to operate if VDDA > VDDA_UVLO. Without this condition, the RT9759 will reset ADC_EN to disable. The ADC function can operate in continuous mode or 1-shot mode. Users can enable ADC function and select conversion mode via I^2C serial interface control (0x0C). In continuous mode, the ADC function will convert all ADC channel and report ADC data to related registers (0x16 to 0x27) continuously. In 1-shot mode, ADC function will reset ADC_EN bit to 0 after converting each ADC channel. Each ADC channel can be enabled or disabled via I^2C serial interface control (0x14 to 0x15). The device uses ADC conversion data to detect all alarm function, TSBAT_OTP and TSBUS_OTP protection. Due to this feature, the ADC function will be forced to convert each ADC channel with continuous mode and ADC cannot be controlled via register after charging. The Figure 6 is ADC function operation flow chart; Users can follow the flow chart to control ADC function. While reading the data of registers 0x16 to 0x27, high byte has to be read firstly, and then the following is low byte. Moreover, high byte and low byte have to be read with I^2C multi-byte reading method in one transmission, which is terminated with one STOP condition.

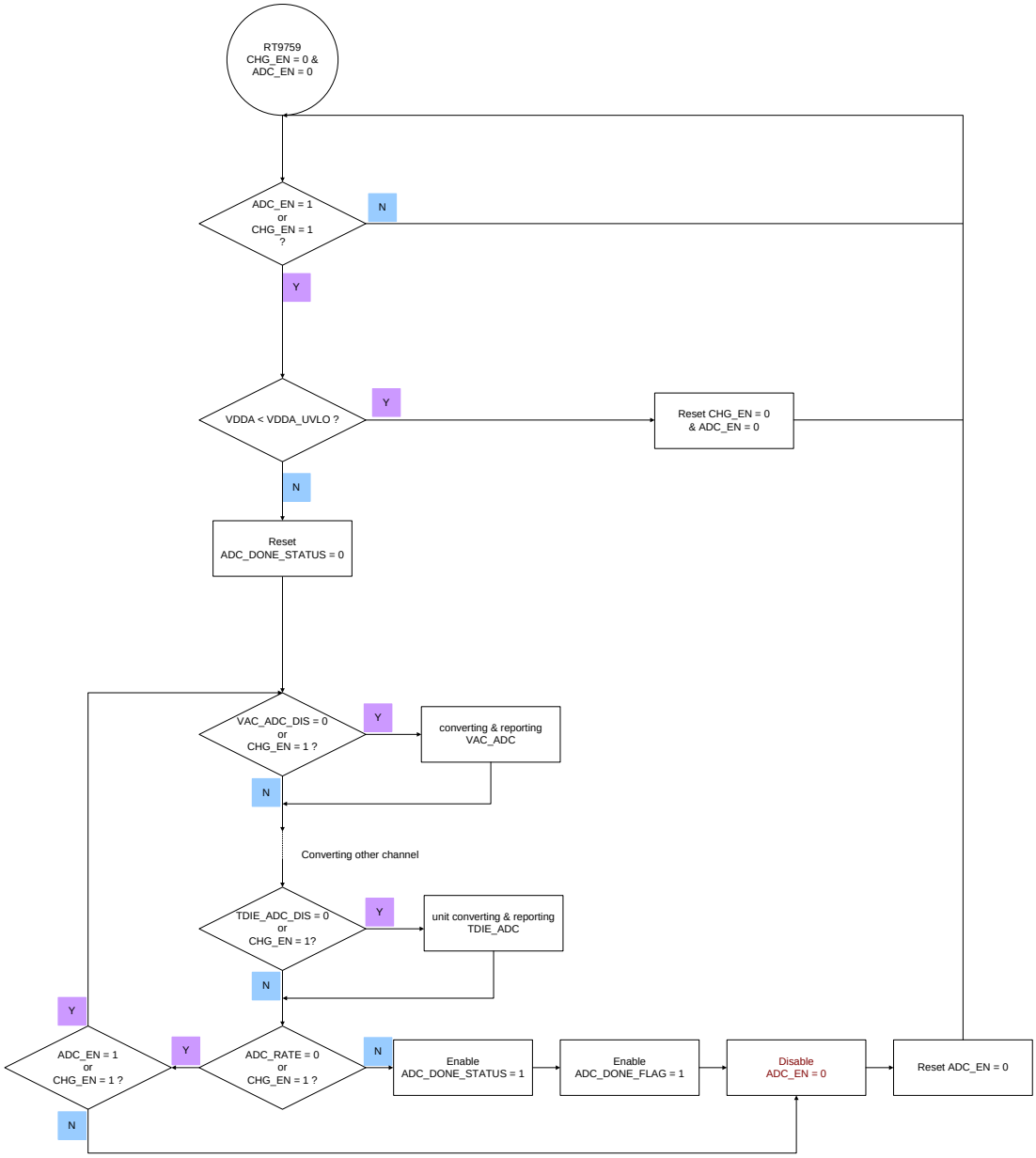


Figure 6. ADC Function Operation Flow Chart

Protection Feature

The RT9759 integrates 15 protections to protect device charging in unexpected condition. All protection activations are based on CHG_EN and ADC_EN bit except VAC_OVP. Users need to set CHG_EN or ADC_EN bit to 1 to enable related protection. Table 2 shows the enable condition and protect method for each protection.

Table 2. Protection Function Activation List

Protection Function	Enable Condition	Protection Method
VAC_OVP	VAC > VAC_INSERT	Turn off Q1 and Reset CHG_EN = 0
VBUS_OVP	CHG_EN = 1 or ADC_EN =1	Reset CHG_EN = 0
VBAT_OVP	CHG_EN = 1 or ADC_EN = 1	Reset CHG_EN = 0
VOUT_OVP	CHG_EN = 1 or ADC_EN =1	Reset CHG_EN = 0
IBUS_OCP	CHG_EN = 1	Reset CHG_EN = 0
IBUS_UCP	CHG_EN = 1	Reset CHG_EN = 0
IBAT_OCP	CHG_EN = 1	Reset CHG_EN = 0
TDIE_OTP	CHG_EN = 1 or ADC_EN = 1	Reset CHG_EN = 0
TSBUS_OTP	CHG_EN = 1 or ADC_EN = 1	Reset CHG_EN = 0
TSBAT_OTP	CHG_EN = 1 or ADC_EN = 1	Reset CHG_EN = 0
VDR_OVP	CHG_EN = 1	Reset CHG_EN = 0
CFLY_DIAG	CHG_EN = 1	Reset CHG_EN = 0
CON_OCP	CHG_EN = 1	Reset CHG_EN = 0
VBUS_LOW_ERR	CHG_EN = 1 (before switching) or ADC_EN = 1	Reset CHG_EN = 0
VBUS_HIGH_ERR	CHG_EN = 1 (before switching) or ADC_EN = 1	Reset CHG_EN = 0

- **VAC Pin Over-Voltage Protection (VAC_OVP)**

  The RT9759 integrates VAC_OVP function to monitor adaptor voltage by VAC pin and control external MOSFET by OVPGATE pin. The VAC_OVP function is powered by VAC pin, it will be enabled if VAC voltage is higher than VAC_INSERT. The device will provide a $V_{OVPGATE}$ voltage to turn on external MOSFET if VAC is higher than VAC_INSERT for a $t_{VAC\_INSERT\_DEG}$ time. If the VAC voltage is higher than VAC_OVP threshold, the device will start to turn off external MOSFET after a $t_{VAC\_OVP\_RE}$ time and it will turn off the external MOSFET within $t_{VAC\_OVP\_OFF}$ time. The Figure 7 shows the timing of VAC_OVP function. Users should make sure the adaptor voltage will not be higher than absolute maximum rating of VAC pin and external MOSFET (prevented by external TVS or...etc.).

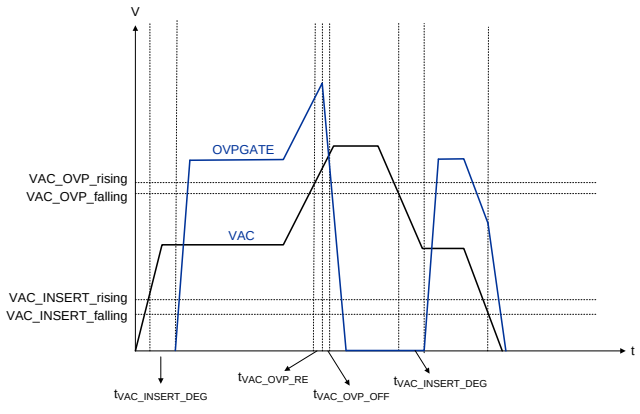


Figure 7. OVPGATE Operation Timing

- **VBUS Charge Voltage Protection (VBUS_HIGH_ERR and VBUS_LOW_ERR)**

  The device integrates VBUS_HIGH_ERR and VBUS_LOW_ERR to prevent users from adjusting wrong VBUS for charge. In no charge condition, if VBUS is higher than VBUS_HIGH_ERR threshold or VBUS lower than VBUS_LOW_ERR threshold, the device will force CHG_EN bit to disable. Both of VBUS_HIGH_ERR and VBUS_LOW_ERR will be disabled after the device successfully start to charge.

- **Input and Output Over-Voltage Protection (VBUS_OVP, VOUT_OVP, VBAT_OVP)**

  The device has VBUS_OVP, VBAT_OVP and VOUT_OVP function to detect input and output charge voltage condition. If input and output charge voltage is higher than protection threshold, the device will turn off charger and reset CHG_EN to disable. The VBUS_OVP function monitors VBUS voltage by VBUS pin and the VOUT_OVP function monitors VOUT voltage by VOUT pin. In high charging current application, the EVB might have large voltage drop between the device and battery pack. For the application, the device integrates VBAT_OVP to monitor differential voltage between BATP and BATN. Users should connect 100Ω with BATP and BATN to battery pack to achieve remote sense for the device. Users can adjust the protected threshold of VBUS_OVP and VBAT_OVP by I^2C serial interface.

- **Input and Output Over-Current Protection (IBUS_OCP, IBAT_OCP)**

  The IBUS_OCP function monitors input current via Q0. If CHG_EN bit is enabled, the Q0 will turn on and IBUS_OCP will start detecting input current. If the IBUS is larger than IBUS_OCP threshold the device will stop charging and reset CHG_EN bit to disable. The IBAT_OCP function detect battery current via SRP and SRN pin. Users should connect a 2mΩ in series with battery pack. The SRN and SRP should connect on the resistor in parallel. The internal protector will convert the differential voltage of SRP and SRN to current value. The ratio between the differential voltage and current value can be determined by register setting. If the current value is larger than IBAT_OCP threshold, the device will stop charging and reset CHG_EN to disable. Users can adjust the IBUS_OCP and IBAT_OCP threshold via register setting.

- **Input Under-Current Protection (IBUS_UCP)**

  The device integrates IBUS_UCP function to prevent reverse current from battery to VBUS. The IBUS_UCP detect input current by Q0. The Figure 8 shows the flow chart of IBUS_UCP, the device enables IBUS_UCP_RISE threshold and counting timer after start charging. Once IBUS is larger than IBUS_UCP_RISE threshold, the device will stop counting timer and enable IBUS_UCP_FALL threshold. If the IBUS is smaller than IBUS_UCP_RISE and the timer already longer than IBUS_UCP_TIMEOUT, the device will enable IBUS_UCP_FALL threshold. After the device enables IBUS_UCP_FALL threshold, if the IBUS is smaller than IBUS_UCP_FALL threshold, the device will stop charging and reset CHG_EN to disable. The Figure 9 shows IBUS_UCP behavior in different application.

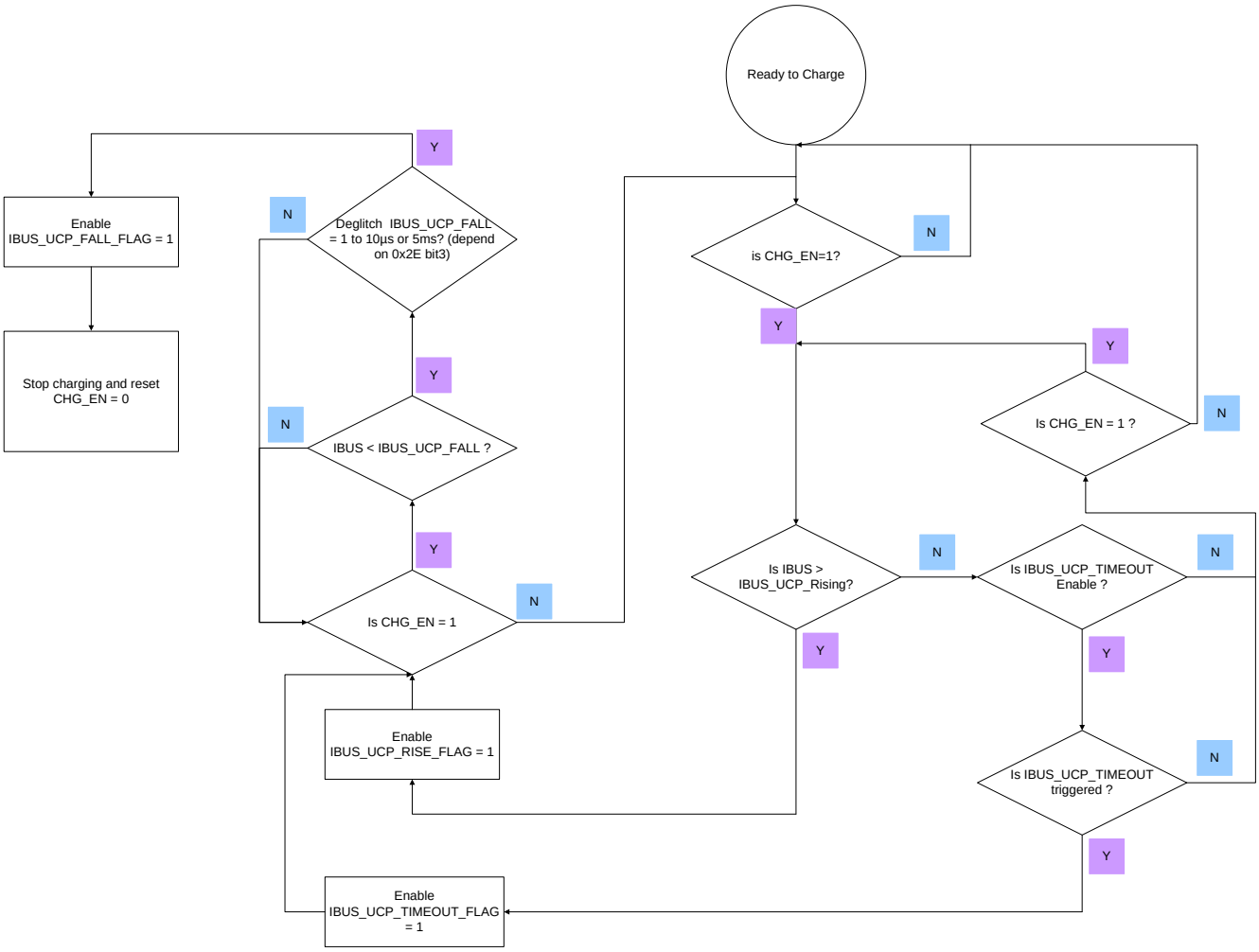


Figure 8. Flow Chart of IBUS_UCP Function

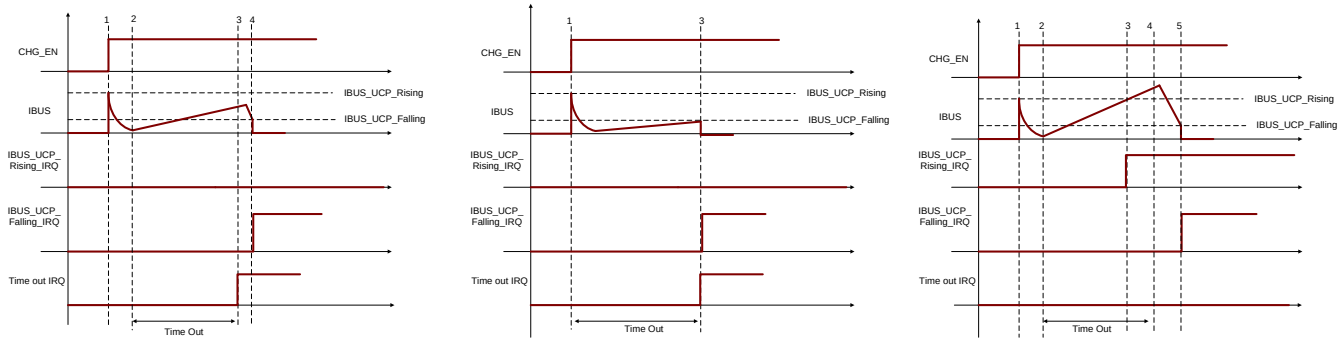
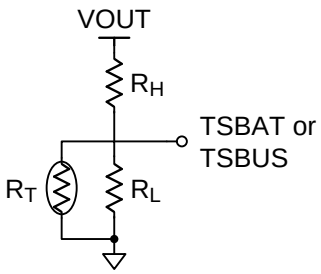


Figure 9. IBUS_UCP Behavior in Different Application

- **Device Thermal Shutdown (TDIE_OTP), BUS and BAT Over-Temperature Protection**

  The device integrates TDIE_OTP, TSBAT_OTP and TSBUS_OTP to prevent system charging in over-temperature condition. The TDIE_OTP function monitors die temperature of the device. If the die temperature is higher than TDIE_OTP threshold, the device will stop charging and reset CHG_EN bit to disable.

  The device monitors BUS connector and battery pack temperature by the voltage of TSBUS and TSBAT pin. Users should connect resistor divider on TSBAT and TSBUS pin. Both resistor divider should be pulled up to VOUT and a negative coefficient thermistor is parallel with the low side resistor. The protection threshold of TSBUS_OTP and TSBAT_OTP are according to TSBUS_ADC, TSBAT_ADC and VOUT_ADC data. Users should not disable TSBUS_ADC, TSBAT_ADC, VOUT_ADC if TS protection is active. The protection threshold is determined by the following equation. If the TS percentage is higher than protection threshold, the device will stop charging and reset CHG_EN to disable.



$$\text{TSVBUS or TSBAT (\%)} = \frac{\frac{1}{\left(\frac{1}{R_L}+\frac{1}{R_T}\right)}}{R_H + \frac{1}{\left(\frac{1}{R_L}+\frac{1}{R_T}\right)}}$$

- **Flying Capacitor Diagnose (CFLY_DIAG)**

  The device integrates CFLY_DIAG function to diagnose the health of flying capacitors. After CHG_EN is enabled, the device starts soft-start process in t_{SOFT_START}. In the soft-start process, the CFLY_DIAG function will diagnose the resistance between CFL and CFH for each phase. If the resistance is smaller than R_{CFLY_DIAG}, the device will stop soft-start process and reset CHG_EN to disable. If the device succeeds to start charging after soft-start process, the CFLY_DIAG function will stop activating. If the CFLY is short after soft-start, the device can be protected by other protections (ex. IBUS_OCP, VBAT_OVP, VOUT_OVP, CON_OCP….).

- **Converter Over-Current Protection (CON_OCP)**

  The device integrates CON_OCP function to detect the converter operating current. If the converter operating current is larger than CON_OCP threshold, the device will stop charging and reset CHG_EN to disable.

- **Dropout Voltage Protection (VDR_OVP)**

  When VBAT_REG or IBAT_REG is activated, it might cause a large voltage drop on external MOSFET. The large voltage drop might cause high power loss and a lot of heat in the system. In order to prevent the situation, the device integrates VDR_OVP function to monitor the voltage drop between VAC and VBUS pin. If the voltage drop is higher than VDR_OVP threshold, the device will stop charging and reset CHG_EN to disable. The threshold of VDR_OVP can be determined by register setting.

Regulation Feature

The device has VBAT_REG and IBAT_REG regulation functions to regulate instant current change and voltage change for the battery. Users can set the regulation threshold by register setting.

The VBAT_REG function monitors differential voltage between BATP and BATN pin. If the differential voltage is higher than VBAT_REG threshold, the device will control OVPGATE voltage to regulate charge current. IBAT_REG function convert the differential voltage between SRN and SRP to current value. If the current value is higher than IBAT_REG threshold, the device will control OVPGATE voltage to regulate charge current. If the regulation functions are triggered and persist for $t_{REG\_TIMEOUT}$, the device will stop charging and reset CHG_EN to disable. When regulation functions are triggered, system should adjust charging condition to prevent the device from triggering the $t_{REG\_TIMEOUT}$ and VDR_OVP.

Alarm Feature

The device integrates 7 alarm functions for system to monitor the charge condition. The alarm functions use the ADC conversion data to monitor the charge condition. Table 3 shows the relationship between alarm functions and ADC channels, users should make sure the ADC channel is enabled when using related alarm functions. If the alarm function is triggered, the device will send an interrupt to alarm system but charger will not stop charging. The Table 4 shows the enable condition for each alarm.

Table 3. Alarm Function with Related ADC Channel

Alarm Function	Related ADC Channel Need Enabled	Sense Node
VBAT_OVP_ALM	VBAT_ADC	BATP and BATN pin
IBAT_OCP_ALM	IBAT_ADC	SRP and SRN pin
IBAT_UCP_ALM	IBAT_ADC	SRP and SRN pin
VBUS_OVP_ALM	VBUS_ADC	VBUS pin
IBUS_OCP_ALM	IBUS_ADC	Q0
TDIE_OTP_ALM	TDIE_ADC	DIE temperature
TSBUS_TSBAT_OTP_ALM	TSBAT_ADC, TSBUS_ADC, VOUT_ADC	TSBAT, TSBUS, VOUT pin

Table 4. Alarm Function Activation List

Alarm Function	Enable Condition
VBUS_OVP_ALM	CHG_EN = 1 or ADC_EN =1
VBAT_OVP_ALM	CHG_EN = 1 or ADC_EN =1
IBUS_OCP_ALM	CHG_EN = 1
IBAT_OCP_ALM	CHG_EN = 1
IBAT_UCP_ALM	CHG_EN = 1
TDIE_OTP_ALM	CHG_EN = 1 or ADC_EN =1
TSBUS_TSBAT_OTP_ALM	CHG_EN = 1 or ADC_EN =1

I^2C serial Interface

The RT9759 integrates I^2C interface for host to program charging parameter and monitor device status. The interface requires a serial clock line (SCL) and a serial data line (SDA). The host should initiate a data transfer on the bus and generates the clock signals to permit that transfer. The device operates with address 66H or 65H to receive control input from the host. The SCL and SDA pin are open drain structures. Users should connect a supply voltage via a current source or pull-up resistors on SCL and SDA. The Figure 10 shows the I^2C waveform information, the data line must be stable during the high period of SCL line. The high or low state of SDA can only change when SCL line is low.

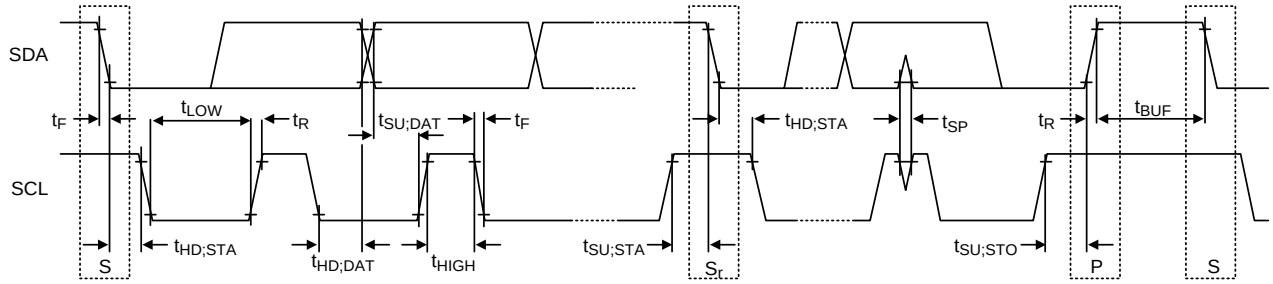


Figure 10. I²C Waveform Information

The RT9759 operates as an I²C slave device with address 66H or 65H (depends on pull low resistance of CDRVL). Every byte on SDA line must be 8 bit long. The Figure 11 shows the byte format of SDA and SCL line. All of transactions begin with a START pattern and can be terminated with a STOP pattern. After START, the master should send a slave address. The slave address is 7-bits long followed by the eighth bit as a data direction bit (R/W). The direction bit setting to 0 indicates a transmission and 1 indicates a request for data. The master should take an acknowledge bit after every byte. The master should release SDA line during the acknowledge clock pulse so the slave device can pull low the SDA line to signal the master that the byte was successfully received. The RT9759 supports multi read/write and SCL line can be up to 3.4MHz.

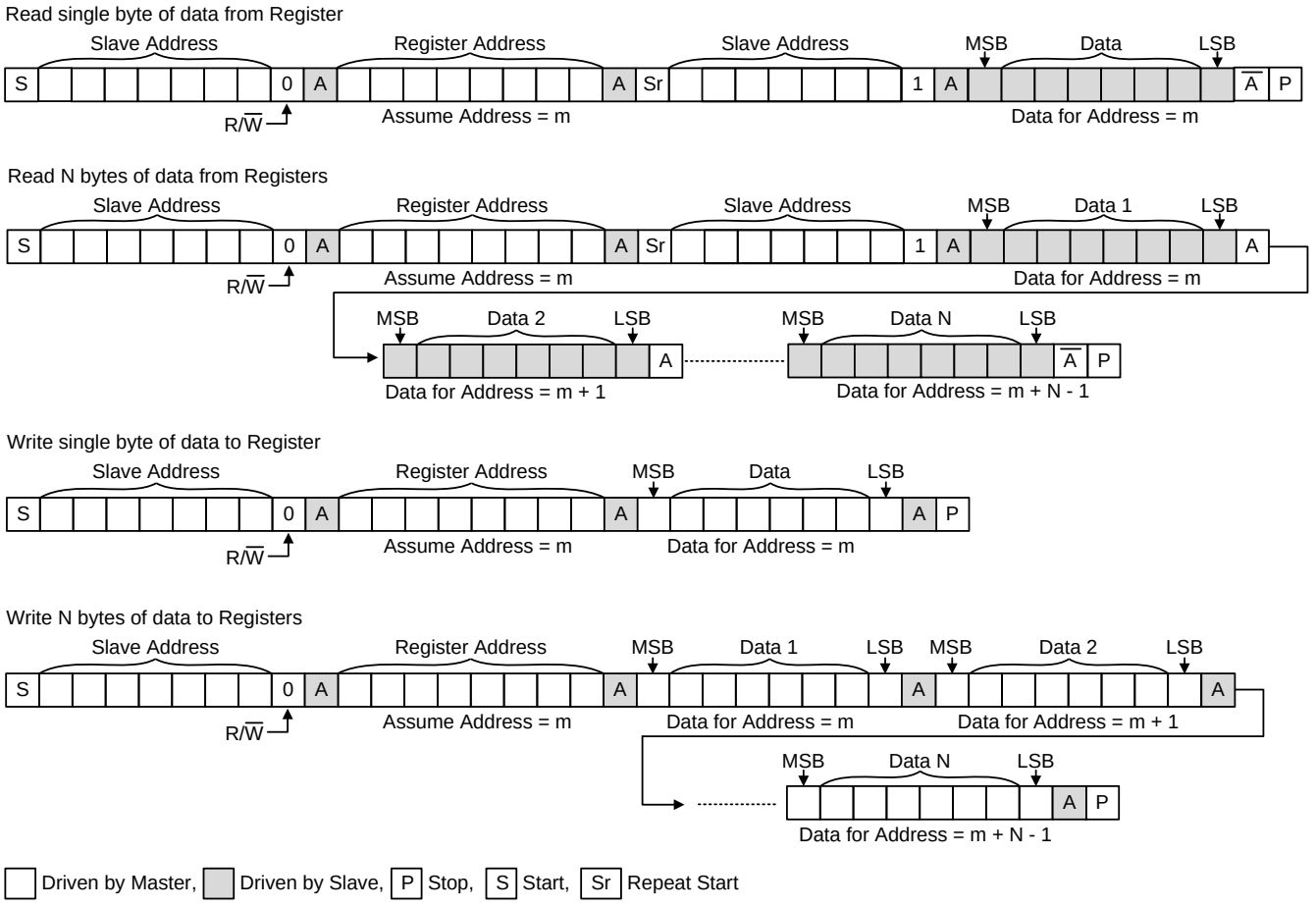


Figure 11. Read and Write Function

Interrupt (INT), STAT, FLAG AND MASK

The INT pin is an open drain structure; users should connect a supply voltage via a current source or pull-up resistors on the pin. When the device triggers an event, the INT pin will pull low for t_{INT} to notify host. The register map shows all state, flag and control bit of the device.

When the device triggers the event with FLAG, it will send an INT signal to host and set the FLAG bit to 1. The FLAG bit can be cleared after read. The device will not send another INT signal until the FLAG is cleared and a new event occurs again. The MASK bit can disable INT pin to send a signal to host. The STAT and FLAG bit are still updated even though the MASK bit is set to 1.

The STAT bits show current statue of the device and are updated as the status change. All of STAT bits will not send INT signal to system when the STAT bit is triggered except SWITCHING_STAT.

Spread Spectrum

The device integrated spread spectrum function for users to optimize the EMI influence on system design. The device switching frequency is decided by register 0x0B. The spectral density will concentrate on the switching frequency. Users can enable the spread spectrum function by set 0x0C register. After the spread spectrum function is enabled, the device will modulate the switching frequency for ±16% to reduce the spectral density.

Parallel Application

For high capacity battery charging application, it is available to use two RT9759 in parallel architecture. The advantages of using parallel architecture are reducing cable losses, improve efficiency of charge system and cut down charging period. The high power solution that uses two RT9759 are shown in Figure 12. The address and configuration mode can be configured by CDRVL_ADDRMS pin while device powers up.

In order to avoid unstable ripple issue while charging with parallel architecture, the RT9759 is established with synchronization function at the TSBAT_SYNCOUT pin and BATP_SYNCIN pin. The TSBAT_SYNCOUT pin provides synchronization pulses with frequency equal to twice switching frequency and 50% duty cycle. The BATP_SYNCIN pin is used to receive pulses for synchronization.

The TSBAT_SYNCOUT pin and BATP_SYNCIN pin are multi-function pins that depends on different configuration. While the RT9759 is set as master (RT9759_M), the TSBAT_SYNCOUT pin is set as synchronization output and BATP_SYNCIN pin is set as battery positive sense. While the RT9759 is set as slave (RT9759_S), the TSBAT_SYNCOUT pin is set as TSBAT function and the BATP_SYNCIN pin is set as synchronization input.

In parallel application, only master device's OVP MOSFET is used. Furthermore, the OVPGATE function and battery current sensing function are turned off in slave device. If the RT9759s are used to charge in parallel application, the slave device's OVPGATE, SRP and SRN pin can be left floating.

If parallel architecture is used, the start-up sequence should be compiled with the rules below. The RT9759 set as slave (RT9759_S) should be enabled before host enables the RT9759 set as master (RT9759_M) in order to achieve parallel application. The RT9759_S will not switch until the BATP_SYNCIN pin receives synchronization pulses provided by the RT9759_M. The communication flow between smart wall adapter and parallel charge system is shown in Figure 13.

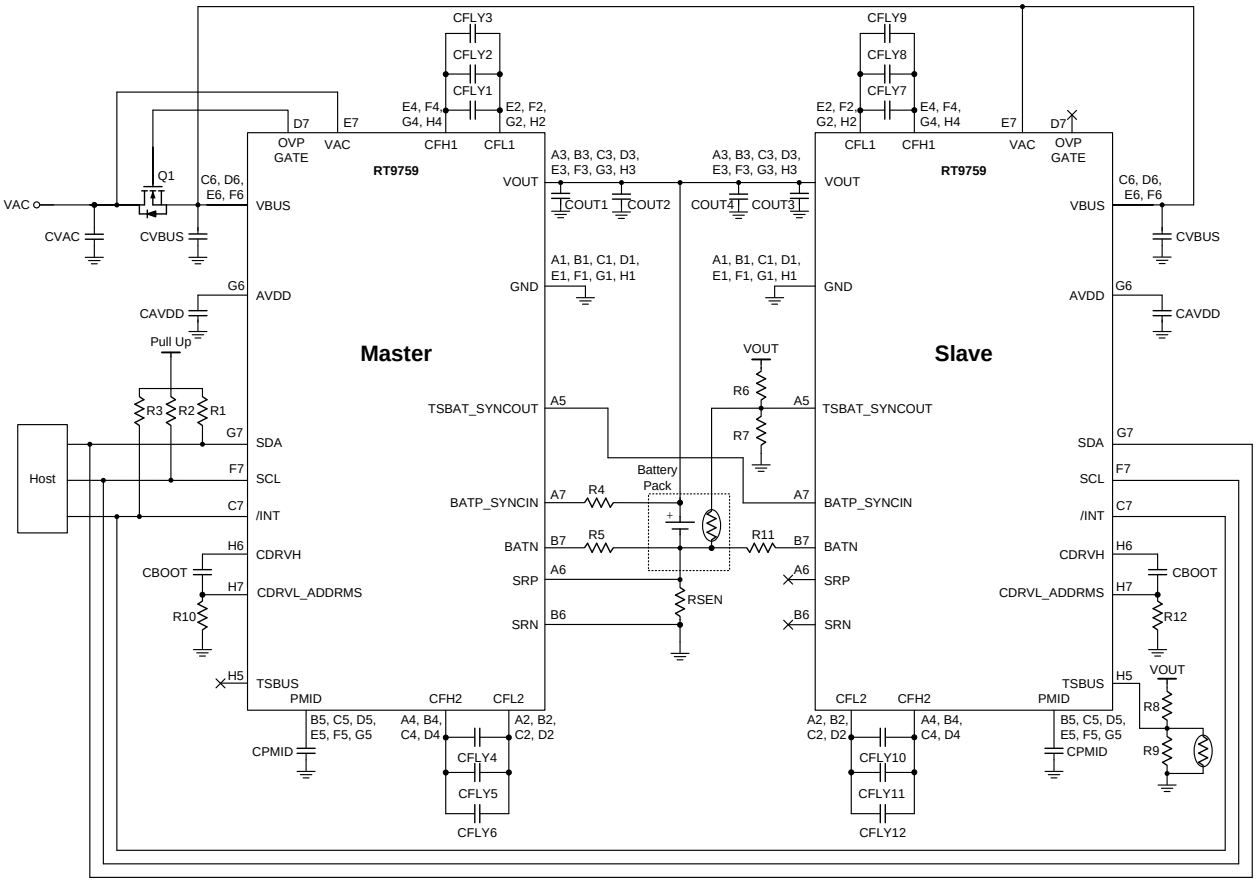


Figure 12. Parallel Application Circuit

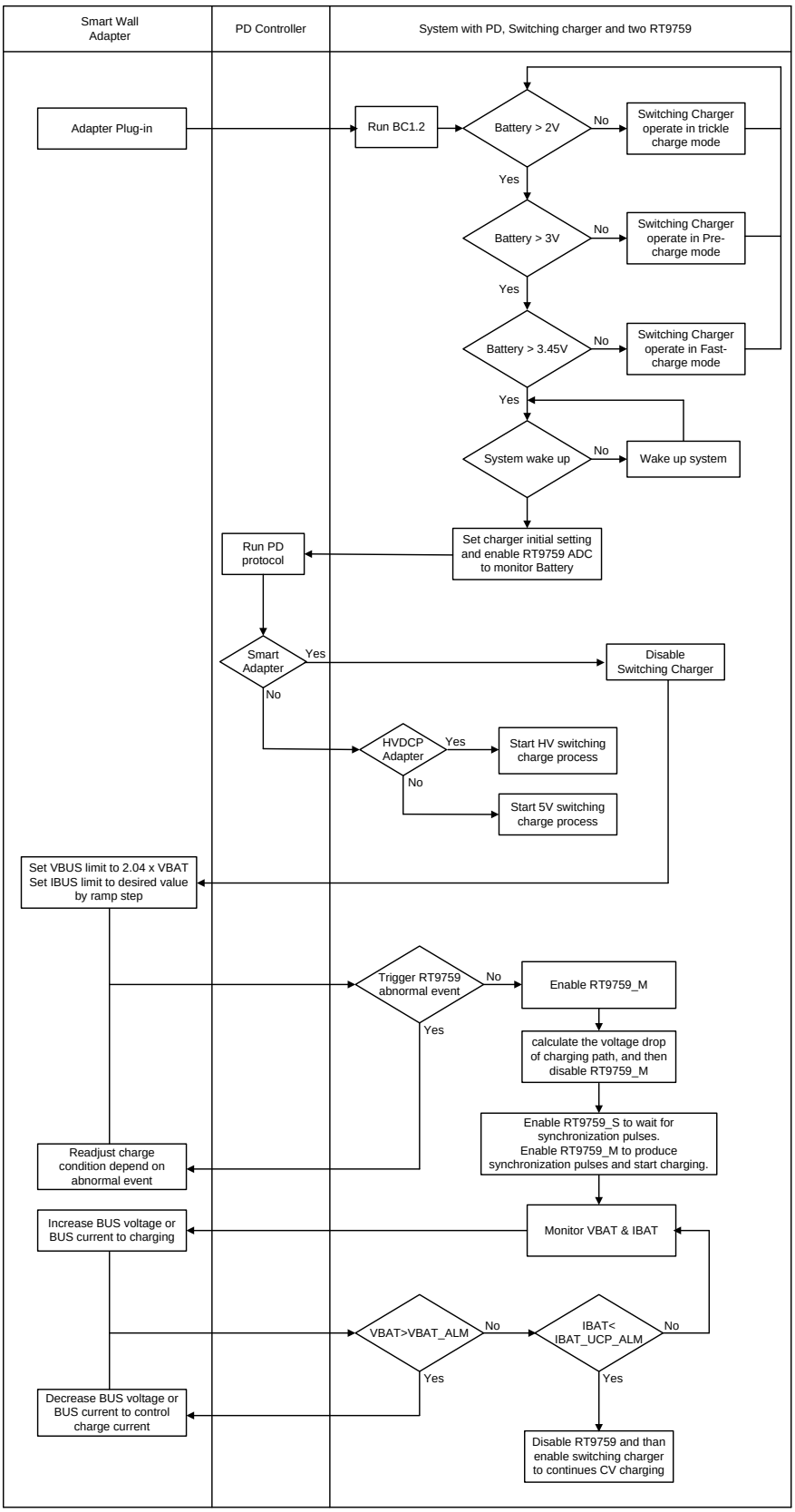


Figure 13. System Control Flow Chart with Parallel Charge system

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For a continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-56B 3.35x3.35 (BSC) package, the thermal resistance, θ_{JA}, is 24°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated below :

$P_{D(MAX)}$ = (125°C - 25°C) / (24°C/W) = 4.16W for a WL-CSP-56B 3.35x3.35 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 14 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

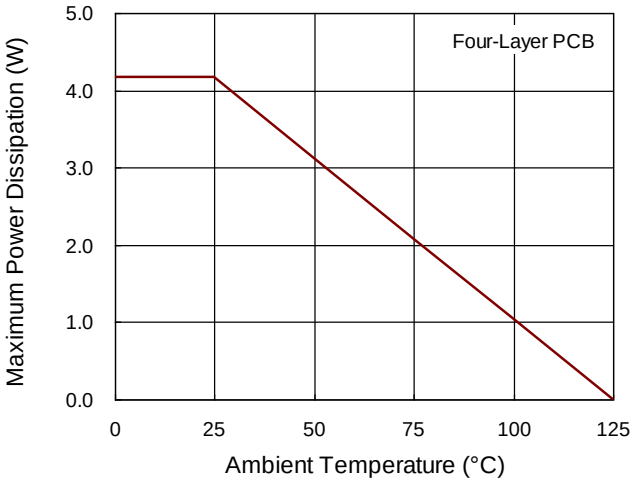


Figure 14. Derating Curve of Maximum Power Dissipation

Layout Considerations

The RT9759 layout guidelines are recommended as below :

- Place low ESR bypass capacitor to GND for PMID/VOUT/ VBUS pin. The bypass capacitor needs to be placed as close as possible to RT9759.
- The capacitor of AVDD/CDRVL/CDRVH_ADDR should be placed as close as possible to RT9759.
- Place flying caps with the RT9759 on same layer. The flying caps should be placed as close as possible to the RT9759. The path of flying caps should be as small as possible.
- The VBUS and VOUT traces should be as wide as possible to accommodate high charge current.
- Place differential line for VBATP/VBATN and SRP/SRN. Do not route the differential line across power pad especially the flying caps.

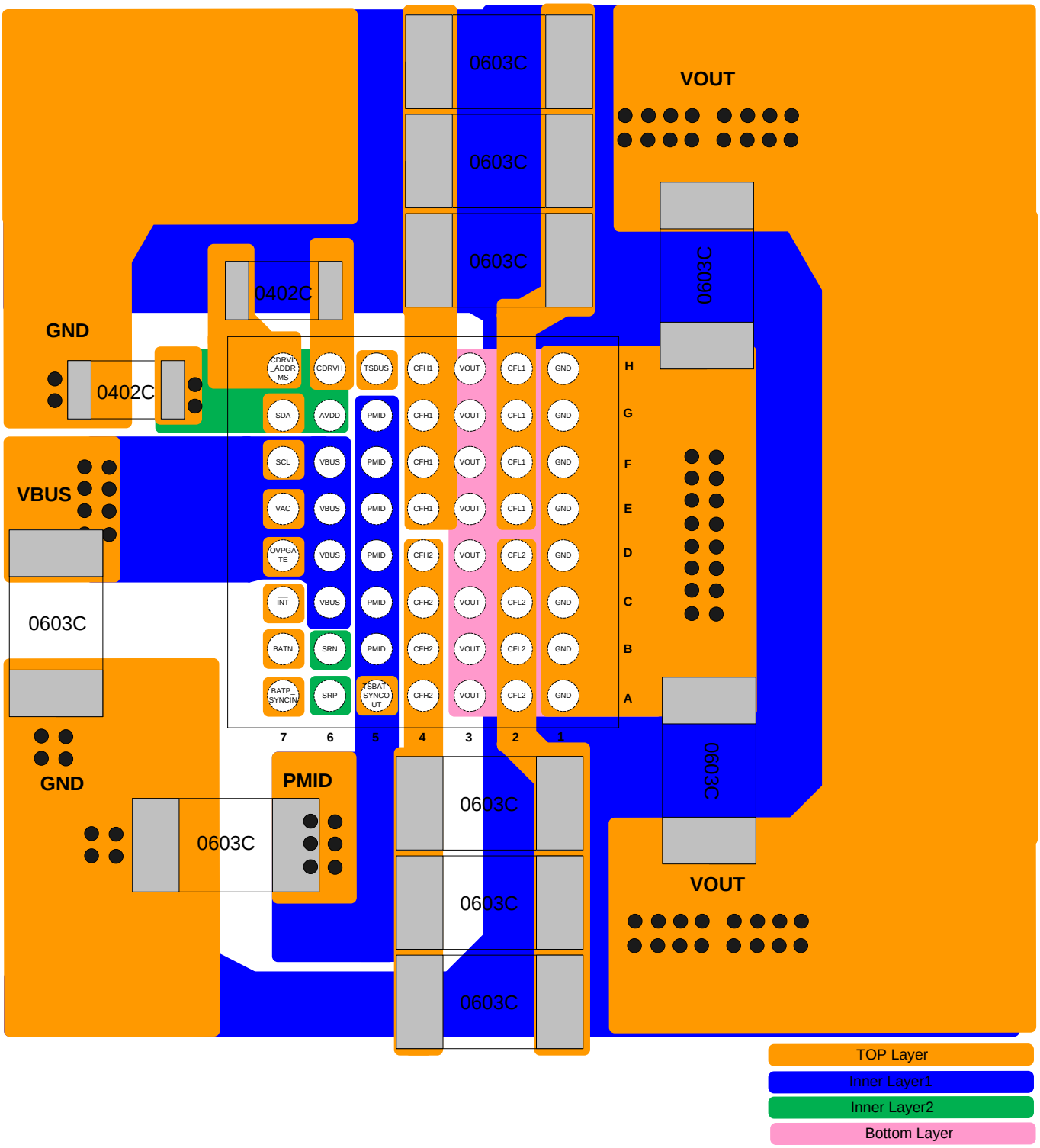
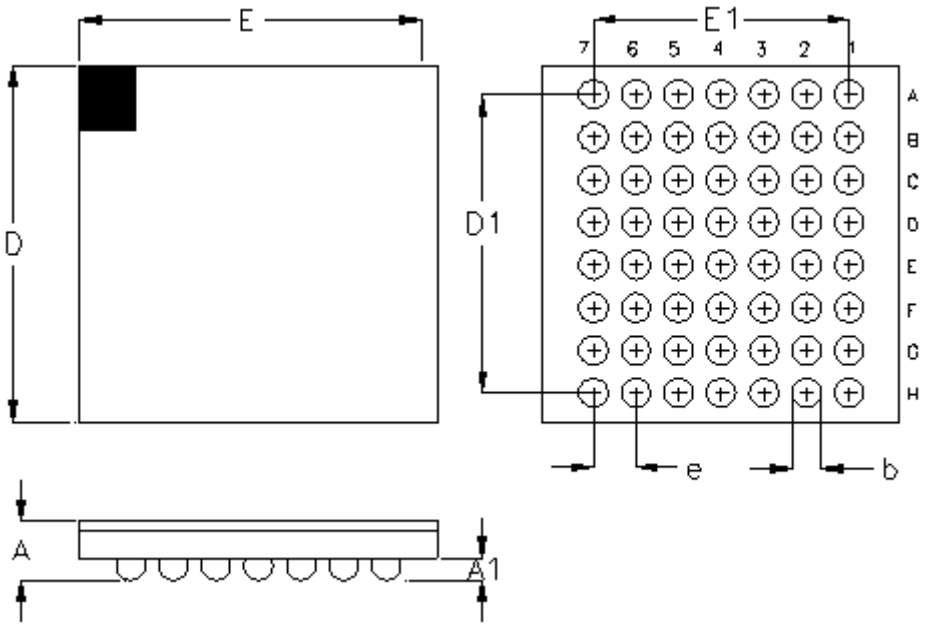


Figure 15. PCB Layout Guide

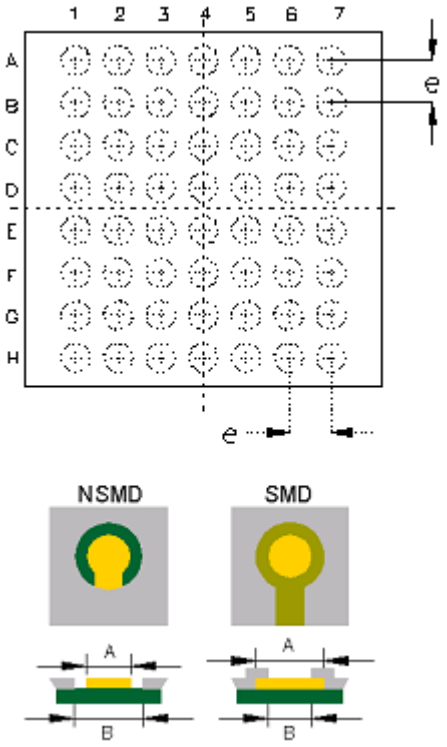
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	3.310	3.390	0.130	0.133
D1	2.800		0.110	
E	3.310	3.390	0.130	0.133
E1	2.400		0.094	
e	0.400		0.016	

56B WL-CSP 3.35x3.35 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP3.35x3.35-56(BSC)	56	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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单击下面可查看定价，库存，交付和生命周期等信息

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