High Efficiency, Synchronous Buck with Dual Linear Controllers

General Description

The RT9206 is a low cost, combo power controller, which integrates a synchronous step-down voltage-mode PWM and two HV linear controllers. Directly drive external N-MOSFET makes it easy to implement a high efficiency and cost attractive power solution. Voltage mode control loop and constant operation frequency with external compensation network provide better stability in wide operation range. Adjustable operation frequency up to 600kHz can minimize the inductor size and PCB space. It is particularly suitable in wide input voltage range (from 4.75V to 28V) and multi-output applications.

Linear controller features flexible linear power design. Delivered power can be simply decided by external N-MOSFET selection. Output voltage level is chosen via external resistor divider. The 0.8V internal reference can satisfy most of the applications. Under voltage lockout provide cost effective protection of output.

RT9206 provides complete safety protection function: soft start, over current protection, over voltage and under voltage protection. Set current limit by choosing different MOSFET. Synchronous Buck control mode provides excellent over voltage protection by turning on low side MOSFET to prevent any damage of end device from abnormal voltage stress as over voltage condition occurs.

Ordering Information

RT9206 □ □

- Package Type
  S : SOP-16
- Lead Plating System
  P : Pb Free
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

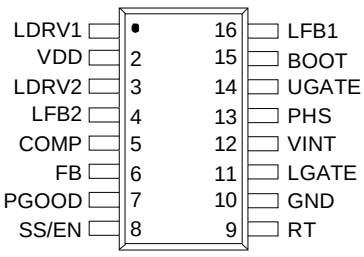
- **Wide Input Range (4.75V to 28V)**
- **0.8V Internal Reference**
- **High Efficiency Synchronous Buck Topology**
- **Integrate two HV Linear Controllers**
- **Low cost N-MOSFET Design**
- **Duty Cycle from 0% to 90%.**
- **Adjustable switching frequency from 200kHz to 600kHz, Default 200kHz**
- **Sense OCP by low Side MOSFET $R_{DS(ON)}$**
- **Power Good Signal Output**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- LCD Monitor
- Desk Note
- IEEE1394 Client
- Desktop IA
- Broadband

Pin Configurations

(TOP VIEW)



SOP-16

Typical Application Circuit

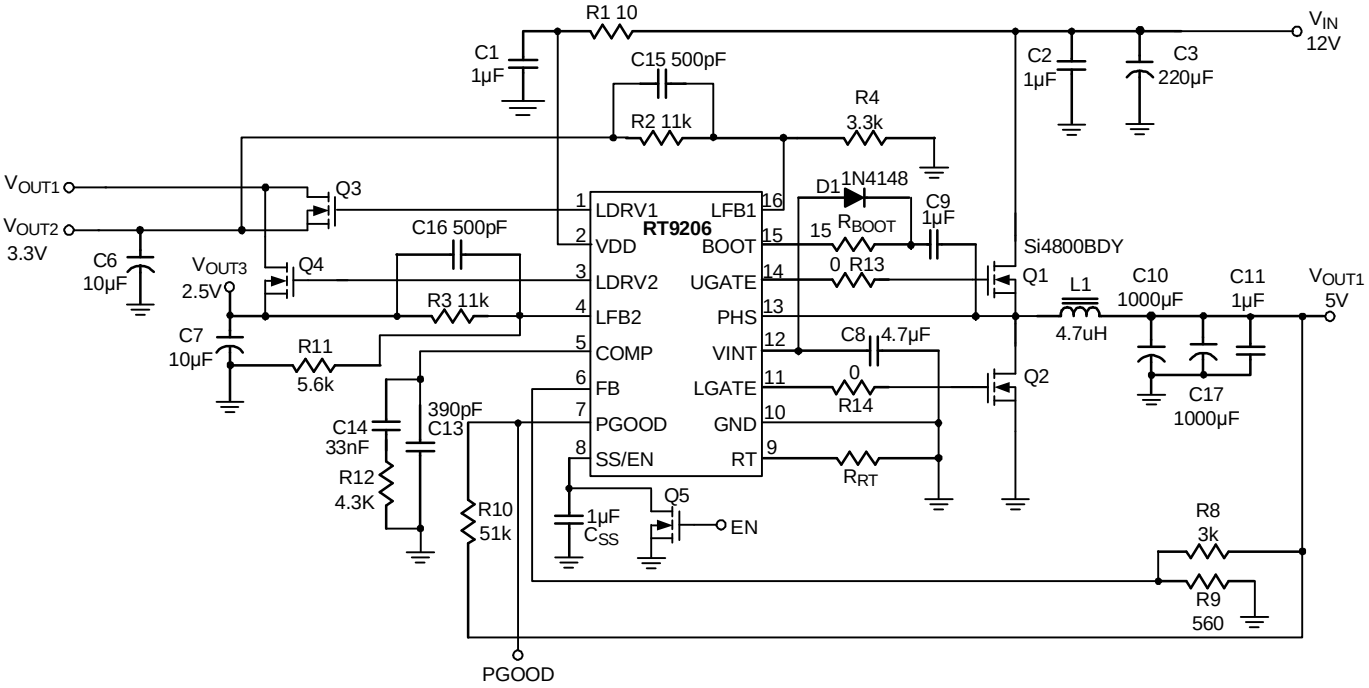


Figure 1. Typical Application for 12V Input

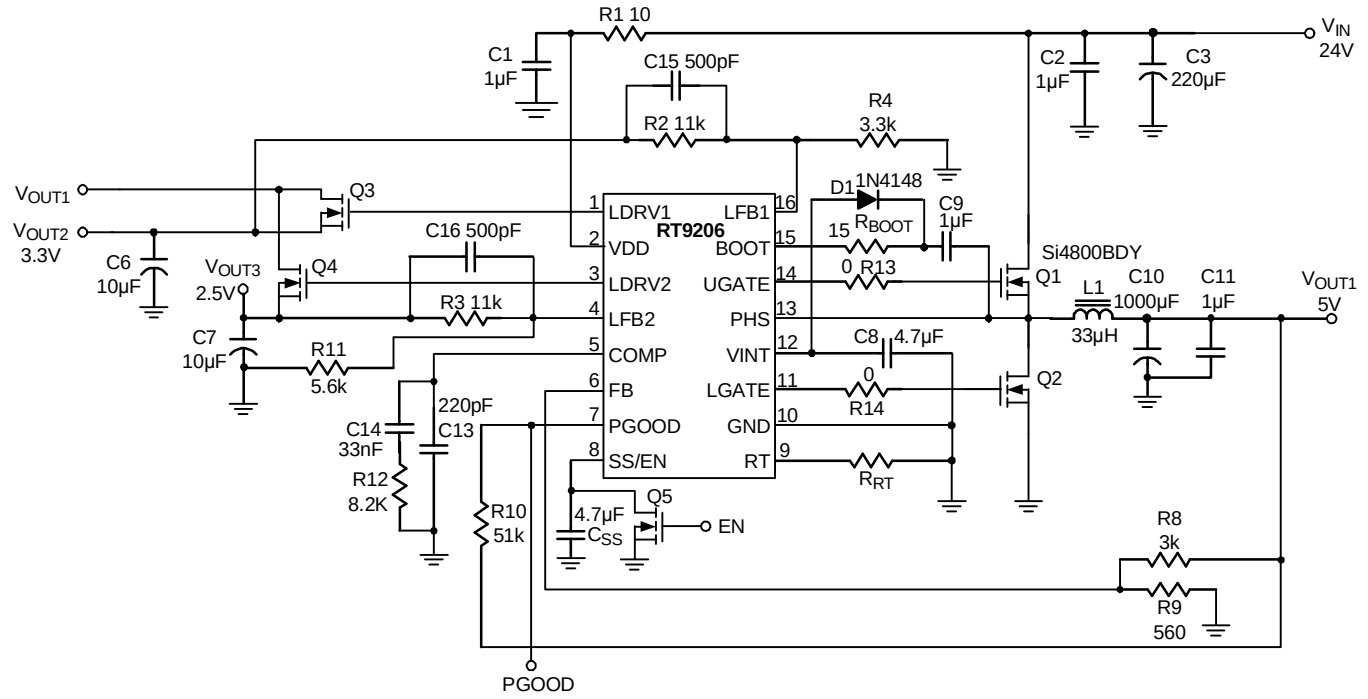
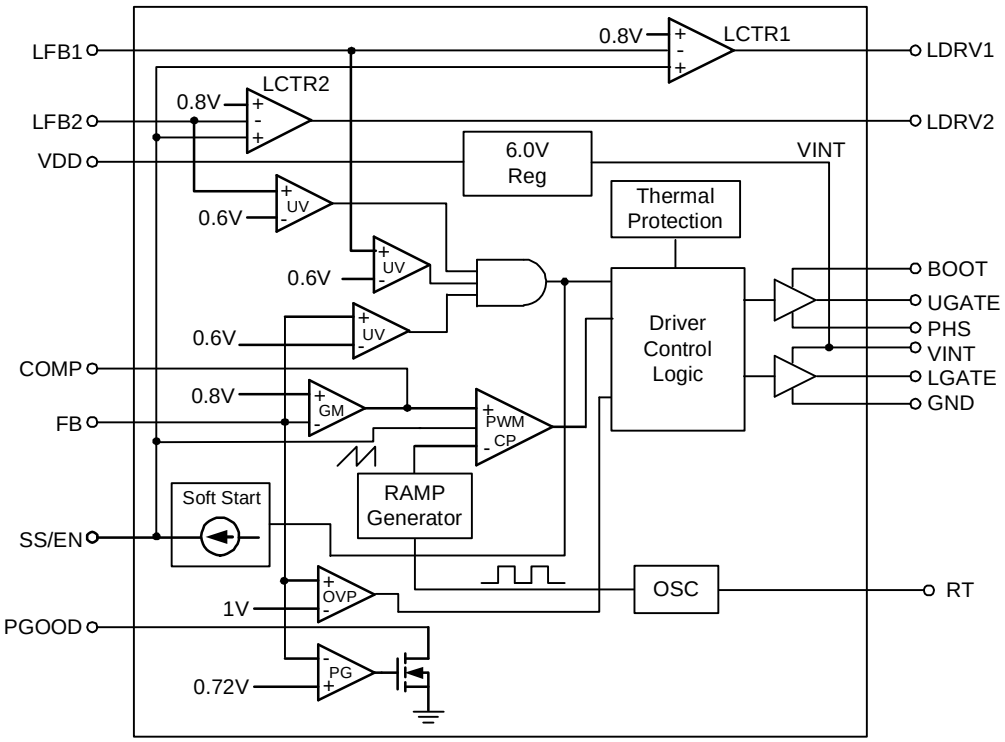


Figure 2. Typical Application for 24V Input

Note : R_{BOOT} is a must to suppress ringing spike.

Function Block Diagram



Operation

Introduction

The RT9206 is a combo controller, which integrates an adjustable frequency, voltage mode synchronous step down controller and two HV linear controllers. The synchronous step down controller consists of an internal precision reference, an internal oscillator, an error amplifier, a PWM comparator, control logic and floating gate driver, a programmable soft-start, a power good indicator, an over voltage protection, an over temperature protection and short circuit protection.

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier, which is the amplified error signal from the sensed output voltage and the voltage on non-inverting input, which is connected with internal 0.8V reference voltage. The amplified error signal is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulse of variable duty-cycle, which drivers the two N-Channel external MOSFETs.

The timing of the synchronous converter is provide through an internal oscillator circuit and can be programmed between 200kHz to 600kHz via an external resistor connected between RT pin and ground.

Soft-Start

RT9206 has a programmable soft-start to control the output voltage rise time and limit the current surge at the start-up. The soft-start will begin while V_{DD} rises above POR threshold for correct start-up. Soft-start function operates by an internal sourcing current to charge an external capacitor to around the voltage of VINT. The soft-start signal, SS pin, is the third input non-inverting input of the PWM comparator. Before soft-start signal reach the bottom of the sawtooth ramp, inverting input of the PWM comparator, the soft-start current is twice of the normal soft-start current. Once the soft-start signal reach the bottom of the ramp, the soft-start current became normal, and start to increase duty cycle from zero to the point the feedback loop takes control.

Power On Reset (POR)

The power on reset circuit assures that the MOSFET driver outputs remain in the off state whenever the V_{DD} supply voltages lower than the POR threshold.

Over Current Protection

Whenever the over-current is occurred in soft-start or in normal operation period, It will shut down PWM signal, the MOSFET driver outputs remain in the off state, and latch soft-start signal low until restart V_{DD} supply voltage.

Over Voltage Protection

Once over-voltage protection occurred, it will turn on low side MOSFET and latch soft-start signal low to prevent end device form abnormal voltage stress. Restart V_{DD} supply voltage will release the protection.

Power Good Indicator

The power good indicator is an open drain output to show whether the synchronous converter output ready or not. The power good indicator is available after soft-start end.

Short-Circuit Protection

The short-circuit phenomenon is sensed by the drop of output voltage, synchronous converter and two linear controller. Once the short-circuit occurred, the drop of output voltage lower than the under voltage threshold, 0.6V on feedback, the PWM signal will shut down and both of the external MOSFET will turn off and soft-start signal latch low. Soft-start signal, SS, is also connected to two linear controller error amplifier non-inverting input. Therefore, whenever the drop of output of the synchronous converter or two linear controllers lower than under voltage threshold, all MOSFET drivers will turn off.

Pin Description

LDRV1(Pin 1)

Linear controller 1 (LCTR1) driver. Connect to the gate of external N-Channel MOSFET pass transistor to form a positive linear regulator

VDD (Pin 2)

Input supply voltage

LDRV2 (Pin 3)

Linear controller 2 (LCTR2) driver. Connect to the gate of external N-Channel MOSFET pass transistor to form a positive linear regulator

LFB2 (Pin 4)

LDO2 feedback input. The feedback set point is 0.8V. Connect to a resistive divider between the positive linear regulator output and GND to adjust the output voltage.

COMP (Pin 5)

Switching regulator compensation pin.

FB (Pin 6)

Switching regulator feedback input. The feedback set point is 0.8V. Connect to a resistive divider between the switching regulator output and GND to adjust the output voltage.

PGOOD (Pin 7)

Open drain power good indicator. PGOOD is low when switching regulator output voltage is lower than 10% of its regulation voltage. Connect a pull high resistor between PGOOD and switching regulator output for pull high logic level voltage.

SS/EN (Pin 8)

Soft start input with 8uA sourcing current and IC enable control.

RT (Pin 9)

Operational frequency setting. Connect a resistor between RT and GND to set operational frequency. The operational frequency will nominally run at 200kHz when open.

The formula between resistor setting and operational frequency are as follows:

$$R_{RT} = \frac{62 \times 10^8}{F_{OSC} - 200 \times 10^3}$$

GND (Pin 10)

Ground

LGATE (Pin 11)

Low side gate driver. Drives low side N-MOSFET with a voltage swing between VINT and GND

VINT (Pin 12)

Internal 6.0V regulator output. The low side gate driver and control circuit and external bootstrap diode are powered by this voltage. Decouple this pin to power ground with a 4.7uF or greater ceramic capacitor close to the VINT pin.

PHS (Pin 13)

Inductor connection with (-) terminal bootstrap flying capacitor connection.

UGATE (Pin 14)

High side gate driver. Drives high side N-Channel MOSFET with a voltage swing between BOOT and PHS

BOOT (Pin 15)

High side floating driver supply with (+) terminal bootstrap flying capacitor connection. Voltage swing is from a diode drop below VINT to VIN + VINT

LFB1 (Pin 16)

LDO1 feedback input. The feed back set point is 0.8V. Connect to a resistive divider between the positive linear regulator output and GND to adjust the output voltage.

Absolute Maximum Ratings (Note 1)

- Supply Voltage (V_{IN}) ---------- –0.3 to 30V
- PHS ---------- –0.6V to 30V
- PHS (PHS Transient Time Interval < 50ns) ---------- –5V
- BOOT, UG to PHS ---------- –0.3V to 7V
- BOOT to GND ---------- –0.3V to 35V
- LDRI1, LDRI2 ---------- –0.3V to 30V
- Power Good Voltage ---------- –0.3V to 7V
- The other pins ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-16 ---------- 0.625W
- Package Thermal Resistance
  SOP-16, θ_{JA} ---------- 90°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Operation Temperature Range ---------- –20°C to 85°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, F_{ADJ} left floating, T_A = 25°C, Unless Otherwise specification)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System Supply Input						
Operation voltage Range	V_{DD}	(Note 4)	4.75	--	28	V
Power On Reset	POR		3.8		4.7	V
Power On Reset Hysteresis			200	--	600	mV
Supply Current	I_{DD}	V_{DD} = 30V, V_{SS} = V_{INT}	--	1.3	4	mA
Shut Down Current	I_{DD}	V_{DD} = 30V, V_{SS} < 0.4V	--	1	3.5	mA
Power Good under Threshold	VFB		82	--	92	%
PG Fault Condition	VPG	I_{PG} = –4mA, VFB = 80%	--	--	0.2	V
Soft-Start						
Soft-start Current	I_{SS}		4	8	12	μA
Normal Operation Voltage	V_{SS}		--	V_{INT}	--	V
Shut down Voltage	V_{SS}		0.4	0.7	--	V

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PWM Section Reference Voltage						
Feedback Voltage	V_{FB}		0.784	0.8	0.816	V
Internal Voltage	V_{INT}	I_{INT} = 10mA	5.0	6	6.5	V
Internal Voltage Source Current	I_{INT}	V_{IN} = 12V	20	--	--	mA
PWM Section Oscillator						
Free Run Frequency	F_{OSC}		160	200	240	kHz
Operation Frequency Setting	F_{OSC}	By setting RT (Note 5)	–30	--	30	%
Ramp Amplitude			--	1.9	--	V
Maximum Duty Cycle			85	90	--	%
Error Amplifier						
GM			--	1.6	--	ms
Compensation Source Current			45	90	140	µA
Compensation Sink Current			45	90	140	µA
Gate Driver						
Upper Gate Source (UGATE1 & 2)	R_{UGATE}		--	5	8	Ω
Upper Gate Sink (UGATE1 & 2)	R_{UGATE}		--	5	8	Ω
Lower Gate Source (LGATE1 & 2)	R_{LGATE}		--	3	5	Ω
Lower Gate Sink (LGATE1 & 2)	R_{LGATE}		--	1.5	3	Ω
Upper Gate Rising Time	T_{R_UGATE}	V_{DD} = 12V, C_{LOAD} = 3nF	--	30	--	ns
Upper Gate Falling Time	T_{F_UGATE}	V_{DD} = 12V, C_{LOAD} = 3nF	--	30	--	ns
Lower Gate Rising Time	T_{R_LGATE}	V_{DD} = 12V, C_{LOAD} = 3nF	--	30	--	ns
Lower Gate Falling Time	T_{F_LGATE}	V_{DD} = 12V, C_{LOAD} = 3nF	--	30	--	ns
Minimum On Time			--	--	400	ns
Protection						
Over Current Threshold			–270	–300	–330	mV
Over Voltage Protection	VFB		0.9	1	1.1	V
Under Voltage Protection	VFB		0.54	0.6	0.66	V
Linear Controller Section Error Amplifier						
Feedback Voltage	LFB1 / LFB2		0.780	0.8	0.824	V
Output Current	LDRV1 / LDRV2		10	--	--	mA
Protection						
Under Voltage Protection	LFB1 / LFB2		0.54	0.6	0.66	V
Over Temperature Protection			125	170	--	°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

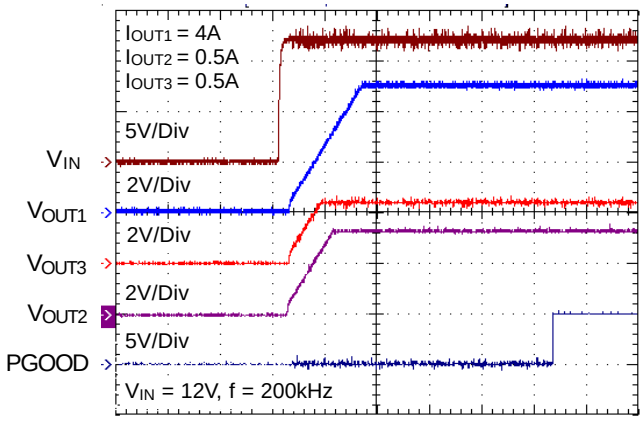
Note 4. $V_{DD} - V_{OUT2}$ or $V_{DD} - V_{OUT3}$ must be higher than 4V to keep linear controller operation

Note 5. $R_{RT} = \frac{62 \times 10^8}{F_{OSC} - 200 \times 10^3}$

Note 6. The LDOs are not suitable for low noise applications

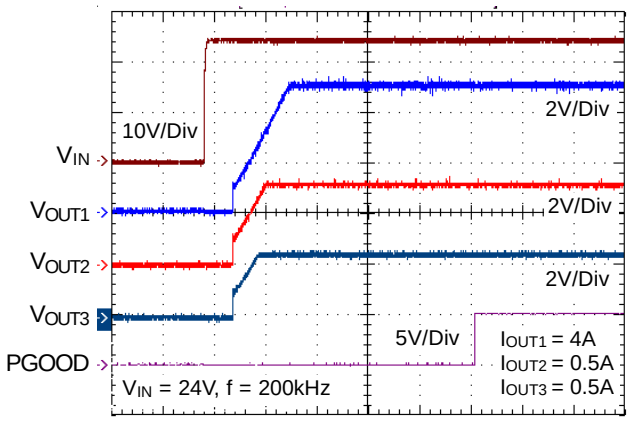
Typical Operating Characteristics

Power On



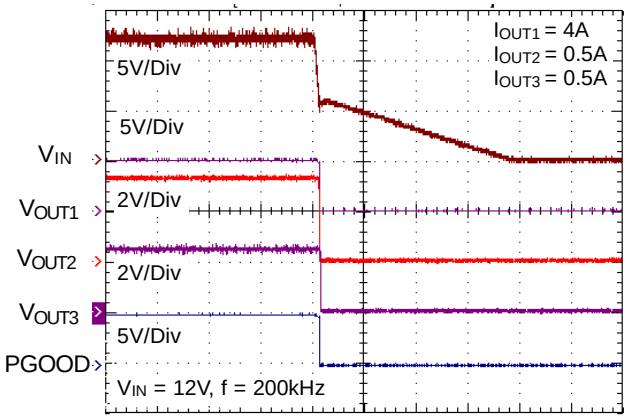
Time (100ms/Div)

Power On



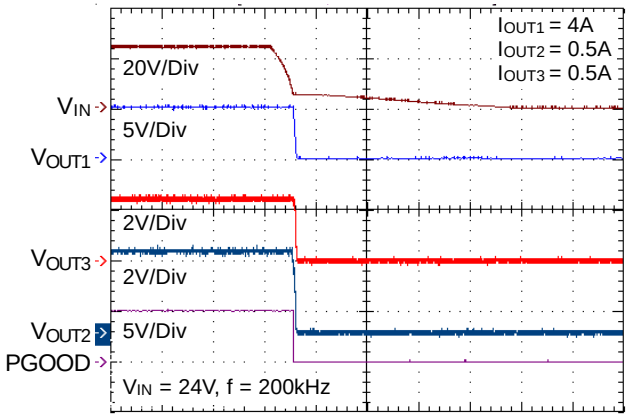
Time (200ms/Div)

Power Off



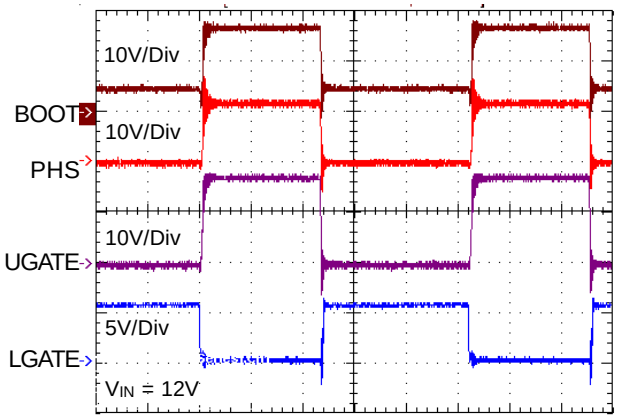
Time (20ms/Div)

Power Off



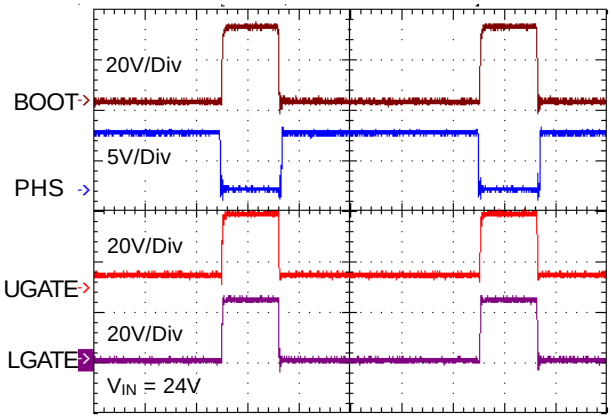
Time (20ms/Div)

Bootstrap Wave Form



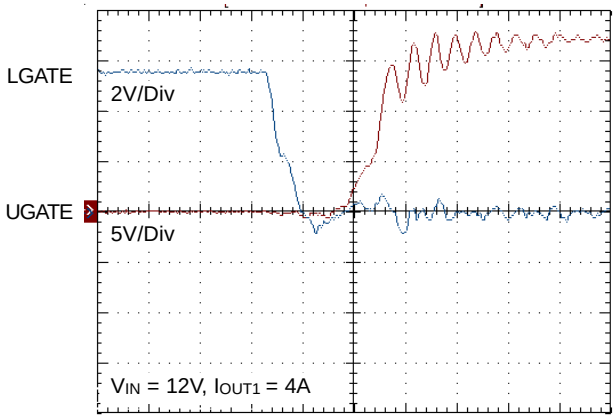
Time (1µs/Div)

Bootstrap Wave Form



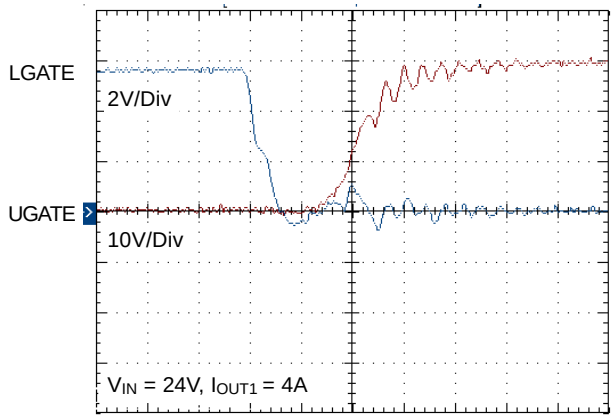
Time (1µs/Div)

Dead Time



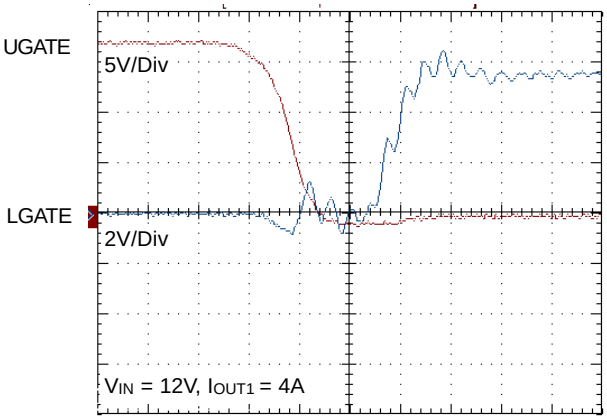
Time (20ns/Div)

Dead Time



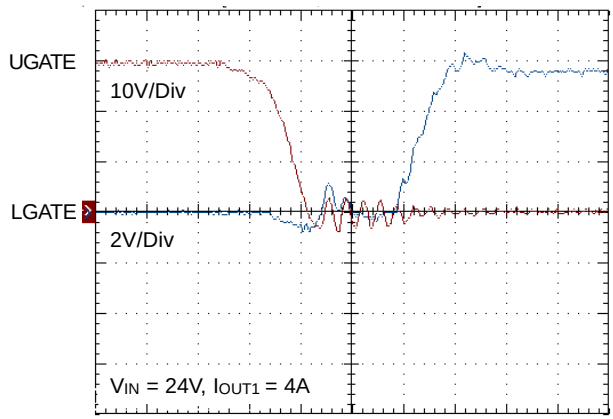
Time (20ns/Div)

Dead Time



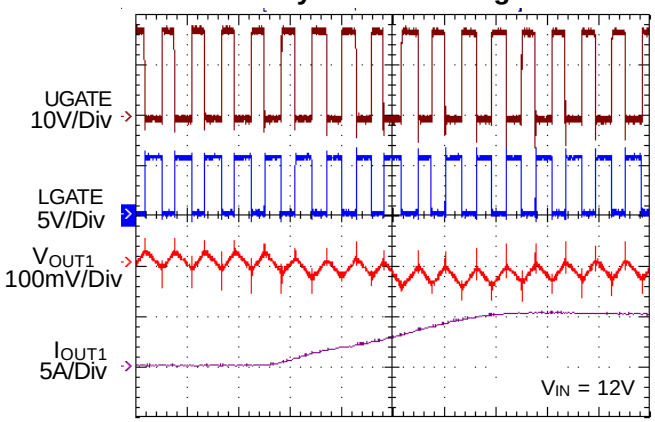
Time (20ns/Div)

Dead Time



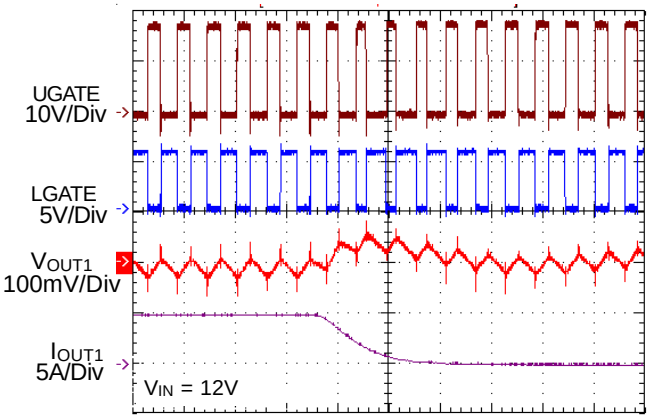
Time (20ns/Div)

Dynamic Loading



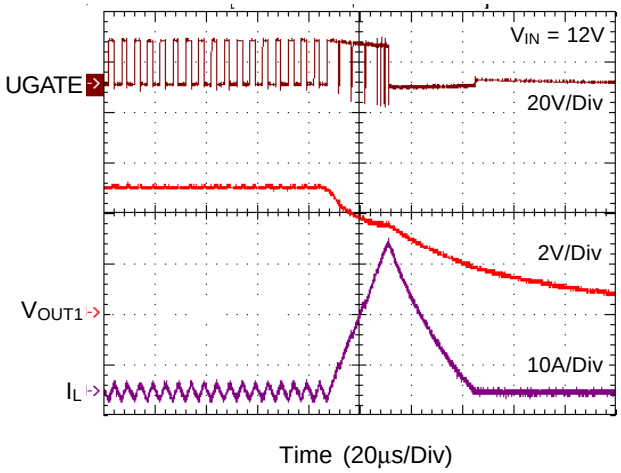
Time (10µs/Div)

Dynamic Loading

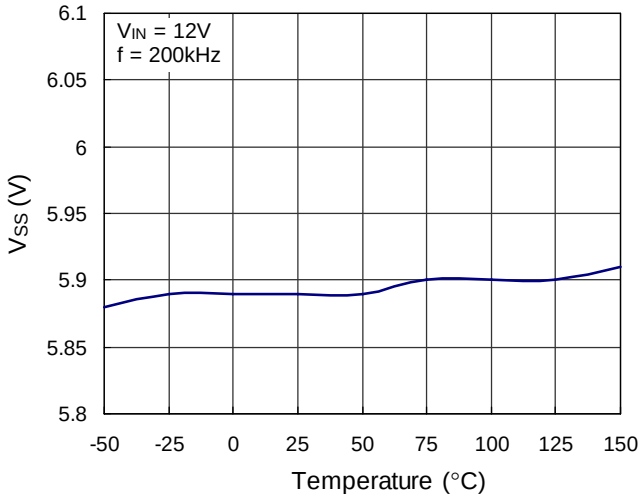


Time (10µs/Div)

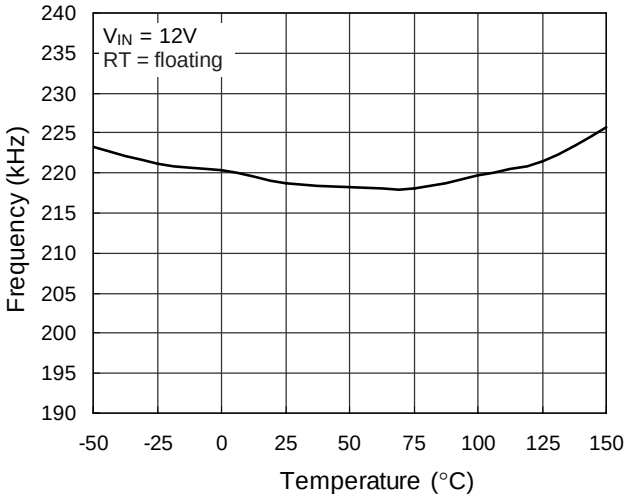
Short Latch



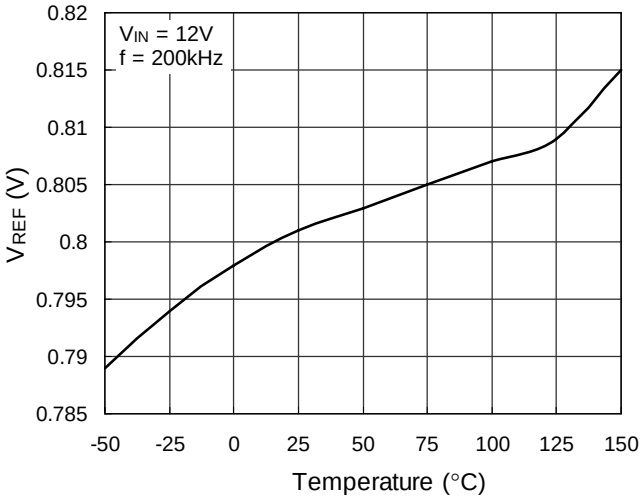
Soft Start vs. Temperature



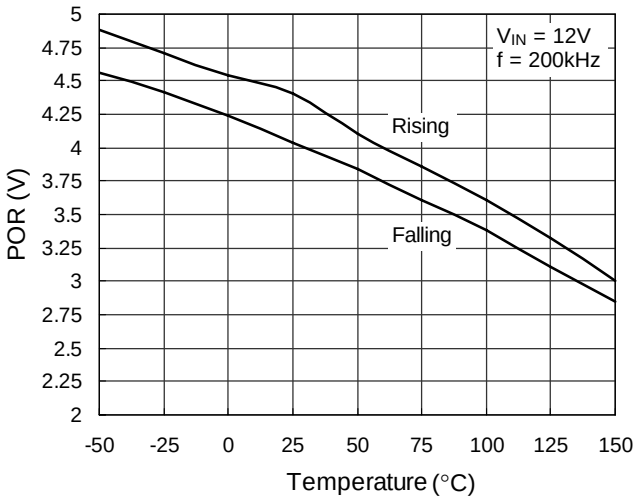
Oscillator Frequency vs. Temperature



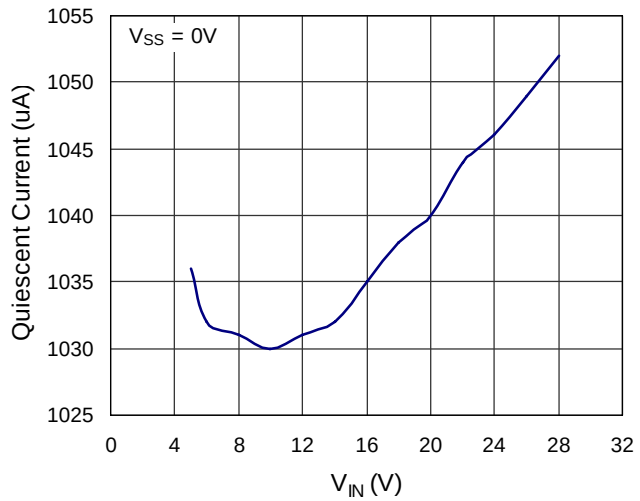
Reference Voltage vs. Temperature

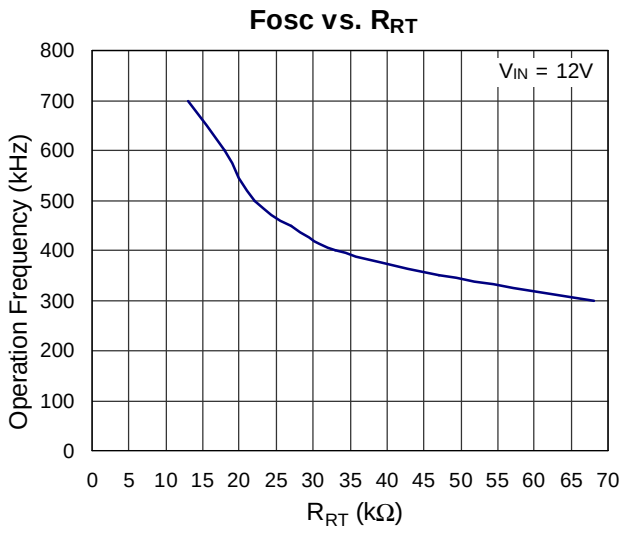


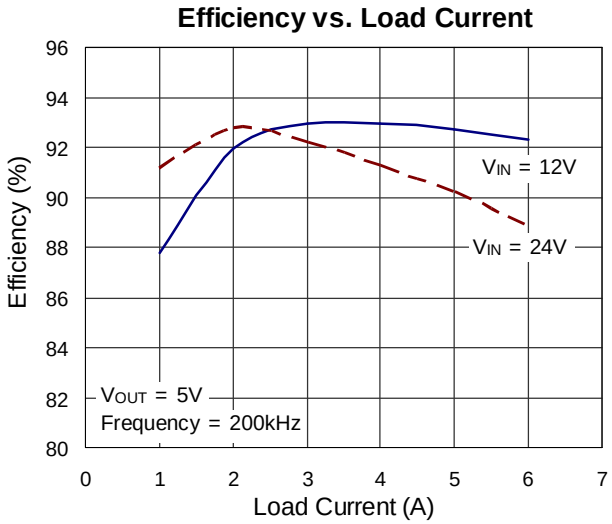
POR(Rising/Falling) vs. Temperature

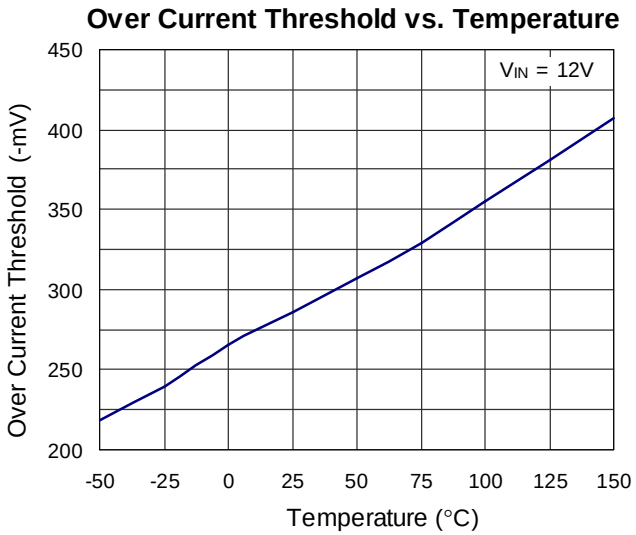


Quiescent Current vs. Input Voltage









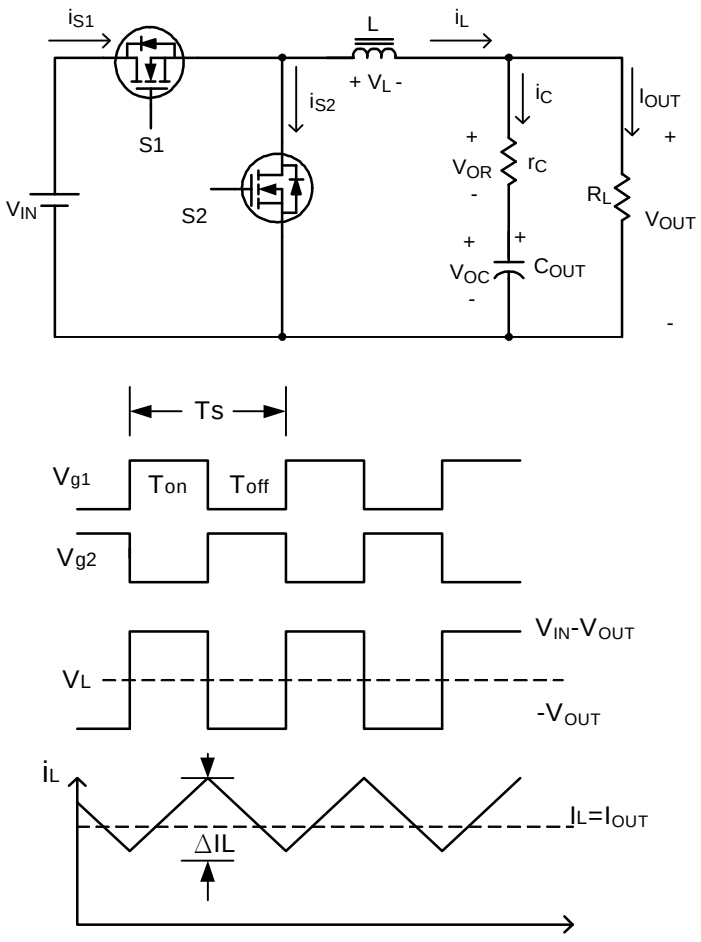
Application Information

Synchronous Buck Converter

The RT9206 is specifically designed for synchronous buck converter with wide input voltage from 4.75V to 28V and operating frequency from 200kHz to 600kHz. To fully utilize its advantages, peripheral components should be appropriately selected. The following information provides basic considerations for component selection.

Output Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. Low inductance value has smaller size, but results in low efficiency, large ripple current and high output ripple voltage. Generally, an inductor that limits the ripple current (ΔI_L) between 20% and 50% of output current is appropriate. Figure 1 shows the typical topology of synchronous step-down converter and its related waveforms.



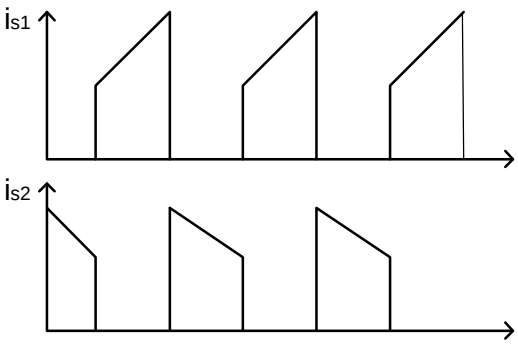


Figure 1.The waveforms of synchronous step-down converter

According to Figure 1 the ripple current of inductor can be calculated as follows :

$$V_{IN} - V_{OUT} = L\frac{\Delta I_L}{\Delta t};\Delta t = \frac{D}{fs};D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times fs \times \Delta I_L} \quad (1)$$

Where :

V_{IN} = Maximum input voltage

V_{OUT} = Output Voltage

$\Delta t = S_1$ turn on time

ΔI_L = Inductor current ripple

f_S = Switching frequency

D = Duty Cycle

r_C = Equivalent series resistor of output capacitor

Output Capacitor Selection

The selection of output capacitor depends on the output ripple voltage requirement. Practically, the output ripple voltage is a function of both capacitance value and the equivalent series resistance (ESR) r_C. Figure 2 shows the related waveforms of output capacitor.

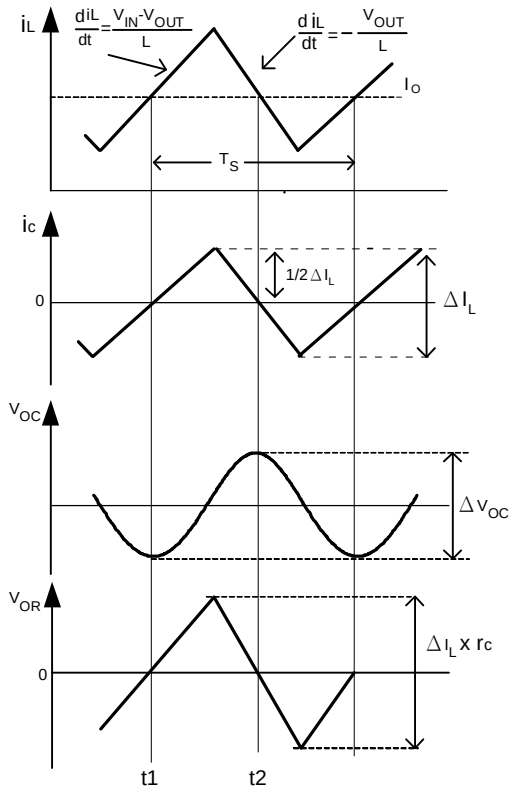


Figure 2. The related waveforms of output capacitor.

The AC impedance of output capacitor at operating frequency is quite smaller than the load impedance, so the ripple current (ΔI_L) of the inductor current flows mainly through output capacitor. The output ripple voltage is described as :

$$\Delta V_{OUT} = \Delta V_{OR} + \Delta V_{OC} \quad (2)$$

$$\Delta V_{OUT} = \Delta I_L \times r_C + \frac{1}{C_O}\int_{t1}^{t2} i_C \, dt \quad (3)$$

$$\Delta V_{OUT} = \Delta I_L \times r_C + \frac{1}{8}\frac{V_{OUT}}{C_O L}(1-D)T_S^2 \quad (4)$$

where ΔV_{OR} is caused by ESR and ΔV_{OC} by capacitance.

For electrolytic capacitor application, typically 90~95% of the output voltage ripple is contributed by the ESR of output capacitor. So Equation (4) could be simplified as :

$$\Delta V_{OUT} = \Delta I_L \times r_C \quad (5)$$

Users could connect capacitors in parallel to get calculated ESR.

Input Capacitor Selection

The selection of input capacitor is mainly based on its maximum ripple current capability. The buck converter draws pulsewise current from the input capacitor during the on time of S1 as shown in Figure 1. The RMS value of ripple current flowing through the input capacitor is described as :

$$I_{rms} = I_O\sqrt{D(1-D)} \quad (A) \quad (6)$$

The input capacitor must be cable of handling this ripple current. Sometime, for higher efficiency the low ESR capacitor is necessarily.

Power MOSFET Selection

The selection of MOSFETs is based on consideration of maximum gate-source voltage (Vgs), drain-source voltage (Vdss), maximum drain current (Id), drain-source on-state resistance $R_{DS(ON)}$ and thermal management. The MOSFETs are driven by V_{INT} that is internally regulated as 6.0V. Low threshold voltage MOSFET should be selected to guarantee that it could fully turn on at Vgs = 6.0V.

The total power dissipation of external MOSFETs consists of conduction and switching losses. The conduction losses of high side and low side MOSFETs are described by equation (7) and (8), respectively.

(High-side MOSFET)

$$P_{H\text{-}CON} = I_0^2 \times D \times R_{DS(ON)} \times q_r \quad (W) \quad (7)$$

(Low-side MOSFET)

$$P_{L\text{-}CON} = I_0^2 \times (1-D) \times R_{DS(ON)} \times q_r \quad (W) \quad (8)$$

Where

q_r is temperature dependency of $R_{ds(on)}$

The total switching loss is approximated as.

$$P_{SW} = I_{OUT} \times \frac{V_{DS(OFF)}}{2} \times (t_r + t_f) \times f_s \quad (W) \quad (9)$$

Where

$V_{DS(OFF)}$ is voltage from drain to source at MOSFET off time.

t_r and t_f are rise-time and fall-time, respectively.

I_{OUT} = Load current

f_s = Switching frequency

The MOSFET should be capable of handling the power loss over the entire operating range.

Design Example:

Design the power stage for a synchronous step-down converter having the following specifications:

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A, ΔV_{OUT} < 25mV, switching frequency = 200kHz, to determine the value of inductor and output capacitor (Using electrolytic capacitor).

First, select ripple current of inductor is 20% of output current, from equation (1)

$$L = (12 - 5) \times \frac{5}{12 \times 200K \times 0.2 \times 5} = 14.58 mH$$

Select L = 15µH

From equation (5)

$$25mV = 1 \times r_C$$

Select two electrolytic capacitors C = 470µF, r_C = 43mΩ in parallel.

Setting the Current Limit

The RT9206 limits output current by sensing low side MOSFET voltage drop (V_{SD}) when it turns on. The drop voltage caused by on-state resistance $R_{DS(ON)}$ is described as :

$$V_{SD} = R_{DS(ON)} \times I_L \quad (10)$$

When V_{SD} >300mV, the current limit function will be activated and latch the controller. So the current limit function can be set by MOSFETs selection. The relation of maximum inductor current $I_{L(LIM)}$ and on-state resistance of MOSFET ($R_{DS(ON)}$) is described as :

$$R_{DS(ON)} = \frac{300 \times 10^{-3}}{I_{L(LIM)}} \quad (\Omega) \quad (11)$$

Setting the Output voltage

The output voltage is set by external voltage divider and reference voltage. The feedback pin (FB, LFB1, and LFB2) is connected to the inverting input of error amplifier and is referenced to 0.8V reference voltage at non-inverting input as shown in Figure 3.The output voltage is set by the following equation.

$$V_{OUT} = (1 + \frac{Ra}{Rb}) \times 0.8 \quad (12)$$

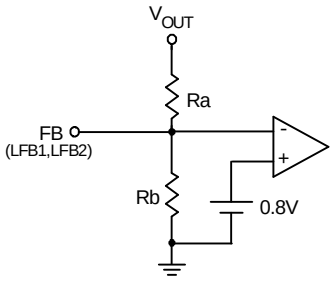


Figure 3. The connected diagram of external voltage divider and reference voltage

If high value resistors are used, the input bias current of FB pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-start setting

Figure 4 shows the typical soft-start timing waveforms of RT9206. The soft-start time of Buck converter can be set by selecting the soft-start capacitance value. The delay time between input voltage applied and output voltage starting to ramp up (T_{DELAY}) is calculated as: The total time from input voltage applied to output voltage buildup (T_{VR}) is calculated as :

$$T_{VR} = 57 \times C_{SS} \times 10^6 \quad (ms) \quad (13)$$

The effective soft-start time (T_{SS}) during that output voltage ramps up from zero to set voltage is calculated as :

$$T_{SS} = (320 \times \frac{V_{OUT}}{V_{IN}}) \times 10^6 \times C_{SS} \quad (ms) \quad (14)$$

Besides, appropriate soft-start capacitor should be selected so that the start-up current will not trigger the current limit function. And make sure that the input power source could supply the soft-start current.

The total time from input voltage applied to power good signal pull-high (T_{PGOOD}) is calculated as :

$$T_{PG} = 640 \times C_{SS} \times 10^6 \quad (ms) \quad (15)$$

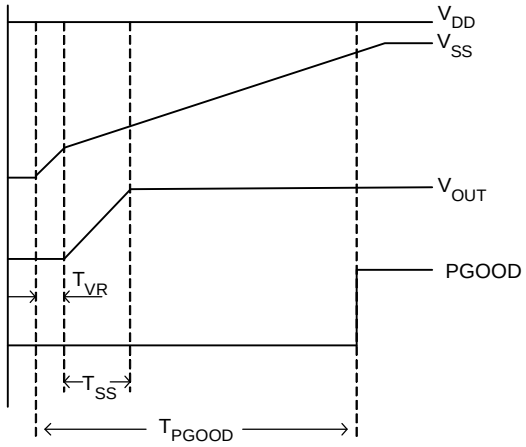


Figure 4. The soft-stat timing diagram of RT9206

For the example of C_{SS} = 1μF, V_{IN} = 12V, V_{OUT} = 5V, then T_{VR} = 57ms, T_{SS} = 133ms and T_{PGOOD} = 640ms.

Shutdown

The power stage can be shutdown by pulling soft-start pin below 0.7V. During shutdown, both of high side MOSFET (S1) and low side MOSFET (S2) are turned off.

Setting the switching frequency

The switching frequency can be set by a resistor (R_{RT}) connecting between RT and GND pins. Equation (16) describes the relationship of R_{RT} and switching frequency. As R_T open the normally operated frequency is 200kHz.

$$R_{RT} = \frac{62\times10^8}{f_S - 200\times10^3} \ (\Omega) \qquad (16)$$

R_{RT} Connecting Between RT and GND Pins	
f_S(kHz)	R_{RT} (kΩ)
250	120
300	55
350	37.5
400	30.6
450	24.4
500	22.5
550	19.3
600	16.8

Boost Component Selection

The booststrap gate drive circuit is used to drive high side N-channel MOSFET. The boost capacitor should be a good quality and can operate in high frequency. The value of boost capacitor depends on the total gate charge (Q_{Hg}) to turn on the MOSFETs. Assuming steady state operation, the following equation can be used to calculate the capacitance value to achieve the targeted ripple voltage DV_{BOOT}.

$$C_{BOOT} = \frac{Q_{Hg}}{\Delta V_{BOOT}} \qquad (F)$$

The capacitor in the range of 0.1μF to 1μF is generally adequate for most applications.

The VINT pin bypass capacitor C_{INT} needs to charge the boost capacitor, to drive the low side MOSFET, and to power the RT9206. C_{INT} should locate near VINT and GND pins with short and wide traces. Generally, a 4.7μF high frequency ceramic capacitor is recommended.

Feedback Compensation

The RT9206 is a voltage mode controller. The control loop is a single voltage feedback loop including a trans-conductance error amplifier and a PWM comparator.

To achieve fast transient response and accurate output regulation, appropriate feedback compensation is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin. Generally, the phase margin in a range of 45° to 60° is desirable. Figure 4 shows the simplified diagram of synchronous buck converter and control loop.

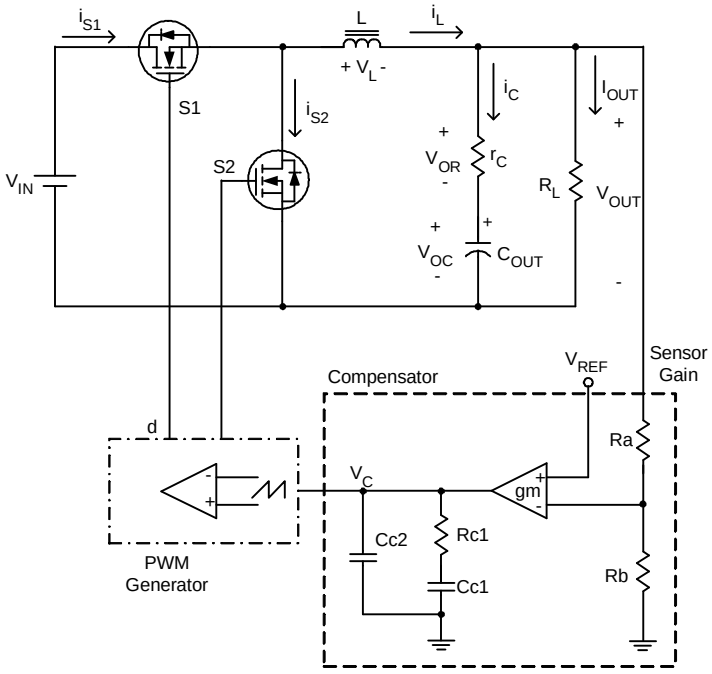


Figure 5. The simplified diagram for synchronous Buck converter and control loop.

From control system point of view, the block diagram of Figure 5 is shown in Figure 6.

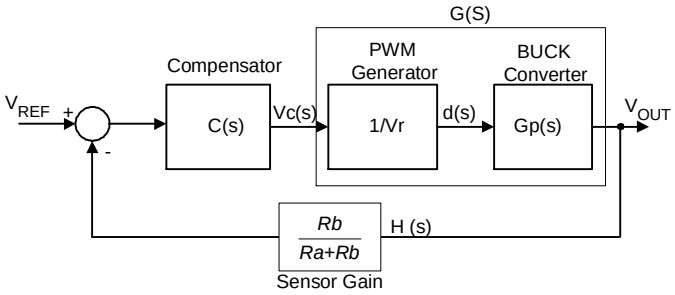


Figure 6. The control block diagram of synchronous Buck converter

First, deriving the accurate small-signal models of power stage, the equation (18) is the transfer function of $v_O(s)/d(s)$, which be obtained by space averaging technique.

$$G_{P(S)} = \frac{V_{OUT(S)}}{d_{(S)}} = \frac{1 + rc \times C_O \times S}{S^2 \times L \times C_O + S(\frac{L}{R_L} + rc \times C_O) + 1} \times V_{IN} \quad (18)$$

Next, deriving the transfer function $d(s)/v_C(s)$ of the direct duty ratio pulse-width modulator (PWM Generator). The transfer function $T_m(s)$ of the modulator is given by

$$T_{m(S)} = \frac{d_{(S)}}{V_{C(S)}} = \frac{1}{Vr} \quad (19)$$

where, V_r is the amplitude of ramp-waveform which is listed in datasheet.

For simplification, the transfer function of PWM generator and Buck converter can is combined. The resulting is shown in equation (20)

$$G_{(S)} = \frac{V_{OUT(S)}}{V_{C(S)}} = \frac{1 + rc \times C_O \times S}{S^2 \times L + C_O \times S(\frac{L}{R_L} + rc \times C_O) + 1} \times \frac{V_{IN}}{Vr} \quad (20)$$

The transfer function of Equation (20) is a second order system and Bode plot is shown in Figure 7.

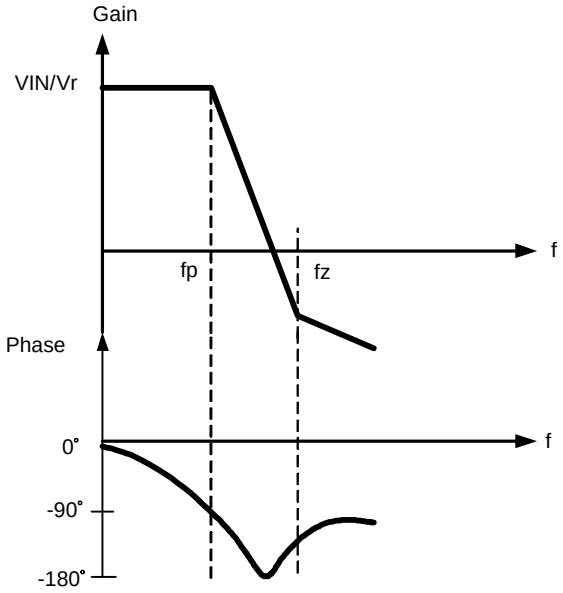


Figure 7. The Bode plot of Buck power stage

In Figure 7, the resonance of the output LC filter produces a double pole and –40dB/decade slop. The resonance frequency is expressed as follows :

$$f_P = \frac{1}{2p \times \sqrt{L \times C_O}} \quad (Hz) \quad (21)$$

The Effective Series Resistance (ESR) of capacitor and capacitance introduces one zero into system, the zero is given as :

$$fz = \frac{1}{2p \text{ x rc x } C_O} \quad (Hz) \qquad (22)$$

In the voltage-mode Buck converter shown in Figure 5, the loop gain of system is

$$T_{L(S)} = C_{(S)} \text{ x } \frac{1}{Vr} \text{ x } G_{P(S)} \text{ x } H_{(S)} = C_{(S)} \text{ x } G_{(S)} \text{ x } H_{(S)} \qquad (23)$$

The desired loop gain and phase margin is show in the Bode plot of Figure 8.

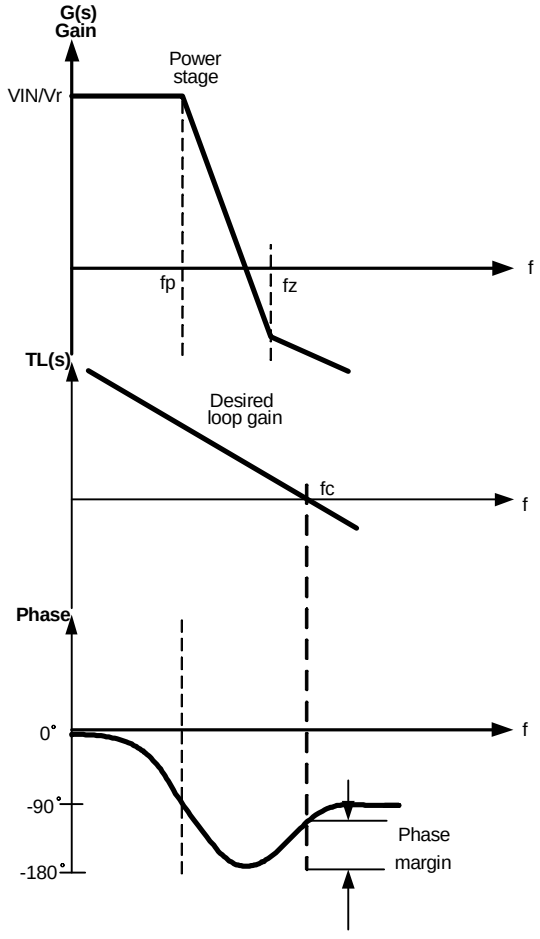


Figure 8. The Bode plot of desired loop gain and phase margin

Where the f_C is zero crossover frequency defined as the frequency when the loop gain equals unity. Typically, f_C be chosen in range 1/10 to 1/20 of switching frequency. f_C determines how fast the dynamic load response is. The higher f_C with the faster dynamic response, and the phase margin in the range of 45° to 60° is desirable.

So, the transfer function of compensator C(s) must be designed to meet these requirements. In many applications, use an electrolytic capacitor as the output capacitor, if the zero (f_Z) caused by Effective Series Resistance (ESR) of capacitor is a few kHz and smaller than 8 times f_P, the type 2 (PI) can be used to get desired compensation. Figure 9 shows the typical type 2 trans-conductance error amplifier and the Bode plot is also shown in Figure 10.

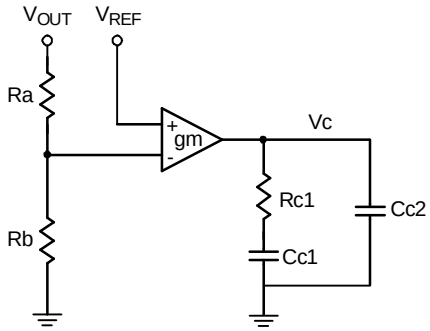


Figure 9. The typical type 2 trans-conductance error amplifier.

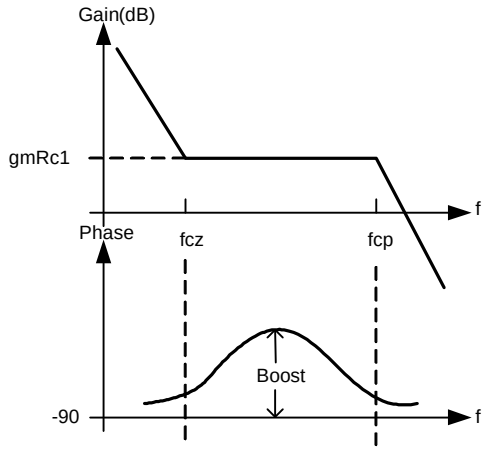


Figure 10. The Bode plot of type 2 trans-conductance error amplifier

The design procedure as following :

(1). Selecting the zero crossover frequency f_C is 1/10 to 1/20 switching frequency. Then according equation (24) set the resistor R_{C1} to determine the zero crossover frequency.

$$R_{C1} \approx \frac{Vr \times L \times f_C}{V_{IN} \times gm \times r_C} \times \frac{V_{OUT}}{V_{REF}} \quad (\Omega) \qquad (24)$$

(2). Place the zero of compensator is 70% fp that is resonance frequency of power stage. The compensator capacitor Cc1 can be selected to set the zero. The equation is shown in following :

$$C_{C1} = \frac{\sqrt{L \times C_O}}{0.7 \times R_{C1}} \quad (F) \qquad (25)$$

(3). Set a second pole to suppress the switching noise. Assume the pole is one half of switching frequency f_s, which results in capacitor Cc2 as shows in following:

$$C_{C2} = \frac{1}{p \times R_{C1} \times f_s - \frac{1}{C_{C1}}} \approx \frac{1}{p \times R_{C1} \times f_s} \quad (F) \qquad (26)$$

Design example

Design example of type 2 compensator: the schematic is shown in Figure 4, where the parameters as following : V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A, switching frequency = 200kHz, L = 15µH, C_O = 940µF, r_C = 22mΩ, the parameters of RT9206 as following : gm = 1.6ms, ramp amplitude = 1.9V, and reference voltage Vref = 0.8V.

Step1. Determine the power stage poles and zeros. The pole caused by the output inductor and output capacitor is calculated as :

$$f_P = \frac{1}{2p\sqrt{L \times C_O}} = \frac{1}{2p\sqrt{15m \times 940m}} = 1.34kHz$$

$$f_Z = \frac{1}{2p \times r_C \times C_O} = \frac{1}{2p \times 22m\Omega \times 940mF} = 7.7kHz$$

Step2. Determine the zero crossover frequency and compensated type.

Select desired zero-crossover frequency :

$f_C \leq f_S/10 \sim f_S/20$

Select f_C = 20kHz

Step3. Determine desired location of poles and zeros for type2 compensator.

Select:

$$f_{CZ} = 0.7 \times f_P = 0.7 \times 1.34kHz = 938Hz$$

Assume

$$f_{CP} = \frac{f_S}{2} = 100kHz$$

Step4. Calculate the real parameters-resistor and capacitors for type2 compensator.

From equation (21), the R_{C1} is calculated as following :

$$R_{C1} = \frac{f_C \times L \times Vr}{r_C \times V_{IN} \times gm} \times \frac{V_{OUT}}{V_{REF}}$$

$$= \frac{20kHz \times 15mH \times 1.9}{22m\Omega \times 12V \times 1.6ms} \times \frac{5V}{0.8V} = 8.4k\Omega$$

Select R_{C1} = 8.2kΩ

Calculate C_{C1} from equation (25)

$$C_{C1} = \frac{\sqrt{L \times C_O}}{0.7 \times R_{C1}} = \frac{\sqrt{15m \times 940m}}{0.7 \times 8.2k} = 20.7nF$$

Select C_{C1} = 22nF

Second capacitor C_{C2} can be calculated using equation (26)

$$C_{C2} = \frac{1}{p \times R_{C1} \times f_S} = \frac{1}{p \times 8.2k\Omega \times 200kHz} = 194pF$$

Select C_{C2} = 220pF

Linear Regulator

Output Capacitor Selection

Solid tantalum capacitors are recommended for use on the output capacitors of LDO because their typical ESR is very close to the ideal value required for loop compensation. Tantalums also have good temperature stability: a good quality tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of 125°C to –40°C. ESR will vary only about 2X going from the high to low temperature limits.

Linear Regular MOSFETs Selection

The main consideration of pass MOSFETs of linear regulator is package selection for efficient removal of heat. The power dissipation of a linear regulator is

$$P_{linear} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (W) \quad (26)$$

The criterion for selection of package is the junction temperature below the maximum desired temperature with the maximum expected ambient temperature.

Layout Consideration

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. First, place the PWM power stage components. Mount all the power components and connections in the top layer with wide copper areas. The MOSFETs of Buck, inductor, and output capacitor should be as close to each other as possible. This can reduce the radiation of EMI due to the high frequency current loop. If the output capacitors are placed in parallel to reduce the ESR of capacitor, equal sharing ripple current should be considered. Place the input capacitor directly to the drain of high-side MOSFET. The MOSFETs of linear regulator should have wide pad to dissipate the heat. In multilayer PCB, use one layer as power ground and have a separate control signal ground as the reference of the all signal. To avoid the signal ground is effect by noise and have best load regulation, it should be connected to the ground terminal of output. Furthermore, follows below guidelines can get better performance of IC :

- The IC needs a bypassing ceramic capacitor C1 as a R-C filter to isolate the pulse current from power stage and supply to IC, so the ceramic capacitor C1 should be placed adjacent to the IC.
- Place the high frequency ceramic decoupling close to the power MOSFETs.
- The feedback part should be placed as close to IC as possible and keep away from the inductor and all noise sources.
- The components of bootstraps (C8, C9 and D1) should be closed to each other and close to MOSFETs.
- The PCB trace from UGATE and LGATE of controller to MOSFETs should be as short as possible and can carry 1A peak current.
- Place all of the components as close to IC as possible.

Figure 11 shows the typical PCB layout of synchronous Buck converter with RT9206 controller

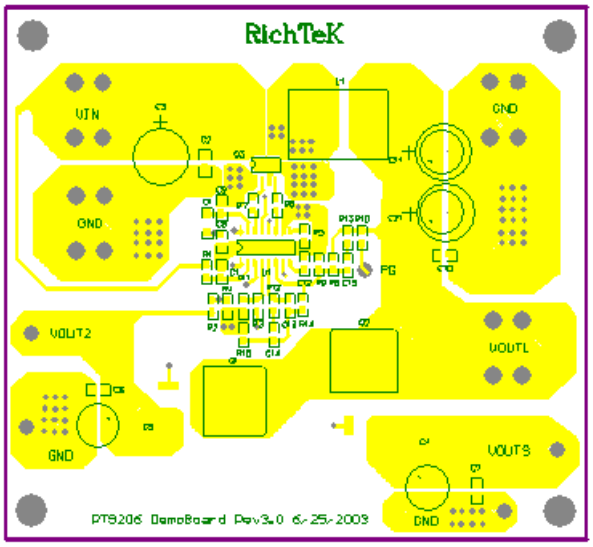
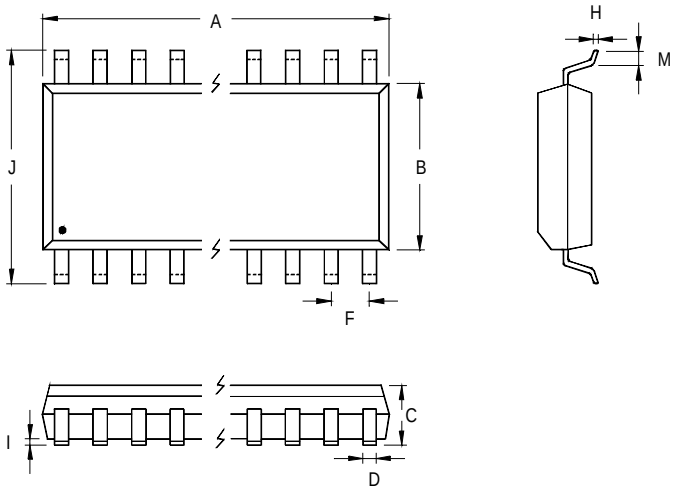


Figure 11. The PCB layout of synchronous Buck converter with RT9206 controller

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	9.804	10.008	0.386	0.394
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

16-Lead SOP Plastic Package

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