6A, 6V, Synchronous Step-Down Converter with REFIN

General Description

The RT2660A in thermally enhanced VQFN-20L 3.5x4 package is a full featured 6V, 6A synchronous step-down DC-DC converter designed specifically for Double Data Rate (DDR) memory termination, which provides a continuous 6A sink and source current and fixed 1/2 DDQ at output. The current mode COT architecture with external compensation allows the transient response to be optimized over a wide range of loads and achieves nearly constant switching frequency over line, load, and output voltage ranges. The multiple sets of over-current limit and switching frequency offer an optimized power chain for application design.

Efficiency is maximized through the integrated 20mΩ/ 10mΩ MOSFETs, and cycle-by-cycle current limit provides protection against shorted outputs. Output external tracking function, output soft discharge, power good indicating, output droop support are all featured in the RT2660A. In addition, the device is specified from 0°C to 85°C to perform an excellent regulation with an accurate 1% reference voltage over temperature.

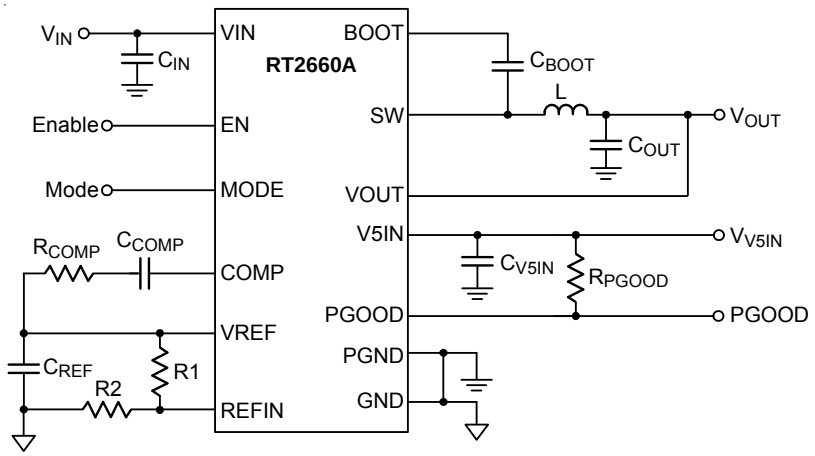
Features

- **Continuous 6A Sink or Source Output Current Ability and Droop Design for DDR Memory Termination Applications**
- **Low $R_{DS(ON)}$ Power N-MOSFET Switches 20mΩ/ 10mΩ**
- **Input Voltage Range : 0.8V to 6V**
- **Output Adjustable from 0.4V to 2V**
- **Current-Mode Constant On-Time Control Design Enables Fast Transient Response**
- **Supports All MLCC Output Capacitor and SP/ POSCAP with Robust Loop Stabilization**
- **Selectable 600kHz or 1MHz Switching Frequency**
- **Supports Pre-Biased Start-Up**
- **Selectable Over-Current Protection**
- **Various Operation Mode Selection for Different Application Requirements**
- **External Tracking Start-Up Application**
- **Enable Input Control and Power Good Indicator**
- **Under-Voltage and Over-Voltage Protection**

Applications

- DDR-2/3/4 VTT Regulation (1/2V_{DDQ}) for Enterprise Servers, Ethernet Switches and Routers, Global Storage, GSM Base Station, and Industrial equipments
- Enterprise POL (using precision internal VREF)

Simplified Application Circuit



Ordering Information

RT2660A □□

- Package Type
  QV : VQFN-20L 3.5x4 (V-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- A : Latched OVP and UVP

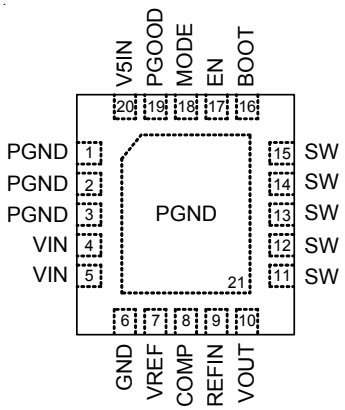
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

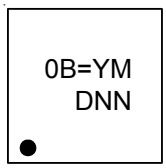
Pin Configuration

(TOP VIEW)



VQFN-20L 3.5x4

Marking Information



0B= : Product Code

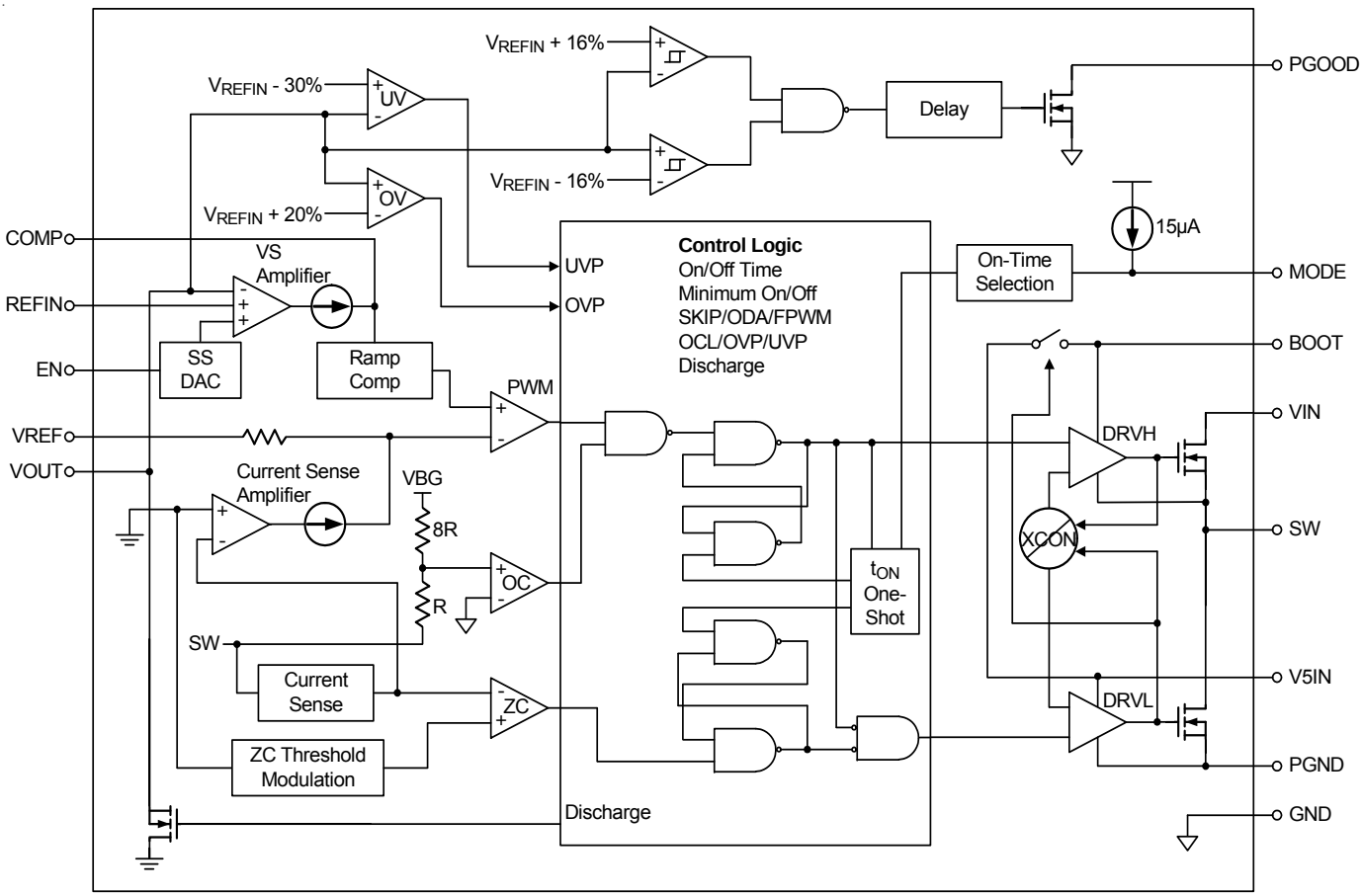
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2, 3, 21 (Exposed Pad)	PGND	Power ground. Provide the ground return path for the low-side power MOSFET and positive input of an internal amplifier for current sensing circuit. The exposed pad must be soldered to a large PCB and connected to PGND for minimum power dissipation.
4, 5	VIN	Power input. Supplies the power switches of the device.
6	GND	Signal ground. Provides the return path for control circuitry and internal reference.
7	VREF	Reference output. A specified 2V reference output is supplied by internal linear regulator. Decouple with a 0.22μF capacitor or greater between this pin and GND.
8	COMP	Compensation node. The current comparator threshold increases with this control voltage. Connect external compensation elements between this pin and VREF pin to stabilize the control loop.
9	REFIN	Reference input. The output voltage is targeted by reference input, which is applied from 0.4V to 2V.
10	VOUT	Output voltage monitor node. A negative input of the gm error amplifier and it is allowed to be a discharge path if any protection is triggered.
11 to 15	SW	Switch node. SW is the switching node that supplies power to the output and connect the output LC filter from SW to the output load.
16	BOOT	Bootstrap supply for high-side gate driver. Connect a 100nF or greater capacitor from SW to BOOT to power the high-side switch.

Pin No.	Pin Name	Pin Function
17	EN	Enable control input. Floating this pin or connecting this pin to logic high can enable the device and connecting this pin to GND can disable the device.
18	MODE	Mode selection node. There are 8 modes in RT2660A. Connect the specified resistance to GND for selecting different modes of switching frequencies, OC limit thresholds, and light-load operations.
19	PGOOD	Power good indicator output. This pin is an open-drain logic output that is pulled to ground when the output voltage is lower or higher than its specified threshold under the conditions of OVP, OTP, dropout, EN shutdown, or during slow start.
20	V5IN	Fixed 5V supply voltage input. Supplies the control circuitry and internal reference of the device.

Functional Block Diagram



Operation

The RT2660A is a synchronous low voltage step-down converter that can support the V5IN range from 4.5V to 5.5V and the output current can be up to 6A. The RT2660A uses a constant on-time, current mode architecture. In steady-state operation, the high-side N-MOSFET is turned on when the current feedback reaches COMP level which is the amplified difference between the reference voltage and the feedback voltage.

The switching frequency of 600kHz or 1000kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is set using the mode pin.

The RT2660A reduces the external component count by integrating the boot recharge MOSFET. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and SW pins. The boot capacitor voltage is monitored by an BOOT detection circuit and turns off the high-side MOSFET when the voltage falls below a threshold voltage.

The SS pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin for slow start. The SS pin is discharged before the output power up to ensure a repeatable restart after an over-temperature fault, UVLO fault or disable condition.

The error amplifier EA adjusts COMP voltage by comparing the output voltage to the REFIN voltage. When the load increases, it causes a drop in the feedback voltage relative to the reference, then the COMP voltage rises to allow higher inductor current to match the load current.

Bootstrap Voltage (Boot) and Low Dropout Operation

The RT2660A has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage. When the BOOT voltage is lower than the threshold voltage, low-side MOSFET turns on and built-in bootstrap MOSFET will recharge the BOOT capacitor. The high-side MOSFET is always turned off when BOOT voltage is lower than threshold voltage.

PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation :

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

Error Amplifier

The RT2660A has a transconductance amplifier. The error amplifier compares the V_{OUT} voltage to the REFIN voltage The REFIN voltage can comes from external power source or taps off the voltage divider from the 2V VREF. The transconductance of the error amplifier is 1000μA/V during normal operation. The frequency compensation components are placed between the COMP pin and ground.

Auto-Zero Current Detector

The auto-zero current detector circuit senses the SW waveform to adjust the zero current threshold voltage. When the current of low-side MOSFET decreases to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can adjust for different conditions to get better efficiency.

Protection Features

The RT2660A has many features to protect the device.

Under-Voltage Protection (UVLO)

The RT2660A continuously monitors the voltage on the V5IN pin to ensure that the voltage level is high enough to bias the device properly and to provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.3V and has a nominal hysteresis of 440mV. If the 5V UVLO limit is reached, the converter transitions the phase node into an off function. And the converter remains in the off state until the device is reset by cycling 5V until the 5V POR is reached (2.3V nominal). The power input does not have an UVLO function.

Power Good

The RT2660A has one open-drain power good (PGOOD) pin. The PGOOD pin de-asserts as soon as the EN pin is pulled low or an under-voltage condition on V5IN or any other fault is detected.

Output Over-Voltage Protection (OVP)

In addition to the power good function described above, the RT2660A has additional OVP and UVP thresholds and protection circuits.

An OVP condition is detected when the output voltage is approximately 120% x V_{REFIN}. In this case, the converter de-asserts the PGOOD signals and performs the over-voltage protection function. During OVP, the low-side MOSFET is always on before triggering a negative over-current. When a negative OC is also tripped, the low-side MOSFET is no longer continuously on, and pulsed signals are generated to limit the negative inductor current.

For the RT2660A OVP latch mode, when the VOUT pin voltage drops below 400mV, the low-side MOSFET is turned off and the converter latches off. The converter remains in the off state until the device is reset by cycling 5V until the 5V POR is reached or when the EN pin is toggled off and on.

Output Under-Voltage Protection (UVP)

Output under-voltage protection works in conjunction with the current protection described in the over-current protection and over-current limit sections. If the output voltage drops below 68% of V_{REFIN}, after approximately a 256μs delay, the device stops switching and enters UVP.

For the RT2660A UVP latch mode, the device stop switching and enter latch mode. The converter remain in the off state until the device is reset by VIN or EN.

Over-Current Protection (OCP)

Both positive and negative over-current protection are provided in the RT2660A :

- Over-Current Limit (OCL)

  The RT2660A has cycle-by-cycle over current limiting protection. The inductor current is monitored during the low-side MOSFET turning on. When the inductor current is larger than the over current trip level, the high-side MOSFET turns off until the current drops below the OCL limit. Because the RT2660A uses a valley current limiting scheme, the average output current limit calculation is valley OCL trip level plus half of the inductor ripple current.

- Negative OCL

  The negative OCL circuit acts when the converter is sinking current from the output capacitor(s). The converter continues to act in a valley mode, the absolute value of the negative OCL set point is typically –9.3A or –7.3A (depending on mode selection).

Over-Temperature Protection (OTP)

The RT2660A has an over-temperature protection. When the device triggers the OTP, the device shuts down. Until the temperature drops below the low temperature threshold, the OTP relieves and the device re-soft starts.

Absolute Maximum Ratings (Note 1)

- Supply and Boot-to-Switch Input Voltages, VIN, V5IN, and (V_{BOOT} – V_{SW}) ---------- –0.3V to 7V
- Boot Pin Input Voltage, BOOT ---------- –0.3V to 14V
- Switch Node Input Voltage, SW ---------- –2V to 7V
- Switch Node, SW (<10ns) ---------- –5V to 10V
- EN Pin Input Voltage ---------- –0.3V to 7V
- MODE and REFIN Pin Input Voltages ---------- –0.3V to 3.6V
- VOUT Pin Input Voltage ---------- –1V to 3.6V
- COMP and VREF Output Voltages ---------- –0.3V to 3.6V
- PGOOD Output Voltage ---------- –0.3V to 7V
- PGND Output Voltage ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-20L 3.5x4 ---------- 3.49W
- Package Thermal Resistance (Note 2)
  VQFN-20L 3.5x4, θ_{JA} ---------- 28.6°C/W
  VQFN-20L 3.5x4, θ_{JC} ---------- 5.4°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  CDM (Charged Device Model) ---------- 1kV

Recommended Operating Conditions (Note 4)

- Input Supply Voltage, VIN ---------- 0.8V to 6V
- Input Logic Supply Voltage, V5IN ---------- 4.5V to 5.5V
- Output Voltage, V_{OUT} ---------- 0.4V to 2V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 5V, PGND = GND, T_A = –40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
V5IN Supply Input Operating Voltage	V_{5IN}	(Note 5)	4.5	5	5.5	V
VIN Supply Input Operating Voltage	V_{IN}	(Note 5)	0.8	--	6	V
V5IN Quiescent Current		V_{EN} = high	--	1.1	2	mA
V5IN Shutdown Current		V_{EN} = low	--	0.2	7	μA
VIN Shutdown Current			--	0.2	10	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V5IN Under-Voltage Lockout Threshold	V_{5IN_UVLO}	V_{EN} = high, V_{IN} rising	4.2	4.37	4.5	V
V5IN Under-Voltage Lockout Threshold Hysteresis	ΔV_{5IN_UVLO}		--	440	--	mV
V5IN Reset Threshold		OVP latch is reset when V_{V5IN} < reset threshold	1.5	2.3	3.1	V
Enable Voltage						
Enable Input Voltage	V_{IH}	V_{EN} rising	2	--	--	V
	V_{IL}	V_{EN} falling	--	--	0.5	
Enable Input Current			--	--	1	μA
Reference Voltage						
VREF Voltage	V_{VREF}	I_{VREF} = 0μA	1.98	2	2.02	V
		I_{VREF} = 50μA	1.975	2	2.025	
VREF Under-Voltage Lockout Threshold	V_{VREF_UVLO}	V_{EN} = high, V_{VREF} rising	--	1.8	--	
VREF Under-Voltage Lockout Hysteresis	ΔV_{VREF_UVLO}		--	100	--	mV
VREF Sink Current		V_{VREF} = 2.05V	--	2.5	--	mA
SW and BOOT						
Constant On-Time		V_{IN} = 5V, V_{OUT} = 1.05V, f_S = 1MHz (Note 5)	--	210	--	ns
		V_{IN} = 5V, V_{OUT} = 1.05V, f_S = 600kHz (Note 5)	--	310	--	
Minimum Off-Time		V_{IN} = 5V, V_{OUT} = 1.05V, f_S = 1MHz, V_{OUT} < V_{REFIN}	--	270	--	
Internal BOOT Switch On-Resistance		I_{BOOT} = 10mA, T_A = 25°C	--	--	10	Ω
Internal BOOT Switch Leakage Current		V_{BOOT} = 13V, V_{SW} = 6V	--	--	1	μA
Default Soft-Start						
Soft-Start Time	t_{SS}	From V_{EN} = High to V_{OUT} = 95%V_{REFIN}	--	1.6	--	ms
Soft-Start Delay Time		From V_{EN} = High to V_{OUT} ≥ 0V	--	260	--	μs
Error Amplifier and PWM Comparator						
Error Amplifier Trans-Conductance	gm		--	1	--	mA/V
Common Mode Input Voltage Range	V_{CM}	(Note 5)	0	--	2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Mode Input Voltage Range	V_{DM}		0	--	80	mV
Error Amplifier Sinking Current		V_{COMP} = 2V, $V_{OUT} - V_{REFIN}$ = –80mV	--	80	--	µA
Error Amplifier Sourcing Current		V_{COMP} = 2V, $V_{OUT} - V_{REFIN}$ = 80mV	--	–80	--	
Error Amplifier Input Offset		T_A = 25°C	--	0	--	mV
Error Amplifier –3dB Frequency		(Note 5)	4.5	6	7.5	MHz
Zero Crossing Comp Internal Offset	V_{ZXOFF}		--	0	--	mV
Current Limit and Internal Current Sense						
Low-Side Switch Sourcing Current Limit		Valley detection	--	7.6	--	A
Low-Side Switch Sinking Current Limit			--	–9.3	--	
Current Sense Trans-Impedance	R_{CS}	Low-side current sensing	43	53	57	mΩ
Power Good						
Power Good Falling Threshold		V_{OUT} falling (Fault)	--	84	--	%V_{REFIN}
Power Good Rising Hysteresis		V_{OUT} rising (Good)	--	8	--	
Power Good Rising Threshold		V_{OUT} rising (Fault)	--	116	--	
Power Good Falling Hysteresis		V_{OUT} falling (Good)	--	–8	--	
Minimum VIN Voltage for Indicating PGOOD		I_{PGOOD} sinks 2mA	0.7	0.9	1.1	V
Power Good Enable Delay Time		External tracking	--	8	--	ms
Power Good Indicating Good Delay Time			0.8	1	1.2	
Power Good Indicating Fault Delay Time			--	10	--	µs
Power Good Pull Low Voltage		PGOOD = fault, V_{V5IN} = 4.5V, I_{PGOOD} sinks 4mA	--	--	0.3	V
Power Good Leakage Current		PGOOD = good, V_{PGOOD} = 5.5V	–1	0	1	µA
VOUT						
VOUT Accuracy		V_{REFIN} = 1V, non-droop application	–1	--	+1	%V_{REFIN}
VOUT Soft Discharge Resistance			--	42	--	Ω
Over-Voltage Protection Threshold			115	120	125	%V_{REFIN}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Under-Voltage Protection Threshold		Device latches off and begins to soft discharge	65	68	71	%V_{REFIN}
Over-Voltage Protection Delay Time		From V_{OUT} > 120%V_{REFIN} to OVP trip	--	10	--	μs
Under-Voltage Protection Delay Time		From V_{OUT} < 68%V_{REFIN} to UVP trip	--	256	--	
Under-Voltage Protection Enable Delay Time		From V_{EN} = high to UVP enable	--	2	--	ms
		External tracking application, from V_{OUT} ≥ 0V to UVP enable	--	8	--	
Over-Temperature Protection						
Thermal Shutdown Threshold	T_{SD}		--	145	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	
Mode Selection						
MODE Threshold Voltage		Threshold 1	80	130	180	mV
		Threshold 2 (Note 5)	200	250	300	
		Threshold 3	370	420	470	
		Threshold 4	1765	1800	1850	
MODE Input Current			--	15	--	μA

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by design.

Typical Application Circuit

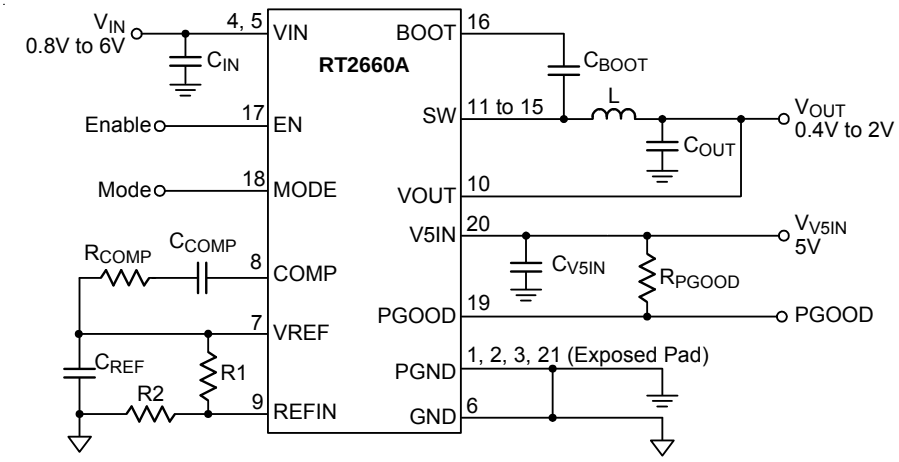
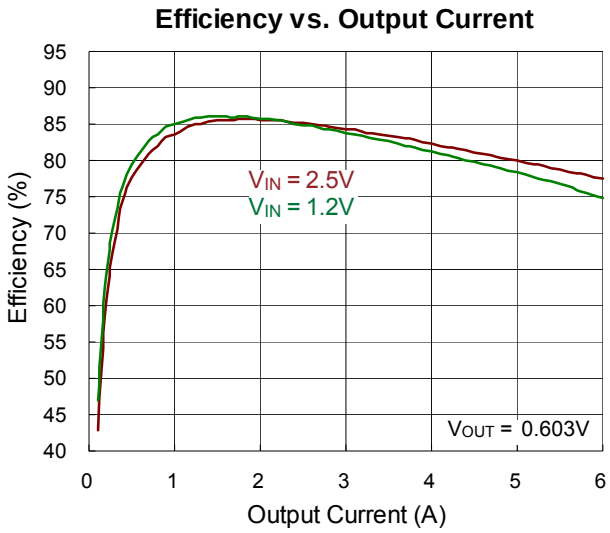
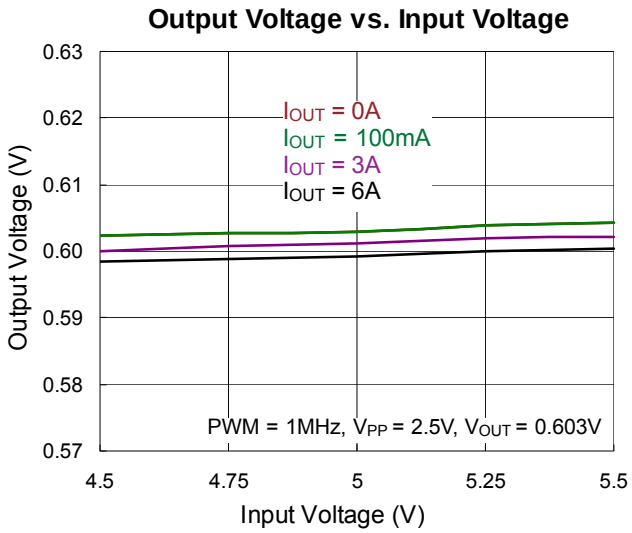


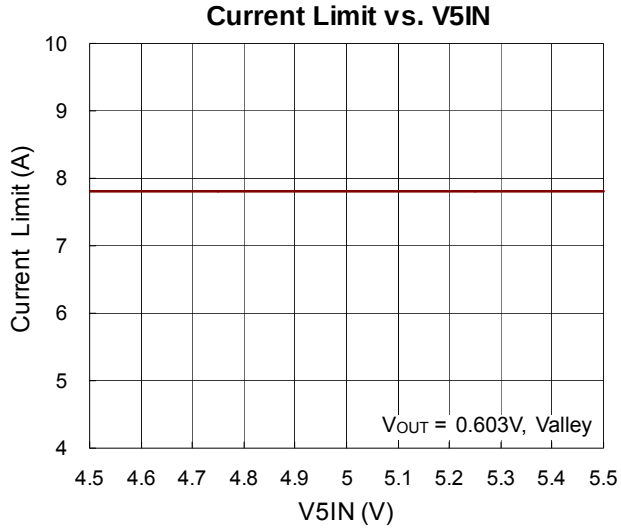
Table 1. Mode Definitions

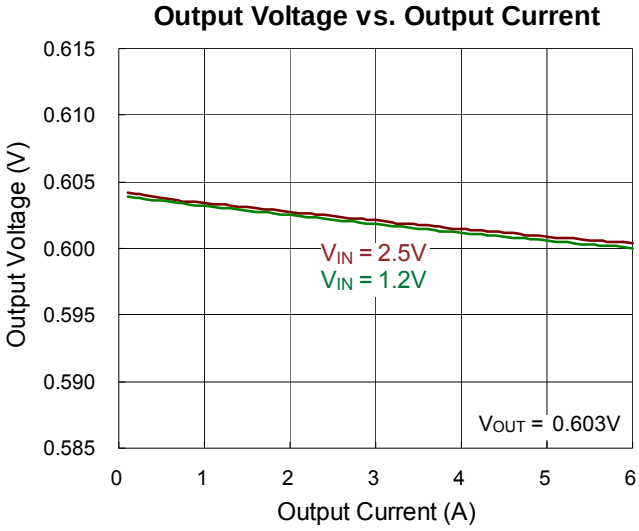
Mode	Mode Resistance (kΩ)	Light-Load Power Saving Mode	Switching Frequency (f_{SW})	Over Current Limit (OCL) Valley (A)
1	0	SKIP	600kHz	7.6
2	12		600kHz	5.4
3	22		1MHz	5.4
4	33		1MHz	7.6
5	47	PWM	600kHz	7.6
6	68		600kHz	5.4
7	100		1MHz	5.4
8	Open		1MHz	7.6

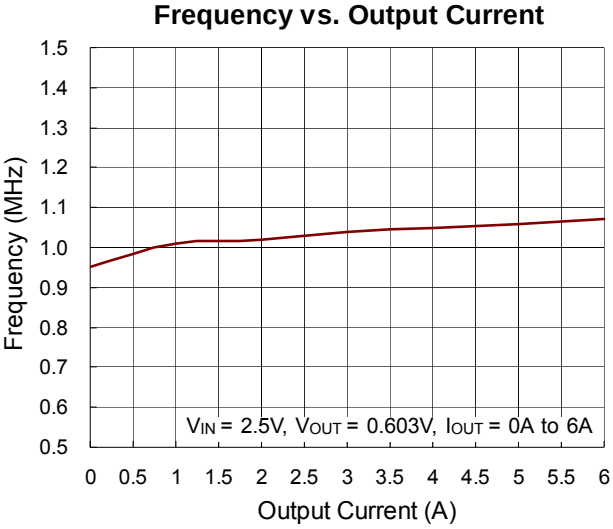
Typical Operating Characteristics

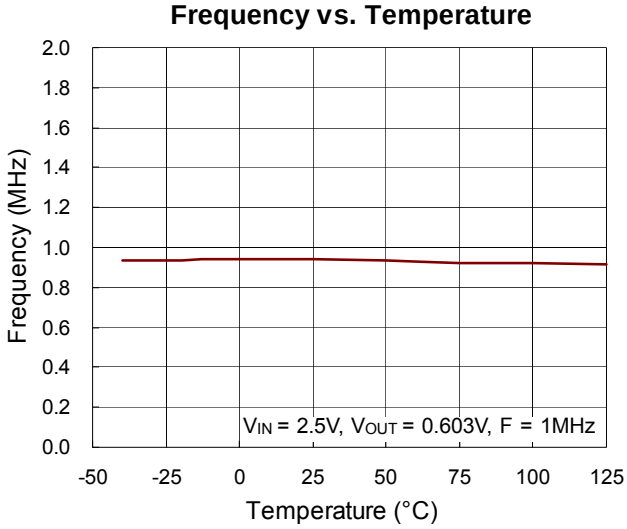




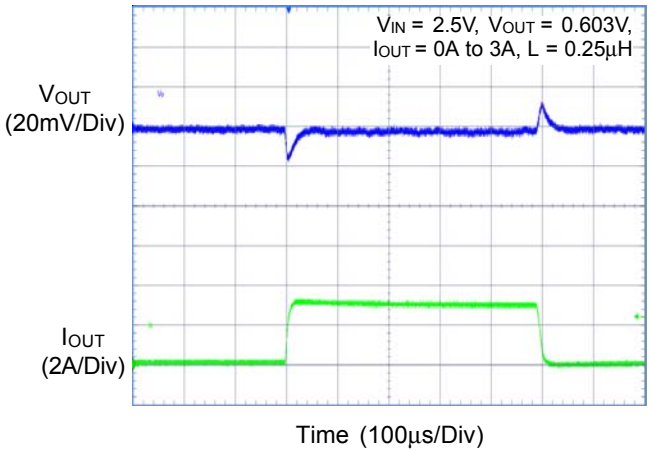




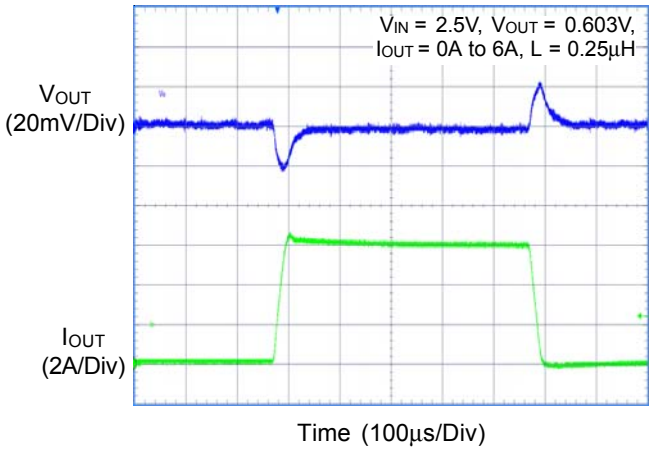




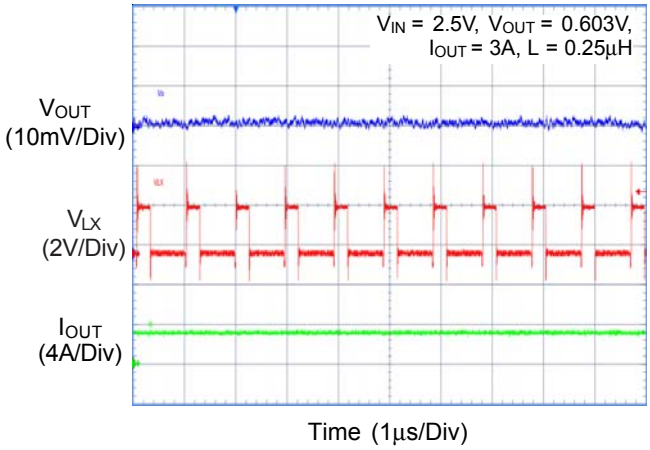
Load Transient Response



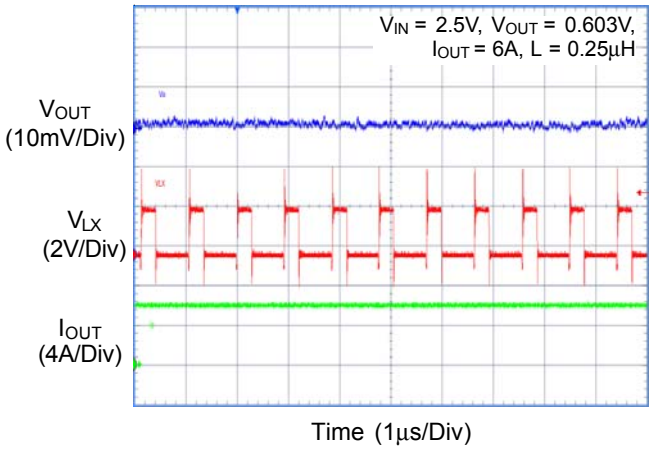
Load Transient Response



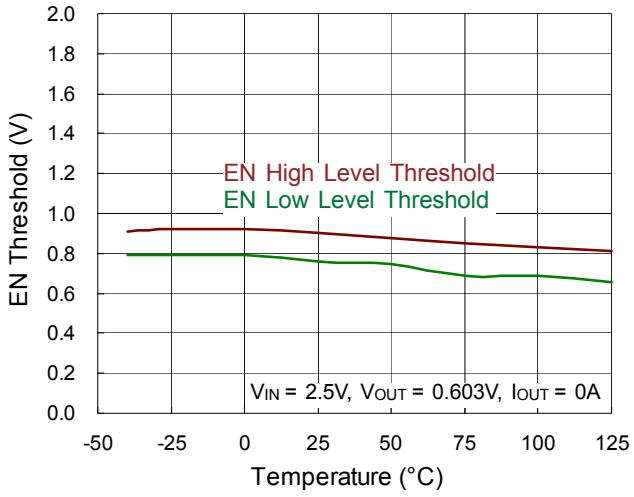
Output Ripple Voltage



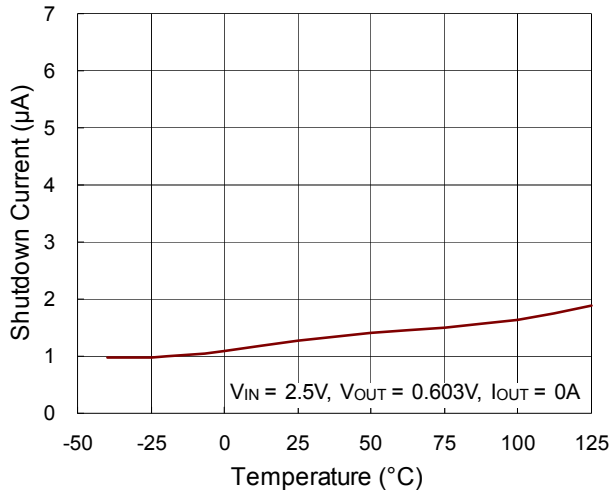
Output Ripple Voltage



EN Threshold vs. Temperature



Shutdown Current vs. Temperature



Application Information

The RT2660A employs current mode COT architecture that provides ease of use, low external component count and fast transient response. The Synchronous buck regulator capable of delivering up to 6A continuous current and set switching frequency up to 1MHz.

Some feature of Current mode COT

- Effective bandwidth is very high
- No slope compensation necessary
- Double complex zero at half the switching frequency term of fixed frequency peak CM converter disappears.

Operation of Current Mode COT

Referring to Figure 1, V_{COMP} is the amplified difference between the reference voltage and the feedback voltage. V_{CS} is valley current sense voltage (sensing the inductor current). The PWM comparator senses where the two waveforms cross and triggers the on time generator.

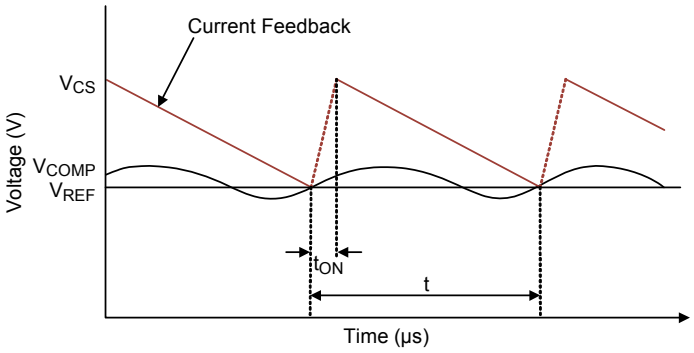


Figure 1. Current Mode COT Waveforms

Adaptive Constant On-Time Control

Adaptive on time generator makes the system operate in fixed frequency when V_{IN} or V_{OUT} change. The technique improves COT by making the one-shot on-time proportional to V_{OUT} and inversely proportional to VIN. In this way, an on-time is chosen as approximately what it would be for an ideal fixed-frequency PWM in similar input/output voltage conditions.

The on-time calculates equation of the buck converter as shows as follows :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where

f_{SW} is operate frequency.

Non-Droop Mode Operation

The RT2660A can be configured as a non-droop solution. The benefit of a non-droop approach is that load regulation is flat, therefore, in a system where tight DC tolerance is desired, the non-droop approach is recommended. For the Intel system agent application, non-droop is recommended as the standard configuration. The non-droop approach can be implemented by connecting a resistor and a capacitor between the COMP and the VREF pins. The purpose of the type II compensation is to obtain high DC feedback gain while minimizing the phase delay at unity gain cross over frequency of the converter.

The value of the resistor (R_C) can be calculated using the desired unity gain bandwidth of the converter, and the value of the capacitor (C_C) can be calculated by knowing where the zero location is desired. The capacitor C_P is optional, but recommended. Its appropriate capacitance value can be calculated using the desired pole location.

Figure 2 shows the basic implementation of the non-droop mode using the RT2660A.

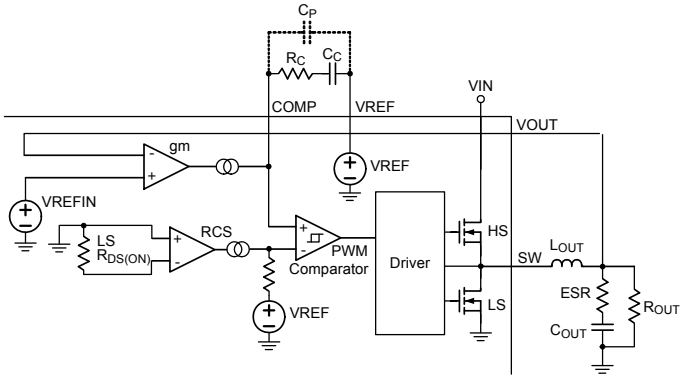


Figure 2. Non-Droop Mode

Droop Mode Operation

The terminology for droop is the same as *load line* or *voltage positioning* as defined in the Intel CPU VCORE specification. Based on the actual tolerance requirement of the application, load-line set points can be defined to maximize either cost savings (by reducing output capacitors) or power reduction benefits.

Accurate droop voltage response is provided by the finite gain of the droop amplifier. The equation for droop voltage is shown below Equation :

$$V_{DROOP} = \frac{R_{CS} \times I_{OUT}}{R_{DROOP} \times gm}$$

Where

- R_{CS} is current sense Trans-Impedance.
- R_{DROOP} is the value of resistor from the COMP pin to the VREF pin.
- gm is the Error Amplifier Trans-Conductance.

Figure 3 shows the basic implementation of the droop mode using the RT2660A.

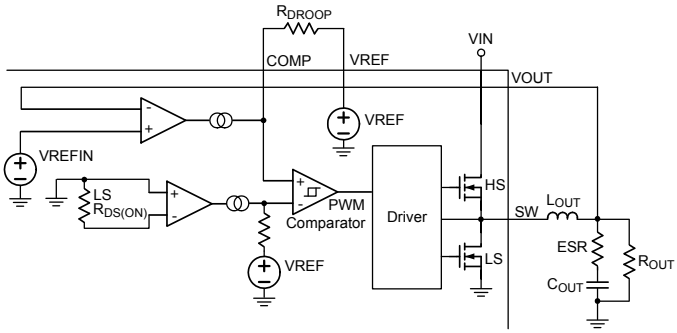


Figure 3. DROOP Mode

Power Sequences

Tracking Mode

In a tracking application, VDDQ can be VIN or it can be an additional voltage rail. Thus, R1 = R2 both in Figure 4 and Figure 5.

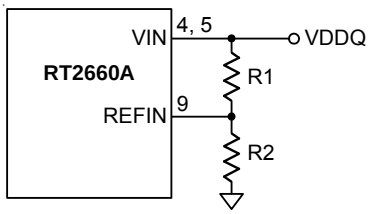


Figure 4. Tracking Configuration 1

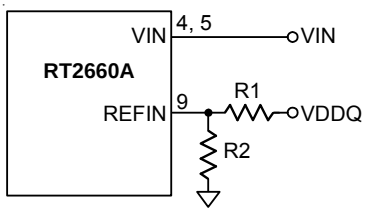


Figure 5. Tracking Configuration 2

The RT2660A can be configured for tracking application. When tracking configuration is desired, output voltage is also regulated to the REFIN voltage which comes from an external power source. In order for the RT2660A to track mode (see Figure 6). The valid REFIN voltage range is between 0.4V to 2V.

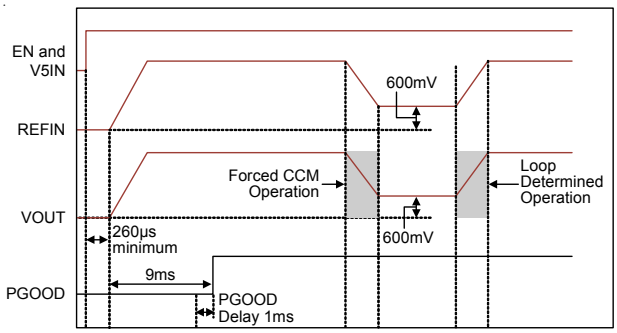


Figure 6. Tracking Startup Timing

Non-Tracking Mode

The RT2660A can be configured for non-tracking application. When non-tracking is configured, output voltage is regulated to the REFIN voltage which taps off the voltage dividers from the 2V reference voltage. Either the EN pin or the V5IN pin can be used to start up the device. The RT2660A uses internal voltage servo DAC to provide a 1.6ms soft-start time during soft-start initialization. (See Figure 7)

In a non-tracking application, the output voltage is determined by the resistive divider between the VREF pin and the REFIN pin.

$$V_{OUT} = V_{REF} \times \frac{R2}{R1+R2}$$

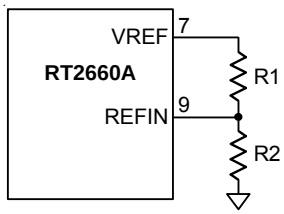


Figure 7. Non-Tracking Condition

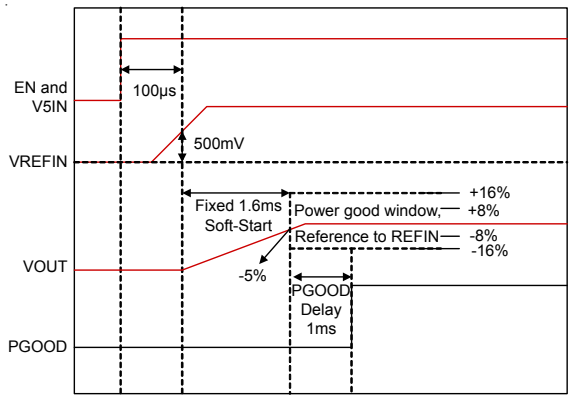


Figure 8. Non-Tracking Startup Timing

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.4(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{DD}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Stability Considerations

Setting the crossover frequency should be less than 1/5 of the switching frequency.

$$f_{CO} = \frac{1}{2\pi} \times \frac{gm}{C_{OUT}} \times \frac{R_C}{R_S} = 60kHz$$

Where

$$R_S = 53m\Omega,\ gm = 1000\mu A/V,\ C_{OUT} = 160\mu F$$

$$\text{So } R_C = \frac{60kHz \times 53m\Omega \times 160\mu F \times 2 \times 3.14}{1000\mu s} = 3.2k\Omega$$

Choose R_C value of 3.9kΩ. Then determine C_C, using the below equation :

$$f_z = \frac{f_{CO}}{5} = \frac{1}{2\pi \times R_C \times C_C}$$

To calculate C_C = 3.4nF, Choose the capacitor value of 2.2nF.

Then determine C_P, set the pole more than the switching frequency, using the below equation :

$$C_P = \frac{1}{2\pi \times R_C \times 2f_S} = \frac{1}{2 \times 3.9k\Omega \times 2 \times 600kHz} = 34pF$$

Choose the C_P to 33pF.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-20L 3.5x4 package, the thermal resistance, θ_{JA}, is 28.6°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (28.6°C/W) = 3.49W for a VQFN-20L 3.5x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

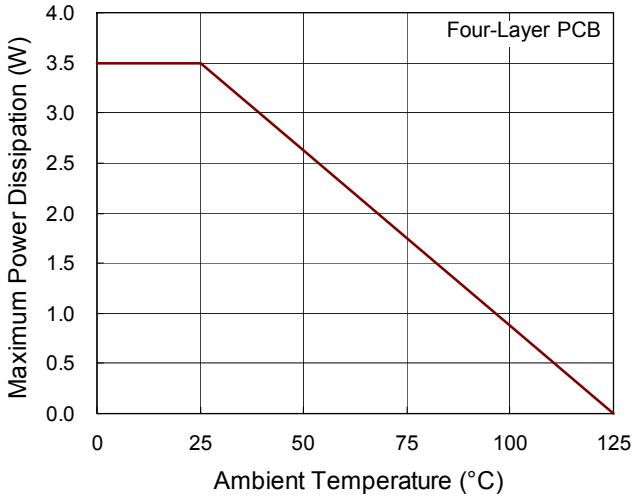


Figure 9. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT2660A.

- A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the GND pin at one point that is then connected to the PGND pin close to the IC. The exposed pad should be connected to GND.
- Connect the terminal of the input capacitor(s), C_{IN}, as close as possible to the VIN pin. This capacitor provides the AC current into the internal power MOSFETs.
- SW node is with high frequency voltage swing and should be kept within small area. Keep all sensitive small-signal nodes away from the SW node to prevent stray capacitive noise pick-up.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components.

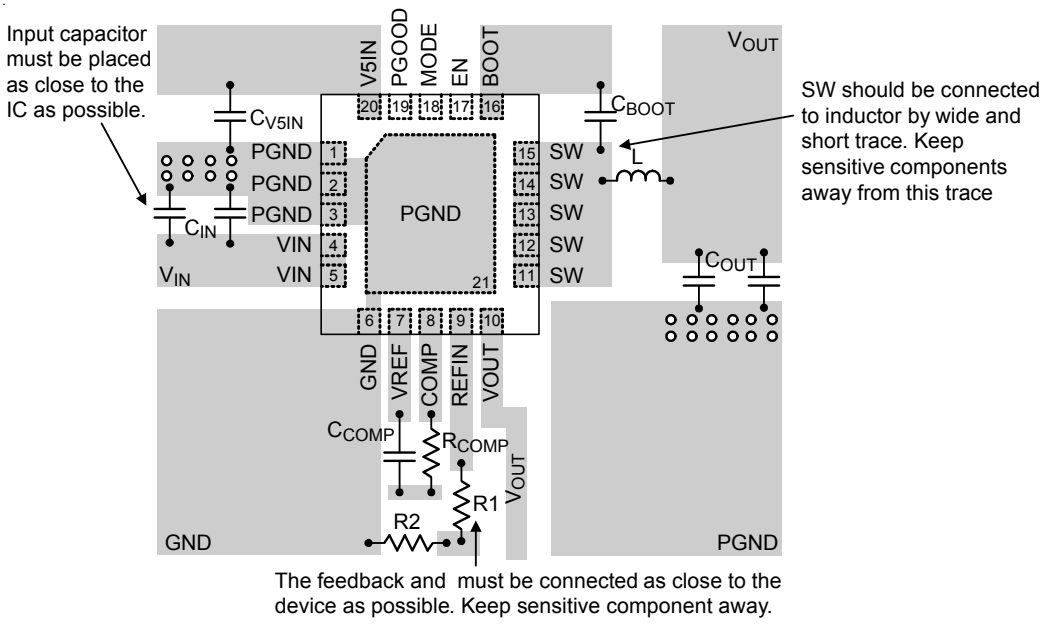


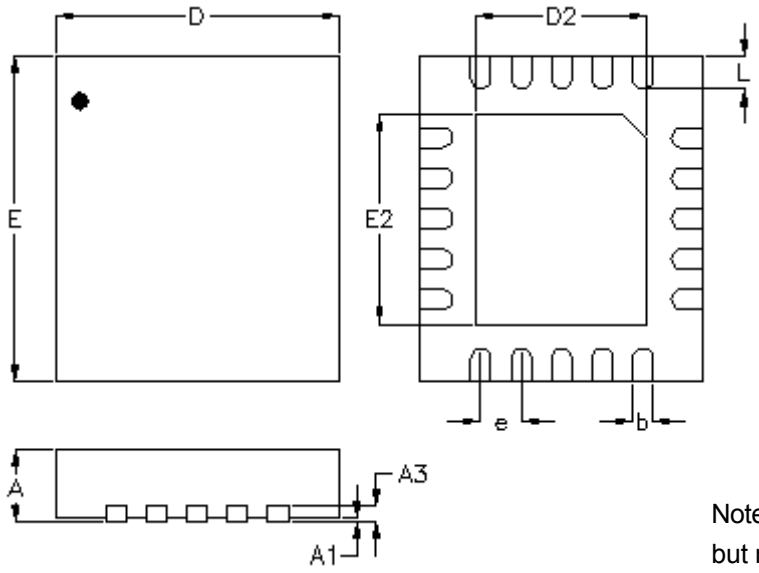
Figure 10. PCB Layout Guide

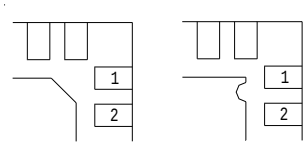
Table 2. Inductors

Recommended component selection for Typical Application.

Component Supplier	Series	Inductance (μH)	DCR (mΩ)	Current Rating (A)	Dimensions (mm)
TDK	SPM5030T-R35	0.35	2.1	14.9	5x5x3
Pulse	PA2509.201NL	0.2	0.35	32	7x8.5x8
WE	744308025	0.25	0.37	25	7x10x6.8

Outline Dimension





DETAIL A

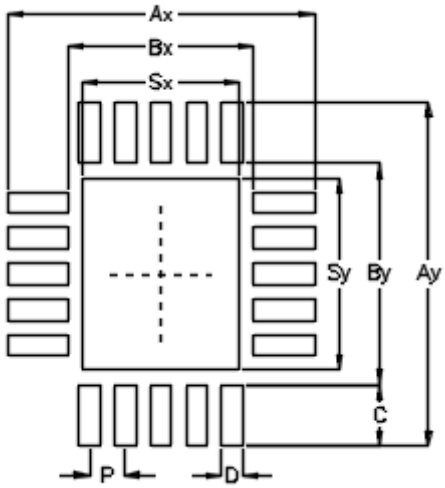
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	3.400	3.600	0.134	0.142
D2	2.050	2.150	0.081	0.085
E	3.900	4.100	0.154	0.161
E2	2.550	2.650	0.100	0.104
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 20L QFN 3.5x4 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3.5*4-20	20	0.50	4.30	4.80	2.60	3.10	0.85	0.30	2.20	2.70	±0.05

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单击下面可查看定价，库存，交付和生命周期等信息

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