# 2A, 18V, 700kHz ACOT™ Synchronous Step-Down Converter

## General Description

The RT7274/79/80/81 is a synchronous step-down DC/DC converter with Advanced Constant On-Time (ACOT™) mode control. It achieves high power density to deliver up to 2A output current from a 4.5V to 18V input supply. The proprietary ACOT™ mode offers an optimal transient response over a wide range of loads and all kinds of ceramic capacitors, which allows the device to adopt very low ESR output capacitor for ensuring performance stabilization. In addition, RT7274/79/80/81 keeps an excellent constant switching frequency under line and load variation and the integrated synchronous power switches with the ACOT™ mode operation provides high efficiency in whole output current load range. Cycle-by-cycle current limit provides an accurate protection by a valley detection of low-side MOSFET and external soft-start setting eliminates input current surge during startup. Protection functions include thermal shutdown for RT7274/79/80/81; output under voltage protection and output over voltage protection for RT7279/80 only.

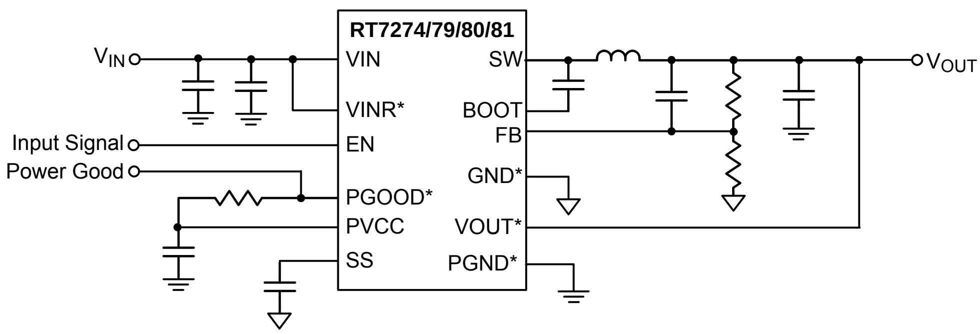
## Features

- **ACOT™ Mode Enables Fast Transient Response**
- **4.5V to 18V Input Voltage Range**
- **2A Output Current**
- **High Efficient Internal N-MOSFET Optimized for Lower Duty Cycle Applications**
- **105mΩ Internal Low-Side N-MOSFET**
- **Advanced Constant On-Time Control**
- **Allows Ceramic Output Capacitor**
- **700kHz Switching Frequency**
- **Adjustable Output Voltage from 0.765V to 8V**
- **Adjustable and Pre-biased Soft-Start**
- **Cycle-by-Cycle Current Limit**
- **Input Under Voltage Lockout**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

## Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

## Simplified Application Circuit




* : VINR pin for TSSOP-14 (Exposed Pad) only.
VOUT pin for TSSOP-14 (Exposed Pad) only.
PGND pin for TSSOP-14 (Exposed Pad) and WDFN-10L 3x3 only.
PGOOD pin for TSSOP-14 (Exposed Pad) and WDFN-10L 3x3 only.
GND pin for TSSOP-14 (Exposed Pad) and SOP-8 (Exposed Pad) only.

## Ordering Information

**Discontinuous Operating Mode**

RT7274□□
- Package Type
  SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

RT7280□□
- Package Type
  CP : TSSOP-14 (Exposed Pad)
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

**Forced PWM Mode**

RT7279□□
- Package Type
  CP : TSSOP-14 (Exposed Pad)
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

RT7281□□
- Package Type
  SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

## Marking Information

RT7274GSP

RT7274
GSPYMDNN

RT7274GSP : Product Number
YMDNN : Date Code

RT7280GCP

RT7280
GCPYMDNN

RT7280GCP : Product Number
YMDNN : Date Code

RT7280GQW

2Y=YM
DNN

2Y= : Product Code
YMDNN : Date Code

RT7279GCP

RT7279
GCPYMDNN

RT7279GCP : Product Number
YMDNN : Date Code

RT7279GQW

2Z=YM
DNN

2Z= : Product Code
YMDNN : Date Code

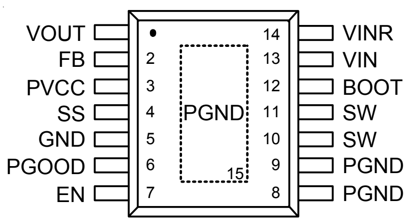
RT7281GSP

RT7281
GSPYMDNN

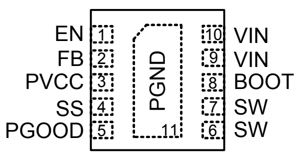
RT7281GSP : Product Number
YMDNN : Date Code

## Pin Configurations

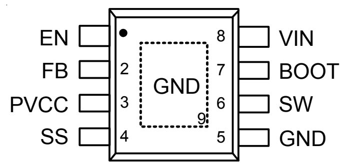
(TOP VIEW)




TSSOP-14 (Exposed Pad)




WDFN-10L 3x3



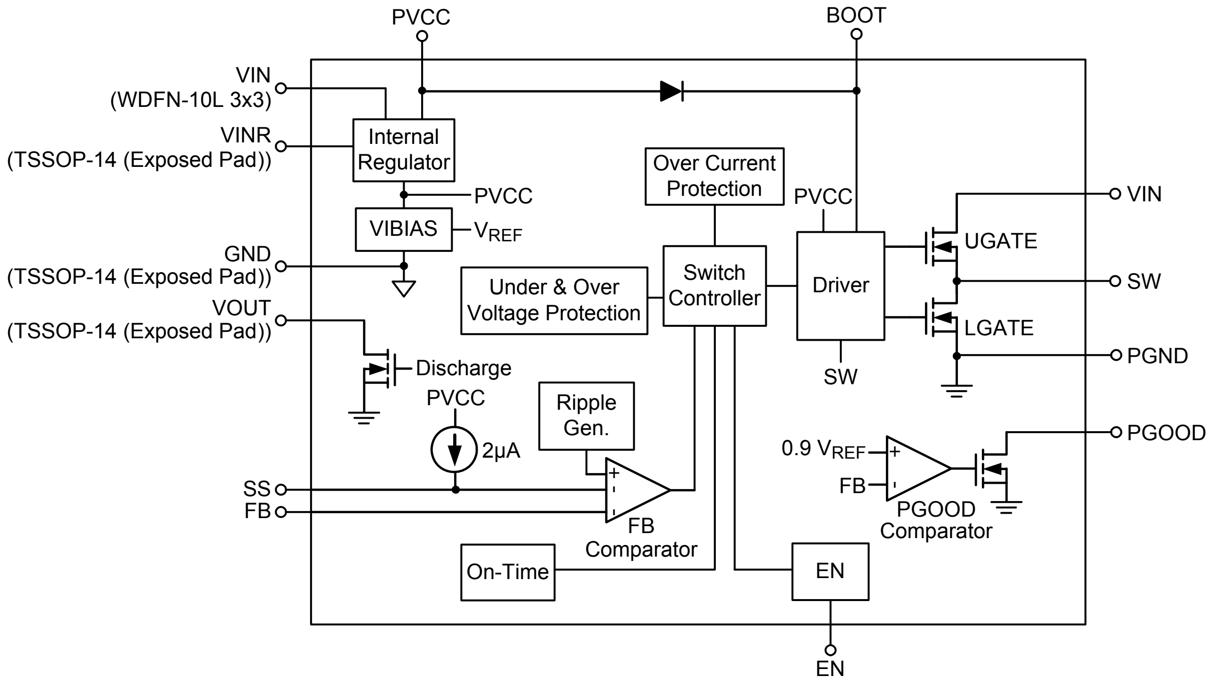

SOP-8 (Exposed Pad)

## Functional Pin Description

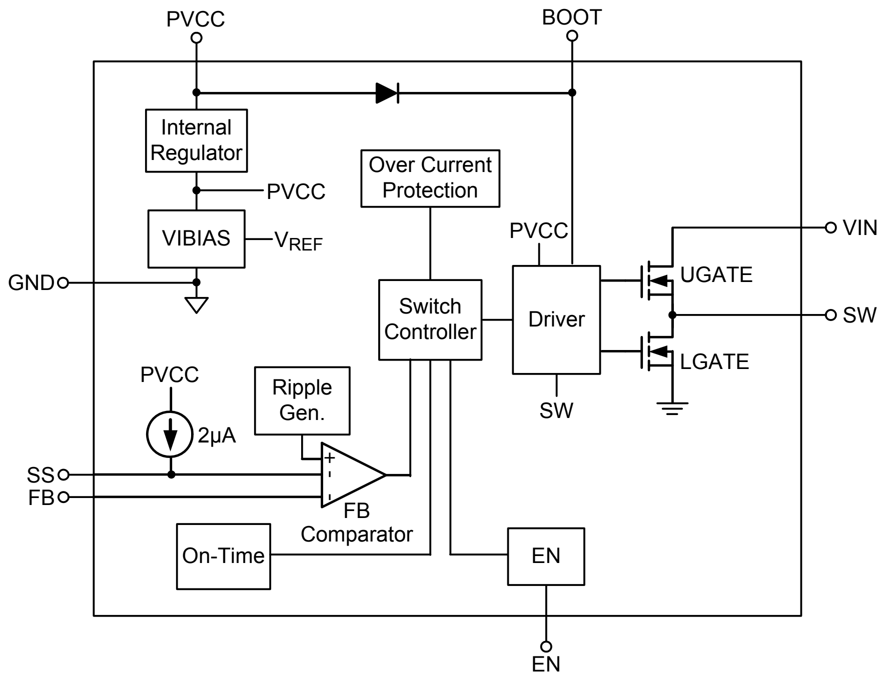
| Pin No. | | | Pin Name | Pin Function |
|---|---|---|---|---|
| TSSOP-14 (Exposed Pad) | WDFN-10L 3x3 | SOP-8 (Exposed Pad) | | |
| 1 | -- | -- | VOUT | Output Voltage Sense Input. This terminal is used for On-Time Adjustment. |
| 2 | 2 | 2 | FB | Feedback Input Voltage. Connect with feedback resistive divider to the output voltage. |
| 3 | 3 | 3 | PVCC | 5.1V Power Supply Output. PVCC is the output of the internal 5.1V linear regulator powered by VIN (WDFN-10L 3x3) or VINR (TSSOP-14L (Exposed Pad)). Connect a 1μF capacitor from this pin to GND. |
| 4 | 4 | 4 | SS | Soft-Start Control. Connect an external capacitor between this pin and GND to set the soft- start time. |
| 5 | -- | 5, 9 (Exposed Pad) | GND | Analog Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |
| 6 | 5 | -- | PGOOD | Open Drain Power Good Output. |
| 7 | 1 | 1 | EN | Enable Control Input. |
| 8, 9, 15 (Exposed Pad) | 11 (Exposed Pad) | -- | PGND | Power Ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation. |
| 10, 11 | 6, 7 | 6 | SW | Switch Node. |
| 12 | 8 | 7 | BOOT | Bootstrap Supply for High-Side Gate Driver. Connect a 0.1μF capacitor between the BOOT and SW pin. |
| 13 | 9, 10 | 8 | VIN | Power Input. It is connected to the drain of the internal high-side MOSFET. Connect VIN to the input capacitor. For the WDFN-10L 3x3 package, VIN also supplies power to the internal linear regulator. |
| 14 | -- | -- | VINR | Supply Input for Internal Linear Regulator to the Control Circuitry. |

## Function Block Diagram

### For TSSOP-14 (Exposed Pad) and WDFN-10L 3x3 Package




### For SOP-8 (Exposed Pad) Package



## Detailed Description

The RT7274/79/80/81 are high-performance 700kHz 2A step-down regulators with internal power switches and synchronous rectifiers. They feature an Advanced Constant On-Time (ACOT™) control architecture that provides stable operation with ceramic output capacitors without complicated external compensation, among other benefits. The input voltage range is from 4.5V to 18V and the output is adjustable from 0.765V to 8V.

The proprietary ACOT™ control scheme improves upon other constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. The RT7274/79/80/81 are optimized for ceramic output capacitors. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

### Constant On-Time (COT) Control

The heart of any COT architecture is the on-time one-shot. Each on-time is a pre-determined "fixed" period that is triggered by a feedback comparator. This robust arrangement has high noise immunity and is ideal for low duty cycle applications. After the on-time one-shot period, there is a minimum off-time period before any further regulation decisions can be considered. This arrangement avoids the need to make any decisions during the noisy time periods just after switching events, when the switching node (SW) rises or falls. Because there is no fixed clock, the high-side switch can turn on almost immediately after load transients and further switching pulses can ramp the inductor current higher to meet load requirements with minimal delays.

Traditional current mode or voltage mode control schemes typically must monitor the feedback voltage, current signals (also for current limit), and internal ramps and compensation signals, to determine when to turn off the high-side switch and turn on the synchronous rectifier. Weighing these small signals in a switching environment is difficult to do just after switching large currents, making those architectures problematic at low duty cycles and in less than ideal board layouts.

Because no switching decisions are made during noisy time periods, COT architectures are preferable in low duty cycle and noisy applications. However, traditional COT control schemes suffer from some disadvantages that preclude their use in many cases. Many applications require a known switching frequency range to avoid interference with other sensitive circuitry. True constant on-time control, where the on-time is actually fixed, exhibits variable switching frequency. In a step-down converter, the duty factor is proportional to the output voltage and inversely proportional to the input voltage. Therefore, if the on-time is fixed, the off-time (and therefore the frequency) must change in response to changes in input or output voltage.

Modern pseudo-fixed frequency COT architectures greatly improve COT by making the one-shot on-time proportional to $V_{OUT}$ and inversely proportional to $V_{IN}$. In this way, an on-time is chosen as approximately what it would be for an ideal fixed-frequency PWM in similar input/output voltage conditions. The result is a big improvement but the switching frequency still varies considerably over line and load due to losses in the switches and inductor and other parasitic effects.

Another problem with many COT architectures is their dependence on adequate ESR in the output capacitor, making it difficult to use highly-desirable, small, low-cost, but low-ESR ceramic capacitors. Most COT architectures use AC current information from the output capacitor, generated by the inductor current passing through the ESR, to function in a way like a current mode control system. With ceramic capacitors the inductor current information is too small to keep the control loop stable, like a current mode system with no current information.

### ACOT™ Control Architecture

Making the on-time proportional to $V_{OUT}$ and inversely proportional to $V_{IN}$ is not sufficient to achieve good constant-frequency behavior for several reasons. First, voltage drops across the MOSFET switches and inductor cause the effective input voltage to be less than the measured input voltage and the effective output voltage to be greater than the measured output voltage. As the load changes, the switch voltage drops change causing a switching frequency variation with load current. Also, at light loads if the inductor current goes negative, the switch dead-time between the synchronous rectifier turn-off and the high-side switch turn-on allows the switching node to rise to the input voltage. This increases the effective on-time and causes the switching frequency to drop noticeably.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. ACOT$^{TM}$ uses this method, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

To achieve good stability with low-ESR ceramic capacitors, ACOT$^{TM}$ uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

### ACOT$^{TM}$ One-shot Operation

The RT7274/79/80/81 control algorithm is simple to understand. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (230ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

### Discontinuous Operating Mode (RT7274/80 Only)

After soft start, the RT7279/81 operates in fixed frequency mode to minimize interference and noise problems. The RT7274/80 uses variable-frequency discontinuous switching at light loads to improve efficiency. During discontinuous switching, the on-time is immediately increased to add "hysteresis" to discourage the IC from switching back to continuous switching unless the load increases substantially.

The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for 700kHz switching and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

### Current Limit

The RT7274/79/80/81 current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between source and drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the upper current limit, the on-time one-shot is inhibited until the inductor current ramps down below the upper current limit plus a wide hysteresis band of about 1A and drops below the lower current limit level. Thus, only when the inductor current is well below the upper current limit is another on-time permitted. This arrangement prevents the average output current from greatly exceeding the guaranteed upper current limit value, as typically occurs with other valley-type current limits. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level (see next section) the IC will stop switching to avoid excessive heat.

The RT7279/81 also includes a negative current limit to protect the IC against sinking excessive current and possibly damaging the IC. If the voltage across the synchronous rectifier indicates the negative current is too high, the synchronous rectifier turns off until after the next high-side on-time. RT7274/80 does not sink current and therefore does not need a negative current limit.

#### Output Over-voltage Protection and Under-voltage Protection

The RT7279/80 include output over-voltage protection (OVP). If the output voltage rises above the regulation level, the high-side switch naturally remains off and the synchronous rectifier turns on. If the output voltage remains high the synchronous rectifier remains on until the inductor current reaches the negative current limit (RT7279) or until it reaches zero (RT7280). If the output voltage remains high, the IC's switches remain off. If the output voltage exceeds the OVP trip threshold for longer than 5μs (typical), the IC's OVP is triggered.

The RT7279/80 include output under-voltage protection (UVP). If the output voltage drops below the UVP trip threshold for longer than 250μs (typical) the IC's UVP is triggered.

There are two different behaviors for OVP and UVP events for the TSSOP-14 (Exposed Pad) packages.

- **Latch-Off Mode (TSSOP-14 (Exposed Pad) Only)**
- The RT7280GCP/RT7279GCP, use latch-off mode OVP and UVP. When the protection function is triggered the IC will shut down. The IC stops switching, leaving both switches open, and is latched off. To restart operation, toggle EN or power the IC off and then on again.
- **Hiccup Mode (WDFN-10L 3x3 Only)**
- The RT7279GQW/RT7280GQW, use hiccup mode OVP and UVP. When the protection function is triggered, the IC will shut down for a period of time and then attempt to recover automatically. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the overload or short circuit is removed.

#### Shut-down, Start-up and Enable (EN)

The enable input (EN) has a logic-low level of 0.4V. When $V_{EN}$ is below this level the IC enters shutdown mode and supply current drops to less than 10μA. When $V_{EN}$ exceeds its logic-high level of 1.6V the IC is fully operational. Between these 2 levels there are 2 thresholds (1.2V typical and 1.4V typical). When $V_{EN}$ exceeds the lower threshold the internal bias regulators begin to function and supply current increases above the shutdown current level. Switching operation begins when $V_{EN}$ exceeds the upper threshold. Unlike many competing devices, EN is a high voltage input that can be safely connected to VIN (up to 18V) for automatic start-up.

#### Input Under-voltage Lock-out

In addition to the enable function, the RT7274/79/80/81 feature an under-voltage lock-out (UVLO) function that monitors the internal linear regulator output (PVCC). To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when PVCC drops below the UVLO-falling threshold. The IC resumes switching when PVCC exceeds the UVLO-rising threshold.

#### Soft-Start (SS)

The RT7274/79/80/81 soft-start uses an external pin (SS) to clamp the output voltage and allow it to slowly rise. After $V_{EN}$ is high and PVCC exceeds its UVLO threshold, the IC begins to source 2μA from the SS pin. An external capacitor at SS is used to adjust the soft-start timing. The available capacitance range is from 2.7nF to 220nF. Do not leave SS unconnected.

During start-up, while the SS capacitor charges, the RT7274/79/80/81 operate in discontinuous switching mode with very small pulses. This prevents negative inductor currents and keeps the circuit from sinking current. Therefore, the output voltage may be pre-biased to some positive level before start-up. Once the $V_{SS}$ ramp charges enough to raise the internal reference above the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated level. After $V_{SS}$ rises above about 2.2V output over-and under-voltage protections are enabled and the RT7279/81 begins continuous-switching operation.

#### Internal Regulator (PVCC)

An internal linear regulator (PVCC) produces a 5.1V supply from VIN that powers the internal gate drivers, PWM logic, reference, analog circuitry, and other blocks. If VIN is 6V or greater, PVCC is guaranteed to provide significant power for external loads.

### PGOOD Comparator

PGOOD is an open drain output controlled by a comparator connected to the feedback signal. If FB exceeds 90% of the internal reference voltage, PGOOD will be high impedance. Otherwise, the PGOOD output is connected to PGND.

### External Bootstrap Capacitor (C6)

Connect a 0.1μF low ESR ceramic capacitor between BOOT and SW. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET switch.

### Over Temperature Protection

The RT7274/79/80/81 includes an Over Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 25°C the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN, VINR ---------- –0.3V to 21V
- Switch Node, SW ---------- –0.8V to ($V_{IN}$ + 0.3V)
- Switch Node, SW (<10ns) ---------- –5V to 25V
- BOOT to SW, PVCC ---------- –0.3V to 6V
- PVCC to VIN (WDFN-10L 3x3) or VINR (TSSOP-14 (Exposed Pad)) ---------- –18V to 0.3V
- Other Pins ---------- –0.3V to 21V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  TSSOP-14 (Exposed Pad) ---------- 2.50W
  WDFN-10L 3x3 ---------- 1.67W
  SOP-8 (Exposed Pad) ---------- 2.04W
- Package Thermal Resistance (Note 2)
  TSSOP-14 (Exposed Pad), $\theta_{JA}$ ---------- 40°C/W
  WDFN-10L 3x3, $\theta_{JA}$ ---------- 60°C/W
  WDFN-10L 3x3, $\theta_{JC}$ ---------- 7.5°C/W
  SOP-8 (Exposed Pad), $\theta_{JA}$ ---------- 49°C/W
  SOP-8 (Exposed Pad), $\theta_{JC}$ ---------- 15°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{IN}$ = 12V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | | |
| Supply Current (Shutdown) | | | $V_{EN}$ = 0V | -- | 1 | 10 | μA |
| Supply Current (Quiescent) | | | $V_{EN}$ = 3V, $V_{FB}$ = 1V | -- | 0.7 | -- | mA |
| **Logic Threshold** | | | | | | | |
| EN Voltage | Logic-High | $V_{IH}$ | | 1.6 | -- | 18 | V |
| | Logic-Low | $V_{IL}$ | | -- | -- | 0.4 | |
| EN Pin Resistance to GND (RT7274/81) | | | $V_{EN}$ = 12V | 220 | 440 | 880 | kΩ |
| **$V_{FB}$ Voltage and Discharge Resistance** | | | | | | | |
| Feedback Threshold Voltage | | $V_{FB\_TH}$ | 4.5V ≤ $V_{IN}$ ≤ 18V | 0.757 | 0.765 | 0.773 | V |
| Feedback Input Current | | $I_{FB}$ | $V_{FB}$ = 0.8V | –0.1 | 0 | 0.1 | μA |
| VOUT Discharge Resistance | | $R_{DIS}$ | EN = 0V, $V_{VOUT}$ = 0.5V | -- | 50 | 100 | Ω |

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **$V_{PVCC}$ Output** | | | | | | | |
| $V_{PVCC}$ Output Voltage | | $V_{PVCC}$ | $6V \le V_{IN} \le 18V$, $0 < I_{PVCC} < 5mA$ | 4.7 | 5.1 | 5.5 | V |
| Line Regulation | | | $6V \le V_{IN} \le 18V$, $I_{PVCC} = 5mA$ | -- | -- | 20 | mV |
| Load Regulation | | | $0 < I_{PVCC} < 5mA$ | -- | -- | 100 | mV |
| Output Current | | $I_{PVCC}$ | $V_{IN} = 6V$, $V_{PVCC} = 4V$ | -- | 110 | -- | mA |
| **$R_{DS(ON)}$** | | | | | | | |
| Switch On-Resistance | High-Side | $R_{DS(ON)\_H}$ | | -- | 150 | -- | mΩ |
| | Low-Side | $R_{DS(ON)\_L}$ | | -- | 105 | -- | |
| **Current Limit** | | | | | | | |
| Current Limit | | $I_{LIM}$ | $L_{SW} = 2\mu H$ | 2.5 | 3.5 | 4.7 | A |
| **Thermal Shutdown** | | | | | | | |
| Thermal Shutdown Threshold | | $T_{SD}$ | | -- | 150 | -- | °C |
| Thermal Shutdown Hysteresis | | $\Delta T_{SD}$ | | -- | 25 | -- | °C |
| **On-Time Timer Control** | | | | | | | |
| On-Time | | $t_{ON}$ | $V_{IN} = 12V$, $V_{OUT} = 1.05V$ | -- | 145 | -- | ns |
| Minimum Off-Time | | $t_{OFF(MIN)}$ | | -- | 230 | -- | ns |
| **Soft-Start** | | | | | | | |
| SS Charge Current | | | $V_{SS} = 0V$ | 1.4 | 2 | 2.6 | μA |
| SS Discharge Current | | | $V_{SS} = 0.5V$ | 0.05 | 0.1 | -- | mA |
| **UVLO** | | | | | | | |
| UVLO Threshold | | | Wake up $V_{PVCC}$ | 3.55 | 3.85 | 4.15 | V |
| | | | Hysteresis | -- | 0.3 | -- | |
| **Power Good (RT7279/80)** | | | | | | | |
| PGOOD Threshold | | | FB Rising | 85 | 90 | 95 | % |
| | | | FB Falling | -- | 85 | -- | |
| PGOOD Sink Current | | | PGOOD = 0.5V | -- | 5 | -- | mA |
| **Output Under Voltage and Over Voltage Protection (RT7279/80)** | | | | | | | |
| OVP Trip Threshold | | | OVP Detect | 115 | 120 | 125 | % |
| OVP Delay Time | | | | -- | 5 | -- | μs |
| UVP Trip Threshold | | | UVP Detect | 65 | 70 | 75 | % |
| | | | Hysteresis | -- | 10 | -- | |
| UVP Delay Time | | | | -- | 250 | -- | μs |

**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

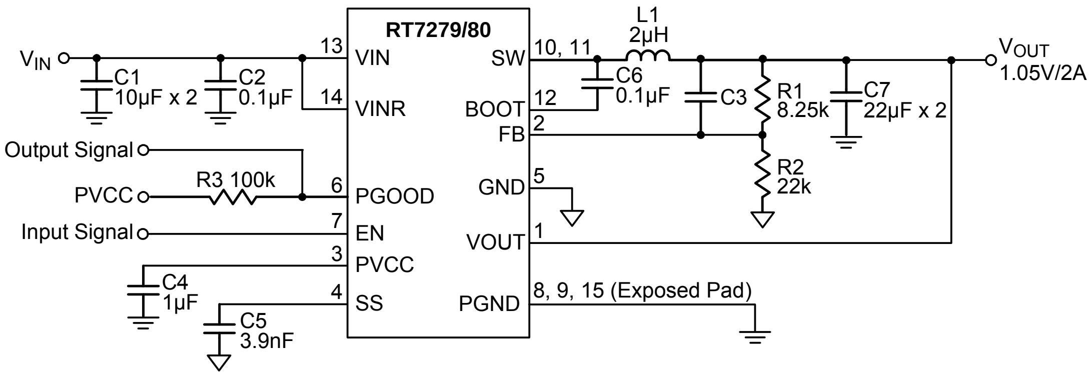
**Note 2.** $\theta_{JA}$ is measured at $T_A = 25°C$ on a high effective thermal conductivity four-layer test board per JEDEC 51-7. $\theta_{JC}$ is measured at the exposed pad of the package. The PCB copper area of exposed pad is $70mm^2$.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

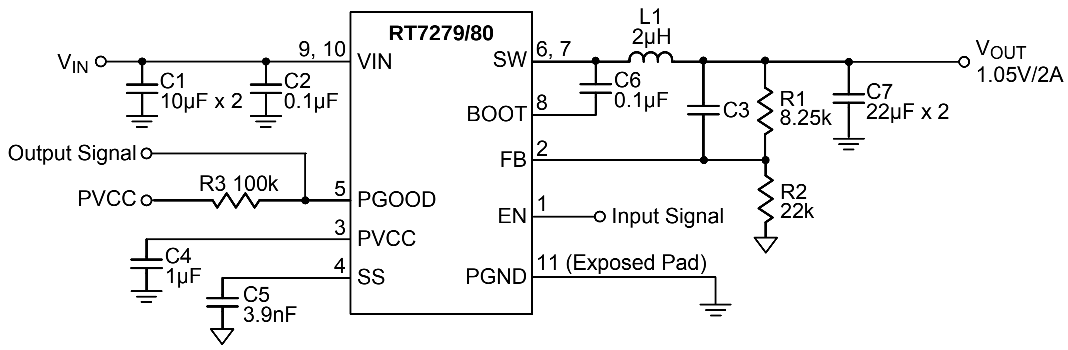
**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Application Circuit

### For TSSOP-14 (Exposed Pad) Package




### For WDFN-10L 3x3 Package




### For SOP-8 (Exposed Pad) Package

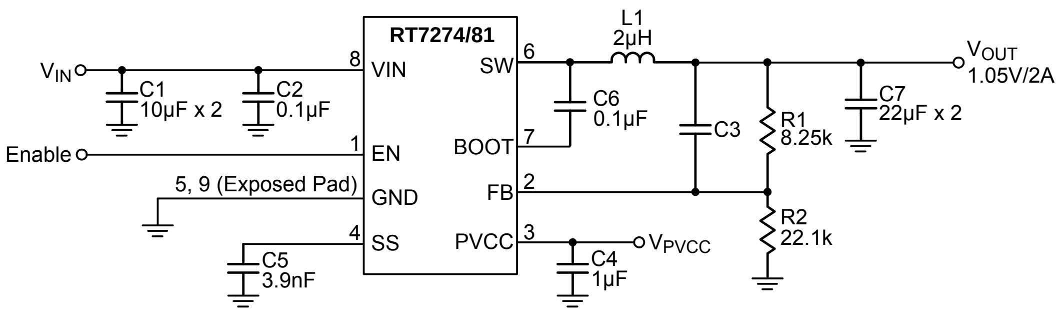
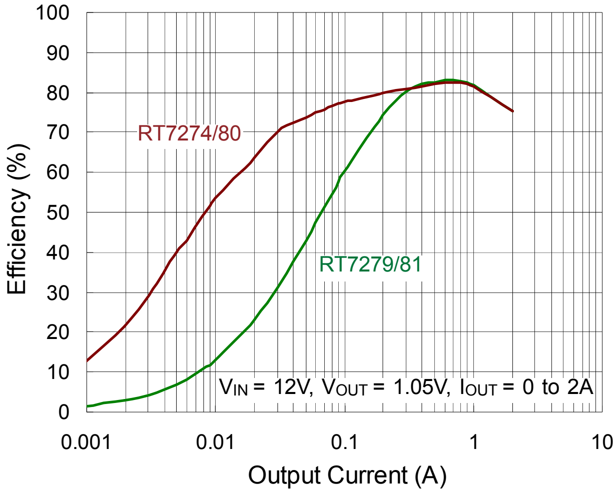



**Table 1. Suggested Component Values**

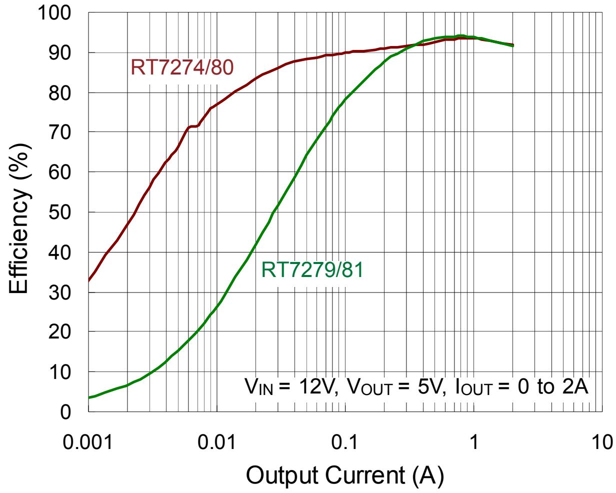
| $V_{OUT}$ (V) | R1 ([redacted] | R2 ([redacted] | C3 (pF) | L1 ([redacted]H) | C7 ([redacted]F) |
|---|---|---|---|---|---|
| 1 | 6.81 | 22.1 | -- | 2 | 22 to 68 |
| 1.05 | 8.25 | 22.1 | -- | 2 | 22 to 68 |
| 1.2 | 12.7 | 22.1 | -- | 2 | 22 to 68 |
| 1.8 | 30.1 | 22.1 | 5 to 22 | 3.3 | 22 to 68 |
| 2.5 | 49.9 | 22.1 | 5 to 22 | 3.3 | 22 to 68 |
| 3.3 | 73.2 | 22.1 | 5 to 22 | 3.3 | 22 to 68 |
| 5 | 124 | 22.1 | 5 to 22 | 4.7 | 22 to 68 |
| 7 | 180 | 22.1 | 5 to 22 | 4.7 | 22 to 68 |

## Typical Operating Characteristics

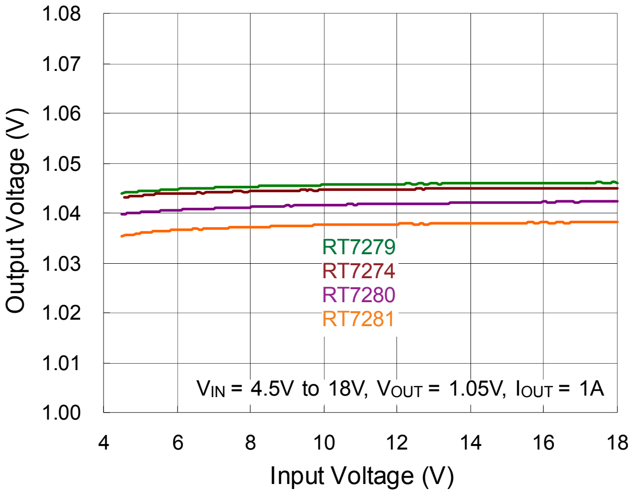
### Efficiency vs. Output Current



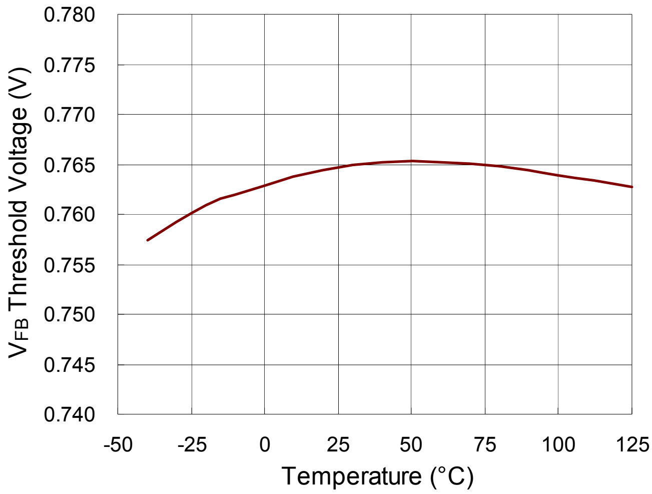

### Efficiency vs. Output Current



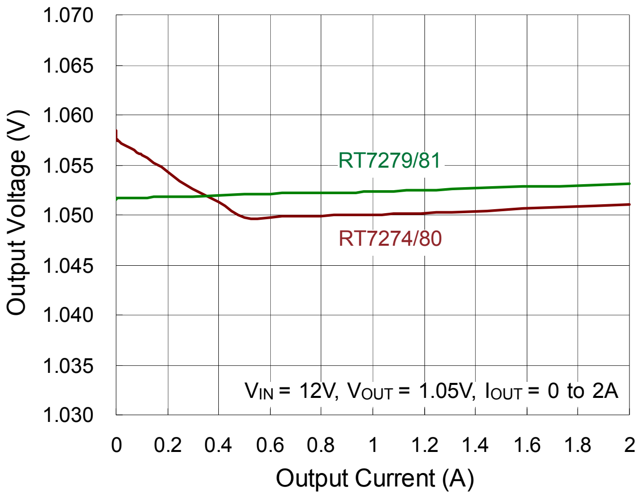

### Output Voltage vs. Input Voltage



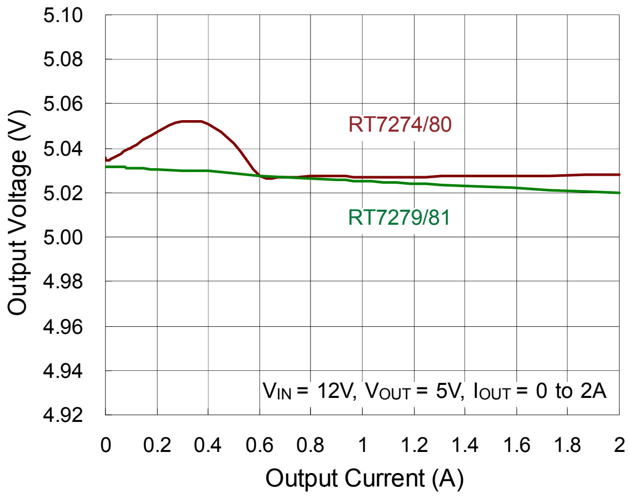

### $V_{FB}$ Threshold Voltage vs. Temperature

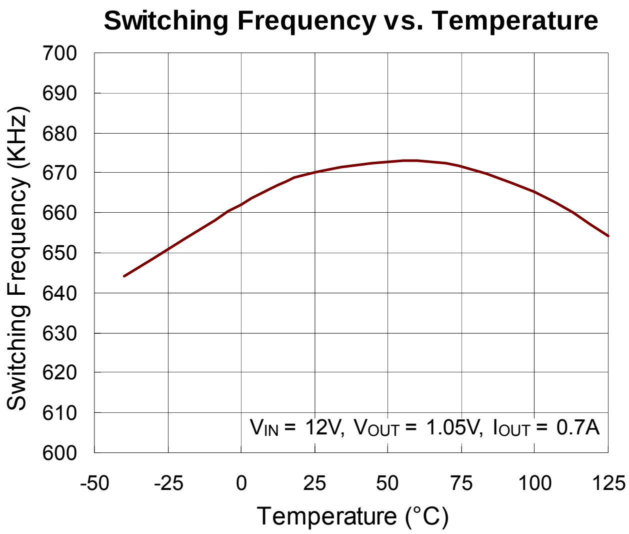


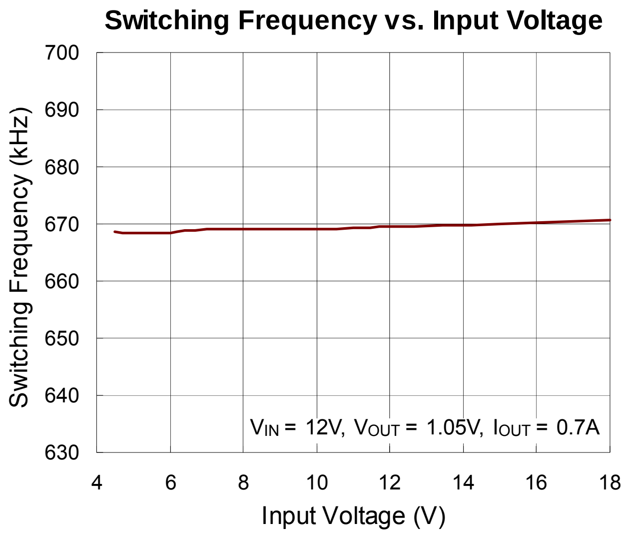

### Output Voltage vs. Output Current

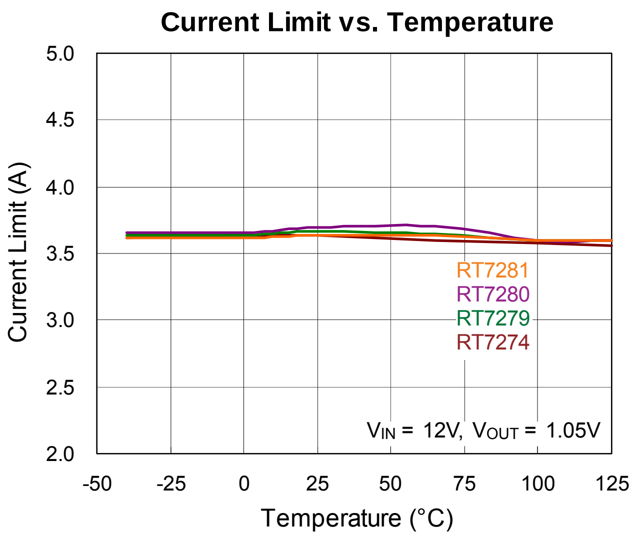


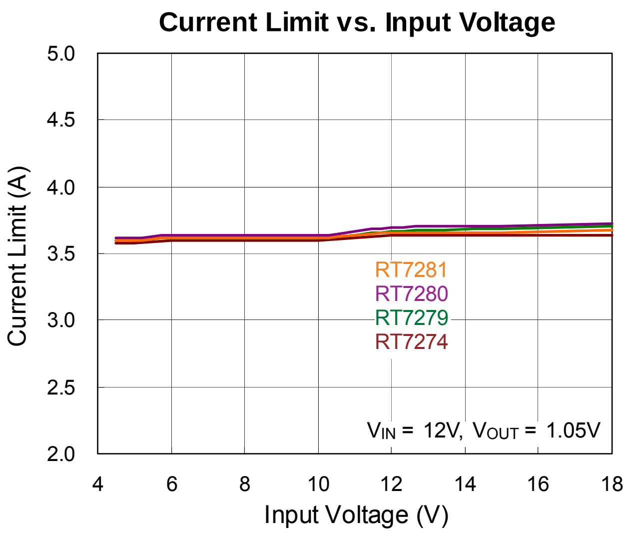

### Output Voltage vs. Output Current

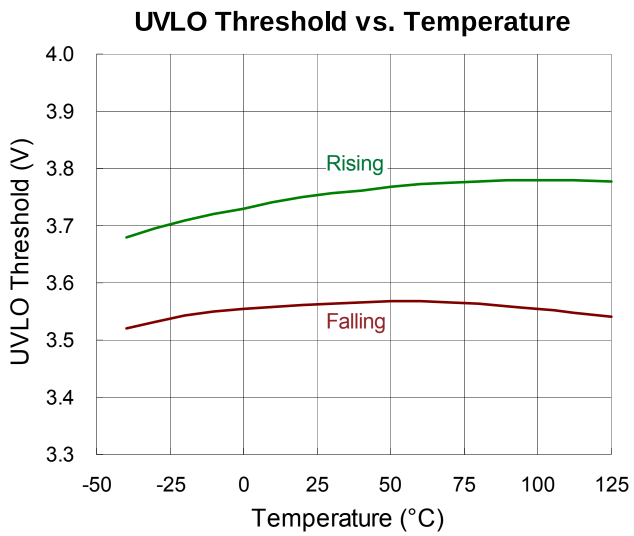


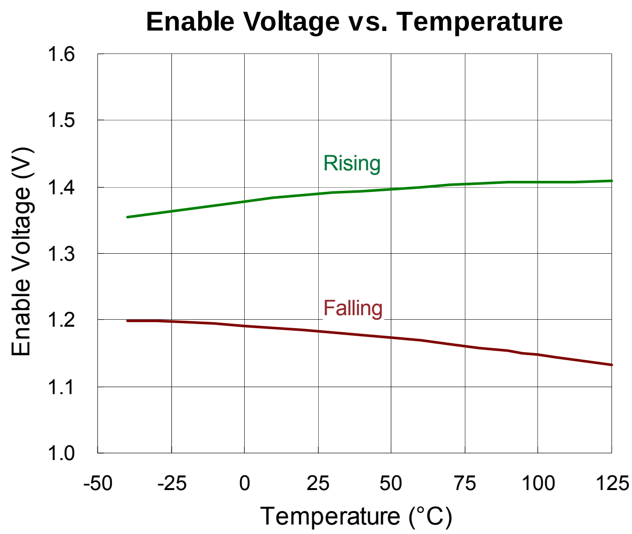

Switching Frequency vs. Temperature
Switching Frequency (KHz)
700
690
680
670
660
650
640
630
620
610
600
-50
-25
0
25
50
75
100
125
Temperature (°C)
VIN = 12V, VOUT = 1.05V, IOUT = 0.7A

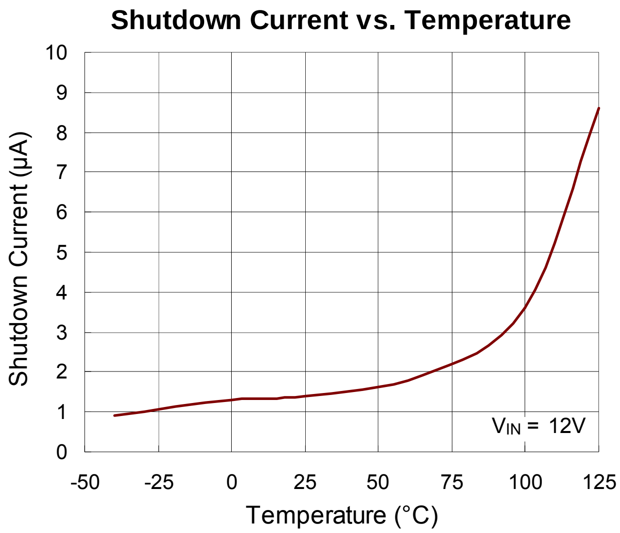

Switching Frequency vs. Input Voltage
Switching Frequency (kHz)
700
690
680
670
660
650
640
630
4
6
8
10
12
14
16
18
Input Voltage (V)
VIN = 12V, VOUT = 1.05V, IOUT = 0.7A

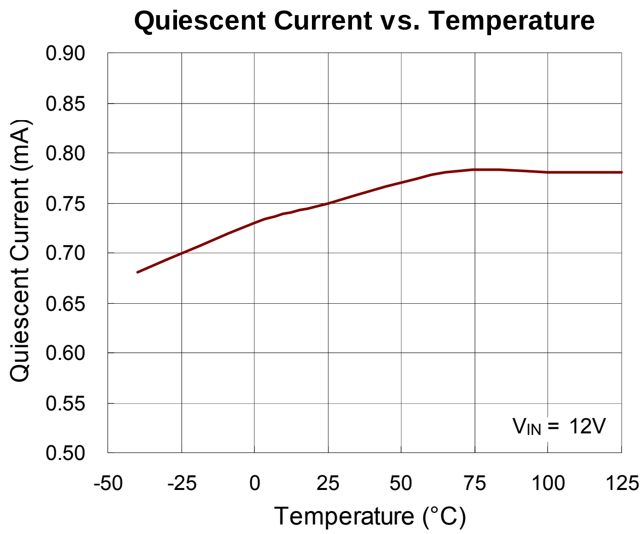

Current Limit vs. Temperature
Current Limit (A)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
-50
-25
0
25
50
75
100
125
Temperature (°C)
RT7281
RT7280
RT7279
RT7274
VIN = 12V, VOUT = 1.05V

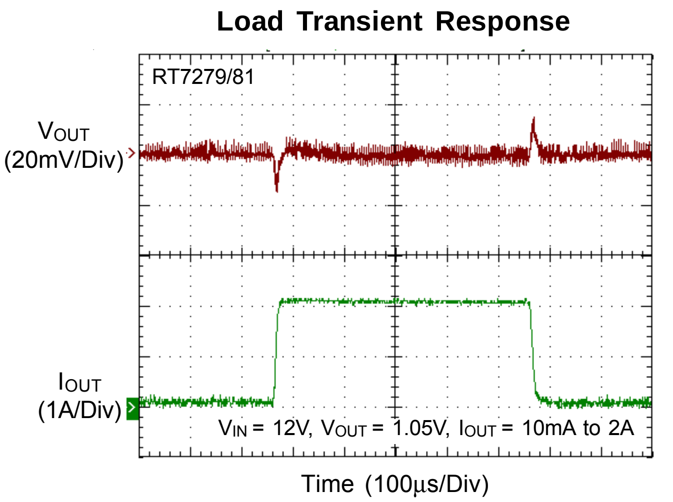

Current Limit vs. Input Voltage
Current Limit (A)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
4
6
8
10
12
14
16
18
Input Voltage (V)
RT7281
RT7280
RT7279
RT7274
VIN = 12V, VOUT = 1.05V

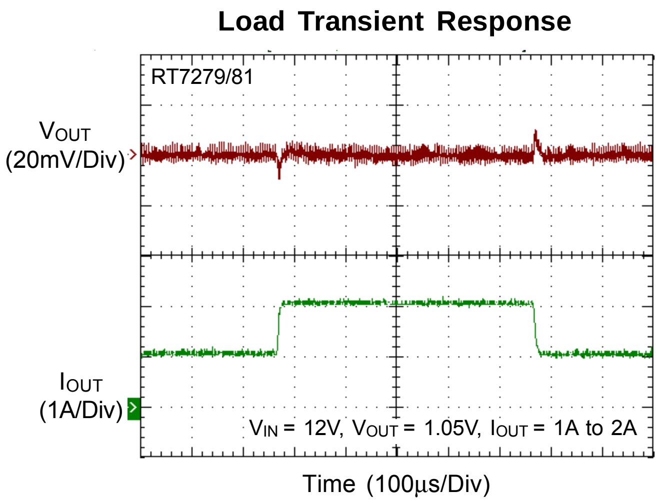

UVLO Threshold vs. Temperature
UVLO Threshold (V)
4.0
3.9
3.8
3.7
3.6
3.5
3.4
3.3
-50
-25
0
25
50
75
100
125
Temperature (°C)
Rising
Falling

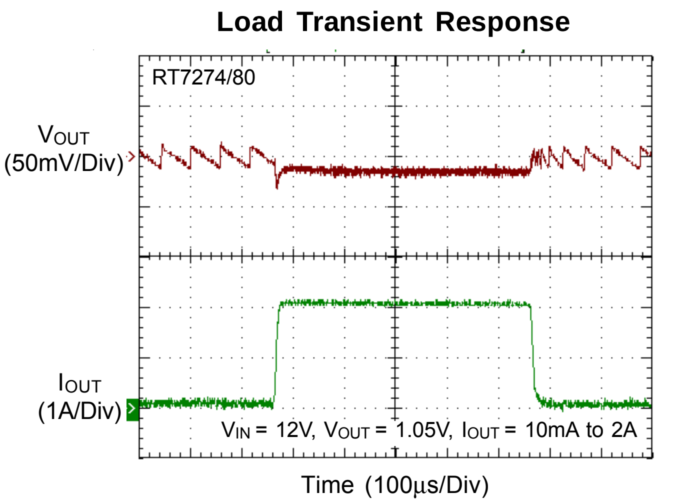

Enable Voltage vs. Temperature
Enable Voltage (V)
1.6
1.5
1.4
1.3
1.2
1.1
1.0
-50
-25
0
25
50
75
100
125
Temperature (°C)
Rising
Falling

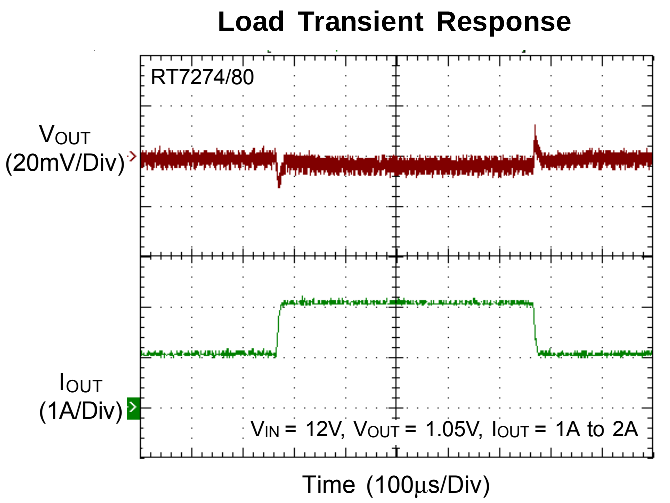

Shutdown Current vs. Temperature
Shutdown Current (µA)
Temperature (°C)
VIN = 12V


Quiescent Current vs. Temperature
Quiescent Current (mA)
Temperature (°C)
VIN = 12V

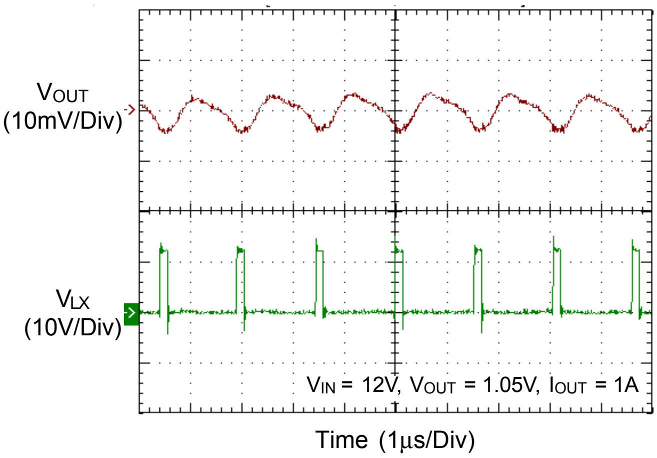

Load Transient Response
RT7279/81
VOUT (20mV/Div)
IOUT (1A/Div)
VIN = 12V, VOUT = 1.05V, IOUT = 10mA to 2A
Time (100µs/Div)


Load Transient Response
RT7279/81
VOUT (20mV/Div)
IOUT (1A/Div)
VIN = 12V, VOUT = 1.05V, IOUT = 1A to 2A
Time (100µs/Div)

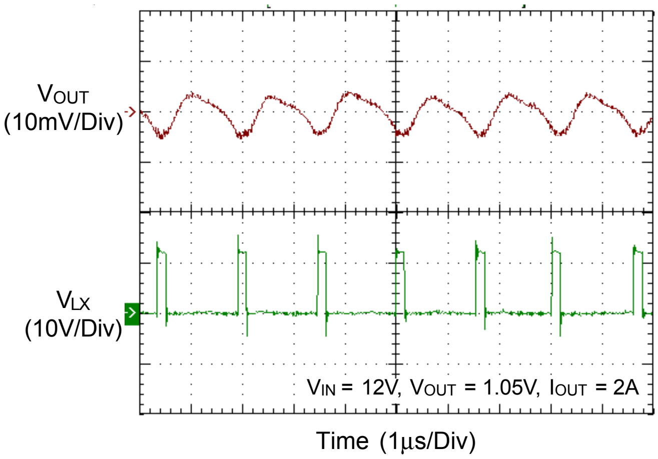

Load Transient Response
RT7274/80
VOUT (50mV/Div)
IOUT (1A/Div)
VIN = 12V, VOUT = 1.05V, IOUT = 10mA to 2A
Time (100µs/Div)


Load Transient Response
RT7274/80
VOUT (20mV/Div)
IOUT (1A/Div)
VIN = 12V, VOUT = 1.05V, IOUT = 1A to 2A
Time (100µs/Div)

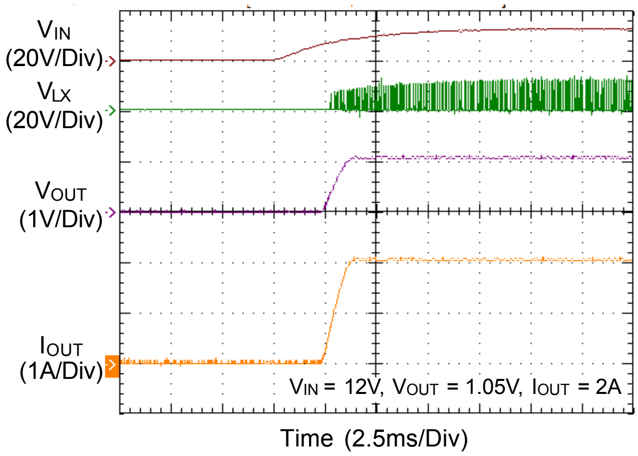
Output Ripple Voltage



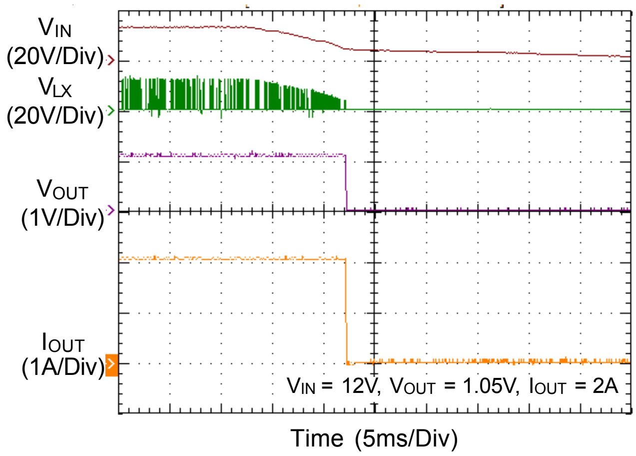

Output Ripple Voltage



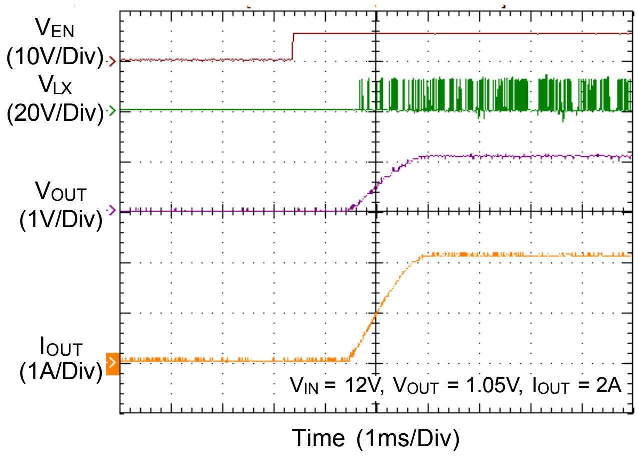

Power On from VIN



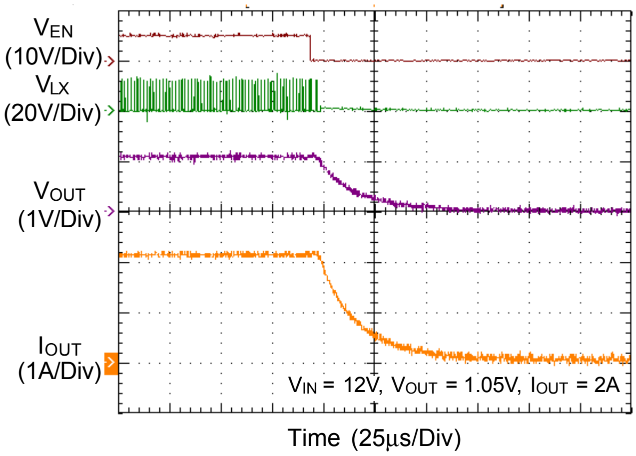

Power Off from VIN



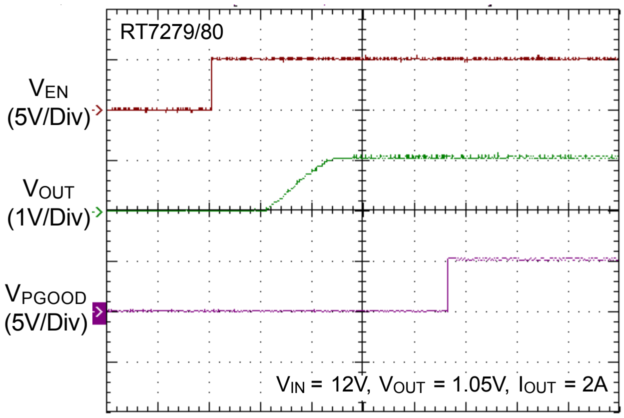

Power On from EN




Power Off from EN

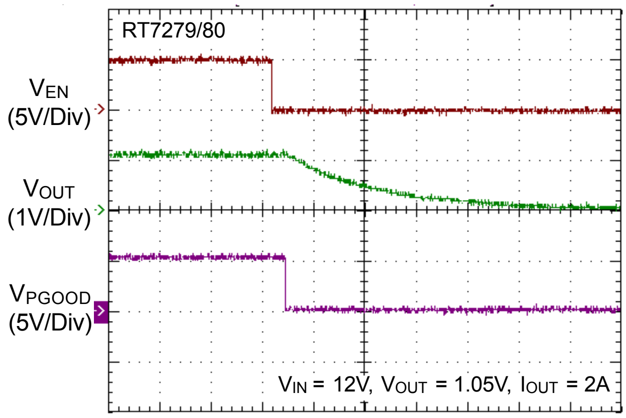


**Power Good from EN On**




Time (1ms/Div)

**Power Good from EN Off**




Time (10μs/Div)

## Application Information

The RT7274/79/80/81 is a synchronous high voltage Buck converter that can support the input voltage range from 4.5V to 18V and the output current up to 2A. It adopts ACOT[TM] mode control to provide a very fast transient response with few external compensation components.

### PWM Operation

It is suitable for low external component count configuration with appropriate amount of Equivalent Series Resistance (ESR) capacitors at the output. The output ripple valley voltage is monitored at a feedback point voltage. The synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal on-time expires, the MOSFET is turned off. The pulse width of this on-time is determined by the converter's input and output voltages to keep the frequency fairly constant over the entire input voltage range.

### Advanced Constant On-Time Control

The RT7274/79/80/81 has a unique circuit which sets the on-time by monitoring the input voltage and SW signal. The circuit ensures the switching frequency operating at 700kHz over input voltage range and loading range.

### Soft-Start

The RT7274/79/80/81 contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing can be programmed by the external capacitor between the SS and GND pins. The chip provides a 2μA charge current for the external capacitor. If a 3.9nF capacitor is used, the soft-start will be 2.6ms (typ.). The available capacitance range is from 2.7nF to 220nF.

$$t_{SS}\ (\text{ms}) = \frac{C5\ (\text{nF}) \times 1.365}{I_{SS}\ (\mu A)}$$

### Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the RT7274/79/80/81 quiescent current drops to lower than 10μA. Driving the EN pin high (>1.6V, <18V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a $R_{EN}$ resistor and $C_{EN}$ capacitor from the VIN pin (see Figure 1).

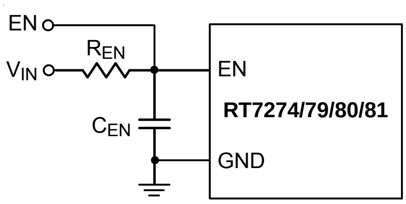



Figure 1. External Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2V is available, as shown in Figure 2. In this case, a 100kΩ pull-up resistor, $R_{EN}$, is connected between the $V_{IN}$ and the EN pins. MOSFET Q1 will be under logic control to pull down the EN pin.

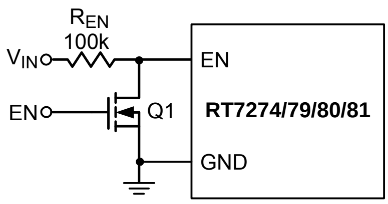



Figure 2. Digital Enable Control Circuit

To prevent enabling circuit when $V_{IN}$ is smaller than the $V_{OUT}$ target value, a resistive voltage divider can be placed between the input voltage and ground and connected to the EN pin to adjust IC lockout threshold, as shown in Figure 3. For example, if an 8V output voltage is regulated from a 12V input voltage, the resistor $R_{EN2}$ can be selected to set input lockout threshold larger than 8V.

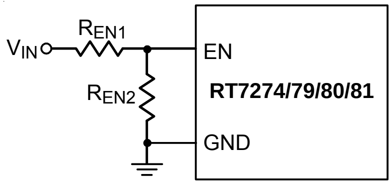



Figure 3. Resistor Divider for Lockout Threshold Setting

### Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 4.

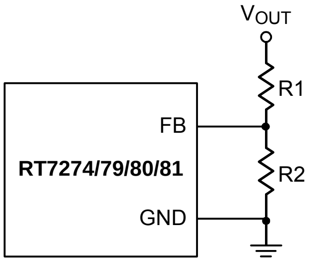



Figure 4. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation. It is recommended to use 1% tolerance or better divider resistors.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right)$$

### Under Voltage Lockout Protection

The RT7274/79/80/81 has Under Voltage Lockout Protection (UVLO) that monitors the voltage of PVCC pin. When the $V_{PVCC}$ voltage is lower than UVLO threshold voltage, the RT7274/79/80/81 will be turned off in this state. This is non-latch protection.

### Over Temperature Protection

The RT7274/79/80/81 equips an Over Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 25°C the main converter will resume operation. To keep operating at maximum, the junction temperature should be prevented from rising above 150°C.

### Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and an output voltage. The ripple current $\Delta I_L$ increases with higher $V_{IN}$ and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal. For the ripple current selection, the value of $\Delta I_L = 0.2(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest $V_{IN}$. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

### Input and Output Capacitors Selection

The input capacitance, $C_{IN}$, is needed to filter the trapezoidal current at the source of the high-side MOSFET. A low ESR input capacitor with larger ripple current rating should be used for the maximum RMS current. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, two 10µF and 0.1µF low ESR ceramic capacitors are recommended.

The selection of $C_{OUT}$ is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for $C_{OUT}$ selection to ensure that the control loop is stable. The output ripple, $\Delta V_{OUT}$ , is determined by :

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple will be highest at the maximum input voltage since $\Delta I_L$ increases with input voltage. Multiple capacitors placed in parallel may need to meet the ESR and RMS current handling requirements.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, $V_{IN}$. A sudden inrush of current through the long wires can potentially cause a voltage spike at $V_{IN}$ large enough to damage the part.

### External Bootstrap Diode

Connect a 0.1μF low ESR ceramic capacitor between the BOOT and SW pins. This capacitor provides the gate driver voltage for the high-side MOSFET. It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65%. The bootstrap diode can be a low cost one such as 1N4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT7274/79/80/81. Note that the external boot voltage must be lower than 5.5V

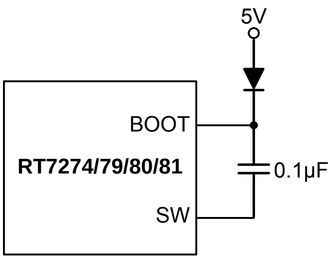



Figure 5. External Bootstrap Diode

### PVCC Capacitor Selection

Decouple with a 1μF ceramic capacitor. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.

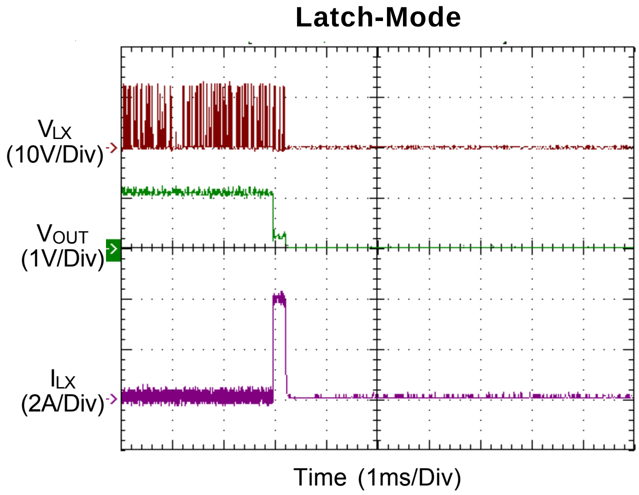
### Over Current Protection

When the output shorts to ground, the inductor current decays very slowly during a single switching cycle. An over current detector is used to monitor inductor current to prevent current runaway. The over current detector monitors the voltage between SW and GND during the low-side MOS turn-on state. This is cycle-by-cycle protection.

### Under Voltage Protection

#### Latch-Off Mode (RT7279/80, TSSOP-14 Only)

For the RT7279GCP/RT7280GCP, it provides Latch-Off Mode Under Voltage Protection (UVP). When the FB pin voltage drops below 70% of the feedback threshold voltage, UVP will be triggered and the RT7279GCP/RT7280GCP will shutdown in Latch-Off Mode. In shutdown condition, the RT7279GCP/RT7280GCP can be reset by the EN pin or power input, VIN.




#### Hiccup Mode (RT7279/80, WDFN-10L 3x3 Only)

For the RT7279GQW/RT7280GQW, it provides Hiccup Mode Under Voltage Protection (UVP). When the FB pin voltage drops below 70% of the feedback threshold voltage, UVP will be triggered and the RT7279GQW/RT7280GQW will shutdown in Hiccup Mode.

Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as overload or short circuit is removed.

## Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For TSSOP-14 (Exposed Pad) package, the thermal resistance, $\theta_{JA}$, is 40°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-10L 3x3 package, the thermal resistance, $\theta_{JA}$, is 60°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOP-8 (Exposed Pad) package, the thermal resistance, $\theta_{JA}$, is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C − 25°C) / (40°C/W) = 2.50W for TSSOP-14 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C − 25°C) / (60°C/W) = 1.67W for WDFN-10L 3x3 package

$P_{D(MAX)}$ = (125°C − 25°C) / (49°C/W) = 2.04W for SOP-8 (Exposed Pad) package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curves in Figure 6 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

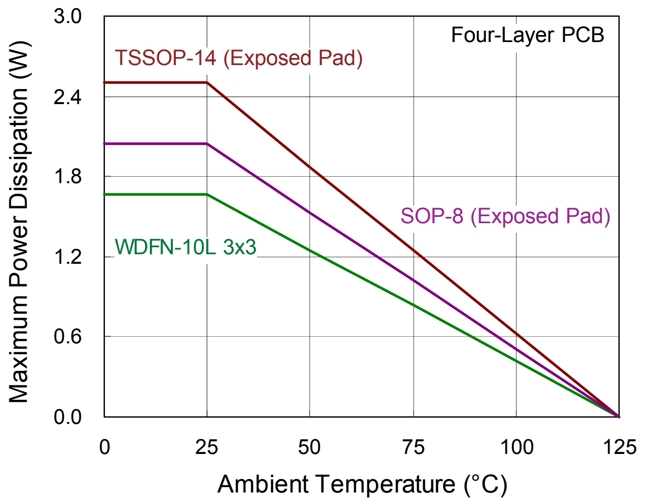
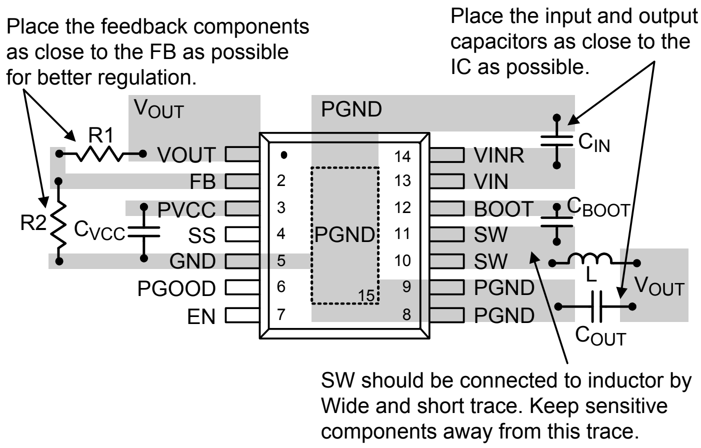



Figure 6. Derating Curve of Maximum Power Dissipation

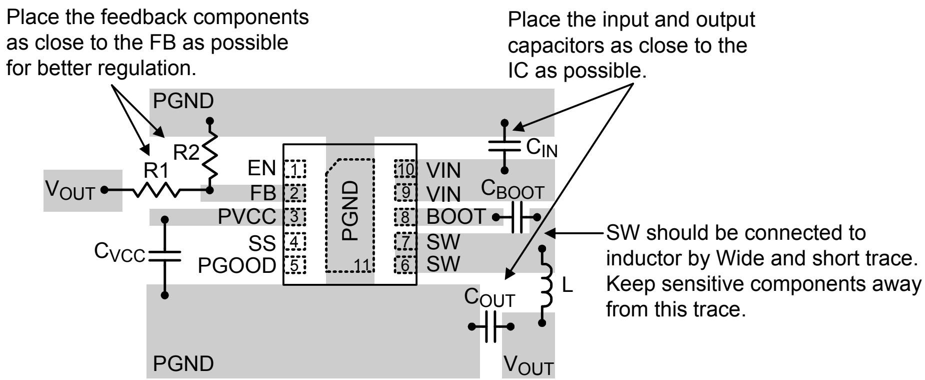
## Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT7274/79/80/81

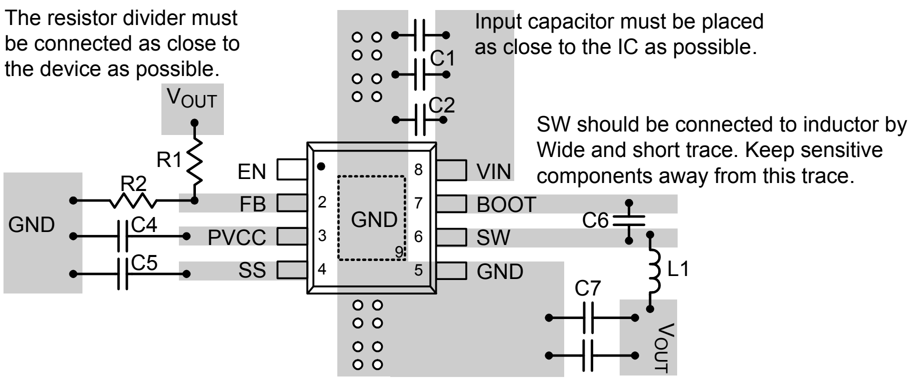
- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT7274/79/80/81 FB pin.
- The GND and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.




(a). For TSSOP-14 (Exposed Pad) Package



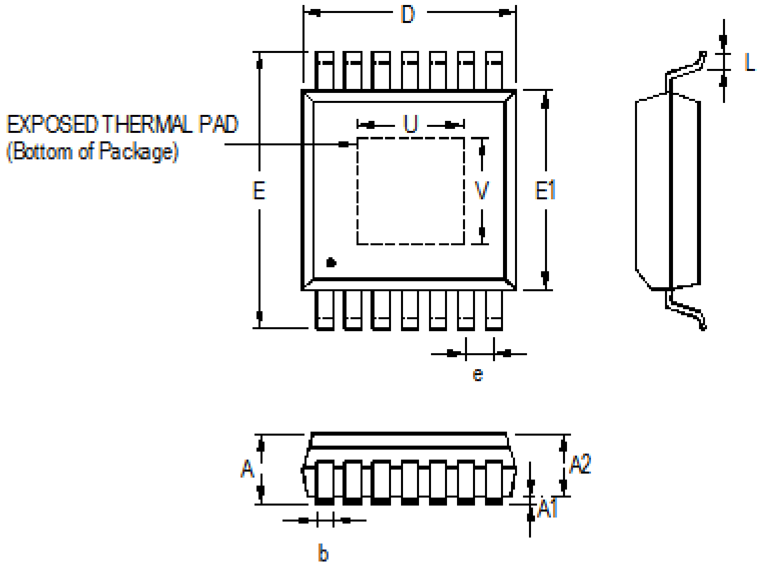

(b). For WDFN-10L 3x3 Package




(c). For SOP-8 (Exposed) Package

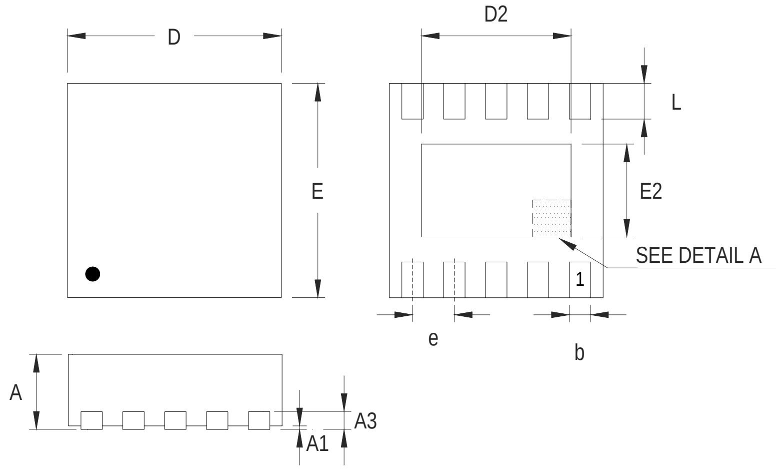
Figure 7. PCB Layout Guide

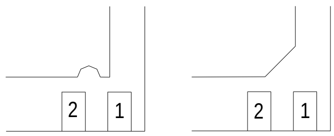
## Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.000 | 1.200 | 0.039 | 0.047 |
| A1 | 0.000 | 0.150 | 0.000 | 0.006 |
| A2 | 0.800 | 1.050 | 0.031 | 0.041 |
| b | 0.190 | 0.300 | 0.007 | 0.012 |
| D | 4.900 | 5.100 | 0.193 | 0.201 |
| e | 0.650 | | 0.026 | |
| E | 6.300 | 6.500 | 0.248 | 0.256 |
| E1 | 4.300 | 4.500 | 0.169 | 0.177 |
| L | 0.450 | 0.750 | 0.018 | 0.030 |
| U | 1.900 | 2.900 | 0.075 | 0.114 |
| V | 1.600 | 2.600 | 0.063 | 0.102 |

**14-Lead TSSOP (Exposed Pad) Plastic Package**



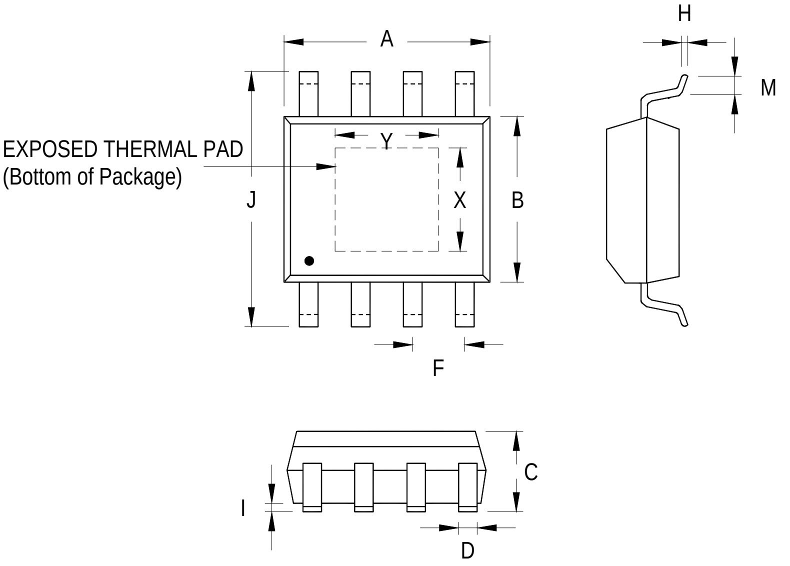

**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| D | 2.950 | 3.050 | 0.116 | 0.120 |
| D2 | 2.300 | 2.650 | 0.091 | 0.104 |
| E | 2.950 | 3.050 | 0.116 | 0.120 |
| E2 | 1.500 | 1.750 | 0.059 | 0.069 |
| e | 0.500 | | 0.020 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

**W-Type 10L DFN 3x3 Package**




| Symbol | | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|---|
| | | Min | Max | Min | Max |
| A | | 4.801 | 5.004 | 0.189 | 0.197 |
| B | | 3.810 | 4.000 | 0.150 | 0.157 |
| C | | 1.346 | 1.753 | 0.053 | 0.069 |
| D | | 0.330 | 0.510 | 0.013 | 0.020 |
| F | | 1.194 | 1.346 | 0.047 | 0.053 |
| H | | 0.170 | 0.254 | 0.007 | 0.010 |
| I | | 0.000 | 0.152 | 0.000 | 0.006 |
| J | | 5.791 | 6.200 | 0.228 | 0.244 |
| M | | 0.406 | 1.270 | 0.016 | 0.050 |
| Option 1 | X | 2.000 | 2.300 | 0.079 | 0.091 |
| | Y | 2.000 | 2.300 | 0.079 | 0.091 |
| Option 2 | X | 2.100 | 2.500 | 0.083 | 0.098 |
| | Y | 3.000 | 3.500 | 0.118 | 0.138 |

**8-Lead SOP (Exposed Pad) Plastic Package**

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