Single Phase PWM Controller with 1-bit VID

General Description

RT8121 is a single phase PWM buck controller with one integrated MOSFET driver for advanced microprocessor application as VR12 VCCIO power. This controller maintains the same features as the multi-phase product family, but reduces the output to one phase for lower current systems. Features of this controller include adjustable operation frequency, power good indication, external error-amp compensation, over voltage protection, over current protection, externally adjustable offset voltage, load transient enhancement (quick response), and enable/ shutdown control to achieve optimal power management solution for various applications. The RT8121 comes in the WQFN-20L 3x3 package.

Ordering Information

RT8121 □ □

Package Type
QW : WQFN-20L 3x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)
Z : ECO (Ecological Element with Halogen Free and Pb free)

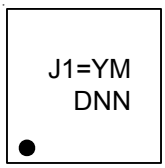
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

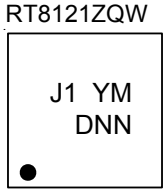
Marking Information

RT8121GQW



J1= : Product Code
YMDNN : Date Code

RT8121ZQW



J1 : Product Code
YMDNN : Date Code

Features

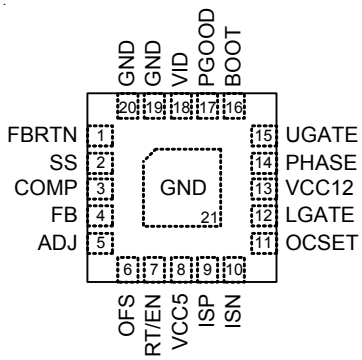
- **Single Phase Power Conversion**
- **One Embedded MOSFET Driver with Internal Bootstrap Diode**
- **1-bit VID Table for VR12 VCCIO**
- **Continuous Differential Inductor DCR Current Sense**
- **Adjustable Soft-Start**
- **Adjustable Frequency Typically at 200kHz**
- **Power Good Indication**
- **Adjustable Over Current Protection**
- **Over Voltage Protection**
- **Over Temperature Protection**
- **Small 20-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- VR12 VCCIO Voltage Regulator
- Low Voltage, High Current DC/DC Converter

Pin Configurations

(TOP VIEW)



WQFN-20L 3x3

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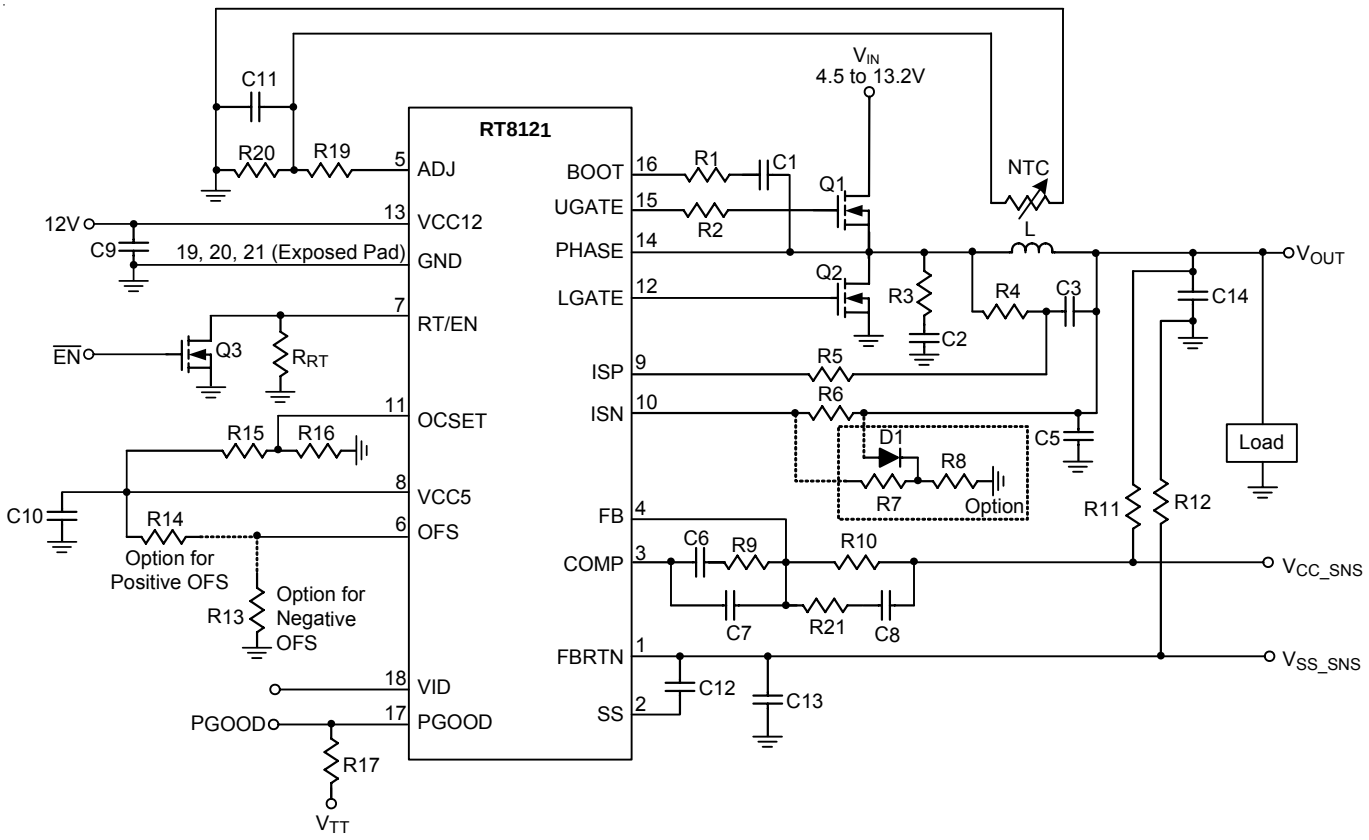
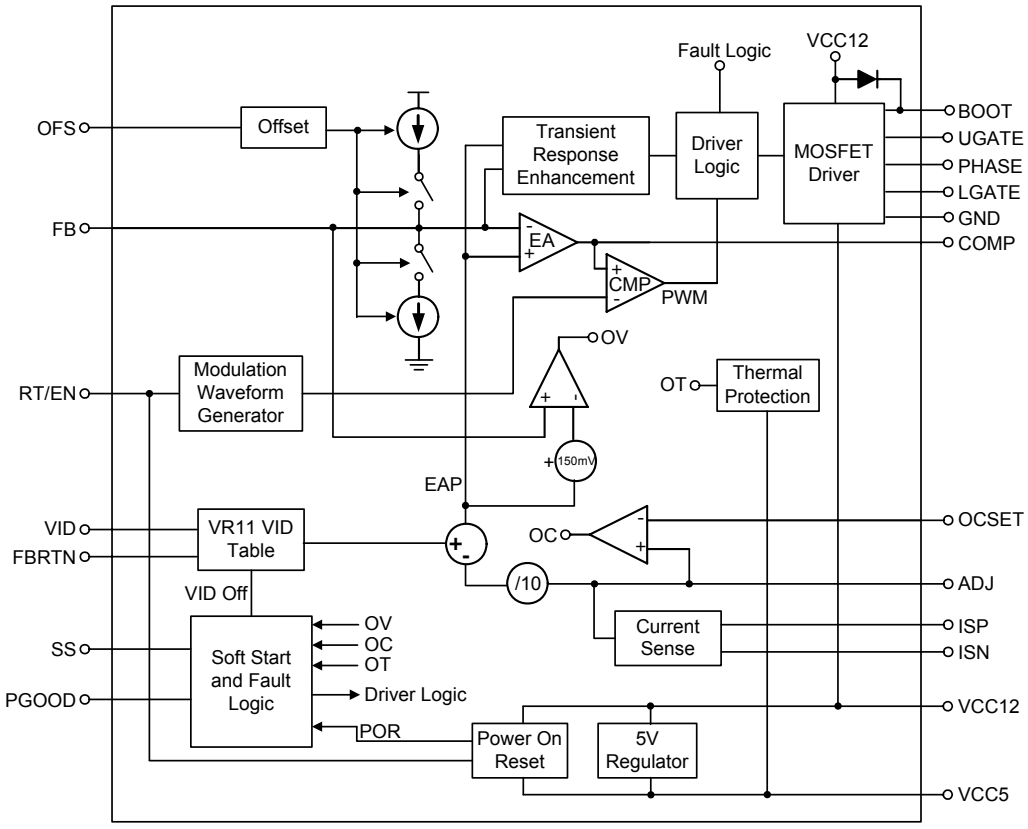
Typical Application Circuit



Function Block Diagram



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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FBRTN	Return Ground. This pin is Negative Node of the differential Remote Voltage sending.
2	SS	Soft-Start Ramp Slope Set Pin. Connect this pin to FBRTN by a Capacitor to Adjust soft-start slew rate.
3	COMP	Compensation Pin. Output of Error Amplifier and Input of PWM comparator.
4	FB	Inverting Input of Error Amplifier.
5	ADJ	Droop Set Pin. Connect a resistor from this pin to GND sets the load line slope.
6	OFS	Voltage Offset Pin. This pin sets no load output voltage offset. Connect a resistor from this Pin to VCC5 or GND to bidirection set the output voltage no-load offset.
7	RT/EN	Switching Frequency Set Pin. Connect this pin to GND by a resistor to adjust switching frequency and operate with droop function.
8	VCC5	Internal 5V Regulator Output.
9	ISP	Non-invertering Input of Current Sense Amplifier.
10	ISN	Invertering Input of Current Sense Amplifier.
11	OCSET	Over Current Protection Threshold Set Pin.
12	LGATE	Lower Gate Driver. This pin drives the gate of low side MOSFETs.
13	VCC12	12V Power Supply Input Pin.
14	PHASE	Switch Node of High Side Driver. Connect this pin to high side MOSFETs sources together with the low side MOSFETs drains and inductor.
15	UGATE	Upper Gate Driver. This pin drives the gate of the high side MOSFETs.
16	BOOT	Bootstrap Power Pin. This pin powers the high side MOSFETs drivers. Connect this pin to the junction of the bootstrap capacitor with the cathode of the bootstrap diode.
17	PGOOD	Power Good Indicator.
18	VID	DAC Voltage Identification Inputs.
19, 20, 21 (Exposed Pad)	GND	Ground Pin. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Table 1. Output Voltage Program

VID	DAC Output Voltage
1	1.050V
0	1.000V

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 15V
- BOOT to PHASE ---------- 1.7V to 15V
- PHASE to GND
  - DC ---------- –2V to 15V
  - <20ns ---------- –5V to 30V
- UGATE to PHASE
  - DC ---------- –0.3V to 15.3V
  - <20ns ---------- –5V to 18V
- LGATE to GND
  - DC ---------- (GND – 0.3V) to (V_{CC} + 0.3V)
  - <20ns ---------- (GND – 5V) to (V_{CC} + 5V)
- Input/Output Voltage ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-20L 3x3 ---------- 1.471W
- Package Thermal Resistance (Note 2)
  - WQFN-20L 3x3, θ_{JA} ---------- 68°C/W
  - WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Power Input Voltage, V_{IN} ---------- 4.5V to 13.2V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC12 Supply Input						
VCC12 Supply Voltage	V_{VCC12}	No Switching	10.8	12	13.2	V
VCC12 Supply Current	I_{VCC12}		--	6	--	mA
VCC5 Power						
VCC5 Supply Voltage	V_{VCC5}	I_{LOAD} = 10mA	4.9	5	5.1	V
VCC5 Output Sourcing	I_{VCC5}		10	--	--	mA
Power On Reset						
VCC12 Rising Threshold	V_{VCC12_th}		9.2	9.6	10	V
VCC12 Hysteresis	V_{VCC12_hys}		--	0.9	--	V
VCC5 Rising Threshold	V_{VCC5_th}		4.4	4.6	4.8	V
VCC5 Hysteresis	V_{VCC5_hys}		--	0.4	--	V

To be continued

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To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RT/EN						
Chip Disable Threshold	V_{DIS}		--	--	0.4	V
Running Frequency	f_{OSC}	R_{RT} = 60kΩ	180	200	220	kHz
RT Pin Voltage	$V_{RT, GND}$	R_{RT} = 60kΩ, when RT connected to GND by a register	1.52	1.6	1.68	V
RT Pin Voltage	$V_{RT, VDD}$	R_{RT} = 60kΩ, when RT connected to V_{CC5} by a register	V_{VCC5} – 1.68	V_{VCC5} – 1.6	V_{VCC5} – 1.52	V
Modulation Gain	A_{RAMP}	R_{RT} = 60kΩ	--	22	--	%/V
Reference Voltage Accuracy						
DAC Accuracy			–0.5	--	0.5	%
VID Input Low Voltage		VID	--	--	0.4	V
VID Input High Voltage		VID	0.8	--	--	V
Error Amplifier						
DC Gain	A_{DC}	No Load	--	80	--	dB
Gain-Bandwidth	GBW	C_{LOAD} = 10pF	--	10	--	MHz
Slew Rate	SR	C_{LOAD} = 10pF	10	--	--	V/μs
Output Voltage Range	V_{COMP}		0.5	--	3.6	V
Maximum Current	I_{EA_SLEW}	Slew	300	--	--	μA
Power Sequence						
PGOOD Low Voltage	V_{PGOOD}	I_{PGOOD} = 4mA	--	--	0.4	V
Soft-Start Delay	TD1		0	--	5	ms
PGOOD Delay	TD3		0.05	--	4	ms
Current Sense Amplifier						
Maximum Current	I_{GMMAX}	V_{CSP} = 1.3V, sink current from CSN	100	--	--	μA
Input Offset Voltage	V_{OSCS}		–1.5	0	1.5	mV
Soft-Start						
Soft-Start Current	I_{SS1}	Slew	12	16	20	μA
VID Change Current	I_{SS2}	Slew	120	160	200	μA
Gate Driver						
UGATE Drive Source	$I_{UGATEsr}$	V_{BOOT} – V_{PHASE} = 12V, V_{UGATE} – V_{PHASE} = 6V	0.6	1	--	A
UGATE Drive Sink	$R_{UGATEsk}$	V_{BOOT} – V_{PHASE} = 12V, V_{UGATE} – V_{PHASE} = 1V	--	1	--	Ω
LGATE Drive Source	$I_{LGATEsr}$	V_{VCC12} = 12V, V_{LGATE} = 6V	0.6	1	--	A
LGATE Drive Sink	$R_{LGATEsk}$	V_{VCC12} = 12V, V_{LGATE} = 1V	--	0.8	--	Ω
Protection						
Over Voltage Threshold	V_{OVP}	Sweep FB Voltage, V_{FB} – V_{EAP}	125	150	175	mV
OCP Input Offset Voltage	V_{OCOFS}		–10	--	10	mV
Thermal Shutdown			--	160	--	°C

To be continued

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Dynamic Characteristic						
UGATE Rise Time	t_{rUGATE}	C_{ISS} = 3000pF	-	15	-	ns
UGATE Fall Time	t_{fUGATE}		-	10	-	ns
LGATE Rise Time	t_{rLGATE}		-	15	-	ns
LGATE Rise Time	t_{fLGATE}		-	10	-	ns

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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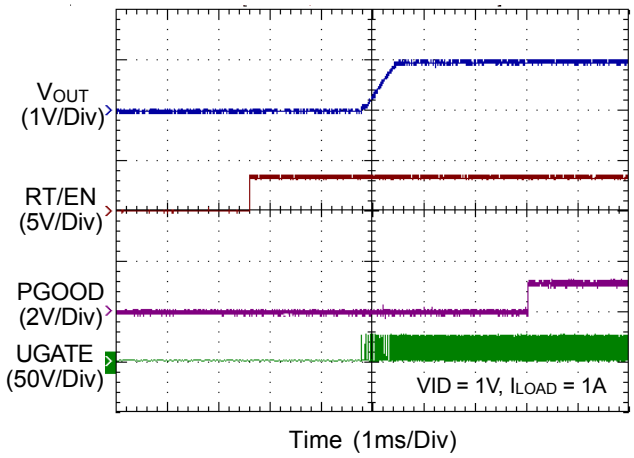
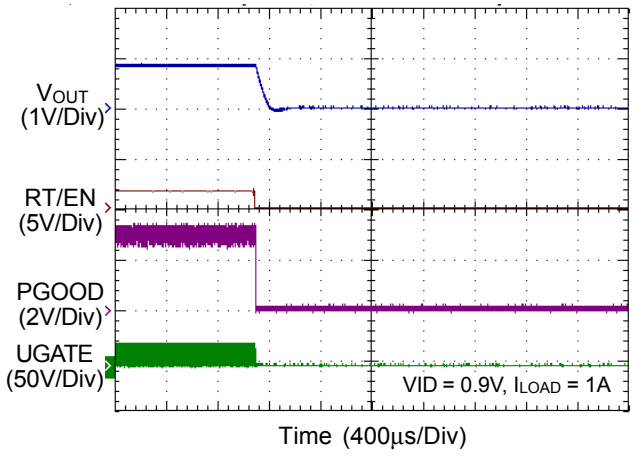
Typical Operating Characteristics

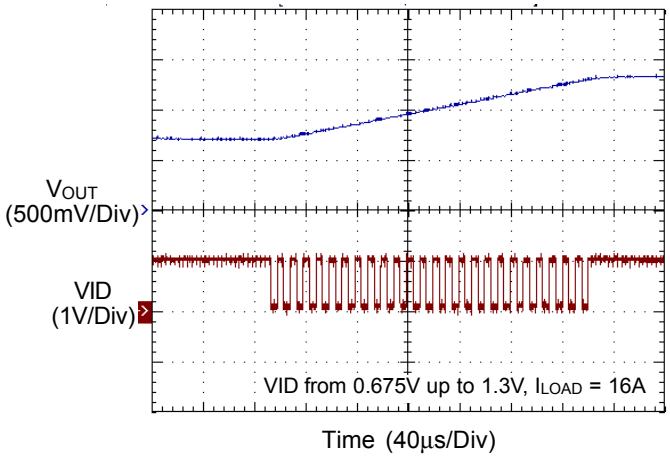
Power On from RT/EN



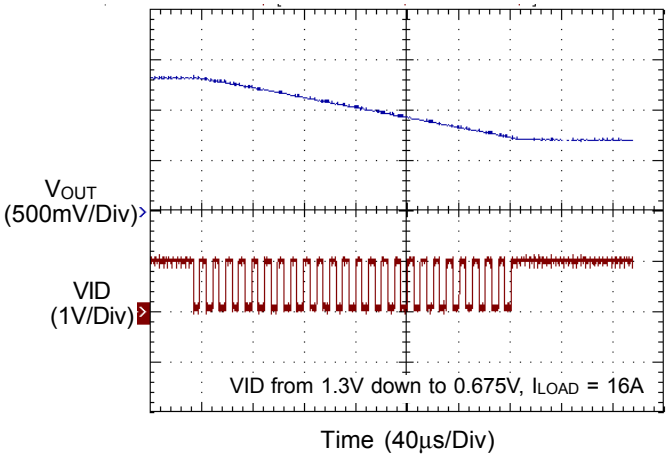
Power Off from RT/EN



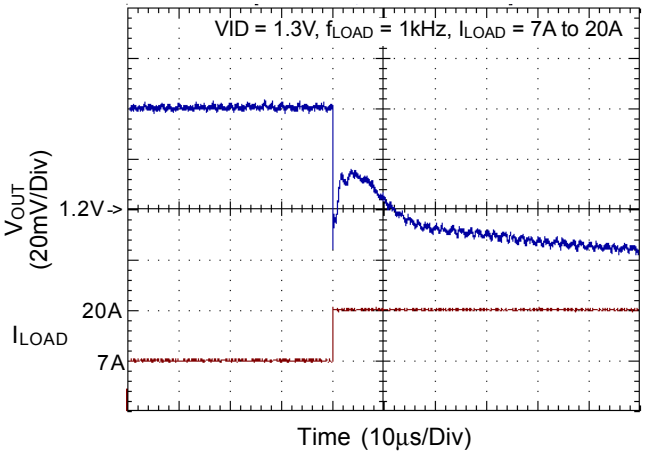
Dynamic VID Up



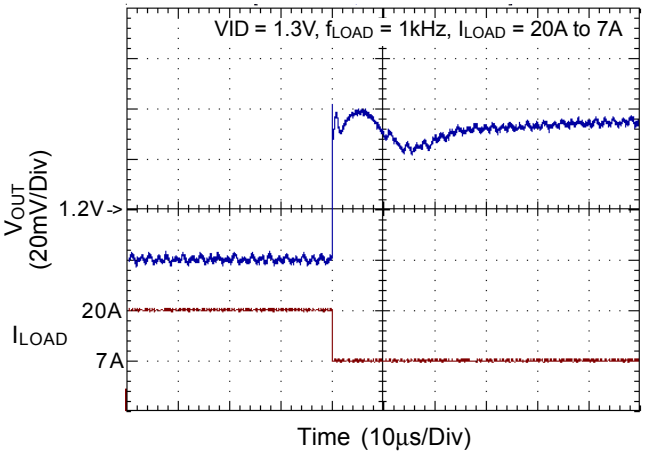
Dynamic VID Down



Load Transient Response



Load Transient Response



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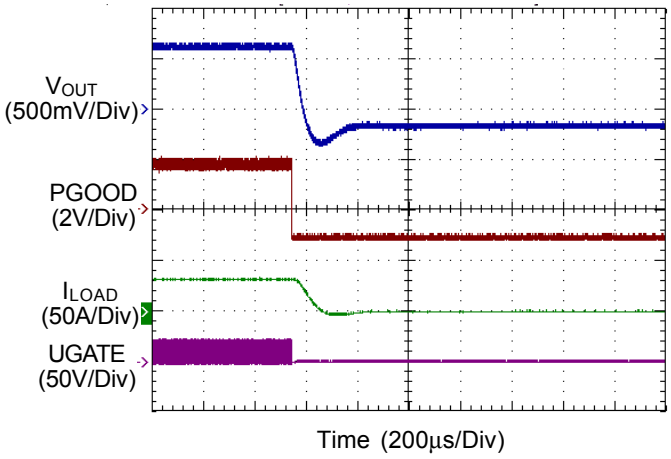
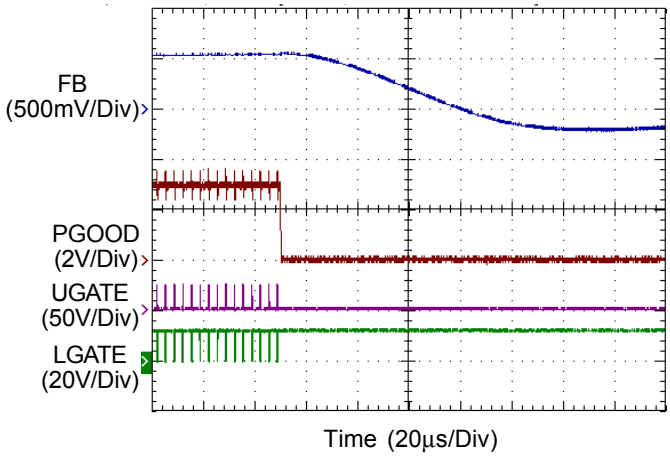
Over Current Protection



Over Voltage Protection



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Applications Information

The RT8121 is a single phase synchronous buck DC/DC converter with embedded MOSFET driver for advanced microprocessor application power.

Supply Voltage, VCC5 Regulation and POR

There are two supply voltage pins built in the RT8121: VCC12 and VCC5. VCC12 is a power input pin which receives external 12V voltage for embedded driver logic operation. VCC5 is a power output pin which is the output of an internal 5V LDO regulator. The mentioned 5V LDO regulator regulates VCC12 to generate a 5V voltage source for internal gate logic and external circuit biasing, e.g., OCP biasing. Since the VCC5 voltage is regulated, the variation of VCC5 (2%) will be much smaller than Platform ATX 5V (5% to 7%). The maximum supply current of VCC5 is 10mA, which is designed only for controller circuit biasing. The recommended configuration of the RT8121 supply voltages is as follows: Platform ATX 12V to the VCC12 pin, and decoupling capacitors on the VCC12 and VCC5 pins (minimum 0.1µF).

The initialization of the RT8121 requires both the voltage on the VCC12 and VCC5 to be ready. Since VCC5 is regulated internally from VCC12, the VCC5 voltage will be ready (>4.6V) after VCC12 reaches about 7V, so there is no power sequence problem between VCC12 and VCC5. After VCC5 > 4.6V and VCC12 > 9.6V, the internal Power-On-Reset (POR) signal goes high. This POR signal indicates the power supply voltages are all ready and initiates soft-start sequence. When POR = low, The RT8121 will try to turn off both high side and low side MOSFETs to prevent catastrophic failure.

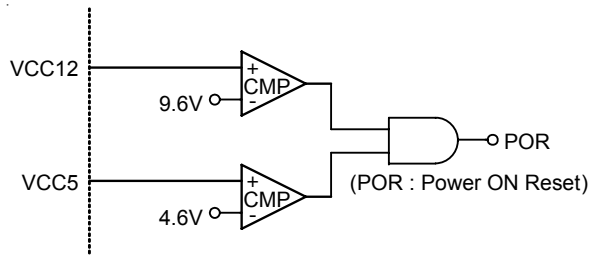

Figure 1. Circuit for Power Ready Detection

Switching Frequency

The switching frequency of the RT8121 is set by an external resistor connected from the RT pin either to GND or to VCC5. If resistor is connected from RT to GND, the load line function will be enable as well. More details will be described in the Load Line section. The frequency vs. different R_{RT} value is shown as Figure 2.

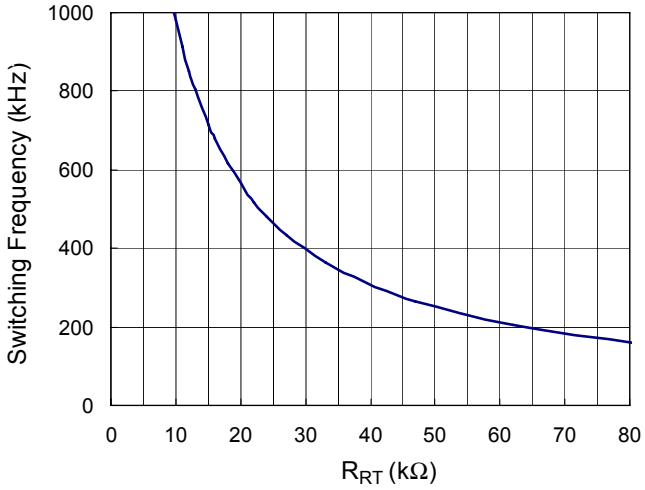

Figure 2. Switching Frequency vs. R_{RT} Resistance

Chip Enable

The enable function of the RT8121 is combined in the RT pin. Besides frequency setting function, pulling the RT pin to GND can also force the IC to enter soft shutdown sequence. It is recommended to connect a control switch from RT pin to GND in parallel with RT setting resistors. The RT8121 will enter soft shutdown sequence when the control switch is turned on.

Soft-Start

The V_{OUT} soft-start slew rate is set by a capacitor from the SS pin to FBRTN. Before Power On Reset (POR = low), the SS pin is held at GND. After Power On Reset (POR = high) and an extra delay of 1600µs (TD1), the controller initiates ramping up. V_{OUT} will always trace V_{EAP} during normal operation of the RT8121, where V_{EAP} is the positive input of compensation error amplifier, which can be described as $V_{EAP} = V_{DAC} - V_{ADJ}$ (The definition of V_{ADJ} will be described later in the Load Line section). After receiving valid VID code, V_{OUT} continues ramping up or

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down to the voltage specified by VID code. After V_{OUT} ramps to $V_{EAP} = V_{DAC} - V_{ADJ}$, the RT8121 stays in this state (TD3) and then asserts PGOOD = high. The ramping slew rate of TD2 is controlled by the external capacitor connected to SS pin. The voltage of the SS pin will always be V_{EAP} + 0.7V, where the mentioned 0.7V is the typical turn-on threshold of an internal power switch. Before PGOOD = high, the slew rate of V_{EAP} is limited to 16μA/C_{SS}. When PGOOD = high, the slew rate of V_{EAP} is limited to 160mA/C_{SS}. The soft start waveform is shown in Figure 4.

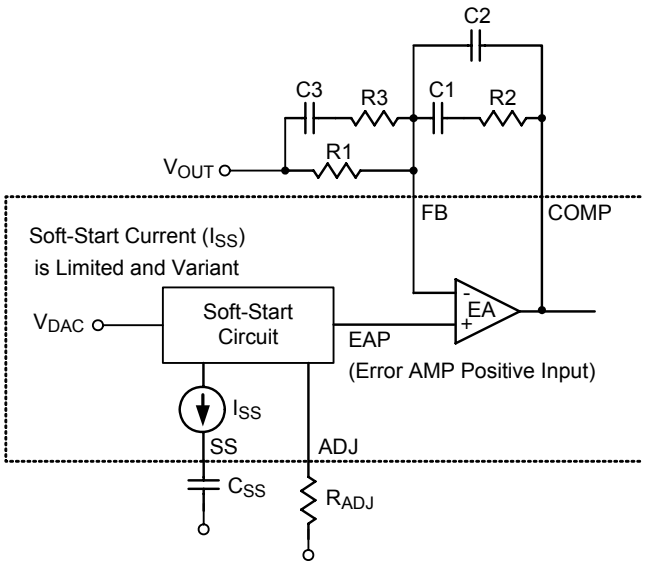

Figure 3. Circuit for Soft-Start and Dynamic VID

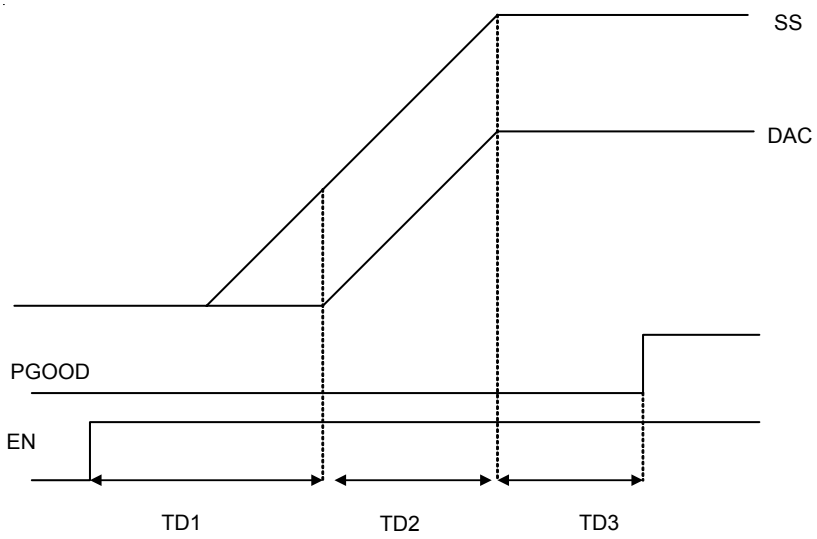

Figure 4. Soft-Start Waveform

TD1 is the delay time from power on reset state to the beginning of V_{OUT} rising.

$$TD1 = 1600\mu s + \frac{0.7V \times C_{SS}}{16\mu A}$$

$$TD2 = \frac{VID \times C_{SS}}{16\mu A}$$

TD3 is the power good delay time.

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Output Voltage Differential Sensing

The RT8121 uses a high-gain low-offset error amplifier for differential sensing. The CPU voltage is sensed between the FB and FBRTN pins. A resistor (R_{FB}) connects FB pin with the positive remote sense pin of the CPU (V_{CCP}), while the FBRTN pin connects directly to the negative remote sense pin of the CPU (V_{CCN}). The error amplifier compares V_{EAP} = (V_{DAC} – V_{ADJ}) with the V_{FB} to regulate the output voltage.

No-Load Offset

In Figure 5, I_{OFSN} and I_{OFSP} are used to generate no-load offset. Either I_{OFSN} or I_{OFSP} is active during normal operation. Connect a resistor from OFS pin to GND to activate I_{OFSN}. I_{OFSN} flows through R_{FB} from the FB pin to V_{CCP}. In this case, a negative no-load offset voltage (V_{OFSN}) is generated.

$$V_{OFSN} = I_{OFSN} \times R_{FB} = \frac{0.8 \times R_{FB}}{R_{OFS}}$$

Connect a resistor from OFS pin to VCC5 to activate I_{OFSP}. I_{OFSP} flows through R_{FB} from V_{CCP} to FB pin. In this case, a positive no-load offset voltage (V_{OFSP}) is generated.

$$V_{OFSP} = I_{OFSP} \times R_{FB} = \frac{6.4 \times R_{FB}}{R_{OFS}}$$

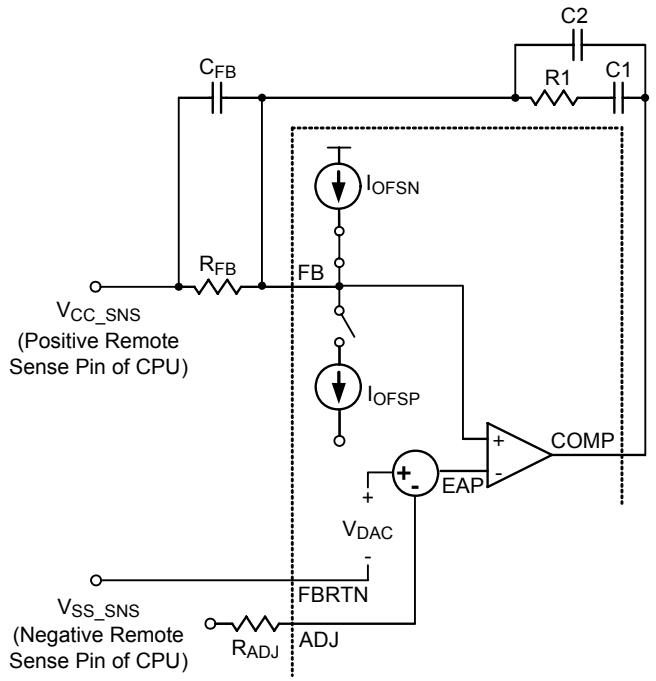

Figure 5. Circuit for V_{OUT} Differential Sensing and No-Load Offset

Load Transient Quick Response

In steady state, the voltage of V_{FB} is controlled to be very close to V_{EAP}. While a load step transient from light load to heavy load could cause V_{FB} to be lower than V_{EAP} by several tens of mV. In conventional buck converter design (without non-linear control) for CPU VR application, due to limited control bandwidth, it is hard for the VR to prevent V_{OUT} undershoot during quick load transient from light load to heavy load. Hence, the RT8121 builds in a state-of-the-art quick response function which detects load transient by comparing V_{FB} and V_{EAP}. If V_{FB} suddenly drops below "V_{EAP}–V_{QR}"where V_{QR} is a predetermined voltage (~40mV), the quick response indicator QR rises up. When QR = high, the RT8121 turns on all high side MOSFETs and turns off all low side MOSFETs. The sensitivity of quick response can be adjusted by varying the values of C_{FB} and R_{FB}. Smaller R_{FB} and/or larger C_{FB} will make QR easier to be triggered. Figure 6 is the circuit and typical waveforms.

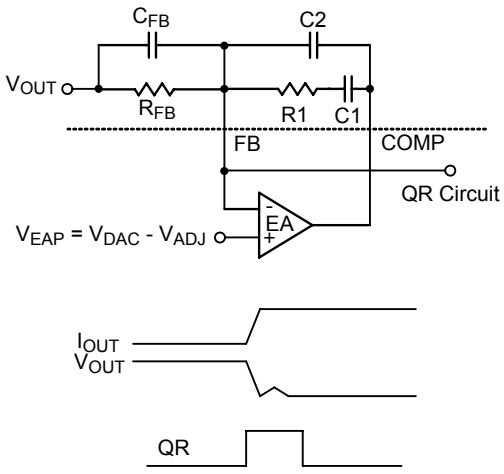

Figure 6. Load Transient Quick Response

Output Current Sensing

The RT8121 provides a low input offset Current Sense Amplifier (CSA) to monitor the output current. The output current of CSA (I_X) is used for load line control and over current protection. In this inductor current sensing topology, R_S and C_S must be set according to the equation below :

$$\frac{L}{DCR} = R_S \times C_S$$

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Then the output current of CSA will follow the equation below :

$$I_X = \frac{I_L \times DCR - V_{OFS\text{-}CSA} + 700n \times (R_{ISP} + R_S - R_{ISN})}{R_{ISN}}$$

700nA is a typical value of the CSA input offset current. $V_{OFS\text{-}CSA}$ is the input offset voltage of CSA. $V_{OFS\text{-}CSA}$ of the RT8121 is smaller than +/- 1.5mV. Usually, "$V_{OFS\text{-}CSA}$ + 700n x (R_{ISP} + R_S - R_{ISN})" is negligible except at very light load and the equation can be simplified as the equation below :

$$I_X = \frac{I_L \times DCR}{R_{ISN}}$$

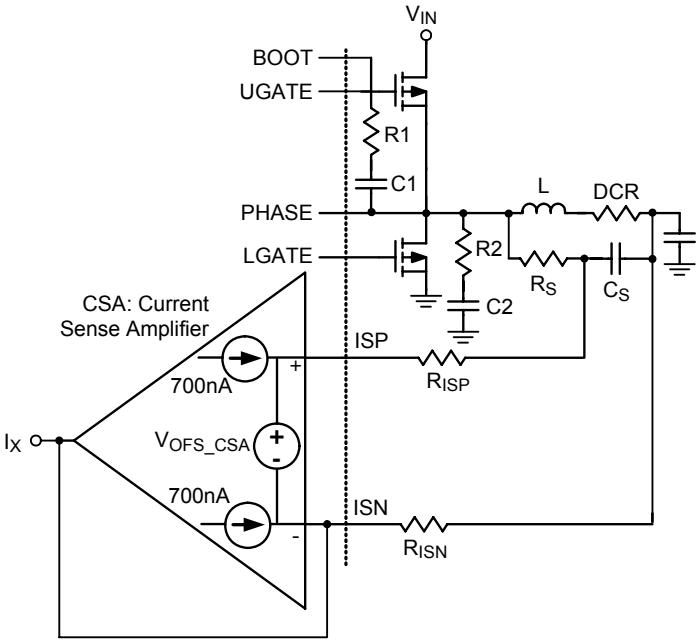

Figure 7. Circuit for Current Sensing

Load Line

The RT8121 utilizes inductor DCR current sense technique for load line control function. The sensed inductor current I_X is multiplied by 0.5 and sent to ADJ pin. After the current 0.5 x I_X injects into the ADJ resistors, the voltage of the ADJ pin is established. The V_{ADJ} is then multiplied by 0.1 and subtracted by V_{DAC} to generate V_{EAP}. Because I_X is a PTC (Positive Temperature Coefficient) current, an NTC (Negative Temperature Coefficient) resistor is needed to connect ADJ pin to GND. If the NTC resistor is properly selected to compensate the temperature coefficient of I_X, the voltage on ADJ pin will be proportional to I_{OUT} without temperature effect. In the RT8121, the positive input of error amplifier is "V_{DAC} – 0.1 x V_{ADJ}" and V_{OUT} will follow "V_{DAC} – 0.1 x V_{ADJ}". Thus, the output voltage which decreases linearly with I_{OUT} is obtained. The load line is defined as :

$$V_{ADJ} = \frac{1}{2} \times I_X \times R_{ADJ}$$

$$LL = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{\frac{1}{10}\Delta V_{ADJ}}{\Delta I_{OUT}} = \frac{1}{2} \times \frac{DCR}{R_{ISN}} \times \frac{1}{10} \times R_{ADJ}$$

Basically, the resistance of R_{ADJ} sets the resistance of the load line. The temperature coefficient of the R_{ADJ} compensates the temperature effect of the load line.

Over Current Protection (OCP)

In Figure 8, V_{OCSET} is equal to VCC5 x R2/(R1 + R2). For the RT8121, V_{ADJ} is proportional to I_{OUT} and is thermally compensated. Once V_{ADJ} is larger than V_{OCSET}, OCP is triggered and latched. The OCP function will not be influenced by enabling or disabling load line since the voltage on the ADJ pin always contains real time information of load current. Once OCP is triggered, the RT8121 will turn off both high side MOSFETs and low side MOSFETs.

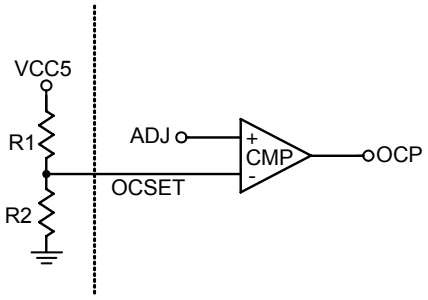

Figure 8. Over Current Protection

Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds "V_{EAP} + 150mV", OVP is triggered and latched. The RT8121 will turn on low side MOSFET and turn off high side MOSFET to protect CPU. A 20μs delay is used in OVP detection circuit to prevent false trigger.

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Over Temperature Protection (OTP)

The over temperature protection function of the RT8121 is built inside the controller to prevent overheat damage. OTP occurs when the die temperature of the RT8121 exceeds 150°C, in which the RT8121 then turns off both high side MOSFETs and low side MOSFETs.

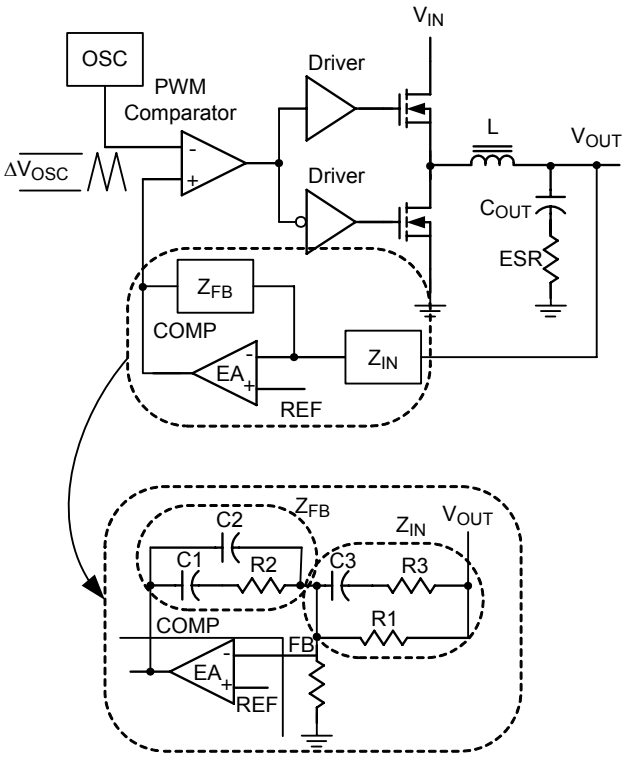

Figure 9. Compensation Circuit

Loop Compensation

The RT8121 is a voltage mode controller and requires external compensation. To compensate a typical voltage mode buck converter, there are two ordinary compensation schemes, commonly known as type-II compensator and type-III compensator. The choice of using type-II or type-III compensator lies with the platform designers, and the main concern deals with the position of the capacitor ESR zero and mid-frequency to high frequency gain boost. Typically, the ESR zero of output capacitor will tend to stabilize the effect of output LC double poles. Hence, the position of the output capacitor ESR zero in frequency domain may influence the design of voltage loop compensation. Figure 9 shows a typical control loop using type-III compensator. Below is the compensator design procedure.

1) Modulator Characteristic

The modulator consists of the PWM comparator and power stage. The PWM comparator compares error amplifier EA output (COMP) with oscillator (OSC) sawtooth wave to provide a pulse-width modulated (PWM) gate-driving signal. The PWM wave is smoothed out by the output filter, L_{OUT} and C_{OUT}. The output voltage (V_{OUT}) is sensed and fed to the inverting input of the error amplifier.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP} (output voltage over the error amplifier output). This transfer function is dominated by a DC gain, a double pole, and an ESR zero as shown in Figure 10.

The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage V_{OSC}. The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter is expressed as :

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires the output capacitor to have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor is expressed as the following equation :

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

2) Design the Compensator

A well-designed compensator regulates the output voltage to the reference voltage V_{REF} with fast transient response and good stability. In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (usually greater than 45°) and the highest bandwidth (0dB crossing frequency, f_C) possible. It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of -20dB/dec.

According to Figure 10, the location of poles and zeros are :

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$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}$$

$$f_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3}$$

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times C3 \times R3}$$

$$f_{P3} = \frac{1}{2\pi \times \frac{C1 \times C2 \times R2}{C1 + C2}}$$

Generally, f_{Z1} and f_{Z2} are designed to cancel the double pole of modulation. Usually, place f_{Z1} at a fraction of the f_{LC}, and place f_{Z2} at f_{LC}. f_{P2} is usually placed at f_{ESR} to cancel the ESR zero. And f_{P3} is placed below switching frequency to cancel high frequency noise.

For given bandwith, R2, f_{Z1}, f_{Z2}, f_{P2}, f_{P3}, then

$$C1 = \frac{1}{2\pi \times f_{Z1} \times R2}$$

$$C3 = \frac{G_{vd@BW}}{2\pi \times f_C \times R2}$$

$$R1 = \frac{1}{2\pi \times f_{Z2} \times C3}$$

$$R3 = \frac{1}{2\pi \times f_{P2} \times C3}$$

$$C2 = \frac{C1}{2\pi \times f_{P3} \times C1 \times R2 - 1}$$

where $G_{vd@BW}$ is open loop gain at cross over frequency

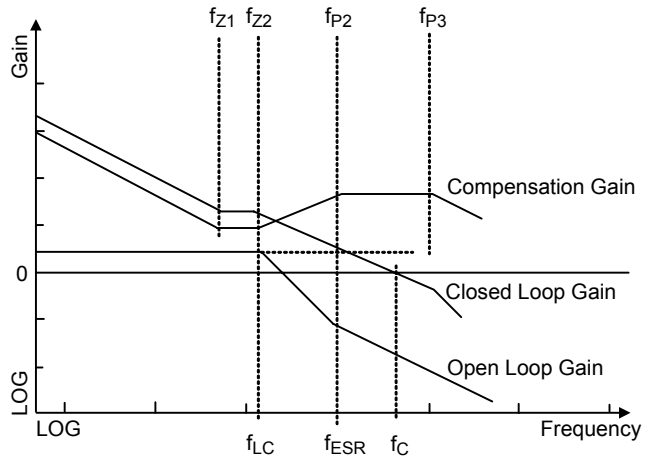

Figure 10. Bode Plot of Loop Gain

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, rate of surrounding airflow and difference between junction to ambient temperature. The maximum power dissipation can be calculated by following the formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance.

For recommended specifications of operating conditions of RT8121, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-20L 3x3 packages, the thermal resistance θ_{JA} is 68°C/W on the standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (68°C/W) = 1.471W for WQFN-20L 3x3 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8121 package, the derating curve in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

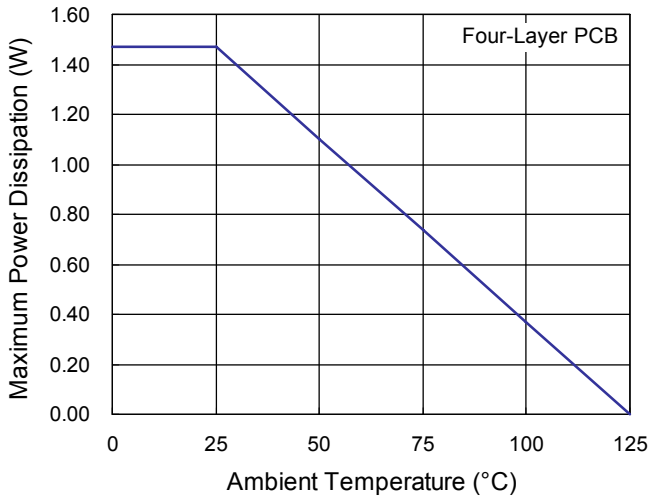

Figure 11. Derating Curve for RT8121 Package

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Layout Considerations

For best performance of the RT8121, the following guidelines must be strictly followed :

- The power components should be placed first. Keep the connection between power components as short as possible.
- The shape of the phase plane (the connection plane between high side MOSFETs, low side MOSFETs and output inductors) has to be as square as possible. Long traces, thin bars or separated islands must be avoided in the phase plane.
- Keep snubber circuits or damping elements near its objects. Phase RC snubbers have to be close to low side MOSFETs, UGATE damping resistor has to be close to high side MOSFETs, and boot to phase damping resistor has to be close to high side MOSFETs and phase plane. Also, keep the traces of these snubber circuits as short as possible.
- The area of V_{IN} plane (power stage 12V V_{IN}) and V_{OUT} plane (output bulk capacitors and inductor connection plane) has to be as wide as possible. Long traces or thin bars must be avoided in these planes. The plane trace width must be wide enough to carry large input/ output current (40mm/A).
- The following traces have to be wide and short : UGATE, LGATE, BOOT, PHASE, and VCC12. Make sure the widths of these traces are wide enough to carry large driving current (at least 40mm).
- The voltage feedback loop contains two traces, VCC and VSS, which are Kelvin sensed from CPU socket or output capacitors. These two traces should have 10mm width and be placed away from high (di/dt) switching elements such as high side MOSFETs, low side MOSFETs, phase plane etc. The circuit elements of voltage feedback loop, such as feedback loop short resistors and voltage loop compensation RCs, have to be kept near the RT8121 and also away from switching elements.
- The current sense mechanism of the RT8121 is fully differential Kelvin sense. Therefore, the current-sense loop of the RT8121 contain two traces : the positive trace(ISP) comes from the positive node the of output inductor (the node connecting phase plane) and the negative trace (ISN) comes from the negative node of the output inductor (the node connecting output plane).

DO NOT connect the current-sense traces from the phase plane or output plane. Only connect these traces from both sides of the output inductor to achieve the goal of precise Kelvin sense. The current-sense feedback loops have to be routed away from switching elements, and the current-sense RC elements have to be put near their respective ISN or ISP pins of the RT8121 and also away from noise switching elements. At lease 10 mm width is suggested for current sense feedback loops.

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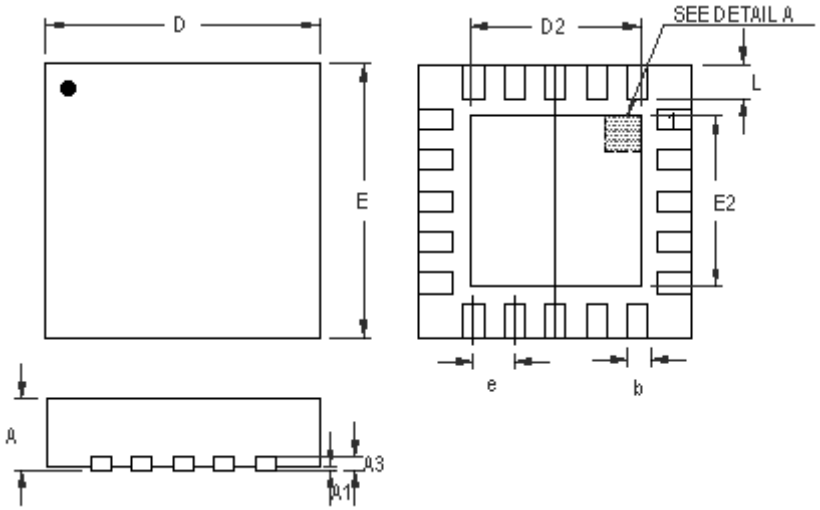
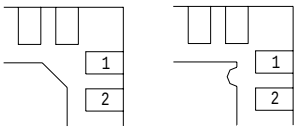
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

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