Single-Phase PWM Controller for CPU / GPU Core Power Supply

General Description

The RT8152A/B is a single phase PWM controller with integrated MOSFET drivers. Moreover, it is compliant with Intel IMVP6.5 Voltage Regulator Specification to fulfill its mobile CPU core and Render core voltage regulator requirements.

The RT8152A/B adopts G-NAVP (Green-Native AVP), which is a Richtek's proprietary topology derived from finite DC gain compensator constant on-time mode, making it an easy-setting PWM controller meeting all Intel AVP (Active Voltage Positioning) mobile CPU/Render requirements. The output voltage of the RT8152A/B is set by 7-bit VID code. The built-in high accuracy DAC converts the VID code ranging from 0V to 1.5V with 12.5mV per step. The system accuracy of the controller can reach 1.5%. The part supports VID on-the-fly and mode change on-the-fly functions that are fully compliant with IMVP6.5 specification. It operates in single phase and diode emulation modes. It can reach up to 90% efficiency in different modes according to different loading conditions. The droop load-line can be easily programmed by setting the DC gain of the error amplifier. With proper compensation, the load transient can achieve optimized AVP performance. This chip controls soft-start and output transition slew rate via a capacitor. It supports both DCR and sense-resistor current sensing.

The RT8152A/B provides power good and thermal throttling output signals for IMVP6.5 Render core specification, and additional clock enabling for CPU core specification. It also features complete fault protection functions including over voltage, under voltage, negative voltage, over current and thermal shutdown. The RT8152A/B is available in WQFN-32L 5x5 small foot print package.

Applications

- IMVP6.5 CPU / Render Core Voltage Regulator
- AVP Step-Down Converter
- Notebook / Desktop Computer / Servers

Features

- **Single Phase PWM Controller with Integrated MOS Driver.**
- **Low-Gain Compensator with CCRCOT Topology (Constant Current Ripple Constant On Time)**
- **7-bit DAC**
- **0.8% DAC Accuracy**
- **1.5% or 11.5mV System Accuracy**
- **Fixed V_{BOOT} (For CPU Core Only)**
- **Differential Remote Voltage Sensing**
- **G-NAVP Topology (Green-Native AVP)**
- **Programmable Output Transition Slew Rate Control**
- **System Thermal Compensated AVP**
- **Ringing Free Mode at Light Load Condition**
- **Fast Transient Response**
- **IMVP6.5 Compatible Power Management States**
- **Power Good**
- **Clock Enable Output (For CPU Core Only)**
- **Thermal Throttling**
- **Current Monitor Output**
- **Switching Frequency Up to 1MHz**
- **OVP, UVP, OCP, OTP, UVLO, NVP**
- **32-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT8152□□□

- Package Type
  QW : WQFN-32L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- BOOT Output Voltage
  A : 1.1V
  B : 1.2V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT8152AGQW

RT8152AGQW : Product Number

YMDNN : Date Code

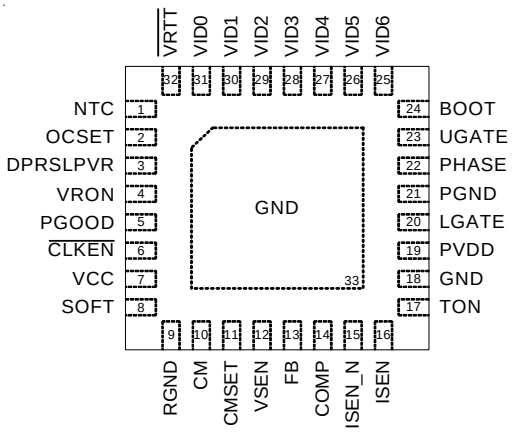
RT8152BGQW

RT8152BGQW : Product Number

YMDNN : Date Code

Pin Configurations

(TOP VIEW)



WQFN-32L 5x5

Typical Application Circuit

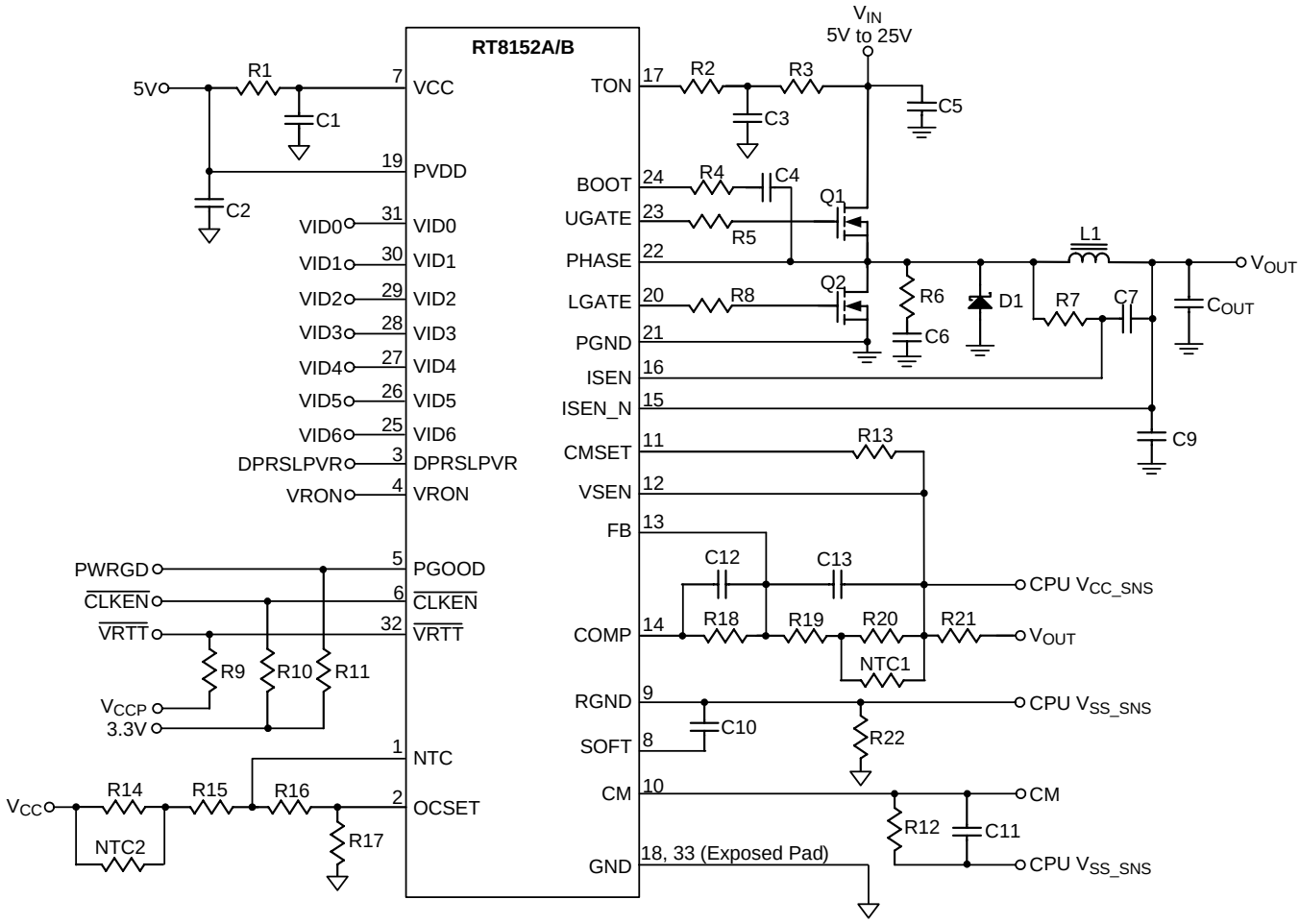


Figure 1. CPU Core Voltage Regulator

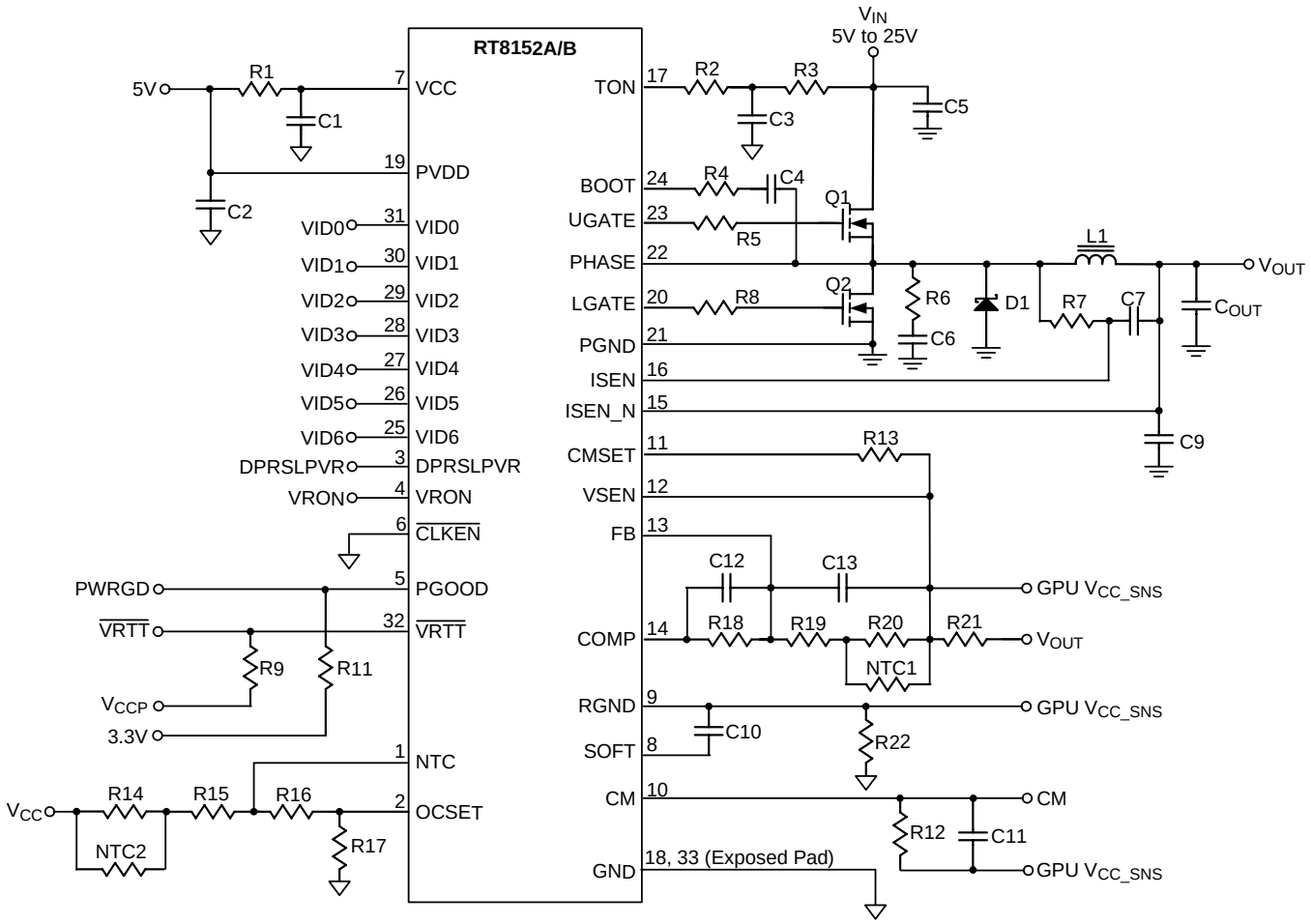


Figure 2. Render Core Voltage Regulator

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	NTC	Thermal Detection Input for $\overline{\text{VRTT}}$ Circuit. Connect this pin with a resistor divider from VCC using NTC on the top to set the thermal management threshold level.
2	OCSET	Over Current Protection Setting. Connect a resistor voltage divider from VCC to ground, the joint of the resistor divider is connected to OCSET pin, with a voltage VOCSET, to set the over current threshold I_{LIM}.
3	DPRSLPVR	Deeper Sleep Mode Signal.
4	VRON	Voltage Regulator Enabler.
5	PGOOD	Power Good Indicator.
6	$\overline{\text{CLKEN}}$	Inverted Clock Enable. Pull high by a resistor for CPU core application. This open-drain pin is an output indicating the start of the PLL locking of the clock chip. Connect to GND for Render application.
7	VCC	Chip Power.
8	SOFT	Soft-Start. This pin provides soft-start function and slew rate controller. The capacitance of the slew rate control capacitor is restricted to be larger than 10nF. The feedback voltage of the converter follows the ramping voltage on the SOFT pin during soft-start and other voltage transitions according to different mode of operation and VID change.
9	RGND	Return Ground. This pin is the negative node of the differential remote voltage sensing.

To be continued

Pin No.	Pin Name	Pin Function
10	CM	Current Monitor Output. This pin outputs a voltage proportional to the output current.
11	CMSET	Current Monitor Output Gain Externally Setting. Connect this pin with one resistor to VSEN while CM pin is connected to ground with one another resistor. In such way, current monitor output gain can be set by the ratio of these two resistors.
12	VSEN	Positive Voltage Sensing Pin. This pin is the positive node of the differential voltage sensing.
13	FB	Feedback. This is the negative input node of the error amplifier.
14	COMP	Compensation. This pin is the output node of the error amplifier.
15	ISEN_N	Negative input of the current sense.
16	ISEN	Positive input of the current sense.
17	TON	Connect this pin to VIN with one resistor.
18, 33 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
19	PVDD	Driver Power.
20	LGATE	Lower Gate Drive. This pin drives the gate of the low side MOSFETs.
21	PGND	Driver Ground.
22	PHASE	This pin is return node of the high-side MOSFET driver. Connect this pin to the high side MOSFET sources together with the low side MOSFET drains and the inductor.
23	UGATE	Upper Gate Drive. This pin drives the gate of the high side MOSFETs.
24	BOOT	Bootstrap Power Pin. This pin powers the high side MOSFET drivers. Connect this pin to bootstrap capacitor.
25 to 31	VID6 to VID0	Voltage ID. DAC voltage identification inputs for IMVP6.5. The logic threshold is 30% of the VCCP as the maximum value for low state and 70% of the VCCP as the minimum value for the high state.
32	$\overline{\text{VRTT}}$	Voltage Regulator Thermal Throttling. This open-drain output pin will be pulled low when the preset temperature level is exceeded.

Table 1. IMVP6.5 VID Code Table

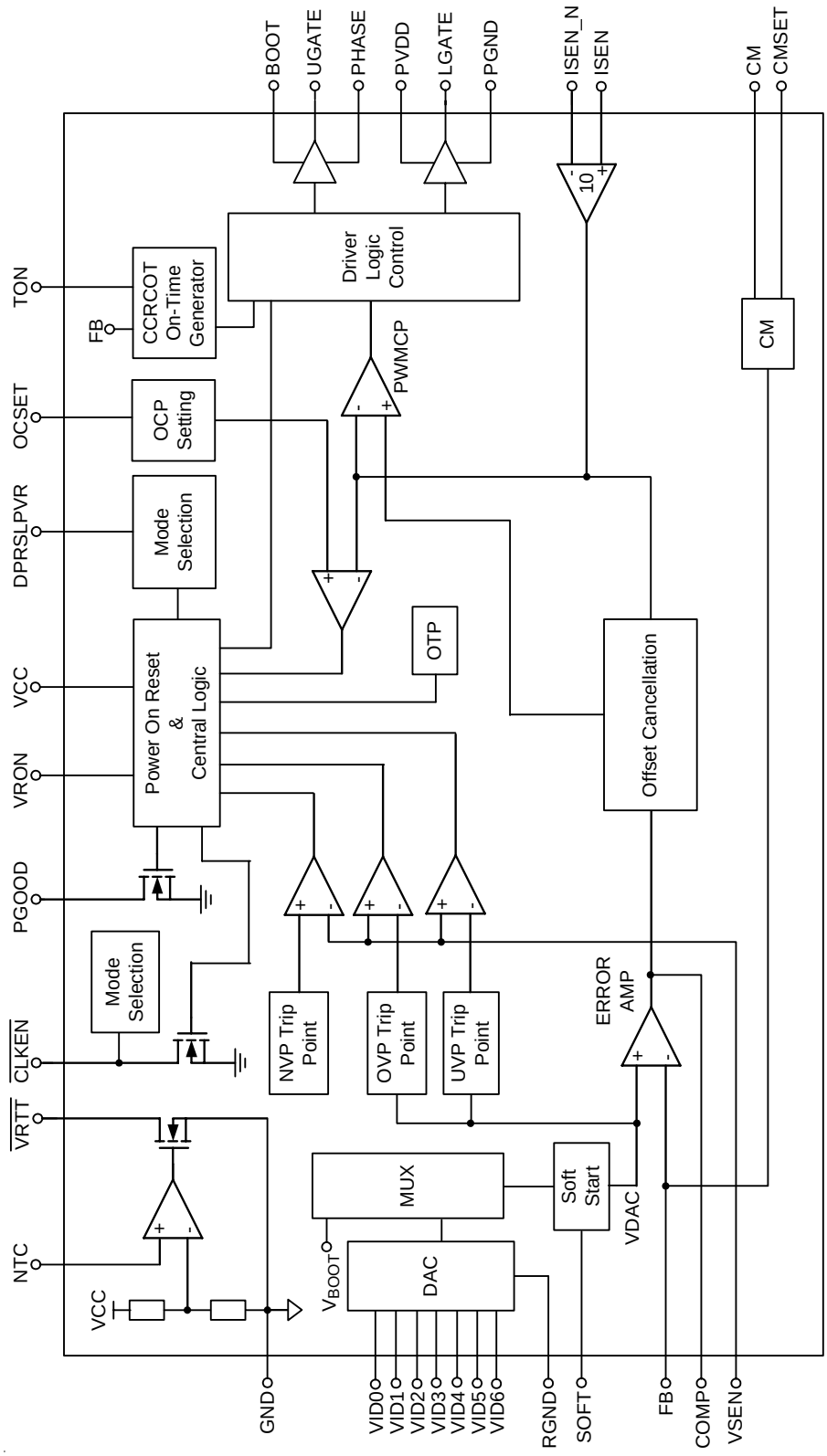
VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
0	0	0	0	0	0	0	1.5000V
0	0	0	0	0	0	1	1.4875V
0	0	0	0	0	1	0	1.4750V
0	0	0	0	0	1	1	1.4625V
0	0	0	0	1	0	0	1.4500V
0	0	0	0	1	0	1	1.4375V
0	0	0	0	1	1	0	1.4250V
0	0	0	0	1	1	1	1.4125V
0	0	0	1	0	0	0	1.4000V
0	0	0	1	0	0	1	1.3875V
0	0	0	1	0	1	0	1.3750V
0	0	0	1	0	1	1	1.3625V
0	0	0	1	1	0	0	1.3500V
0	0	0	1	1	0	1	1.3375V
0	0	0	1	1	1	0	1.3250V
0	0	0	1	1	1	1	1.3125V
0	0	1	0	0	0	0	1.3000V
0	0	1	0	0	0	1	1.2875V
0	0	1	0	0	1	0	1.2750V
0	0	1	0	0	1	1	1.2625V
0	0	1	0	1	0	0	1.2500V
0	0	1	0	1	0	1	1.2375V
0	0	1	0	1	1	0	1.2250V
0	0	1	0	1	1	1	1.2125V
0	0	1	1	0	0	0	1.2000V
0	0	1	1	0	0	1	1.1875V
0	0	1	1	0	1	0	1.1750V
0	0	1	1	0	1	1	1.1625V
0	0	1	1	1	0	0	1.1500V
0	0	1	1	1	0	1	1.1375V
0	0	1	1	1	1	0	1.1250V
0	0	1	1	1	1	1	1.1125V
0	1	0	0	0	0	0	1.1000V
0	1	0	0	0	0	1	1.0875V
0	1	0	0	0	1	0	1.0750V
0	1	0	0	0	1	1	1.0625V
0	1	0	0	1	0	0	1.0500V
0	1	0	0	1	0	1	1.0375V
0	1	0	0	1	1	0	1.0250V
0	1	0	0	1	1	1	1.0125V
0	1	0	1	0	0	0	1.0000V
0	1	0	1	0	0	1	0.9875V
0	1	0	1	0	1	0	0.9750V
0	1	0	1	0	1	1	0.9625V
0	1	0	1	1	0	0	0.9500V
0	1	0	1	1	0	1	0.9375V
0	1	0	1	1	1	0	0.9250V
0	1	0	1	1	1	1	0.9125V
0	1	1	0	0	0	0	0.9000V
0	1	1	0	0	0	1	0.8875V
0	1	1	0	0	1	0	0.8750V
0	1	1	0	0	1	1	0.8625V
0	1	1	0	1	0	0	0.8500V
0	1	1	0	1	0	1	0.8375V
0	1	1	0	1	1	0	0.8250V
0	1	1	0	1	1	1	0.8125V
0	1	1	1	0	0	0	0.8000V
0	1	1	1	0	0	1	0.7875V
0	1	1	1	0	1	0	0.7750V
0	1	1	1	0	1	1	0.7625V
0	1	1	1	1	0	0	0.7500V
0	1	1	1	1	0	1	0.7375V
0	1	1	1	1	1	0	0.7250V
0	1	1	1	1	1	1	0.7125V
1	0	0	0	0	0	0	0.7000V
1	0	0	0	0	0	1	0.6875V

To be continued

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
1	0	0	0	0	1	0	0.6750V
1	0	0	0	0	1	1	0.6625V
1	0	0	0	1	0	0	0.6500V
1	0	0	0	1	0	1	0.6375V
1	0	0	0	1	1	0	0.6250V
1	0	0	0	1	1	1	0.6125V
1	0	0	1	0	0	0	0.6000V
1	0	0	1	0	0	1	0.5875V
1	0	0	1	0	1	0	0.5750V
1	0	0	1	0	1	1	0.5625V
1	0	0	1	1	0	0	0.5500V
1	0	0	1	1	0	1	0.5375V
1	0	0	1	1	1	0	0.5250V
1	0	0	1	1	1	1	0.5125V
1	0	1	0	0	0	0	0.5000V
1	0	1	0	0	0	1	0.4875V
1	0	1	0	0	1	0	0.4750V
1	0	1	0	0	1	1	0.4625V
1	0	1	0	1	0	0	0.4500V
1	0	1	0	1	0	1	0.4375V
1	0	1	0	1	1	0	0.4250V
1	0	1	0	1	1	1	0.4125V
1	0	1	1	0	0	0	0.4000V
1	0	1	1	0	0	1	0.3875V
1	0	1	1	0	1	0	0.3750V
1	0	1	1	0	1	1	0.3625V
1	0	1	1	1	0	0	0.3500V
1	0	1	1	1	0	1	0.3375V
1	0	1	1	1	1	0	0.3250V
1	0	1	1	1	1	1	0.3125V
1	1	0	0	0	0	0	0.3000V

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
1	1	0	0	0	0	1	0.2875V
1	1	0	0	0	1	0	0.2750V
1	1	0	0	0	1	1	0.2625V
1	1	0	0	1	0	0	0.2500V
1	1	0	0	1	0	1	0.2375V
1	1	0	0	1	1	0	0.2250V
1	1	0	0	1	1	1	0.2125V
1	1	0	1	0	0	0	0.2000V
1	1	0	1	0	0	1	0.1875V
1	1	0	1	0	1	0	0.1750V
1	1	0	1	0	1	1	0.1625V
1	1	0	1	1	0	0	0.1500V
1	1	0	1	1	0	1	0.1375V
1	1	0	1	1	1	0	0.1250V
1	1	0	1	1	1	1	0.1125V
1	1	1	0	0	0	0	0.1000V
1	1	1	0	0	0	1	0.0875V
1	1	1	0	0	1	0	0.0750V
1	1	1	0	0	1	1	0.0625V
1	1	1	0	1	0	0	0.0500V
1	1	1	0	1	0	1	0.0375V
1	1	1	0	1	1	0	0.0250V
1	1	1	0	1	1	1	0.0125V
1	1	1	1	0	0	0	0.0000V
1	1	1	1	0	0	1	0.0000V
1	1	1	1	0	1	0	0.0000V
1	1	1	1	0	1	1	0.0000V
1	1	1	1	1	0	0	0.0000V
1	1	1	1	1	0	1	0.0000V
1	1	1	1	1	1	0	0.0000V
1	1	1	1	1	1	1	0.0000V

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- RGND, PGND to GND ---------- –0.3V to 0.3V
- VIDx to GND ---------- –0.3V to V_{CC}+ 0.3V
- DPRSLPVR, VRON to GND ---------- –0.3V to V_{CC}+ 0.3V
- PGOOD, $\overline{CLKEN}$, $\overline{VRTT}$ to GND ---------- –0.3V to V_{CC}+ 0.3V
- VSEN, FB, COMP, SOFT, OCSET, CM, CMSET, NTC to GND ---------- –0.3V to V_{CC}+ 0.3V
- ISEN, ISEN_N to GND ---------- –0.3V to V_{CC}+ 0.3V
- PVDD to PGND ---------- –0.3V to 6.5V
- LGATE to PGND
  - DC ---------- –0.3V to PVDD+ 0.3V
  - <20ns ---------- –2.5V
- PHASE to PGND
  - DC ---------- –0.3V to 28V
  - <20ns ---------- –8V
- BOOT to PHASE ---------- –0.3V to 6.5V
- UGATE to PHASE
  - DC ---------- –0.3V to BOOT – PHASE
  - <20ns ---------- –5V
- TON to GND ---------- –0.3V to 28V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–32L 5x5 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  - WQFN–32L 5x5, θ_{JA} ---------- 36°C/W
  - WQFN–32L 5x5, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 4.5V to 5.5V
- Battery Voltage, V_{IN} ---------- 5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{VCC} + I_{PVDD}	RTON = 130kΩ, VRON = 3.3V, No Loading Current	--	--	10	mA
Shutdown Current	I_{VCC} + I_{PVDD}	V_{RON} = 0V	--	--	5	μA
Soft Start/Slew Rate Control (based on 10nF C_{SS})						
Soft-Start / Soft-Shutdown	I_{SS1}	SOFT = 1.5V	--	20	--	μA
Normal VID Change Slew Current	I_{SS2}	SOFT = 1.5V	40	50	60	μA
Deeper Sleep Exit/VID Change Slew Current	I_{SS3}	For Render Mode Only, SOFT = 1.5V	80	100	120	μA
Reference and DAC						
DC Accuracy	V_{FB}	V_{DAC} = 0.7500 – 1.5000 (No Load, Active Mode)	–0.8	0	0.8	%VID
		V_{DAC} = 0.5000 – 0.7500	–7.5	0	7.5	mV
Boot Voltage	V_{BOOT}	RT8152A	1.089	1.1	1.111	V
		RT8152B	1.188	1.2	1.212	
Error Amplifier						
DC Gain		R_L = 47kΩ	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	--	10	--	MHz
Slew Rate	SR_{COMP}	C_{LOAD} = 10pF (Gain = –4, R_f = 47kΩ, V_{OUT} = 0.5V – 3V)	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V
Maximum Source Current	I_{OUTEA_COMP}	V_{COMP} = 2V	200	250	--	μA
Maximum Sink Current		V_{COMP} = 2V	--	20	--	mA
Current Sense Amplifier						
Input Offset Voltage	V_{OSCS}	I_{SEN} = I_{SEN_N} = 1.5V	–1	--	1	mV
Impedance at Neg. Input	R_{ISEN_N}	I_{SEN_N} = 1.5V	1	--	--	MΩ
Impedance at Pos Input	R_{ISEN}	I_{SEN} = 1.5V	1	--	--	MΩ
DC Gain			--	10	--	V/V
Input Range	V_{ISEN_IN}	V_{DAC} = 1.1V, V_{ISEN_IN} = I_{SEN} - I_{SEN_N}	–50	--	80	mV
TON Setting						
TON Pin Output Voltage	V_{TON}	R_{TON} = 80kΩ, V_{TON} = V_{DAC} = V_{BOOT}	–5	0	5	%
ON-Time Setting	T_{ON}	I_{RTON} = 80μA, V_{TON} = V_{DAC} = V_{BOOT}	--	350	--	ns
R_{TON} Current Range	I_{RTON}	V_{TON} = V_{DAC} = V_{BOOT}	25	--	280	μA
Minimum Off Time	T_{Off}	I_{RTON} = 80μA, V_{DAC} = V_{BOOT}	250	--	500	ns
Protection						
Under Voltage Lock-out Threshold	V_{UVLO}	Falling edge, 80mV Hysteresis	3.9	4.1	4.3	V
Absolute Over Voltage Protection Threshold	V_{OVABS}	(Respect to 1.5V, ± 50mV)	1.45	1.5	1.55	V
Relative Over Voltage Protection Threshold	V_{OV}	(Respect to V_{DAC}, ± 50mV)	250	300	350	mV

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Under Voltage Protection Threshold	V_{UV}	Measured at VSEN respect to unloaded output voltage (UOV) (for 0.8 < UOV < 1.5)	–450	–400	–350	mV
Negative Voltage Protection Threshold	V_{NV}	Measured at VSEN respect to GND	–100	--	--	mV
Current Limit Threshold Voltage	V_{ILIM}	$V_{ISEN} - V_{ISEN\_N} = V_{ILIM}$, V_{OCSET} = 2V, 40 x $V_{ILIM} = V_{OCSET}$	46.5	50	53.5	mV
Thermal Shutdown Threshold	T_{SD}	Typical hysteresis is 10°C	--	160	--	°C
Logic Inputs						
VRON Threshold	V_{IH}	Respect to 3.3V, 70%	2.31	--	--	V
	V_{IL}	Respect to 3.3V, 30%	--	--	0.99	
Leakage Current of VRON			–1	--	1	µA
DAC (VID0 – VID6) and DPRSLPVR	V_{IH}	Respect to 1.1V, 70%	0.77	--	--	V
	V_{IL}	Respect to 1.1V, 30%	--	--	0.33	
Leakage Current of DAC (VID0 – VID6) and DPRSLPVR			–1	--	1	µA
Power Good						
PGOOD Threshold	V_{TH_PGOOD}	CPU Core : VSEN – V_{BOOT}	--	–100	--	mV
		Render : VSEN – V_{DAC}	--	–100	--	
PGOOD Low Voltage	V_{PGOOD}	I_{PGOOD} = 4mA	--	--	0.4	V
PGOOD Delay	T_{PGOOD}	CPU Core, $\overline{CLKEN}$ Low to PGOOD High	3	--	20	ms
		Render Mode VRON High to PGOOD High	3	--	20	
Clock Enable						
$\overline{CLKEN}$ Low Voltage	$V_{\overline{CLKEN}}$	For CPU Core Only, $I_{\overline{CLKEN}}$ = 4mA	--	--	0.4	V
Thermal Throttling						
Thermal Throttling Threshold	V_{OT}	Measure at NTC respect to V_{CC}	--	80	--	%VDD
Thermal Throttling Threshold -Hysteresis	V_{OT_HY}	At V_{CC} = 5V	--	230	--	mV
$\overline{VRTT}$ Output Voltage	$V_{\overline{VRTT}}$	$I_{\overline{VRTT}}$ = 40mA	--	--	0.4	V
Current Monitor						
Current Monitor Output Voltage in Operating Range		V_{DAC} = 0.9V, V_{RCMSET} = 0.82V, R_{CM} = 7.5kΩ, R_{CMSET} = 1.5kΩ	770	800	830	mV
Current Monitor Maximum Output Voltage			--	--	1.15	V
Gate Driver						
Upper Driver Source	$R_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$ = 5V $V_{BOOT} - V_{UGATE}$ = 1V	--	0.7	--	Ω

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Upper Driver Sink	$R_{UGATEsk}$	V_{UGATE} = 1V	--	0.6	--	Ω
Lower Driver Source	$R_{LGATEsr}$	V_{PVDD} = 5V, V_{PVDD} – V_{LGATE} = 1V	--	0.75	--	Ω
Lower Driver Sink	$R_{LGATEsk}$	V_{LGATE} = 1V	--	0.5	--	Ω
Upper Driver Source/Sink Current	I_{UGATE}	V_{BOOT} –V_{PHASE} = 5V V_{UGATE} = 2.5V	--	3	--	A
Lower Driver Source Current	$I_{LGATEsr}$	V_{LGATE} = 2.5V	--	3	--	A
Lower Driver Sink Current	$I_{LGATEsk}$	V_{LGATE} = 2.5V	--	5	--	A
Internal Boot Charging Switch On-Resistance	R_{BOOT}	PVDD to BOOT	--	30	--	Ω

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the package.

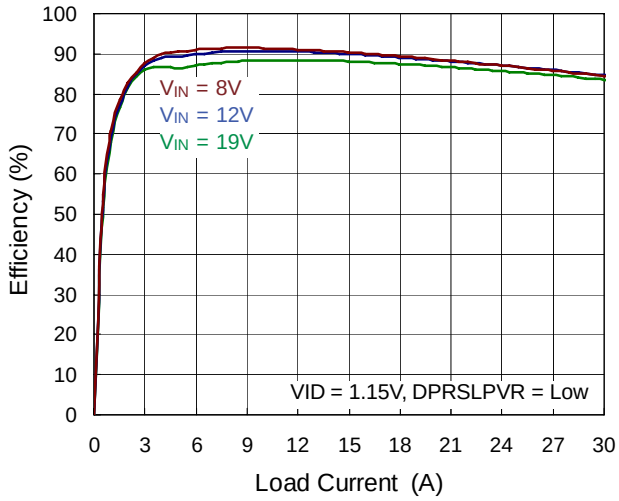
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

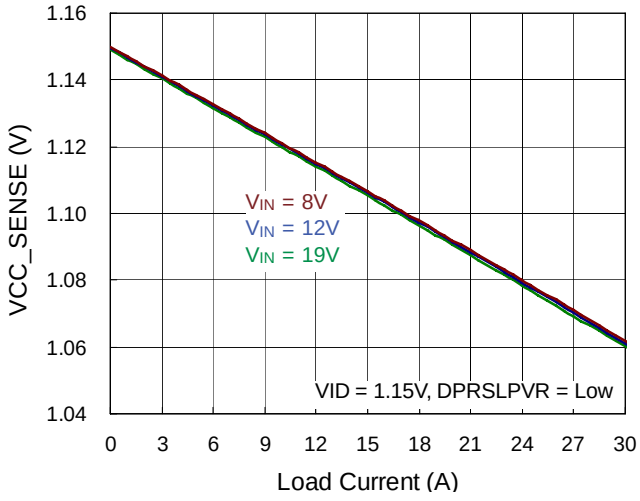
Typical Operating Characteristics

V_{IN} = 12.6V, R_{TON} = 150Ω, L = 0.36µH, C_{OUT} = 330µF, No Load, T_A = 25°C, unless otherwise specified.

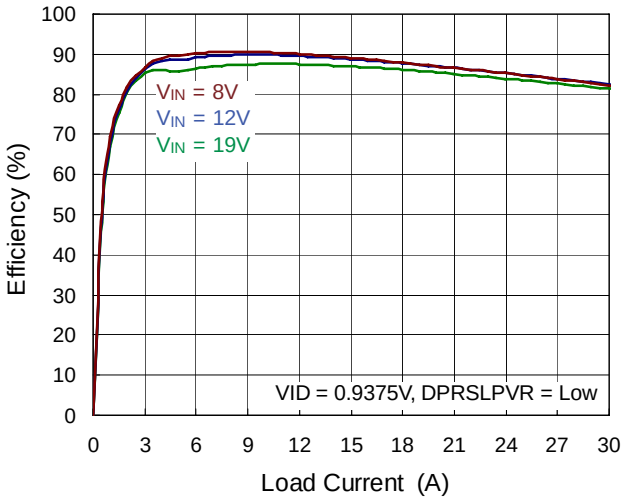
CCM Efficiency vs. Load Current



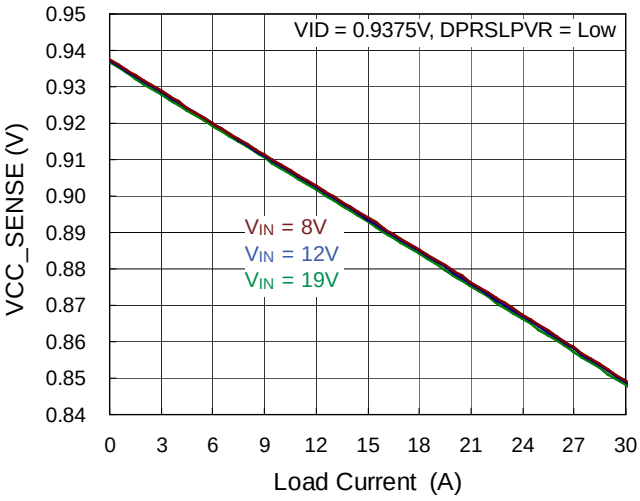
CCM VCC_SENSE vs. Load Current



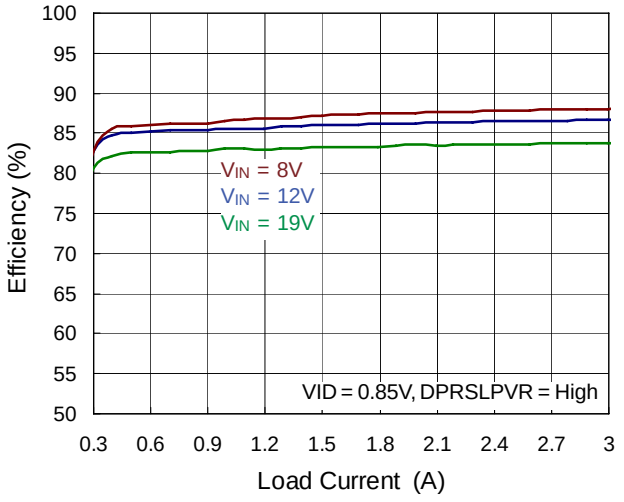
CCM Efficiency vs. Load Current



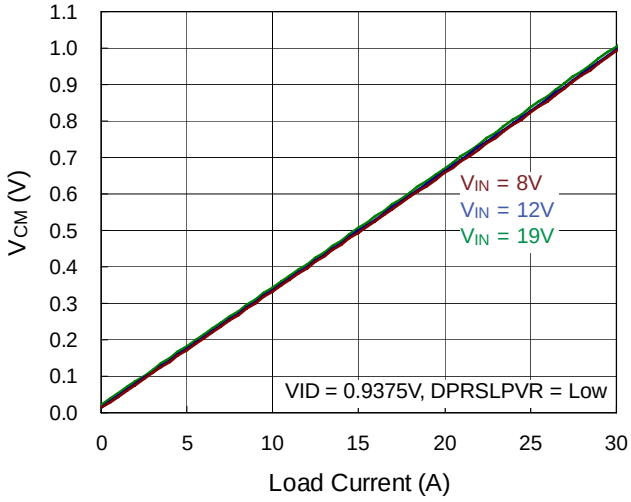
CCM VCC_SENSE vs. Load Current



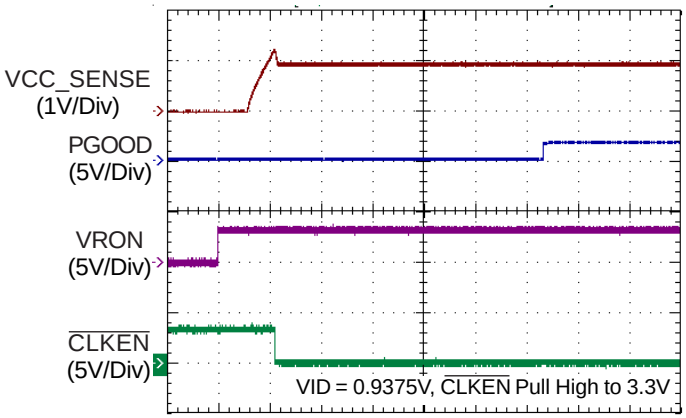
RFM Efficiency vs. Load Current



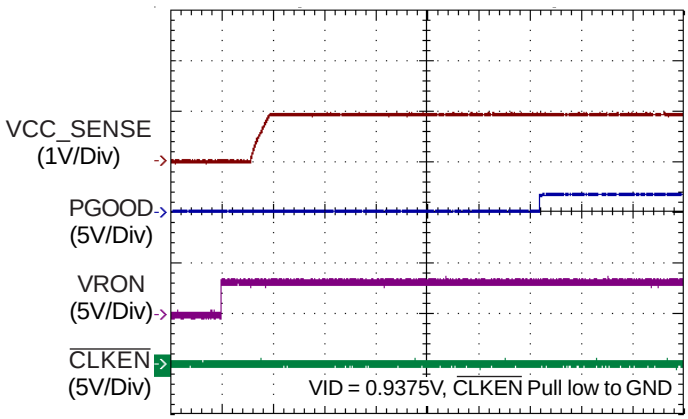
V_{CM} vs. Load Current



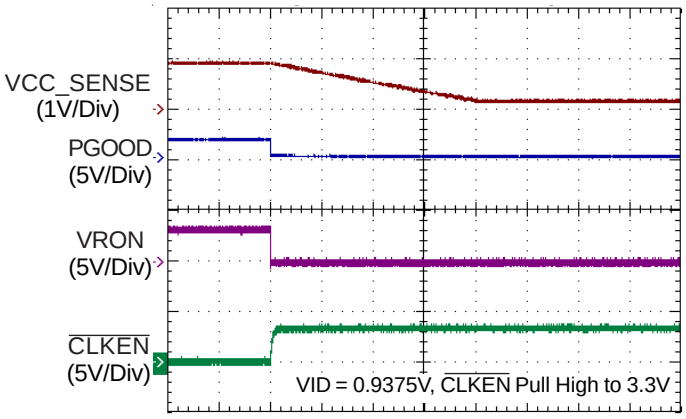
CPU Mode Power On



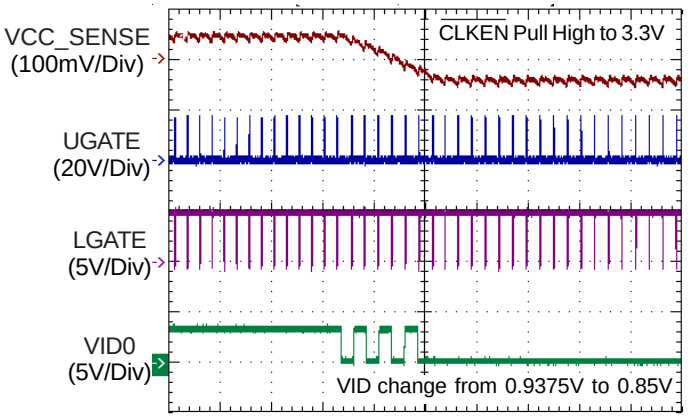
Render Mode Power On



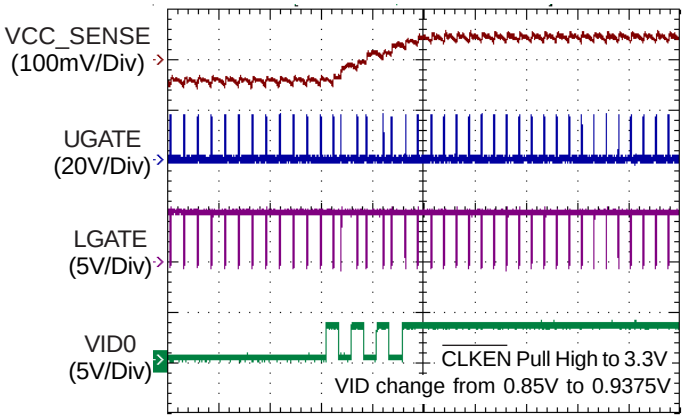
CPU Mode Power Down



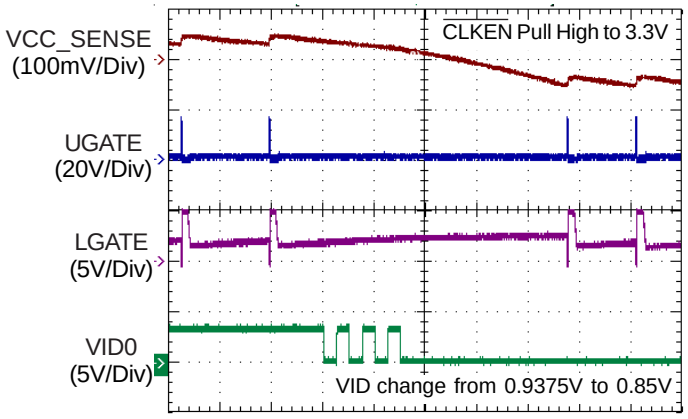
CCM VID Change Down



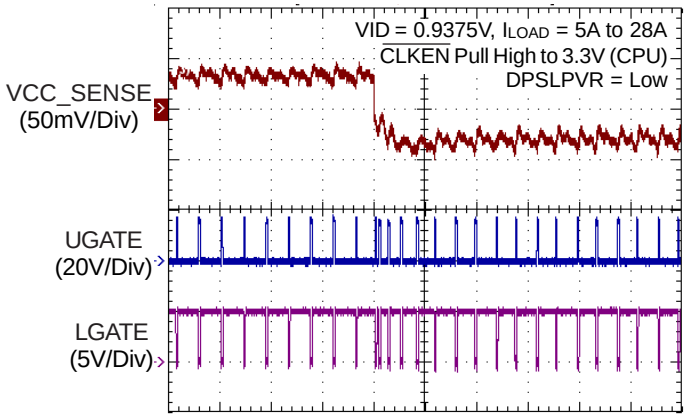
CCM VID Change Up



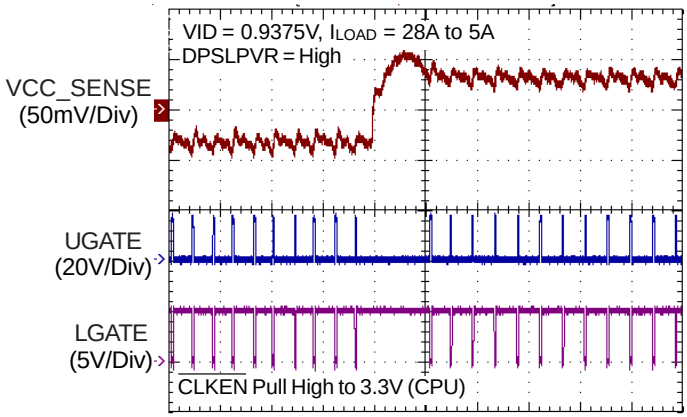
CPU-RFM VID Change Down



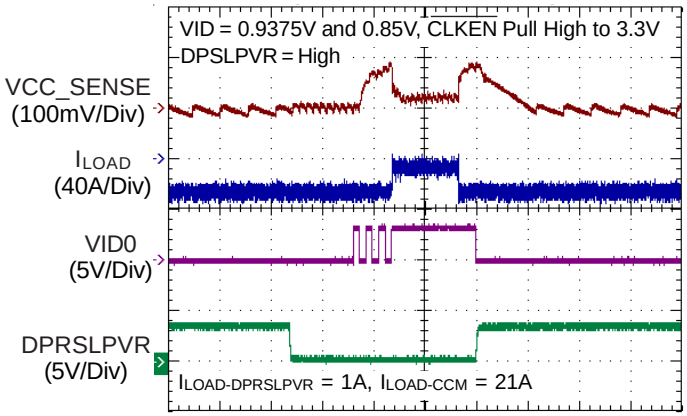
CCM Load Transient Response



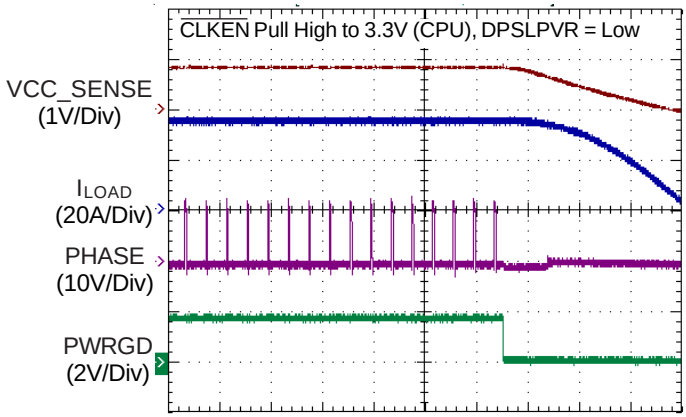
CCM Load Transient Response



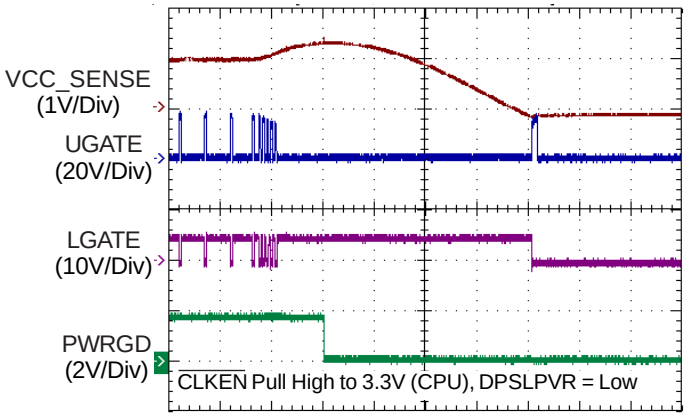
C4 ENTRY / EXIT with VID Change



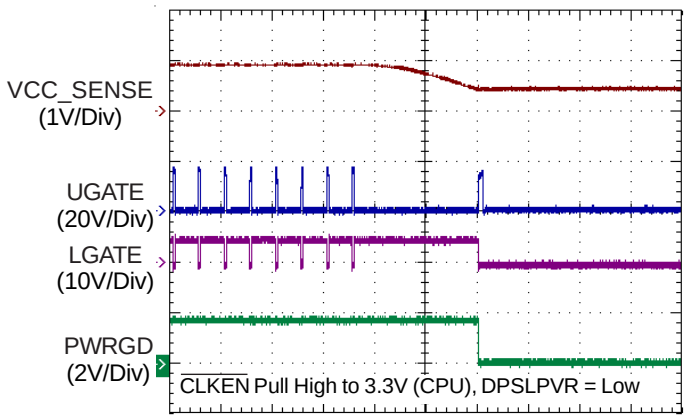
Over Current Protection



Over Voltage Protection



Under Voltage Protection



Application Information

The RT8152A/B is a single-phase PWM controller with embedded gate driver. It is compliant with Intel IMVP6.5 Voltage Regulator Specification to fulfill its mobile CPU and Render voltage regulator power supply requirement. Inductor current are continuously sensed for loop control, droop tuning, and over-current protection. The 7-bit VID DAC and a low offset differential amplifier allow the controller to maintain high regulating accuracy to meet Intel's IMVP6.5 specification.

Design Tool

To help users to reduce the efforts and errors caused by manual calculations using the design concept below, a user-friendly design tool is now available on request.

This design tool calculates all necessary design parameters by entering user's requirements. Please contact Richtek's representatives for details.

Operation Modes

Table 2 shows the RT8152A/B operation modes. When VRON is enable (=1), and within 10μs the RT8152A/B will detect the $\overline{\text{CLKEN}}$ to determine which operation mode is applied. If the $\overline{\text{CLKEN}}$ is low, the RT8152A/B will operate in Render core voltage regulator mode. If the $\overline{\text{CLKEN}}$ is high, the IC will operate in CPU core voltage regulator mode.

DPRSLPVR determines the operation mode of the controller operation in CCM or RFM. The controller enters RFM (Ring Free Mode) when DPRSLPVR = 1 and enters CCM when DPRSLPVR = 0.

Table 2. Control Signal Truth Table for Operation Modes of the RT8152A/B

$\overline{\text{CLKEN}}$	DPRSLPVR	Operation Mode
0 (GND)	0	Render CCM
	1	Render RFM
1 (Pull High)	0	CPU CCM
	1	CPU RFM

Differential Remote Sense Connection

The RT8152A/B includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. CPU contains on-die sense pins V_{CC_SENSE} and V_{SS_SENSE}. Connect RGND to V_{SS_SENSE}. Connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier. Connect VSEN to V_{CC_SENSE} for $\overline{\text{CLKEN}}$, PGOOD, OVP, and UVP detection. The 7 bit VID DAC and the precision voltage reference are referred to RGND for accurate remote sensing.

Current Sense Setting

The RT8152A/B is continuously sensing the inductor current. Therefore, the controller can be less noise sensitive. Low offset amplifiers are used for loop control and over current detection. The internal current sense amplifier gain (A_I) is fixed to be 10. The ISEN and ISEN_N denote the positive and negative input of the current sense amplifier.

Users can either use a current-sense resistor or the inductor's DCR for current sensing. Using inductor's DCR allows higher efficiency as shown in Figure 3. To let

$$\frac{L}{DCR} = R_X \times C_X \quad (1)$$

then the transient performance will be optimum. For example, chose L = 0.36uH with 1mΩ DCR and C_X = 100nF, yields for R_X :

$$R_X = \frac{0.36\mu H}{1m\Omega \times 100nF} = 3.6k\Omega \quad (2)$$

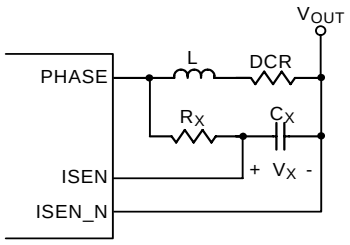


Figure 3. Lossless Inductor Current Sensing

Considering the inductance tolerance, the resistor R_X has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load line requirement with a slow recovery, R_X is chosen too small. Vice versa, with a resistance too large, the output voltage transient has only a small initial dip and the recovery is too fast causing a ring-back.

Using current-sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current-sense resistor, a RC filter is recommended. The RC filter calculation method is similar to the above-mentioned inductor DCR sensing method.

Loop Control

The RT8152A/B adopts Richtek's proprietary G-NAVP™ topology. G-NAVP™ is based on the finite-gain current mode with CCRCOT (Constant Current Ripple Constant On Time) topology. The output voltage, V_{OUT}, will decrease with increasing output load current. The control loop consists of PWM modulator with power stage, current sense amplifier and error amplifier as shown in Figure 4.

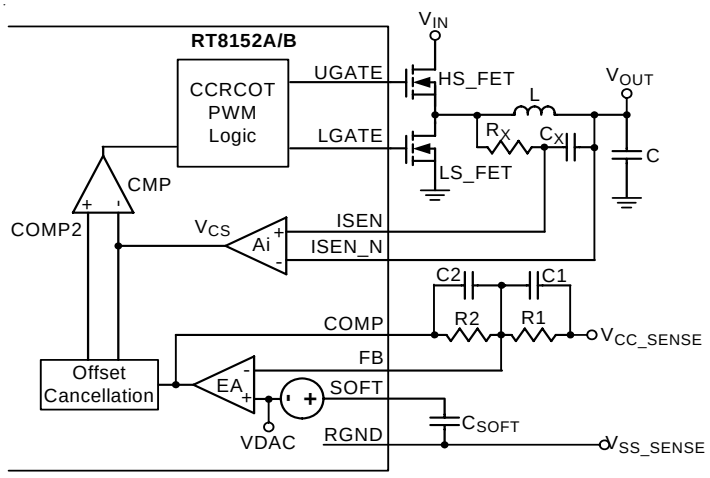


Figure 4. Simplified Schematic for Droop and Remote Sense in CCM

The HS_FET on-time is determined by CCRCOT ON-Time generator. When load current increases, V_{CS} increases, the steady state COMP voltage also increases and makes the V_{OUT} decrease, achieving AVP. A near-DC offset cancellation is added to the output of EA to cancel the inherent output offset of finite-gain current mode controller.

In RFM, HS_FET is turned on with constant T_{ON} when V_{CS} is lower than V_{COMP2}. Once the HS_FET is turned off, LS_FET is turned on automatically. By Ringing-Free Technique, the LS_FET allows only partial of negative current when the inductor free-wheeling current reaches negative. The switching frequency will be proportionately reduced, thus the conduction and switching losses will be greatly reduced.

Output Voltage Droop Setting (with Temperature Compensation)

It's very easy to achieve the Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics. The target is to have

$$V_{OUT} = V_{DAC} - I_{LOAD} \times R_{DROOP} \quad (3)$$

, then solving the switching condition $V_{COMP2} = V_{CS}$ in Figure 4 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{A_I \times R_{SENSE}}{R_{DROOP}} \quad (4)$$

where A_I is the internal current sense amplifier gain. R_{SENSE} is the current sense resistor. If no external sense resistor present, it is the DCR of the inductor. R_{DROOP} is the resistive slope value of the converter output and is the desired static output impedance.

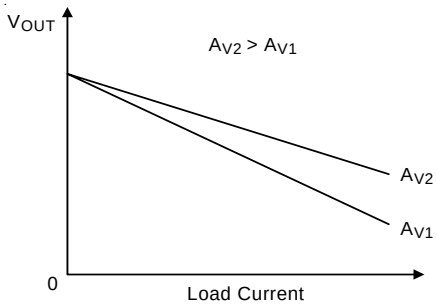


Figure 5. Error Amplifier Gain (Av) Influence on V_{OUT}

Since the DCR of inductor is highly temperature dependent, it affects the output accuracy at hot conditions. Temperature compensation is recommended for the lossless inductor DCR current-sense method. Figure 6 shows a simple but effective way of compensating the temperature variations of the sense resistor using an NTC thermistor placed in the feedback path.

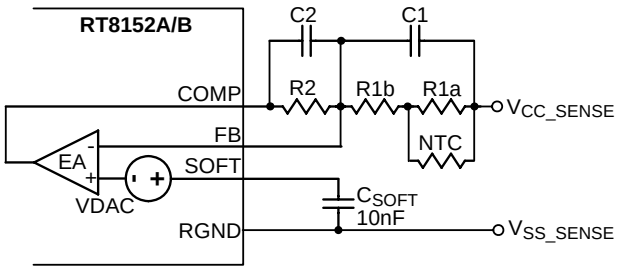


Figure 6. Loop Setting with Temperature Compensation

Usually, R1a is set to equal R_{NTC} (25°C). R1b is selected to linearize the NTC's temperature characteristic. For a given NTC, design is to get R1b and R2 and then C1 and C2. According to (4), to compensate the temperature variations of the sense resistor, the error amplifier gain (Av) should have the same temperature coefficient with R_{SENSE}. Hence

$$\frac{A_{V,\,HOT}}{A_{V,\,COLD}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (5)$$

From (4), we can have Av at any temperature (T) as

$$A_{V,\,T} = \frac{R2}{R1a\,//\,R_{NTC,\,T} + R1b} \quad (6)$$

The standard formula for the resistance of NTC thermistor as a function of temperature is given by :

$$R_{NTC,\,T} = R_{NTC,\,25}\; e^{\left\{\beta\left[\left(\frac{1}{T+273}\right)-\left(\frac{1}{298}\right)\right]\right\}} \quad (7)$$

Where $R_{NTC,\,25}$ is the thermistor's nominal resistance at room temperature, β (beta) is the thermistor's material constant in Kelvins, and T is the thermistor's actual temperature in Celsius.

To calculate DCR value at different temperature can use equation as below :

$$DCR_T = DCR_{25} \text{ x } [1+0.00393 \text{ x } (T-25)] \quad (8)$$

Where the 0.00393 is the temperature coefficient of the copper. For a given NTC thermistor, solving (6) at room temperature (25°C) yields

$$R2 = A_{V,\,25} \text{ x } (R1b + R1a\ //\ R_{NTC,\,25}) \quad (9)$$

Where $A_{V,\,25}$ is the error amplifier gain at room temperature and can be obtained from (4). R1b can be obtained by substituting (9) to (5),

$$R1b = \frac{\frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \times (R1a\,//\,R_{NTC,\,HOT}) - (R1a\,//\,R_{NTC,\,COLD})}{\left(1 - \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}}\right)} \quad (10)$$

Loop Compensation

Optimized compensation of the RT8152A/B allows for best possible load step response of the regulator's output. A compensator with one pole and one zero is adequate for a proper compensation. Figure 4 shows the compensation circuit. Prior design procedure shows how to decide the resistive feedback components of error amplifier gain, the C1 and C2 must be calculated for the compensation. The target is to achieve the constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2 \times \pi \times C \times R_C} \quad (11)$$

Where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2} \quad (12)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching-related noise. Such that,

$$C1 = \frac{1}{(R1b + R1a\,//\,R_{NTC,\,25}) \times \pi \times f_{SW}} \quad (13)$$

TON Setting

High frequency operation optimizes the application for the smaller component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space.Figure 5

shows the On-Time setting circuit. Connect a resistor (R_{TON}) between VIN and TON to set the on-time of UGATE:

$$T_{ON} = \frac{14.5 \times 10^{-12} \times R_{TON} \times 2}{(V_{IN} - VDAC)} \quad (14)$$

Where T_{ON} is UGATE turn on period, V_{IN} is Input voltage of converter, VDAC is DAC voltage.

On-time translate only roughly to switching frequencies. The on-times guaranteed in the Electrical Characteristics are influenced by switching delays in external HS-FET. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in CCM (DPRSLPVR = 0), and during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the PHASE goes high earlier than normal, extending the on-time by a period equal to the HS-FET rising dead time.

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$F_{S(MAX)} = \frac{1}{T_{ON} - T_{HS\text{-}Delay}} \times \frac{VDAC_{(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON\_LS\text{-}FET} + DCR_L - R_{DROOP}\right]}{VIN_{(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON\_LS\text{-}FET} - R_{ON\_HS\text{-}FET}\right]} \quad (15)$$

Where

- Fs_{MAX} is the maximum switching frequency
- $T_{HS\text{-}Delay}$ is the turn on delay of HS-FET
- $VDAC_{(MAX)}$ is the maximum VDAC of application
- VIN_{MAX} is the maximum application Input voltage
- $I_{LOAD(MAX)}$ is the maximum load of application
- $R_{ON\_LS\text{-}FET}$ is the Low side FET $R_{DS(ON)}$
- $R_{ON\_HS\text{-}FET}$ is the High side FET $R_{DS(ON)}$
- DCR_L is the inductor DCR
- R_{DROOP} is the load line setting

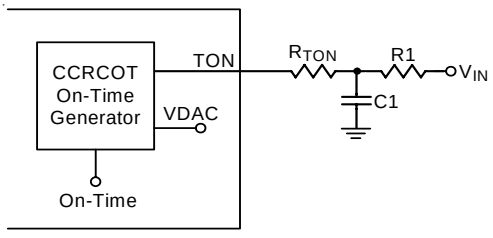


Figure 7. On-Time setting with RC Filter

Soft-Start and Mode Transition Slew Rates

The RT8152A/B uses 3 slew rates for various modes of operation. The three slew rates are internally determined by commanding one of three bi-directional current sources (I_{SS}) on to the SOFT pin. The 7 bit VID DAC and the precision voltage reference are referred to RGND for accurate remote sensing. Hence, connect a capacitor (C_{SOFT}) from SOFT pin to RGND for controlling the slew rate as shown in Figure 6. The capacitance of capacitor is restricted to be larger than 10nF. The voltage (V_{SOFT}) on the SOFT pin is the reference voltage of the error amplifier and is, therefore, the commanded system voltage.

The first current is typically 20μA used to charge or discharge the C_{SOFT} during soft-start, and soft-shutdown. The second current is typically 50μA used during other voltage transitions, including VID change and transitions between operation modes. The third current is typically 100μA used during Render RFM with VID change up transitions.

The IMVP-6.5 specification specifies the critical timing associated with regulating the output voltage. The symbol, SLEWRATE, as given in the IMVP-6.5 specification will determine the choice of the SOFT capacitor, C_{SOFT}, by the following equation :

$$C_{SOFT} = \frac{I_{SS}}{SLEWRATE} \quad (16)$$

Power up Sequence

With the controller's VCC voltage rises above the POR threshold (typ. 4.3V), the power up sequence begins when VRON exceeds the 3.3V logic high threshold. If $\overline{CLKEN}$ = 1 (Pull High), the RT8152A/B will enter CPU mode power up sequence. If the $\overline{CLKEN}$ = 0 (Connect to GND), the controller will enter Render mode power up sequence.

After the RT8152A/B enters CPU mode, VSEN starts ramping up to V_{BOOT} within 1ms. The slew rate during power up is 20μA/C_{SOFT}. The RT8152A/B pulls $\overline{CLKEN}$ low after VSEN gets across V_{BOOT} – 0.1V for 73μs. Right after $\overline{CLKEN}$ goes low, VSEN starts ramping to first VDAC value. After $\overline{CLKEN}$ goes low for approximately 4.7ms, PGOOD is asserted HIGH. DPRSLPVR are valid right after PGOOD is asserted. UVP is masked as long as VSEN is less than V_{BOOT} – 0.1V.

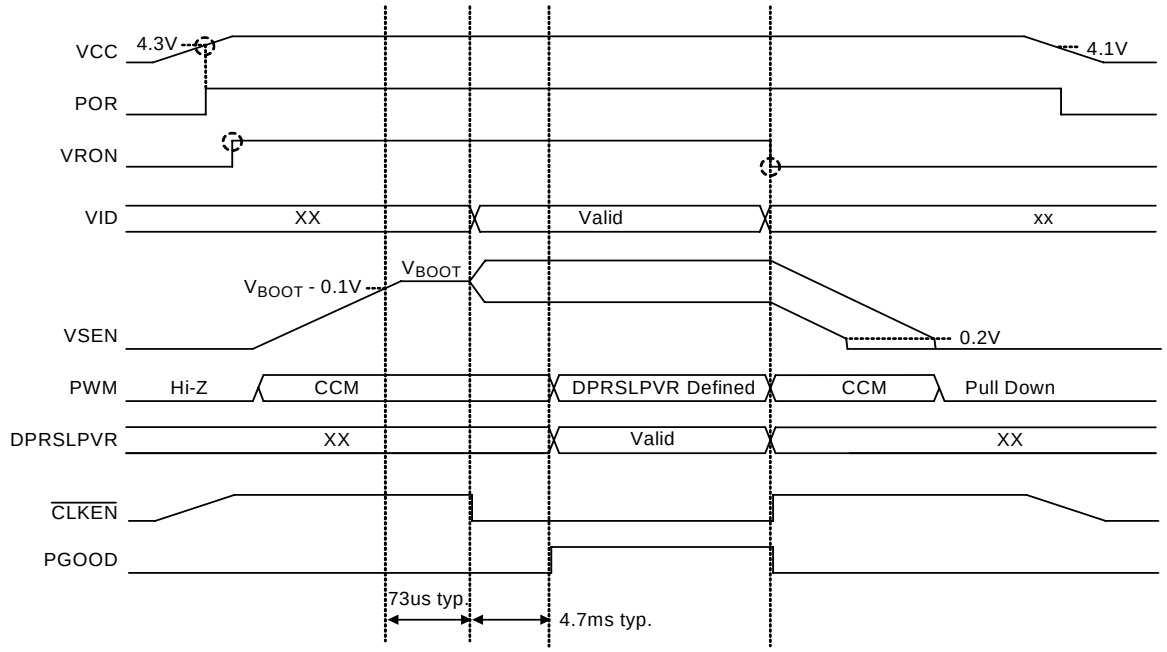


Figure 8. CPU Mode Timing Diagram for Power Up and Power Down

After the RT8152A/B enters Render mode, VSEN starts ramping up to VDAC within 1ms. The slew rate during power up is 20μA/C_{SOFT}. PGOOD is asserted HIGH after VSEN exceeds VDAC – 100mV for 4.77ms (typ.). DPRSLPVR are valid right after PGOOD is asserted. UVP is masked as long as VSEN is less than VDAC – 100mV.

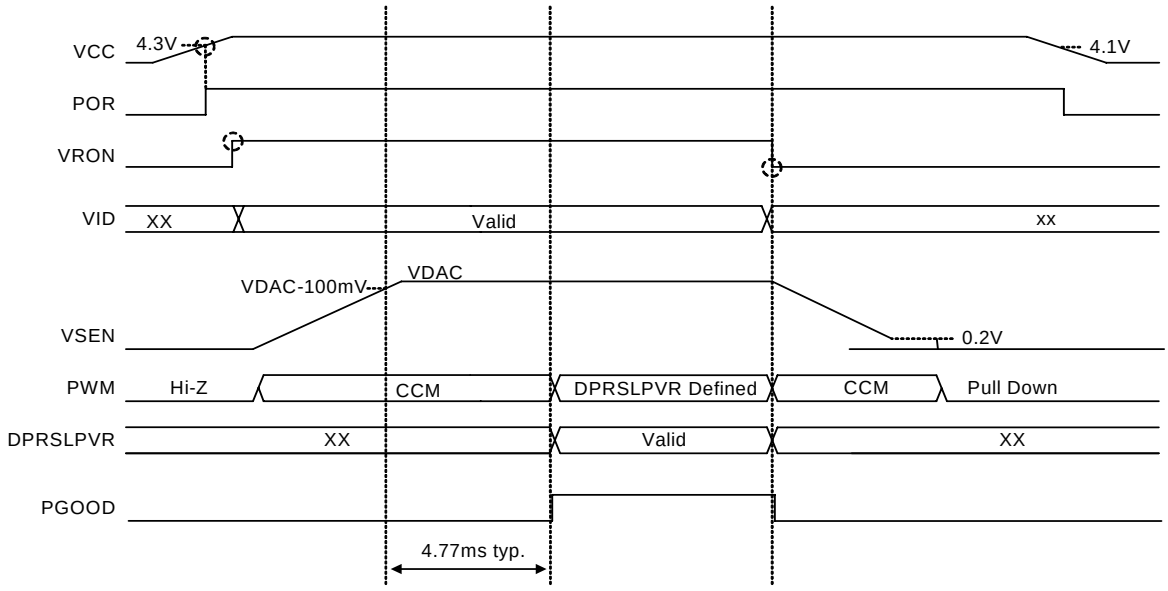


Figure 9. Render Mode Timing Diagram for Power Up and Power Down

Power Down

When VRON goes low, the RT8152A/B enters low-power shutdown mode. PGOOD is pulled low immediately and the V_{SOFT} ramps down with slew rate of 20μA/C_{SOFT}. VSEN also ramps down following V_{SOFT}. After V_{VSEN} is lower than 200mV, the RT8152A/B turns off high side FETs and low side FETs. An internal discharge resistor at VSEN will be enabled and the analog part will be turned off.

Deeper Sleep Mode Transitions

After DPRSLPVR goes high, the RT8152A/B enters deeper sleep mode operation. If the VIDs are set to a lower voltage setting, the output drops at a rate determined by the load and the output capacitance. The internal target V_{SOFT} still ramps as before, and UVP, OCP and OVP are masked for 73μs.

Over Current Protection Setting

The RT8152A/B compares a programmable current limit set point to the voltage from the current sense amplifier output for over current protection (OCP). The voltage applied to OCSET pin defines the desired current limit threshold I_{LIM} :

$$V_{OCSET} = 40 \times I_{LIM} \times R_{SENSE} \quad (17)$$

Connect a resistor voltage divider from VCC to GND, the joint of the resistor divider is connected to OCSET pin as shown in Figure 10. For a given R_{OC2}, then

$$R_{OC1} = R_{OC2} \times \left(\frac{V_{CC}}{V_{OCSET}} - 1 \right) \quad (18)$$

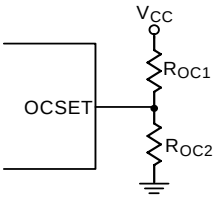


Figure 10. OCP Setting Without Temperature Compensation

RT8152A/B provides current limit function and over current protection. The current limit function is triggered when inductor current exceeds the current limit threshold I_{LIM} defined by V_{OCSET}. When current limit function is tripped, high side MOSFET will be forced off until the over current condition is cleared.

If the current limit function is triggered for 15 switching cycles, OCP will be tripped. Once OCP is tripped, both high side and low side MOSFET will be turn off, and the internal discharge resistor at the VSEN pin will be enabled to discharge output capacitors. OCP is a latched protection, it can only be reset by cycling VRON or VCC.

If inductor DCR is used as current sense component, then temperature compensation is recommended for proper protection under all conditions. Figure 11 shows a typical OCP setting with temperature compensation.

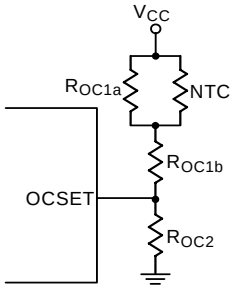


Figure 11. OCP Setting with Temperature Compensation

Generally, the R_{OC1a} must be selected to be equal to thermistor's nominal resistance at room temperature. Ideally, V_{OCSET} has same temperature coefficient with R_{SENSE} (Inductor DCR) :

$$\frac{V_{OCSET,\,HOT}}{V_{OCSET,\,COLD}} = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} \quad (19)$$

$$R_{OC2} = \frac{\alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD} + (1-\alpha) \times R_{EQU,\,25}}{\frac{V_{CC}}{V_{OCSET,\,25}} \times (1-\alpha)} \quad (20)$$

$$R_{OC1b} = \frac{(\alpha - 1) \times R_{OC2} + \alpha \times R_{EQU,\,HOT} - R_{EQU,\,COLD}}{(1-\alpha)} \quad (21)$$

Where

$$\alpha = \frac{R_{SENSE,\,HOT}}{R_{SENSE,\,COLD}} = \frac{DCR_{25} \times [1 + 0.00393 \times (T_{HOT} - 25)]}{DCR_{25} \times [1 + 0.00393 \times (T_{COLD} - 25)]} \quad (22)$$

$$R_{EQU,\,T} = R1a \;//\; R_{NTC,\,T} \quad (23)$$

For example, the following design parameters are given :

DCR = 1mΩ, V_{CC} = 5V, $I_{L,ripple}$ = 9A

R_{OC1a} = $R_{NTC,\ 25}$ = 10kΩ, β_{NTC} = 3450

For –20°C to 100°C operation range, to set OCP trip current I_{TRIP} = 28A

$$I_{LIM} = 28A + \frac{9A}{2} = 32.5A$$

$$V_{OCSET,\ 25} = 40 \times 33A \times 1m\Omega = 1.297V$$

$R_{NTC,\ -20°C}$ = 78.4kΩ, $R_{NTC,100°C}$ = 0.98kΩ

$R_{SENSE,-20°C}$ = 0.82mΩ, $R_{SENSE,100°C}$ = 1.29mΩ

$\Rightarrow$ R_{OC2} = 4.7kΩ, R_{OC1b} = 8.46 kΩ

Over Voltage Protection (OVP)

The OVP circuit is triggered under two conditions:

- Condition 1 : When V_{VSEN} exceeds 1.52V.
- Condition 2 : When V_{VSEN} exceeds V_{DAC} by 300mV (typ.).

If either condition is valid, the RT8152A/B latches the LGATE = 1 and UGATE = 0 as crowbar to the output voltage of VR. Turn on all LS_FETs can lead to very large reverse inductor current and potentially result in negative output voltage of VR. To prevent the CPU from damaging by negative voltage. The RT8152A/B turns off all LS_FETs when V_{VSEN} falls below –100mV.

Under Voltage Protection (UVP)

If V_{VSEN} is lower than V_{DAC} by 400mV (typ.) a UVP fault will be tripped. Once UVP is tripped, both high side and low side MOSFET will be turned off, and the internal discharge resistor at VSEN pin will be enabled. UVP is a latched protection, it can only be reset by cycling VRON or VCC.

Negative Voltage Protection (NVP)

During the state that V_{VSEN} is lower than –100mV, the controller will force LGATE = 0 and UGATE = 0 for preventing negative voltage. Once V_{VSEN} recovers to be higher than 0V, NVP will be suspended and LGATE = 1 will be enabled again.

Over Temperature Protection (OTP)

Over-Temperature Protection prevents the VR from damaging. OTP is considered to be the final protection stage against overheating of the VR. The thermal throttling $\overline{VRTT}$ shall be set to be asserted prior to OTP to manage the VR power. When this measure was insufficient to keep the die temperature of the controller below the OTP threshold, OTP will be asserted and latches. The die temperature of the controller is monitored internally by a temperature sensor. As a result of OTP triggering, a soft shutdown will be launched and V_{VSEN} will be monitored. When V_{VSEN} is less than 200mV, the driver remains in high impedance state and the discharging resistor at VSEN pin will be enabled. A reset can be executed by cycling VCC or VRON.

Thermal Throttling Control

Intel IMVP-6.5 technology supports thermal throttling of the processor to prevent catastrophic thermal damage. The RT8152A/B includes a thermal monitoring circuit to detect an exceeded user-defined temperature on a VR point. The thermal monitoring circuit senses the voltage change across NTC pin. Figure 12 shows the principle of setting the temperature threshold. Connect an external resistor divider between Vcc and GND. This divider uses a negative temperature coefficient (NTC) thermistor and a resistor. The joint of the resistor divider is connected to the NTC pin in order to generate a voltage that is inversely proportional to temperature. The RT8152A/B pulls $\overline{VRTT}$ low if the voltage on the NTC pin is greater than 0.8 x V_{CC}. The internal $\overline{VRTT}$ comparator has a hysteresis of 200mV (typ.) to prevent high frequency $\overline{VRTT}$ oscillation when the temperature is near the setting point. The minimum assertion/de-assertion time for $\overline{VRTT}$ toggling is 1.6ms (typ.).

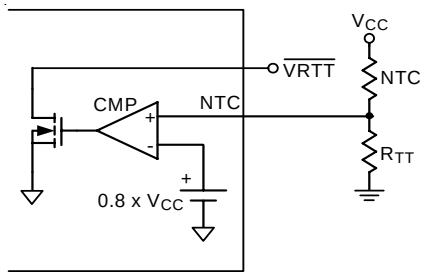


Figure 12. Thermal Throttling Setting Principle

Users can use the same NTC thermistor for both thermal-throttling and current limit setting as shown in Figure 13. Just divide the R_{OC1b} into R_{TTa} and R_{TTb}, and write the V_{NTC} equation at thermal-throttling temperature TT°C :

$$R_{TTa} + R_{TTb} = R_{OC1b} \quad (24)$$

$$\frac{R_{OC2} + R_{TTb}}{R_{OC2} + R_{OC1b} + R_{OC1a} // R_{NTC,\,TT}} \times V_{CC} = 0.8 \times V_{CC} \quad (25)$$

Solving (27) and (28) for R_{TTa} and R_{TTb} as:

$$R_{TTb} = 4 \text{ x } (R_{OC1a} // R_{NTC,\,TT}) - R_{OC2} \quad (26)$$

$$R_{TTa} = R_{OC1b} - R_{TTb} \quad (27)$$

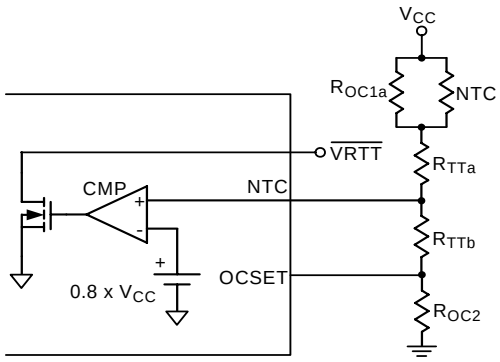


Figure 13. Using Single NTC Thermistor for Thermal-Throttling and Current Limit Setting

Current Monitor

Figure 14 shows the current monitor setting principle. Current monitor needs to meet IMVP6.5 specification, the RT8152A/B is based on the relation between R_{DROOP} and load current to provide an easily setting and high accuracy current monitor indicator.

The current monitor indication voltage V_{CM} equation is shown as :

$$V_{CM} = \frac{2 \times I_{LOAD} \times R_{DROOP} \times R_{CM}}{R_{CMSET}} \quad (28)$$

Where I_{LOAD} is the output load current, R_{DROOP} is the load line setting of applications, R_{CM} and R_{CMSET} is the current monitor current setting resistor.

To find R_{CM} and R_{CMSET} base on :

$$\frac{R_{CM}}{R_{CMSET}} = \frac{V_{CM(MAX)}}{2 \times I_{(MAX)} \times R_{DROOP}} \quad (29)$$

The $V_{CM(MAX)}$ must be kept equal to 1V, $I_{(MAX)}$ is needed to follow the setting current of the IMVP6.5 definition with various CPU. The R_{DROOP} is the load line setting of applications. The $V_{CM(MAX)}$ is clamped not higher than 1.15V.

There is a example for current monitor, the following design parameters are given :

$I_{(MAX)}$ = 30A, R_{DROOP} = 3mΩ,

$V_{CM(MAX)}$ = 1V, R_{CMSET} = 10kΩ

$\Rightarrow$ R_{CM} = 55.6kΩ

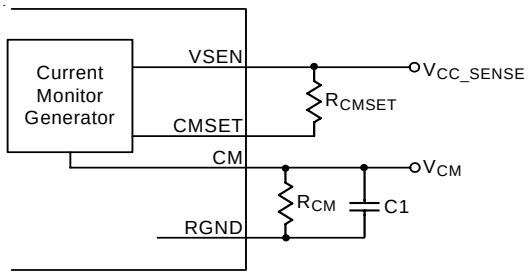


Figure 14. Current Monitor Setting Principle

Inductor Selection

The switching frequency and ripple current determine the inductor value as follows :

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{I_{Ripple-MAX}} \times T_{ON} \quad (30)$$

where T_{ON} is the UGATE turn on period.

Higher inductance yields in less ripple current and hence in higher efficiency. The flaw is the slower transient response of the power stage to load transients. This might increase the need for more output capacitors driving the cost up. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to be saturated at the peak inductor current.

Output Capacitor Selection

Output capacitors are used to obtain high bandwidth for the output voltage beyond the bandwidth of the converter itself. Usually, the CPU manufacturer recommends a capacitor configuration. Two different kinds of output capacitors can be found including, bulk capacitors closely located to the inductors and ceramic output capacitors in

close proximity to the load. Latter ones are for mid-frequency decoupling with especially small ESR and ESL values while the bulk capacitors have to provide enough stored energy to overcome the low-frequency bandwidth gap between the regulator and the CPU.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8152A/B, The maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-32L 5x5 package, the thermal resistance θ_{JA} is 36°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (12°C – 25°C) / (36°C/W) = 2.778W for WQFN-32L 5x5 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8152A/B package, the Figure 15 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

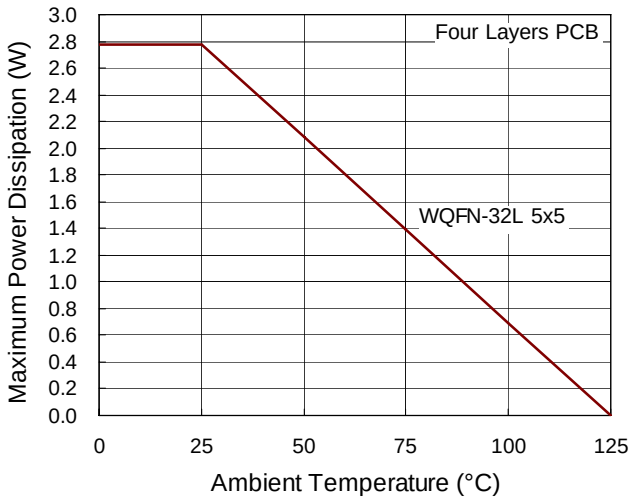


Figure 15. Derating Curve for RT8152A/B Package

Layout Considerations

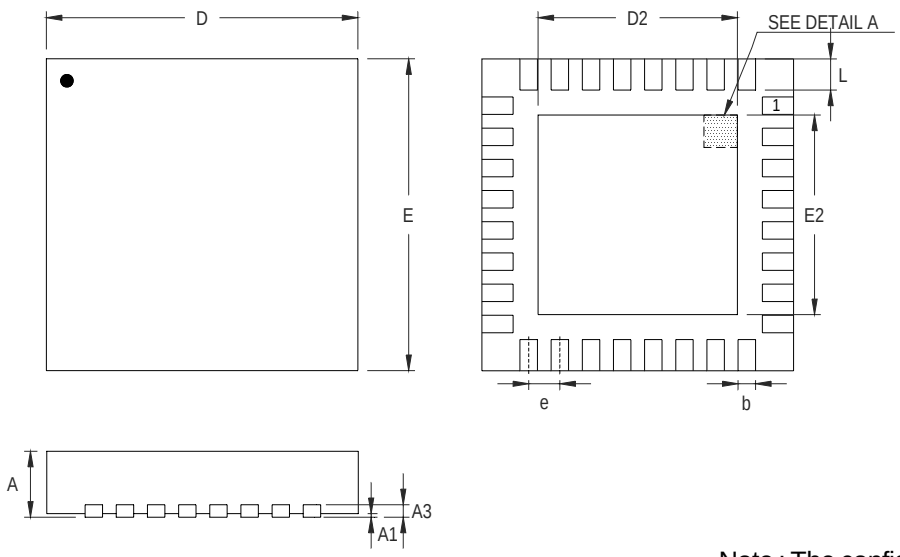
Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for optimum PC board layout :

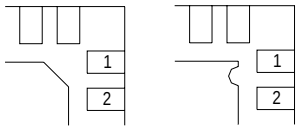
- Keep the high-current paths short, especially at the ground terminals.
- Keep the power traces and load connections short. This is essential for high efficiency.
- The slew rate control capacitor should be connected from SOFT to RGND, and it should be placed physically close to IC.

Connect slew-rate control capacitor at SOFT pin to RGND.

- When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharging path.
- Place the current sense component close to the controller. ISEN and ISEN_N connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee the current sense accuracy. The PCB trace from the sense nodes should be parallel back to controller.
- Route high-speed switching nodes away from sensitive analog areas (SOFT, COMP, FB, VSEN, ISEN, ISEN_N, CM, etc...)

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 32L QFN 5x5 Package

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