Single Phase Synchronous Rectified Buck MOSFET Driver

General Description

The RT9614A is a dual N-Channel MOSFETs driver for synchronous-rectified buck converter. Besides, the power switch is already integrated in this driver to replace external bootstrap diode for reducing system cost and complexity, while allowing the use of higher performance MOSFETs.

The RT9614A is a high performance driver that is capable to drive high/low-side MOSFETs with high speed switching frequency and consuming few of power dissipation. Besides, the operating voltage matches the 30V breakdown voltage of the MOSFET which makes the applications of the RT9614A are more flexible and extensive.

The RT9614A features 4.5V to 13.2V gate driver voltage provided by VCC pin. Further, the RT9614A offers around 30ns propagation delay time for high/low side MOSFETs and 1.1&! sink impedance on low-side gate driver to ensure no shoot-through power loss caused by high dV/dt phase node transitions. By using RT9614A. MOSFET gates can be efficiently switched up to 1MHz and the gate drivers have the capability to drive up to 3nF load. Hence, the RT9614A suits to variety of high-input voltage, high-current and single or multi-phase DC to DC converter applications, such as CPcore voltage and VGA suppliers.

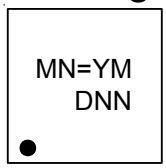
Features

- **Shoot Through Protection**
- **Embedded Bootstrap Diode**
- **Up to 500kHz Operating Frequency**
- **Fast Rising and Falling Time**
- **Tri-State PWM Input**
- **Enable Control**
- **Pre-OVP Protection**
- **8-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Desktop, Systems
- VGA Card

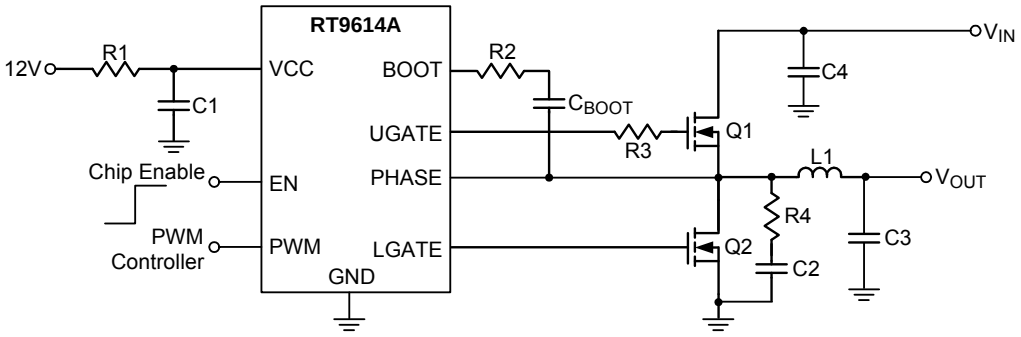
Marking Information



MN= : Product Code

YMDNN : Date Code

Simplified Application Circuit



Ordering Information

RT9614A □□

- Package Type
  QW : WDFN-8L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

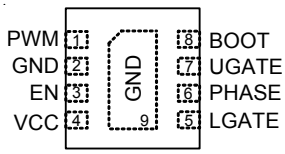
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)

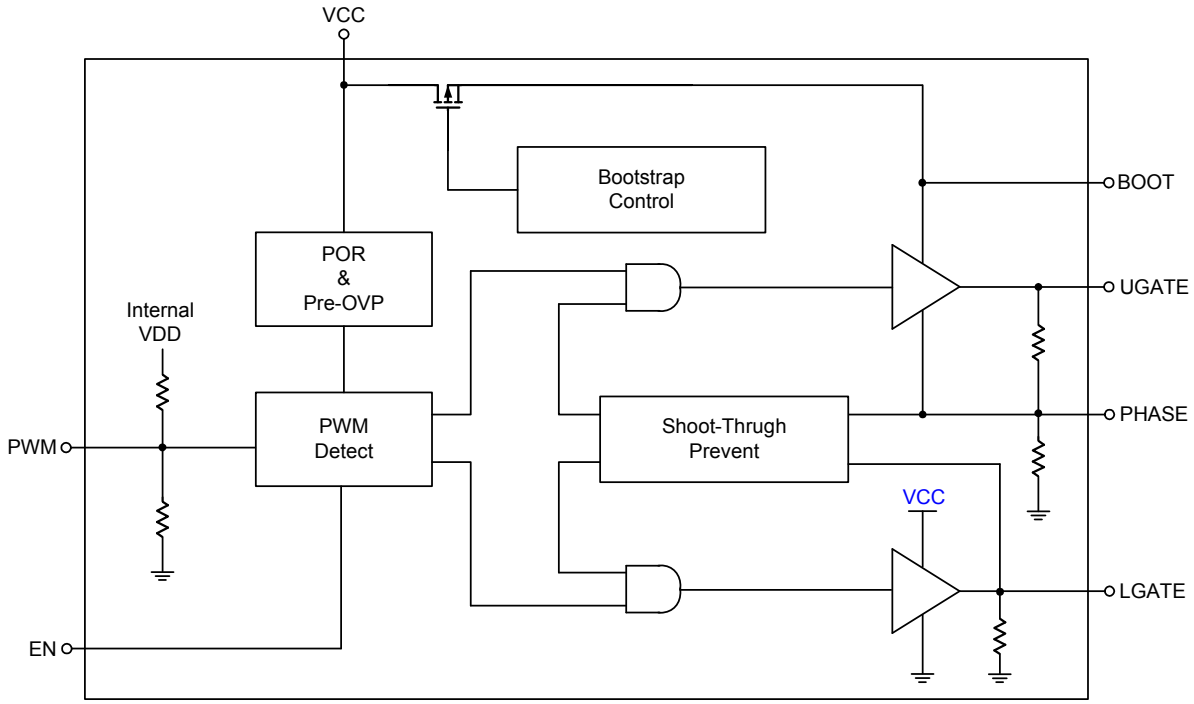


WDFN-8L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PWM	The PWM signal input pin. The external PWM signal determines the both UGATE and LGATE signals. Essentially, UGATE signal is complementary to LGATE signal. If the PWM signal is operated at tri-state voltage, both of UGATE and LGATE signals are turned off.
2, 9 (Exposed Pad)	GND	Ground pin. All signals are referenced to this pin.
3	EN	Enable control input pin (Active High). If the voltage of EN pin rises higher than its threshold, the RT9614A is ready to work and the UGATE/LGATE is ready to be controlled. If the voltage of EN pin falls below its falling threshold, the RT9614A is shut down.
4	VCC	Supply voltage input pin. The VCC supplies power to the analog circuit of RT9614A and the gate drivers. Place a bypass capacitor from this pin to GND for noise immunity.
5	LGATE	Low-side gate driver output pin. Connect this pin to the gate of low-side MOSFET. Notice, DO NOT connect the resistor R_{G_EXT} between LGATE and gate terminal of low-side MOSFET, otherwise it might cause undesired shoot-through since the LGATE voltage is monitored for shoot-through protection.
6	PHASE	Connect this pin to the source of the high-side MOSFET and the drain of the low side MOSFET. This pin provides the driving path of high-side driver. Moreover, the PHASE pin is utilized to implement with Pre-OVP and shoot-through protection.
7	UGATE	High-side gate driver output pin. Connect this pin to the gate of high-side MOSFET.
8	BOOT	Supply bootstrap capacitor output pin. The bootstrap capacitor is charged by this pin while the low-side MOSFET is turned on. Therefore, the bootstrap capacitor can provide the energy to turn on the high-side MOSFET. Connect this pin through the bootstrap capacitor to the PHASE pin.

Functional Block Diagram



Operation

Supply Voltage

The RT9614A can be utilized under VCC=5V or VCC=12V for different application fields, such as NB or desktop. The higher VCC means the higher driving voltage on UGATE and LGATE. In term of efficiency, the higher driving voltage leads to higher driver loss. However, the higher VCC benefits lower conduction loss on MOSFET. Hence, the choice of VCC=12V or 5V is a tradeoff to optimize the system efficiency.

POR

For preventing external MOSFET turned on as VCC is insufficient to drive the gate drivers, the RT9614A implements a POR circuit to keep the driver disable and external high/low-side MOSFETs in an off-state. During power on period, both gate drivers remain low status till VCC reaches to POR rising threshold, typical 4V. As VCC is above POR rising threshold and EN is in high status, the gate drivers are set by PWM input signal. During power off period, VCC falling, POR falling threshold is set to 3.5V (typ.). There is 500mV hysteresis region for preventing VCC raising or falling with very slow slew rate that might be miss-trigger gate drivers.

PWM Operation Principle

As the EN pin is in high status and VCC is over POR rising threshold, the gate drive outputs are defined by the PWM input. Referring to PWM timing diagram as shown in Figure 1, at the period of rising edge of PWM signal, the LAGET is forced to turn low and the non-overlap circuit starts to monitor LGATE voltage level. Once the LGATE is lower than 1.1V, the UGATE is turned on after propagation delay time. The same concept is also used in LGATE turn-on status. In the falling edge of PWM signal, the UGATE is turned off and voltage levels between UGATE and PHASE are monitored. If either of PHASE or UGATE-PHASE is lower than 1.1V, LGATE is turned on after propagation delay time for preventing shoot-through current event.

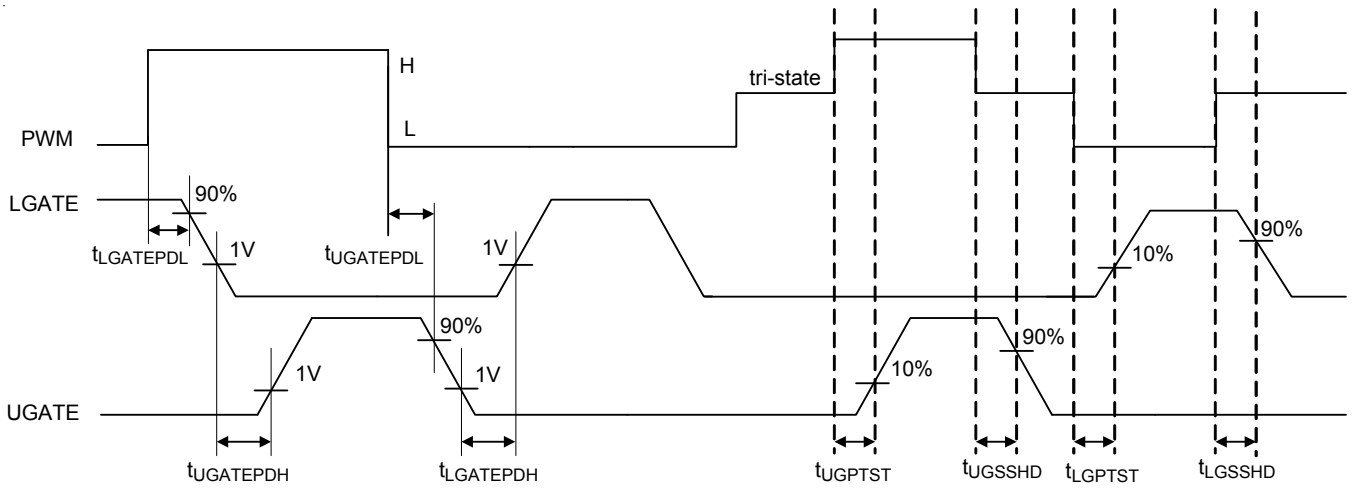


Figure 1. PWM Timing Diagram

Tri-state PWM Input

When PWM signal enters and remains within the tri-state window, the output drivers are disabled and both MOSFET gates are pulled and held low. Once PWM signal leaves the tri-state window, the shutdown state of output drivers is removed. If the PWM signal is left floating, the pin is kept around 1.8V by the internal divider and provide the PWM controller with a recognizable level.

Table 1 lists the logic of EN, PWM, LGATE and UGATE signals

Table 1. Logic of EN, PWM, LGATE and UGATE Signals

EN	PWM	LGATE	UGATE
Low	High or Low	Low	Low
High	Low	High	Low
High	High	Low	High
High	Tri-state	Low	Low

Bootstrap Control

For saving more high-side conduction loss, the voltage of BOOT-PHASE has to close to sourcing voltage VCC. Therefore, the diode of conventional bootstrap circuit is replaced by FET switch, featuring very low drop voltage, in RT9614A that is triggered by LGATE signal. Hence, the bootstrap capacitor is charged by VCC through low-side MOSFET turned on, and V_{CBOOT} is approximately equal to VCC.

Enable and Disable

The RT9614A includes an EN pin for sequence control (independent control). If the voltage of EN pin rises above rising threshold, 1.3V typical, the both UGATE and LGATE are enabled and defined by PWM signal. On the contrary, the RT9614A is shut down when the voltage of EN pin falls below its falling threshold.

Pre-Overvoltage Protection

For preventing any pre-bias voltage on output or short circuit across the high-side MOSFET before EN high, RT9614A applies a PREOVP function on PHASE pin. Before EN high status, PHASE pin voltage is monitored. If PHASE voltage is higher than PREOVP threshold, 2.7V minimum, LAGET is forced to pull high to discharged PHASE voltage. The coming Figure 2 shows the PREOVP operation principle during power-on period.

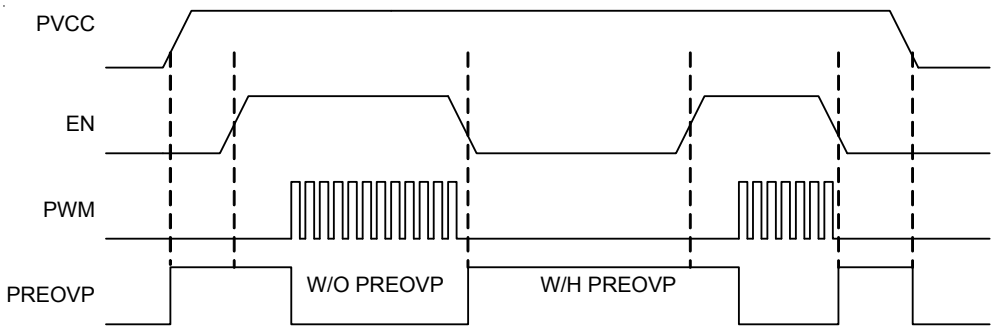


Figure 2. PREOVP Operation Principle

- PREOVP threshold

  2.7V < PREOVP threshold <3V

- Must follow the power-on sequence

  VCC>VCC_{POR_max} is earlier than EN>EN_{rising}

- Driver should connect to Controller

Driver EN connects to controller DRVEN. In this way, PREOVP can normally work in start-up and PS4.

Shoot-through Protection

To prevent overlap between UGATE and LGATE causing additional power losses or circuit damage, the non-overlap circuit is implemented in RT9614A. During the falling edge of PWM signal, UGATE begins to pull low (after propagation delay), and the non-overlap circuit monitors the voltages at the PHASE node, UGATE nodes (UGATE-PHASE). Before LGATE is pulled high, the non-overlap protection circuit ensures that the monitored voltages have been below 1.1V for shoot-through protection. Once the monitored voltage is lower than 1.1V, LGATE begins to turn high after propagation delay time finished. On the other hand, for avoiding shoot-through happening within rising edge of PWM signal, as PWM begins pulling high, LGATE is turned off. Further, the non-overlap circuit starts monitoring the LGATE node voltage. If the LAGET is indeed lower than 1.1V, UGATE is turned on after propagation delay time finished.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VCC ---------- –0.3V to 15V
- BOOT to PHASE ---------- –0.3V to 15V
- PHASE to GND
  - DC ---------- –0.3V to 30V
  - < 100ns ---------- –10V to 35V
- LGATE to GND
  - DC ---------- –0.3V to (VCC + 0.3V)
  - < 100ns ---------- –2V to (VCC + 0.3V)
- UGATE to GND
  - DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - < 100ns ---------- (V_{PHASE} – 2V) to (V_{BOOT} + 0.3V)
- EN, PWM to GND ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-8L 3x3 ---------- 3.22W
- Package Thermal Resistance (Note 2)
  - WDFN-8L 3x3, θ_{JA} ---------- 31°C/W
  - WDFN-8L 3x3, θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 1.5kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 4.5V to 13.2V
- Input Voltage, (V_{IN} + VCC) ---------- < 35V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Power Supply Voltage	V_{CC}		4.5	--	13.2	V
Power Supply Current	I_{VCC}	V_{BOOT} = 12V, PWM input floating	--	120	--	μA
Power On Reset (POR)						
POR Rising Threshold	V_{POR_R}	V_{CC} rising	--	4	4.4	V
POR Falling Threshold	V_{POR_F}	V_{CC} falling	3	3.5	--	V
EN Input						
EN Rising Threshold	V_{ENH}		--	1.3	1.6	V
EN Falling Threshold	V_{ENL}		0.7	1	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Input						
Maximum Input Current	I_{PWM}	PWM = 0V or 5V	--	160	--	μA
PWM Floating Voltage	V_{PWM_FL}	PWM = open	--	1.8	--	V
PWM Rising Threshold	V_{PWM_Rth}		2.3	2.8	3.2	V
PWM Falling Threshold	V_{PWM_FTH}		0.7	1.1	1.4	V
Timing						
UGATE Rising Time	t_{UGATER}	3nF load	--	25	--	ns
UGATE Falling Time	t_{UGATEF}	3nF load	--	12	--	ns
LGATE Rising Time	t_{LGATER}	3nF load	--	24	--	ns
LGATE Falling Time	t_{LGATEF}	3nF load	--	10	--	ns
UGATE Propagation Delay	$t_{UGATEPDH}$	$V_{BOOT} - V_{PHASE}$ = 12V see timing diagram	--	35	--	ns
	$t_{UGATEPDL}$		--	22	--	
LGATE Propagation Delay	$t_{LGATEPDH}$	See timing diagram	--	30	--	ns
	$t_{LGATEPDL}$	See timing diagram	--	8	--	
EN to PWM Delay	$t_{ENTOPWMDL}$		--	3	--	ns
Tri-State to High Delay	t_{UGPTST}		--	30	--	ns
High to Tri-State Delay	t_{UGSSHD}		--	20	--	ns
Tri-State to Low Delay	t_{LGPTST}		--	42	--	ns
Low to Tri-State Delay	t_{LGSSHD}		--	15	--	ns
Output						
UGATE Drive Source	R_{UGATE_SR}	$V_{BOOT} - V_{PHASE}$ = 12V, I_{Source} = 100mA	--	1.7	--	Ω
UGATE Drive Sink	R_{UGATE_SK}	$V_{BOOT} - V_{PHASE}$ = 12V, I_{Sink} = 100mA	--	1.4	--	Ω
LGATE Drive Source	R_{LGATE_SR}	I_{Source} = 100mA	--	1.6	--	Ω
LGATE Drive Sink	R_{LGATE_SK}	I_{Sink} = 100mA	--	1.1	--	Ω

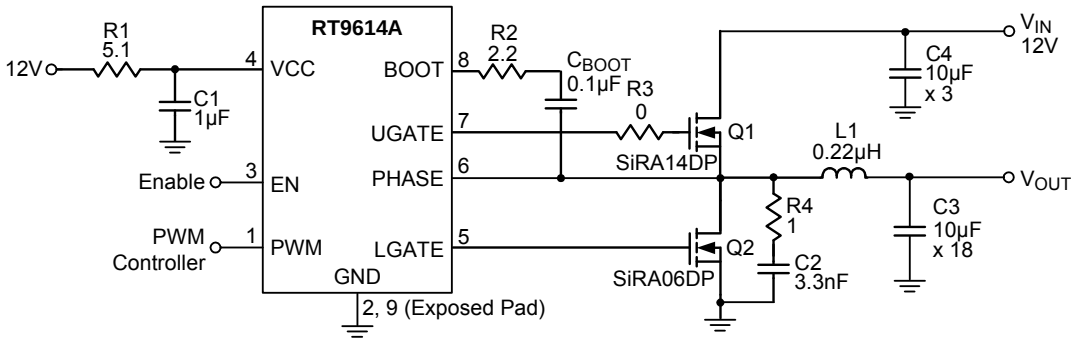
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

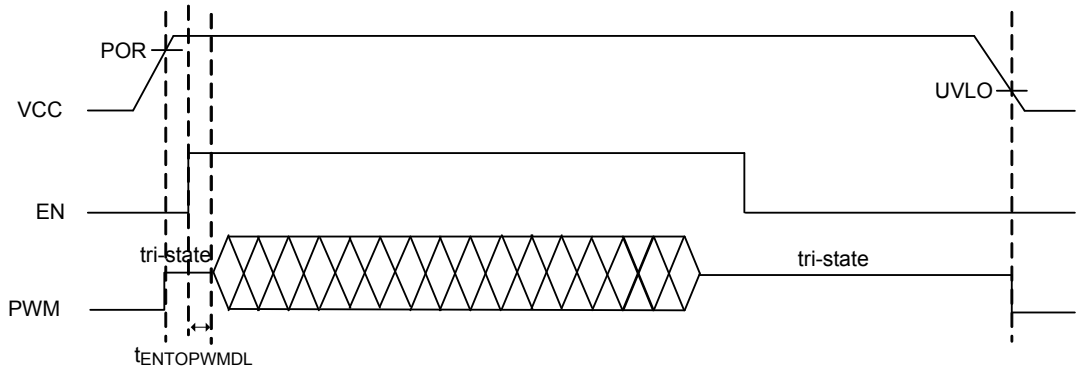
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

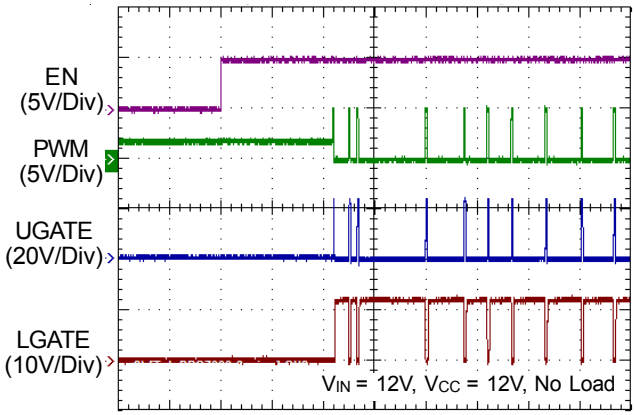


Timing Diagram

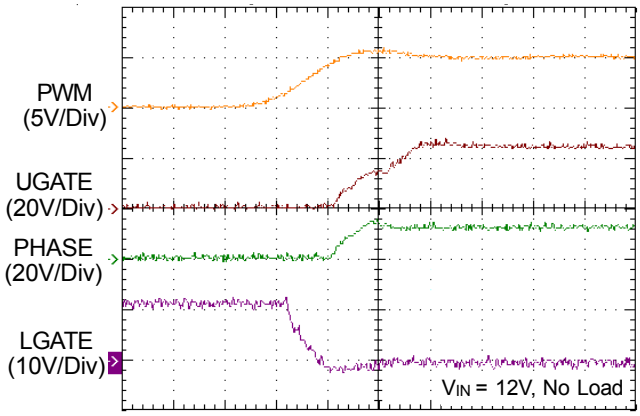


Typical Operating Characteristics

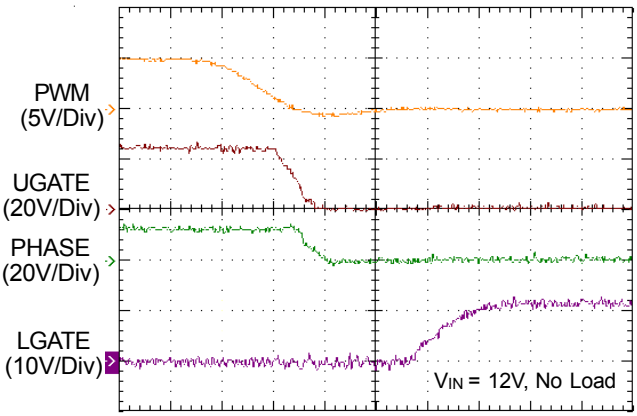
Driver Enable



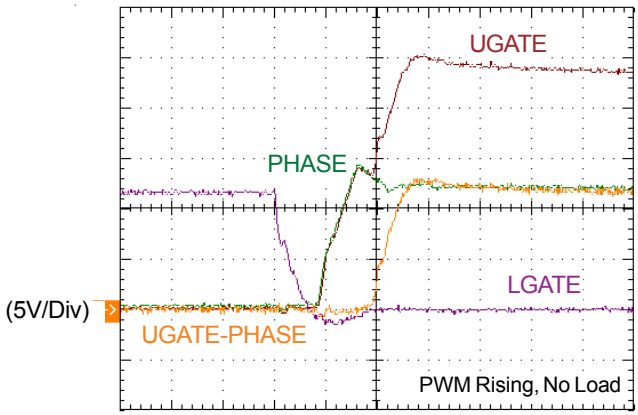
PWM Rising Edge



PWM Falling Edge



Dead Time



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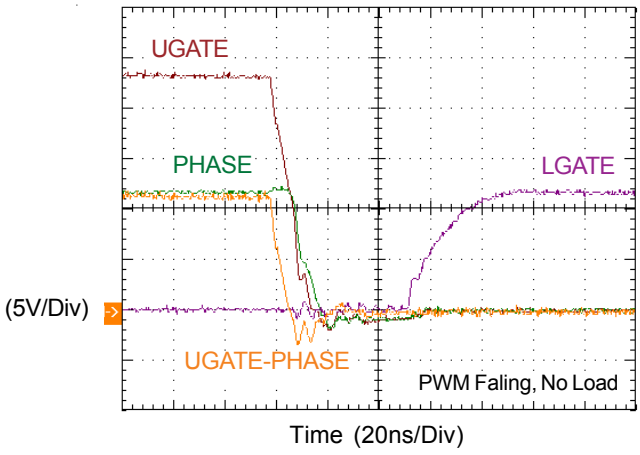

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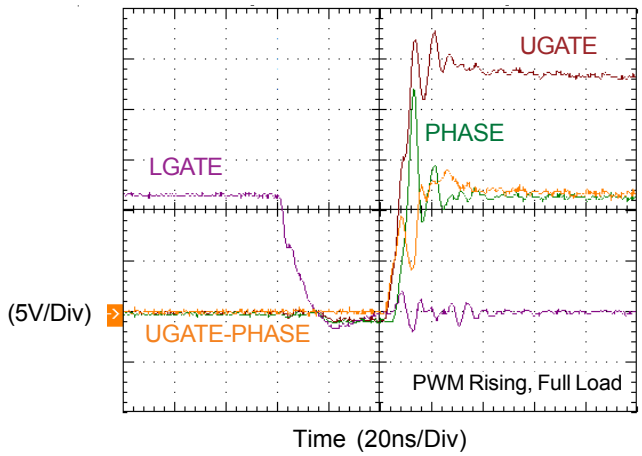
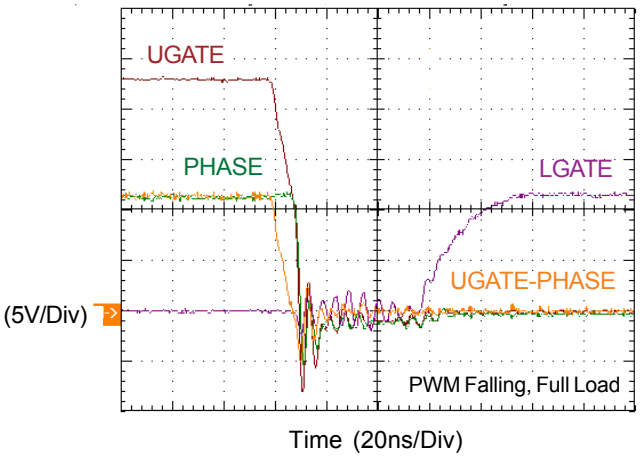
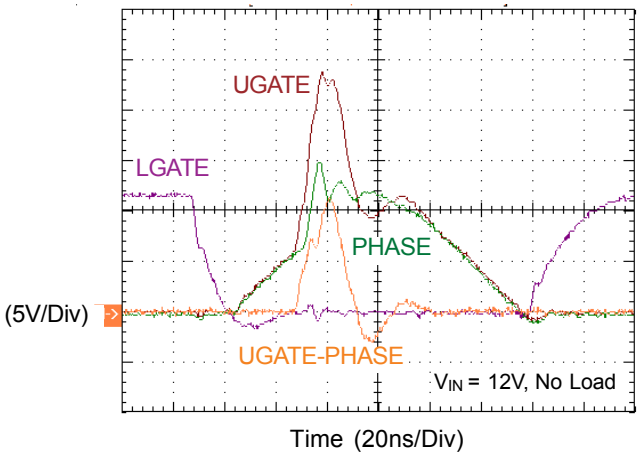


Dead Time



Short Pulse



Application Information

Driving Capability

The basic requirements for a gate driver of MOSFET include an ability to source a sufficient voltage that has to greater than $V_{GS(th)}$ of selected MOSFET, and the satisfactory driving capability for selected MOSFET to achieve target switching frequency and performance. This section describes an example of a MOSFET's gate driver for an N-Channel MOSFET.

The MOSFET's switching behavior is affected by the parasitic components between the devices. That is gate-to-source C_{GS}, gate-to-drain C_{GD} and drain-to-source C_{DS}. Besides, during the MOSFET turning on/off transition, C_{GD} and C_{GS} are charged or discharged through the gate. Hence, the gate driver of MOSFET must consider the variation on those parasitic capacitors. The MOSFET parasitic capacitances can be found in MOSFET datasheet, which is expressed as C_{ISS}, C_{OSS} and C_{RSS}.

$C_{ISS} = C_{GS} + C_{GD}$

$C_{OSS} = C_{GD} + C_{DS}$

$C_{RSS} = C_{GD}$

The following Figure 3 shows the equivalent circuit of high-side MOSFET in turn-on transition.

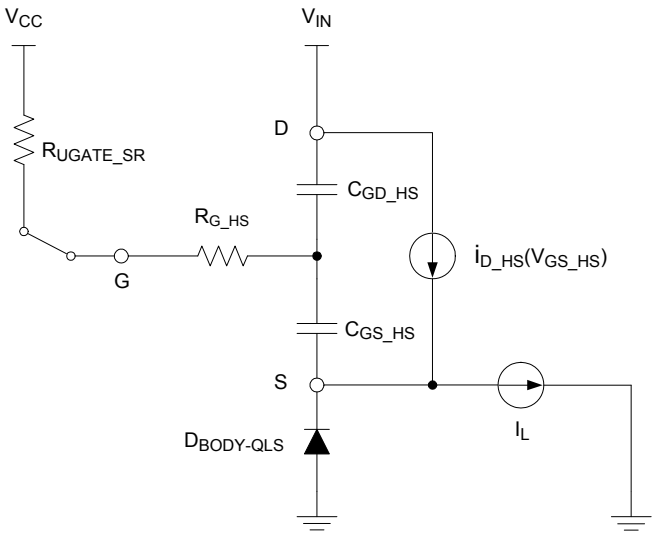


Figure 3. The Equivalent Circuit of High-Side MOSFET in Turn-on Transition

The turn-on transition of high-side MOSFET is broken up into 5 intervals as shown in Figure 4. According to Figure 4, the gate-to-source voltage and driving current in interval t_{1_HS} and t_{2_HS} can be expressed as follows :

$$V_{GS\_HS}(t) = V_{CC} \times (1 - e^{\frac{-t}{(R_{UGATE\_SR} + R_{G\_HS}) C_{ISS\_HS}}})$$

$$i_{g\_HS}(t) = \frac{V_{CC}}{(R_{UGATE\_SR} + R_{G\_HS})} \times e^{\frac{-t}{(R_{UGATE\_SR} + R_{G\_HS}) C_{ISS\_HS}}}$$

The interval t_{1_HS} and t_{2_HS} are defined as

$$t_{1\_HS} = (R_{UGATE\_SR} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{TH\_HS}}\right)$$

$$t_{2\_HS} = (R_{UGATE\_SR} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC} - V_{TH\_HS}}{V_{CC} - V_{GP\_HS}}\right)$$

When V_{GS_HS} reaches to V_{GP_HS}, MOSFET enters to miller plateau and the driving current diverts to discharge C_{GD_HS} for facilitating the rapid voltage change across on V_{DS_HS}. The driving current in interval t_{3_HS} is shown as follows

$$i_{g\_HS}(t) = \frac{V_{CC} - V_{GP\_HS}}{R_{UGATE\_SR} + R_{G\_HS}}$$

The t_{3_HS} can be calculated as

$$t_{3\_HS} = \frac{V_{IN}}{V_{CC} - V_{GP\_HS}} \times (R_{UGATE\_SR} + R_{G\_HS}) \times C_{GD\_HS}$$

Finally, the V_{GS_HS} is continuously charged from V_{GP_HS} to $0.9V_{CC}$ and the high-side MOSFET is fully turned on. The V_{GS_HS} in interval t_{4_HS} can be presented by

$$V_{GS\_HS}(t) = (V_{GP\_HS} - V_{CC}) \times e^{\frac{-t}{(R_{UGATE\_SR} + R_{G\_HS}) C_{ISS\_HS}}} + V_{CC}$$

The t_{4_HS} can be calculated as

$$t_{4\_HS} = (R_{UGATE\_SR} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC} - V_{GP\_HS}}{0.1V_{CC}}\right)$$

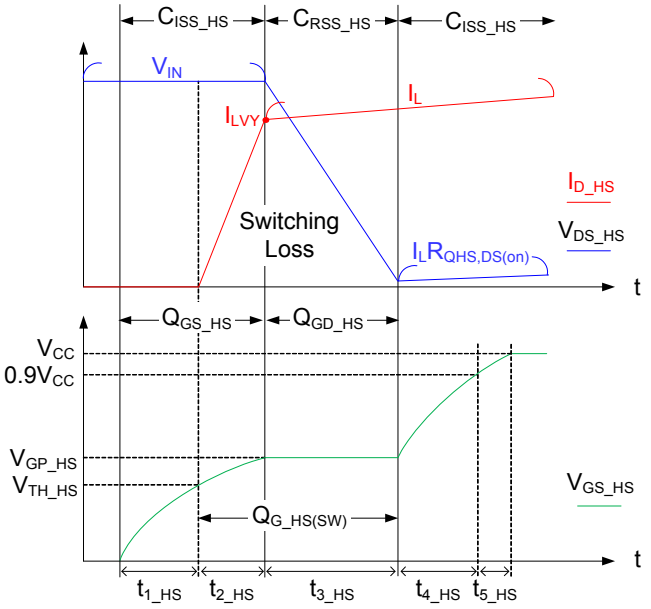


Figure 4. Timing Interval of High-Side MOSFET During Turn-On Transition

The following Figure 5 illustrates the equivalent circuit of high-side MOSFET during turn-off transition.

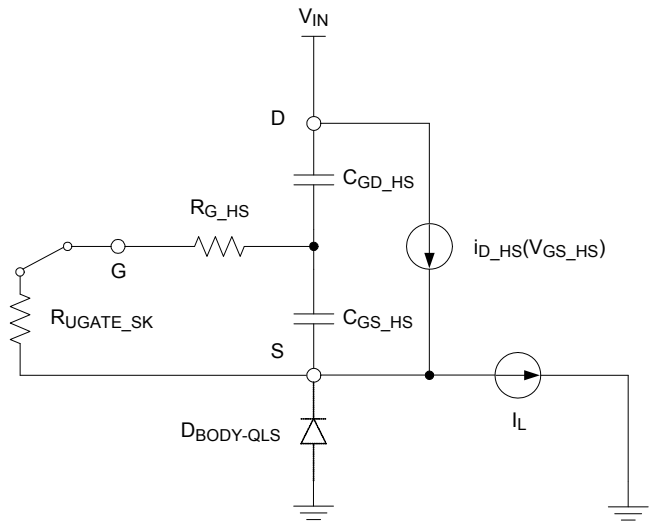


Figure 5. The Equivalent Circuit of High-Side MOSFET in Turn-off Transition

Referring to Figure 6, the timing interval of high-side MOSFET turned off can be separated into 5 regions, and the gate-to-source voltage and driving current in interval t_{6_HS} and t_{7_HS} can be derived as follows :

$$V_{GS\_HS}(t) = V_{CC} \times e^{\frac{-t}{(R_{UGATE\_SK}+R_{G\_HS})C_{ISS\_HS}}}$$

$$i_{g\_HS}(t) = \frac{-V_{GS\_HS}(t)}{R_{UGATE\_SK}+R_{G\_HS}}$$, the symbol "minus" represents the inverse direction of driving current.

The interval t_{6_HS} and t_{7_HS} are defined as follows :

$$t_{6\_HS} = (R_{UGATE\_SK}+R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{10}{9}\right)$$

$$t_{7\_HS} = (R_{UGATE\_SK}+R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(0.9\frac{V_{CC}}{V_{GP\_HS}}\right)$$

When V_{GS_HS} falls to V_{GP_HS}, MOSFET enters to miller plateau and the driving current diverts to charge C_{GD_HS}. The driving current in interval t_{8_HS} is shown as follows

$$i_{g\_HS}(t) = \frac{-V_{GP\_HS}}{R_{UGATE\_SK}+R_{G\_HS}}$$, the symbol "minus" represents the inverse direction of driving current.

The interval t_{8_HS} can be calculated as

$$t_{8\_HS} = \frac{V_{IN}}{V_{GP\_HS}} \times (R_{UGATE\_SK}+R_{G\_HS}) \times C_{GD\_HS}$$

Finally, the V_{GS_HS} further decreases to V_{TH_HS} from V_{GP_HS} and the high-side MOSFET is fully turned off. The V_{GS_HS} of interval t_{9_HS} can be presented in following equation.

$$V_{GS\_HS}(t) = V_{GP\_HS} \times e^{\frac{-t}{(R_{UGATE\_SK}+R_{G\_HS})C_{ISS\_HS}}}$$

The interval t_{9_HS} can be calculated as

$$t_{9\_HS} = (R_{UGATE\_SK}+R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{GP\_HS}}{V_{TH\_HS}}\right)$$

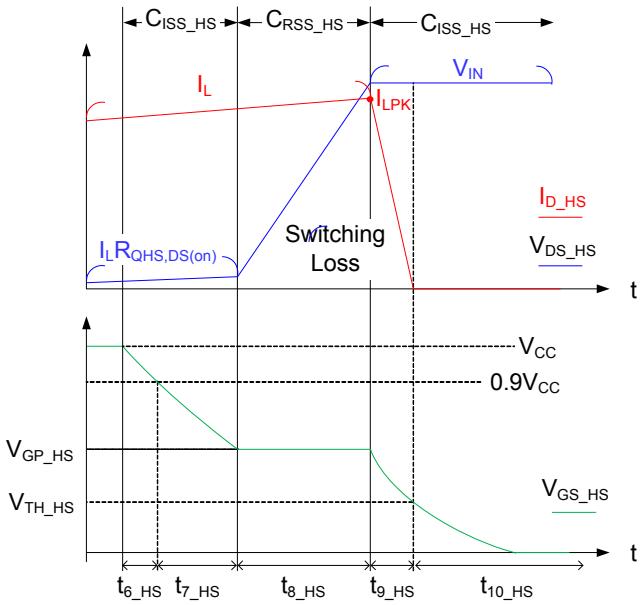


Figure 6 Timing Interval of High-Side MOSFET During Turn-off Transition.

Here is an example for driving capability calculation that input voltage and driver voltage of synchronous buck converter are all 12V (VIN = 12V, VCC = 12V). The selected high-side MOSFET is CSD17301Q5A whose C_{ISS} = 2660pF, C_{GD} = 80pF, V_{TH} = 1.1V, V_{GP} = 1.32V and R_G = 1.3Ω.

Therefore, the maximum driving current for CSD17301Q5A during turning on period can be calculated as follows :

$$I_{g\_HS\_max} = i_{g\_HS}(0)$$

$$= \frac{V_{CC}}{(R_{UGATE\_SR} + R_{G\_HS})} \times e^{\frac{-0}{(R_{UGATE\_SR}+R_{G\_HS})C_{ISS\_HS}}}$$

$$= \frac{12}{1.7+1.3} \times e^{0} = 4A$$

Further, the timing intervals of turn-on transition are expressed in following equations.

$$t_{1\_HS} = (R_{UGATE\_SR} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{TH\_HS}}\right)$$

$$= (1.7+1.3) \times 2660p \times \ln\left(\frac{12}{12-1.1}\right) = 0.77ns$$

$$t_{2\_HS} = (R_{UGATE\_SR} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC} - V_{TH\_HS}}{V_{CC} - V_{GP\_HS}}\right)$$

$$= (1.7+1.3) \times 2660p \times \ln\left(\frac{12-1.1}{12-1.32}\right) = 0.16ns$$

$$t_{3\_HS} = \frac{V_{IN}}{V_{CC} - V_{GP\_HS}} \times (R_{UGATE\_SR} + R_{G\_HS}) \times C_{GD\_HS} = \frac{12}{12-1.32} \times (1.7+1.3) \times 80p = 0.27ns$$

$$t_{4\_HS} = (R_{UGATE\_SR} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{CC} - V_{GP\_HS}}{0.1V_{CC}}\right)$$

$$= (1.7+1.3) \times 2660p \times \ln\left(\frac{12-1.32}{0.1 \times 12}\right) = 17.44ns$$

Finally, fully turned CSD17301Q5A on needs to take about 18.64ns by using RT9414A as gate driver of MOSFET.

$$t_{TOTAL\_ON} = t_{1\_HS} + t_{2\_HS} + t_{3\_HS} + t_{4\_HS}$$

$$= 0.77n+0.16n+0.27n+17.44n = 18.64ns$$

As operating in turn-off region, the maximum of driving

current for CSD17301Q5A is defined.

$$i_{g\_HS\_max} = i_{g\_HS}(0)$$

$$= \frac{-v_{GS\_HS}(0)}{R_{UGATE\_SK} + R_{G\_HS}} = \frac{-12}{1.4+1.3} = -4.44A$$

Further, the timing intervals of turn-off transition are expressed in following equations.

$$t_{6\_HS} = (R_{UGATE\_SK} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{10}{9}\right)$$

$$= (1.4+1.3) \times 2660p \times \ln\left(\frac{10}{9}\right) = 0.76ns$$

$$t_{7\_HS} = (R_{UGATE\_SK} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(0.9\frac{V_{CC}}{V_{GP\_HS}}\right)$$

$$= (1.4+1.3) \times 2660p \times \ln\left(0.9\frac{12}{1.32}\right) = 15.1ns$$

$$t_{8\_HS} = \frac{V_{IN}}{V_{GP\_HS}} \times (R_{UGATE\_SK} + R_{G\_HS}) \times C_{GD\_HS}$$

$$= \frac{12}{1.32} \times (1.4+1.3) \times 80p = 1.96ns$$

$$t_{9\_HS} = (R_{UGATE\_SK} + R_{G\_HS}) \times C_{ISS\_HS} \times \ln\left(\frac{V_{GP\_HS}}{V_{TH\_HS}}\right)$$

$$= (1.4+1.3) \times 2660p \times \ln\left(\frac{1.32}{1.1}\right) = 1.31ns$$

The minimum turn-off request time for CSD17301Q5A by using RT9614A is expressed as follows :

$$t_{TOTAL\_OFF} = t_{6\_HS} + t_{7\_HS} + t_{8\_HS} + t_{9\_HS}$$

$$= 0.76n+15.1n+1.96n+1.31n = 19.13ns$$

Selecting a proper MOSFET, matching up with RT9614A, can reduce the MOSFET turning on/off intervals which can improve the efficiency and speed up the switching frequency for the system.

Power loss of MOSFET

The synchronous buck converter is a widely used in low voltage and high current application fields, such as CPU peripherals. Hence, the high efficiency is always the concern. For improving the efficiency for the whole system, the power losses for every selected device need to be broken up. The section is going to introduce the power losses on MOSFET, which can be divided into two categories, conduction loss and switching loss.

The conduction loss of high-side MOSFET can be represented to

$$P_{COND(QHS)} = I_{D(QHS,RMS)}^2 \times R_{QHS,DS(on)}$$

The conduction loss of low-side MOSFET can be calculated by

$$P_{COND(QLS)} = I_{D(QLS,RMS)}^2 \times R_{QLS,DS(on)} + V_{F\_LS} \times (I_{LPK} \times t_{LGATEPDH} + I_{LVY} \times t_{HGATEPDH}) \times f_S$$

Where:

$I_{D(QHS,RMS)}$ is RMS current of high-side MOSFET.

$R_{QHS,DS(on)}$ is on-resistance of high-side MOSFET.

$I_{D(QLS,RMS)}$ is RMS current of low-side MOSFET.

$R_{QLS,DS(on)}$ is on-resistance of low-side MOSFET.

V_{F_LS} is forward voltage drop of the low-side MOSFET body diode.

I_{LPK} is peak current of inductor

I_{LVY} is valley current of inductor. When the buck converter is operating in DEM, the I_{LVY} is equal to zero.

$t_{LGATEPDH}$ and $t_{UGATEPDH}$ are the propagation delay in gate driver of MOSFET.

f_S is switching frequency.

Driver Loss :

The driver loss can be defined as follows :

$$P_{LOSS\_GDRV\_HS} = Q_{G\_HS} \times V_{CC} \times f_S$$

$$P_{LOSS\_GDRV\_LS} = Q_{G\_LS} \times V_{CC} \times f_S$$

Where

Q_{G_HS} is the total gate charge of high-side MOSFET

Q_{G_LS} is the total gate charge of low-side MOSFET

The switching loss of high/low-side MOSFET can further be classified as turning on/off losses, C_{OSS} loss and reverse recovery loss caused by MOSFET body diode.

High-side MOSFET :

Referring to equation (x) and (x), the turn-on switching loss of high-side MOSFET can be derived as follows :

$$P_{LOSS,HS\_ON} = \frac{1}{2} \times V_{IN} \times I_{LVY} \times (t_{2\_HS} + t_{3\_HS}) \times f_S$$

Referring to equation (x) and (x), the turn-off switching loss of high-side MOSFET can be derived as follows :

$$P_{LOSS,HS\_OFF} = \frac{1}{2} \times V_{IN} \times I_{LPK} \times (t_{8\_HS} + t_{9\_HS}) \times f_S$$

Further, because of C_{OSS} charged and discharged for every switching cycle, the C_{OSS} loss of high-side MOSFET must be considered. The calculation of this loss is as follows

$$P_{LOSS,HS\_COSS} = \frac{1}{2} \times C_{OSS\_HS} \times V_{IN}^2 \times f_S$$

Low-side MOSFET

The turn-on switching loss of low-side MOSFET can be obtained.

$$P_{LOSS,LS\_ON} = \frac{1}{2} \times V_{F\_LS} \times I_{LPK} \times (t_{2\_LS} + t_{3\_LS}) \times f_S$$

Where V_F is forward voltage drop of the low-side MOSFET body diode.

The interval t_{2_LS} and t_{3_LS} of turn-on low-side MOSFET are defined as

$$t_{2\_LS} = (R_{LGATE\_SR} + R_{G\_LS}) \times C_{ISS\_LS} \times \ln\left(\frac{V_{CC} - V_{TH\_LS}}{V_{CC} - V_{GP\_LS}}\right)$$

$$t_{3\_LS} = \frac{V_{F\_LS}}{V_{CC} - V_{GP\_LS}} \times (R_{LGATE\_SR} + R_{G\_LS}) \times C_{GD\_LS}$$

The turn-off switching loss of low-side MOSFET can be obtained.

$$P_{LOSS,LS\_OFF} = \frac{1}{2} \times V_{F\_LS} \times I_{LVY} \times (t_{8\_LS} + t_{9\_LS}) \times f_S$$

The interval t_{8_LS} and t_{9_LS} of turn-off low-side MOSFET are defined as

$$t_{8\_LS} = \frac{V_{F\_LS}}{V_{GP\_LS}} \times (R_{LGATE\_SK} + R_{G\_LS}) \times C_{GD\_LS}$$

$$t_{9\_LS} = (R_{LGATE\_SK} + R_{G\_LS}) \times C_{ISS\_LS} \times \ln\left(\frac{V_{GP\_LS}}{V_{TH\_LS}}\right)$$

The C_{OSS} loss of low-side MOSFET is much smaller and it is generally ignored. However, in order to make the integrity of the loss calculation, it can refer to the following equation.

$$P_{LOSS,LS\_COSS} = \frac{1}{2} \times C_{OSS\_LS} \times V_{F\_LS}^2 \times f_S$$

Additionally, the reverse recovery loss is existing in the body diode of low-side MOSFET when high-side MOSFET is turning on and low-side MOSFET is in off-state. The following equation is the reverse recovery loss.

$$P_{LOSS,LS\_RR} = Q_{RR\_LS} \times V_{IN} \times f_S$$

Where Q_{RR_LS} is reverse recovery charge of low-side MOSFET body diode.

Consequently, through to understand the power loss distributions on MOSFET, it helps to improve the efficiency and raise the system performance.

Bootstrap Capacitor Selection

For saving more power consumption, the transitional bootstrap circuit is replaced by FET switch which is integrated to RT9614A for more space saving. Now, only connect an external capacitor (C_{BOOT}) between BOOT and PHASE. For effectively turning the high-side MOSFET on, the storage energy in C_{BOOT} needs to greater than the total gate charge of high-side MOSFET.

The value of bootstrap capacitor is defined by :

$$C_{BOOT} \geq \frac{Q_g}{\Delta V_{BOOT}}$$

Where

Q_g : Total gate charge

$\Delta V_{BOOT} = V_{CC} - V_{TH}$

ΔV_{BOOT} : Maximum allowable voltage drop on bootstrap capacitor

V_{CC} : Supply voltage of gate driver

V_{TH} : Threshold voltage of the high-side MOSFET

The theoretically C_{BOOT} is illustrated in Figure 7. Moreover, the selection of C_{BOOT} should be considered additionally these effects of DC de-rating, AC de-rating and thermal de-rating. Suggest to use ceramic capacitor as C_{BOOT} who provides good local de-coupling by low ESR.

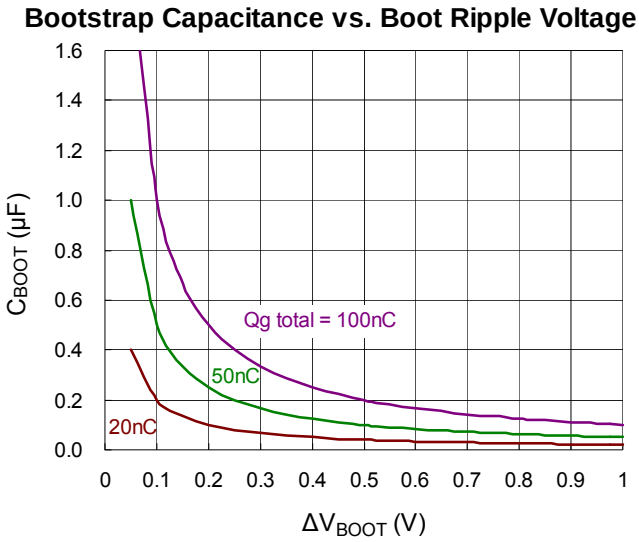


Figure 7 Bootstrap Capacitance vs. Boot Ripple Voltage

Power Dissipation

The power dissipation is related to switching frequency and total gate charge of the selected MOSFET. Calculating the power dissipation in gate drivers of MOSFET is essential to ensure the safe operation. In general design, the power dissipation does not allow larger than specified value and the operation junction temperature should be less than 125°C.

Figure 8 shows the power dissipation test circuit. C_L and C_U are the UGATE and LGATE load capacitors, respectively. The bootstrap capacitor value is 0.1µF. Figure 9 shows the curves of power dissipation. The power dissipation is proportional to the frequency and load capacitance. The higher operated frequency and load capacitance cause the higher power dissipation.

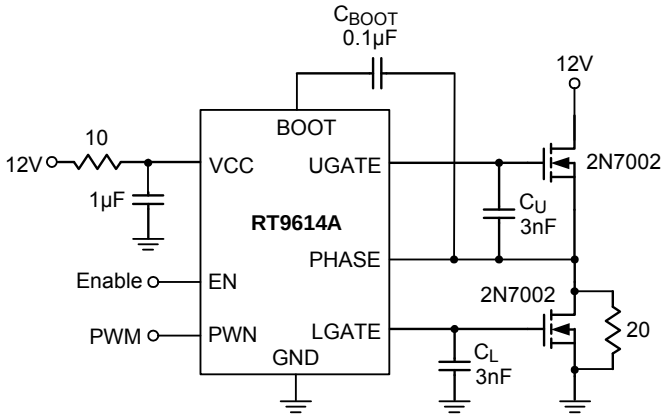


Figure 8. Power Dissipation Test Circuit

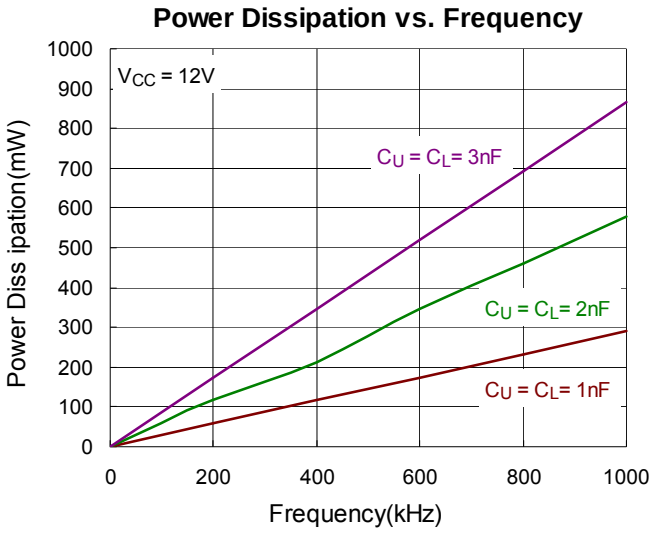


Figure 9. Power Dissipation vs Frequency

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-8L 3x3 , the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (31°C/W) = 3.22W for a WDFN-8L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

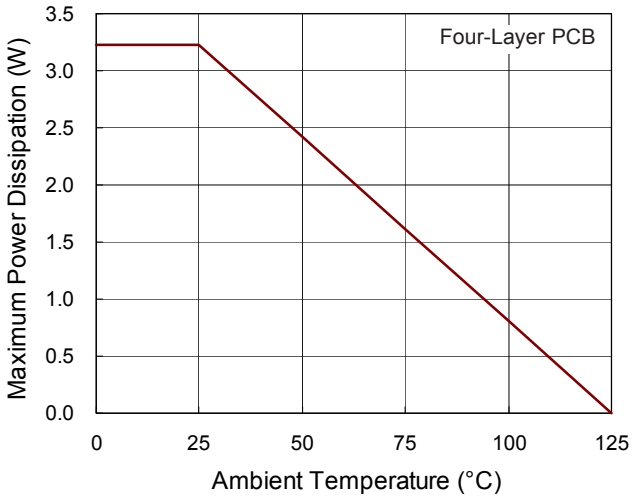


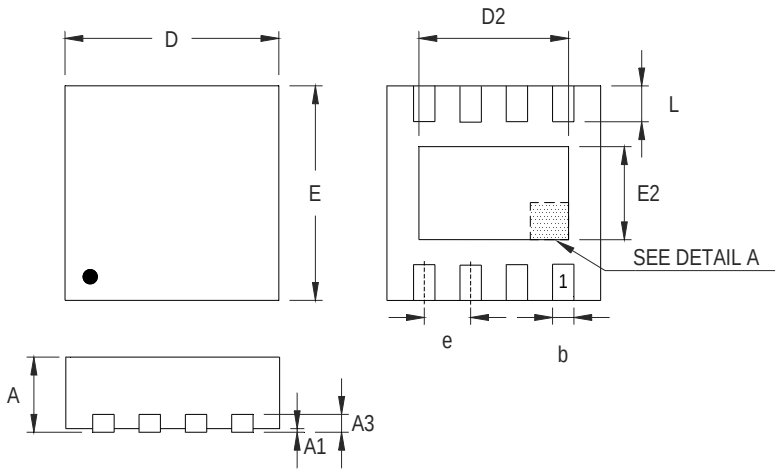
Figure 10. Derating Curve of Maximum Power Dissipation

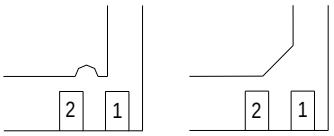
Layout Consideration

The parasitic inductance of PCB and power device could affect the switching characteristics to aggravate PHASE ring, and further decrease efficiency. Hence, to improve the drawbacks caused by PCB layout, these layout rules must be considered.

- Place the RT9614A as close as possible to the MOSFETs for reducing the parasitic components between the devices.
- Place the VCC bypass capacitor as close as possible to the VCC pin. It can help to eliminate the high frequency components caused by switching high/low-side MOSFET.
- Bootstrap capacitor should be placed as close as possible to the BOOT pin and PHASE pin for minimizing the parasitic inductances and reducing the high current trace path including the bootstrap capacitor, GND, VCC bypass capacitor and drain-to-source of low-side MOSFET.
- The paths of gate drivers (UGATE, PHASE, LGATE, GND) should be short and wide so that the parasitic impedance can be reduced. The UGATE and PHASE traces of the high-side driver should be directly connected to gate and source terminals of high-side MOSFET. Moreover, the PHASE trace for gate driver should be independent for the high current path. Similarly, use same rule for LGATE and GND traces on low-side driver.
- Keep the source terminal of high-side MOSFET as close as possible to the drain terminal of the low-side MOSFET. Likewise, keep the connection between source terminal of low-side MOSFET and GND wide and short. Consequently, the impedance between the high/low-side MOSFET and GND can be minimized.
- If changing layers is required, it should use at least two vias for reducing the parasitic inductance.
- Avoid the PWM and enable trace being close to the switching node, otherwise these might suffer from noise interference with high dV/dt.

Outline Dimension





DETAIL A

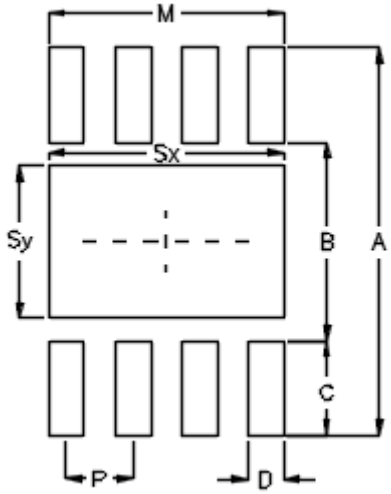
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

W-Type 8L DFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3*3-8	8	0.65	3.80	1.94	0.93	0.35	2.30	1.50	2.30	±0.05

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单击下面可查看定价，库存，交付和生命周期等信息

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