Three-Phase PMSM/BLDC Motor Controller with Pre-Driver

General Description

The RT7083 is an application specific IC designed for PMSM/BLDC motor applications. This two-in-one ASIC integrates several functional circuits, including a 3-phase motor controller, a 3-phase gate driver, three bootstrap diodes, a 5V LDO and a buck converter.

The RT7083 embeds the ARM 32-bit Cortex-M0 core with peripheral circuits to perform sensorless Field Oriented Control (FOC). In addition, this ASIC provides several system level peripheral functions, in which ADC, DAC, communication interface, SVPWM, watchdog timer, current sensing, undervoltage-lockout (UVLO), short circuit protection (SCP) and locked-rotor protection are integrated so as to reduce component count, PCB size and system cost.

Moreover, the RT7083 drives external N-Channel MOSFETs in three half-bridge configuration with built-in bootstrap circuitry up to 58V. A dead time control is designed to prevent shoot-through of the external N-Channel MOSFETs.

The RT7083 is available in WQFN-48L 6x6 package.

Ordering Information

RT7083□□-□□□□□

- Programmed Firmware Code
- Package Type
  QW : WQFN-48L 6x6 (W-Type)
  (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

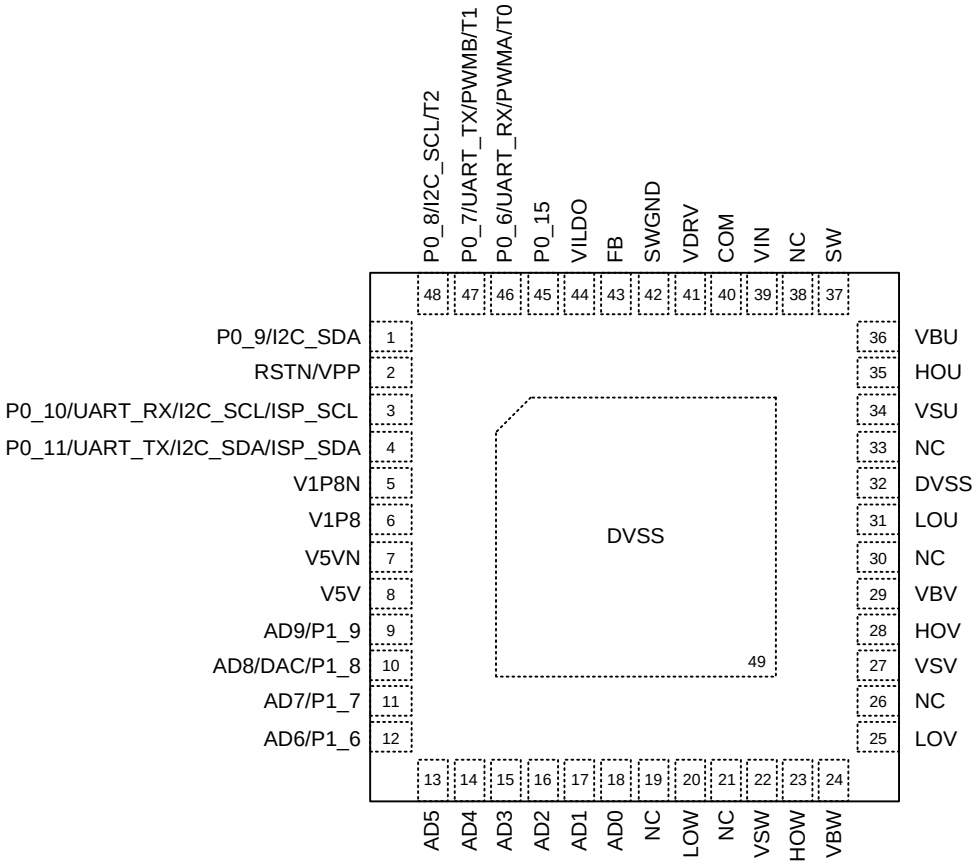
- **Integrates with 3-Phase PMSM/BLDC Controller, Gate Driver, Bootstrap Diodes, 5V LDO and Buck Converter**
- **Input Voltage Range : 7V to 58V**
- **Sensorless, Sine-Wave Field Oriented Control (FOC)**
- **Integrates with Filters at ADC Input**
- **Protections : SCP, UVLO, Locked-Rotor and Thermal Detection**
- **PMSM/BLDC Motor Controller**
  - **ARM 32-bit Cortex-M0 CPU, Frequency up to 60MHz**
  - **Memories Size : 16KB MTP, Internal ROM with Embedded Motor Control Library and 4KB SRAM**
  - **Power Management : Normal or Deep Sleep**
  - **Communication Interface : I^2C and UART**
  - **Configurable ADC Gain : x1, x4, x8, x16**
  - **7-Channel 10-Bit ADC**
    - **AD0 to AD5 for Differential Mode Current Sense**
    - **AD6 to AD9 for System Application**
  - **1-Channel Voltage Type 8-bit DAC for Debugging**
- **Gate Driver**
  - **Floating Channel designed for Bootstrap operation**
  - **Sourcing/Sinking Current : 200mA/500mA**
  - **Built in UVLO functions for all channels**
  - **Matched Propagation Delays for all channels**
- **WQFN-48L 6x6 Package**

Applications

- Fan Applications : Exhaust Fan, Pedestal Fan, Ventilation Fan, etc.
- Water Pump
- Vacuum Cleaner

Pin Configuration

(TOP VIEW)



WQFN-48L 6x6

Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	P0_9	DIO	Pin 9 of GPIO port 0.
	I2C_SDA	DIO	I^2C data pin.
2	RSTN	DI	Low active reset pin.
	VPP	P	8V input power for MTP fast programming
3	P0_10	DIO	Pin 10 of GPIO port 0.
	UART_RX	DI	UART receiving pin.
	I2C_SCL	DIO	I^2C clock pin.
	ISP_SCL	DI	In system programming clock input pin.
4	P0_11	DIO	Pin 11 of GPIO port 0.
	UART_TX	DO	UART transmitting pin.
	I2C_SDA	DIO	I^2C data pin.
	ISP_SDA	DIO	In system programming data input pin.
5	V1P8N	GND	Digital ground
6	V1P8	P	1.8V power pin.
7	V5VN	GND	Analog ground
8	V5V	P	5V power pin.
9	AD9	AI	ADC channel 9 input pin.
	P1_9	DIO	Pin 9 of GPIO port 1.
10	AD8	AI	ADC channel 8 input pin.
	DAC	AO	Voltage type DAC output pin for debugging.
	P1_8	DIO	Pin 8 of GPIO port 1.
11	AD7	AI	ADC channel 7 input pin.
	P1_7	DI	Pin 7 of GPIO port 1.
12	AD6	AI	ADC channel 6 input pin.
	P1_6	DI	Pin 6 of GPIO port 1.
13	AD5	AI	ADC channel 5 differential input pin only.
14	AD4	AI	ADC channel 4 differential input pin only.
15	AD3	AI	ADC channel 3 differential input pin only.
16	AD2	AI	ADC channel 2 differential input pin only.
17	AD1	AI	ADC channel 1 differential input pin only.
18	AD0	AI	ADC channel 0 differential input pin only.
19, 21, 26, 30, 33, 38	NC	--	No internal connection.
20	LOW	VO	Low-side gate output of Phase W.
22	VSW	HVI	High-side floating supply offset voltage of Phase W.
23	HOW	HVO	High-side gate output of Phase W.
24	VBW	HVI	High-side floating supply voltage of Phase W.
25	LOV	VO	Low-side gate output of Phase V.

Pin No.	Pin Name	Type	Pin Function
27	VSV	HVI	High-side floating supply offset voltage of Phase V.
28	HOV	HVO	High-side gate output of Phase V.
29	VBV	HVI	High-side floating supply voltage of Phase V.
31	LOU	VO	Low-side gate output of Phase U.
32, 49 (Exposed Pad)	DVSS	GND	Digital ground
34	VSU	HVI	High-side floating supply offset voltage of Phase U.
35	HOU	HVO	High-side gate output of Phase U.
36	VBU	HVI	High-side floating supply voltage of Phase U.
37	SW	HVO	Switch node of Buck converter
39	VIN	HVI	Input supply voltage
40	COM	GND	Gate driver ground.
41	VDRV	P	High/Low-side driver supply voltage
42	SWGND	GND	Buck converter ground
43	FB	AI	Feedback voltage input of Buck converter
44	VILDO	P	5V LDO supply voltage
45	P0_15	DIO	Pin 15 of GPIO port 0. (Open Drain)
46	P0_6	DIO	Pin 6 of GPIO port 0.
	UART_RX	DI	UART receiving pin.
	PWMA	DO	Programmable PWMA output pin.
	T0	DI	T0 external enable or external clock input pin.
47	P0_7	DIO	Pin 7 of GPIO port 0.
	UART_TX	DO	UART transmitting pin.
	PWMB	DO	Programmable PWMB output pin.
	T1	DI	T1 external enable or external clock input pin.
48	P0_8	DIO	Pin 8 of GPIO port 0.
	I2C_SCL	DIO	I^2C clock pin.
	T2	DI	T2 external enable or external clock input pin.

IO Type Definition :

DIO : Digital input/output pin

DI : Digital input pin

DO : Digital output pin

AI : Analog input pin

AO : Analog output pin

P : Power pin

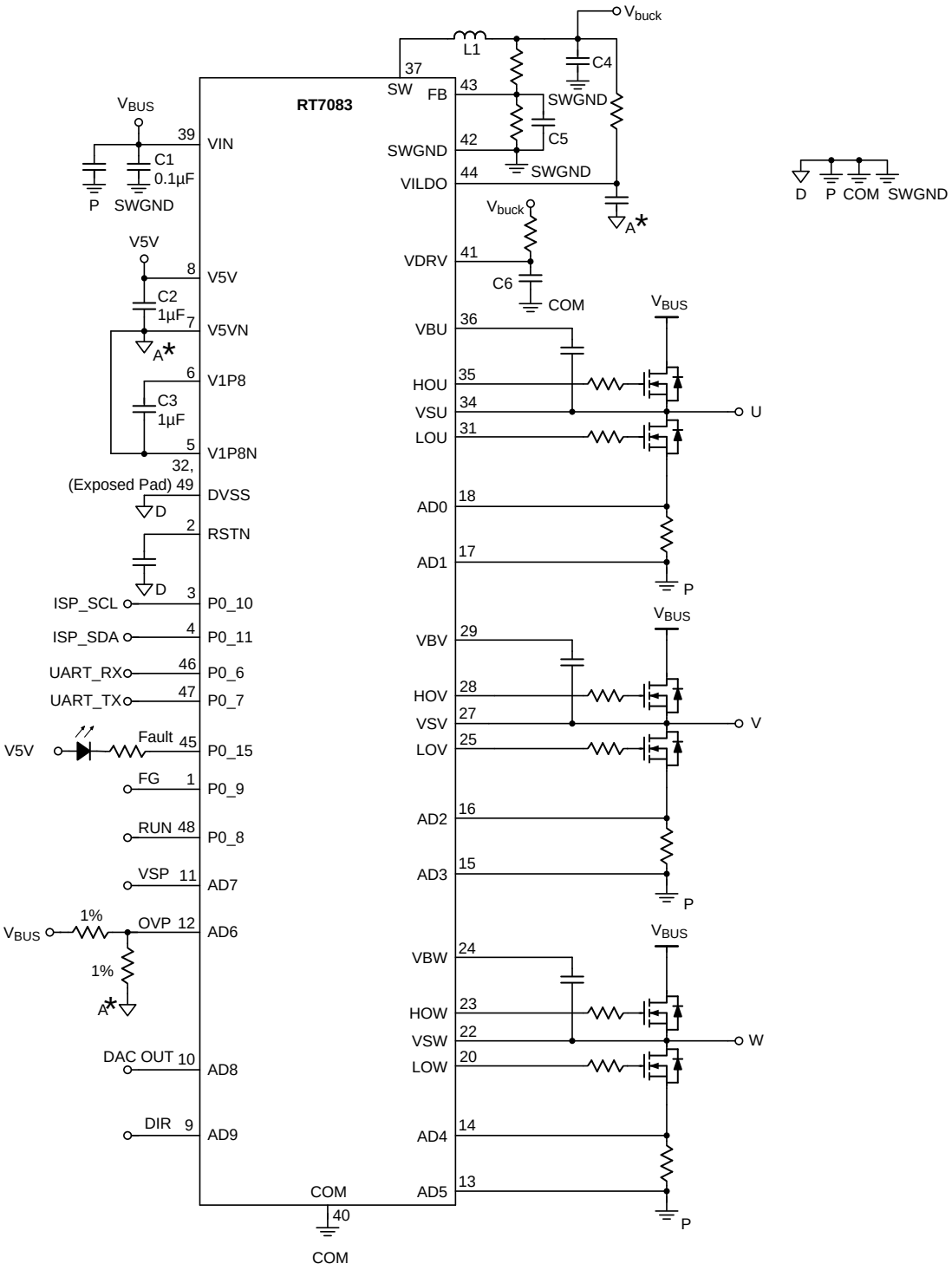
HVI : High voltage (60V) input pin

HVO : High voltage (60V) output pin

VO : Voltage output pin

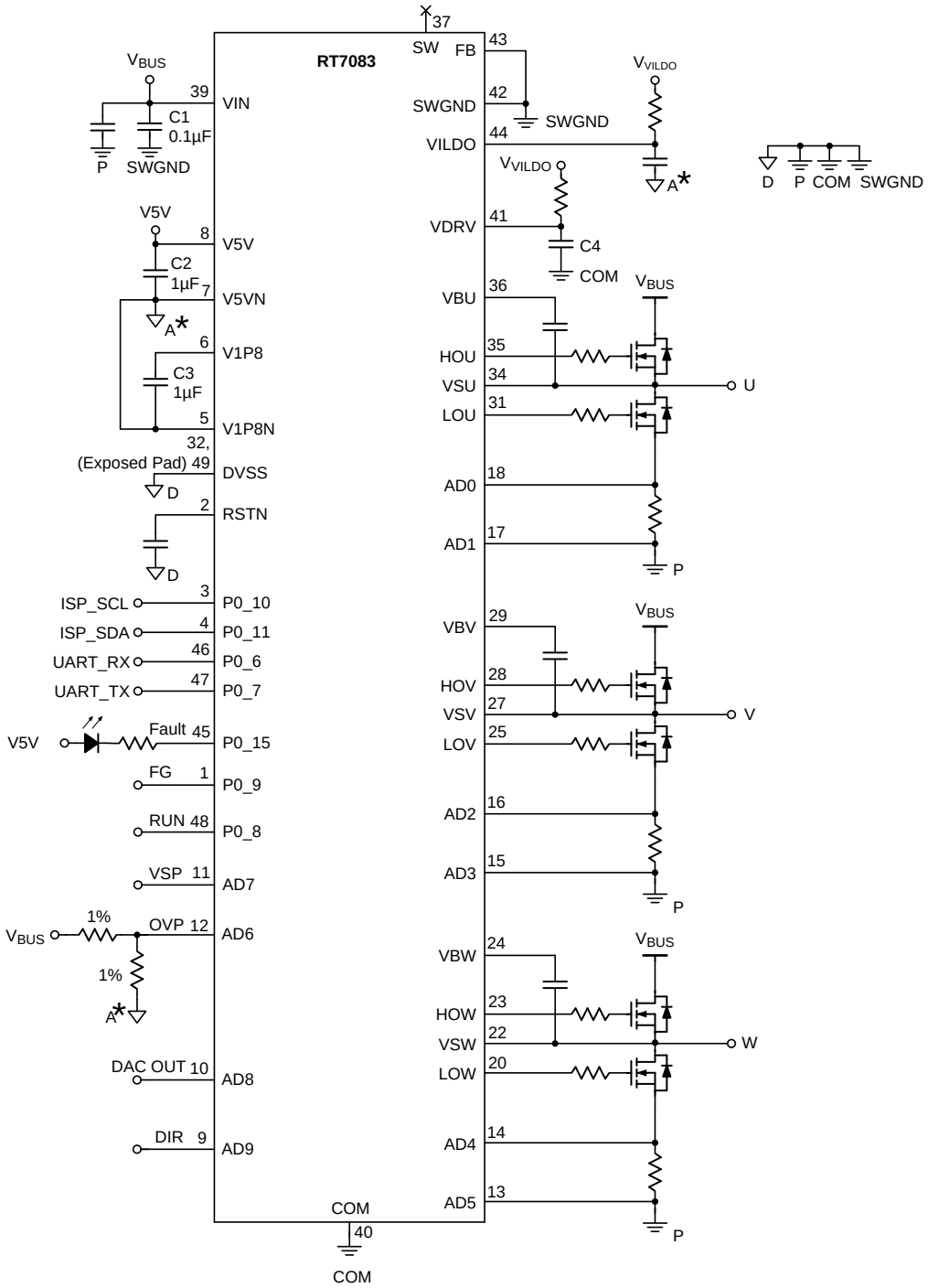
Typical Application Circuit

Application Circuit 1 (With buck converter)



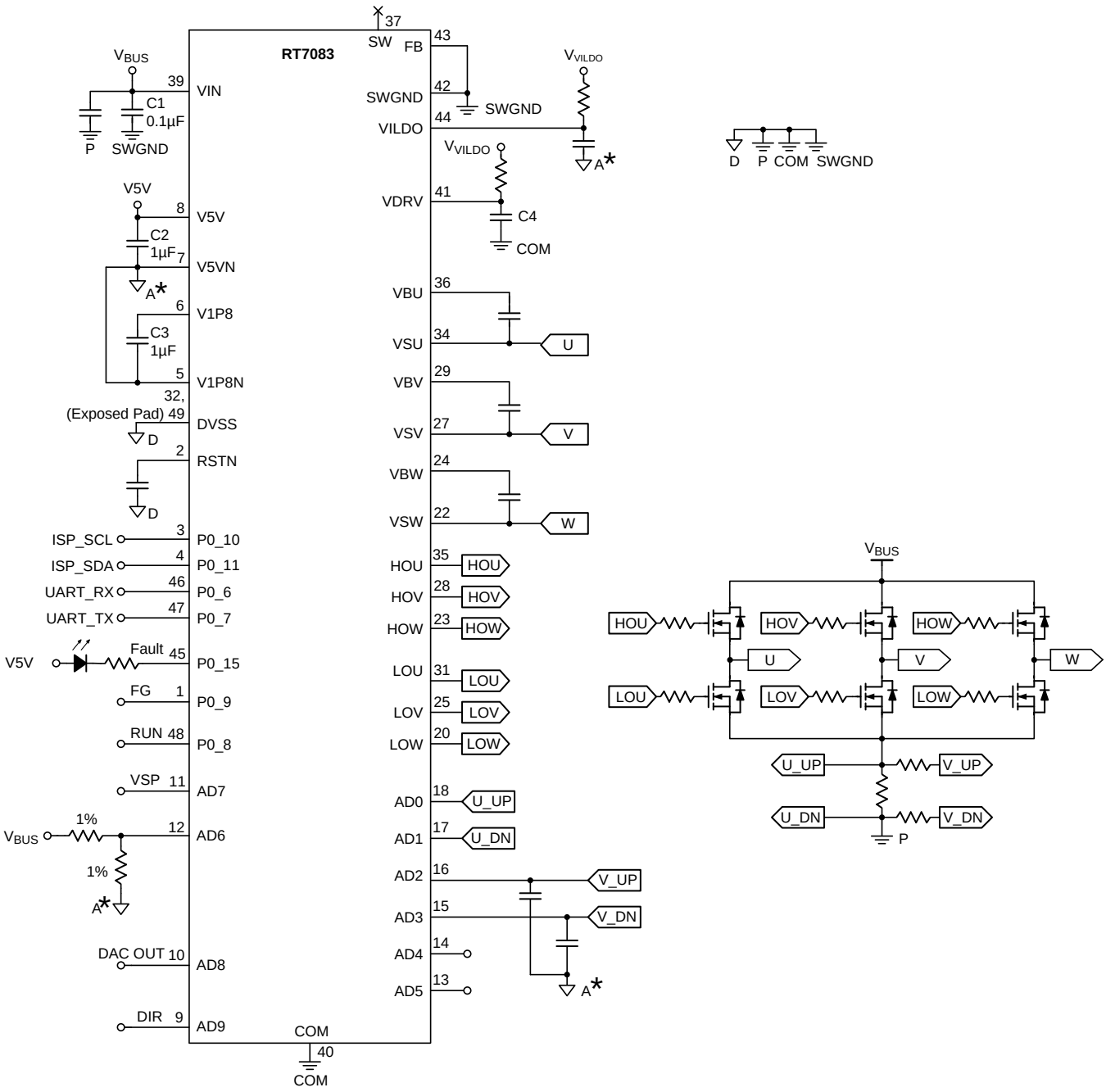
Note :
1. C1 should be as close as possible to the IC and SWGND.
2. C2, C3, C5 and L1 should be as close as possible to the IC.
   (If C2 and C3 can't close to the IC, it should put another 0.1µF close to the IC.)
3. C4 should be as close as possible to the IC and SWGND.
4. C6 should be as close as possible to the IC and COM.
5. L1 : The value of inductor should be determined by VIN. Please refer to Application Information
6. AGND is a separate loop, do not connect to DGND and PGND.

Application Circuit 2 (Without buck converter)



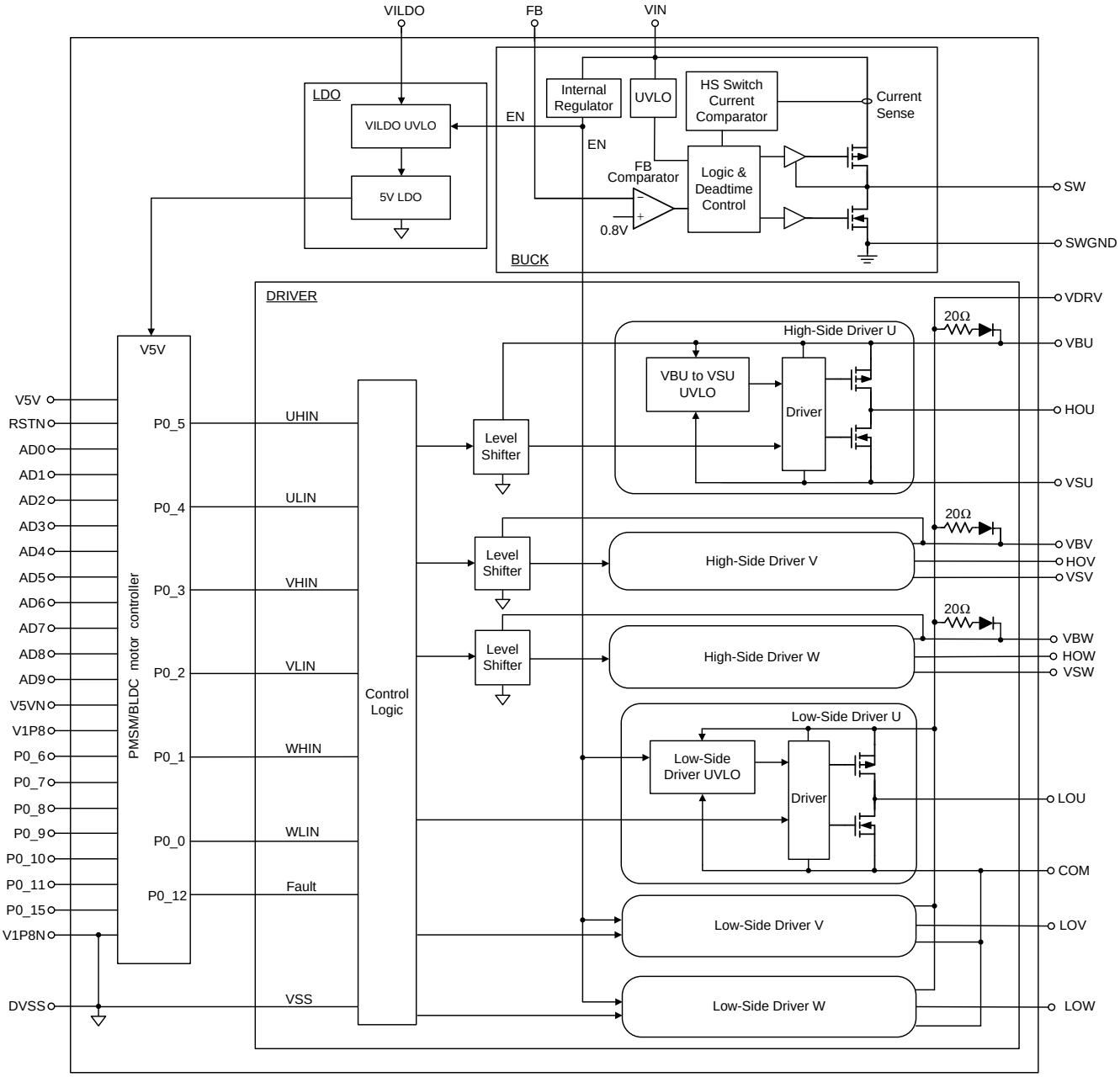
Note :
1. C1 should be as close as possible to the IC and SWGND.
2. C2 and C3 should be as close as possible to the IC.
   (If C2 and C3 can't close to the IC, it should put another 0.1µF close to the IC.)
3. C4 should be as close as possible to the IC and COM.
4. V_{VILDO} should be applied by external power.
5. If Buck converter is inactivated, VIN input voltage must be greater than 5V for internal reference voltage.
6. AGND is a separate loop, do not connect to DGND and PGND.

Application Circuit 3 (One shunt circuit)



Note :
1. C1 should be as close as possible to the IC and SWGND.
2. C2 and C3 should be as close as possible to the IC.
   (If C2 and C3 can't close to the IC, it should put another 0.1µF close to the IC.)
3. C4 should be as close as possible to the IC and COM.
4. V_{VILDO} should be applied by external power.
5. AD4-AD5 are only for differential input.
6. If Buck converter is necessary, please refer to “Typical Application Circuit 1”.
7. AGND is a separate loop, do not connect to DGND and PGND.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V5V ---------- –0.3V to 6.5V
- Supply Input Voltage, VIN ---------- –0.3V to 60V
- VSU, VSV, VSW to COM ---------- –5V to 70V
- VBU, VBV, VBW to COM ---------- –0.3V to 70V
- Driver Supply Voltage, VDRV ---------- –0.3V to 15V
- LDO Supply Voltage, VILDO ---------- –0.3V to 15V
- VSU, VSV, VSW dv/dt ---------- 5V/ns
- Switch Voltage, SW ---------- –0.3V to 60V
- Buck Output Voltage Feedback, FB ---------- –0.3V to 6V
- Voltage of I/O Pin (P0_6 to P0_9) ---------- –0.2V to 6.5V
- Voltage of I/O Pin (P0_10/P0_11/P0_15) ---------- –0.2V to 20V
- Minimum Input Voltage for MTP Fast Programming, Min V_{VPP} (Note 2) ---------- 8V
- Maximum Input Voltage for MTP Fast Programming, Max V_{VPP} (Note 2) ---------- 8.2V
- Voltage of I/O Pin (RSTN) ---------- –0.2V to 9V
- Analog Input Voltage (AD0 to AD5) ---------- –5V to 11V
- Analog Input Voltage (AD6/AD7) ---------- –0.2V to 20V
- Analog Input Voltage (AD8/AD9) ---------- –0.2V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-48L 6x6 ---------- 3.73W
- Package Thermal Resistance (Note 3)
  WQFN-48L 6x6, θ_{JA} ---------- 26.8°C/W
  WQFN-48L 6x6, θ_{JC} ---------- 1.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 5)

- Supply Input Voltage, V5V ---------- 4.5V to 5.5V
- Supply Input Voltage, VIN ---------- 7V to 58V
- VSU, VSV, VSW to COM ---------- –3V to 58V
- VBU, VBV, VBW to COM ---------- –3V to 68V
- Driver Supply Voltage, VDRV ---------- 6.6V to 12V
- LDO Supply Voltage, VILDO ---------- 6.6V to 12V
- LDO Capacitor on V1P8 ---------- 1µF
- Minimum Time Period of RSTN, t_{RSTN} ---------- 100µs
- Ambient Temperature Range ---------- –40°C to 105°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{V5V} = 5V, V_{VIN} = 24V, $V_{DRVH/L}$ = 7V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Section						
System Frequency	f_{SCLK}		58.8	60	61.2	MHz
Slow Clock for Sleep Mode	f_{LCLK}		77.6	80	82.4	kHz
Power Management						
VIN Quiescent Current	I_{VIN_Q}		--	1.7	--	mA
VIN Operating Current	I_{VIN_OP}		--	32	--	mA
V_{V5V} Under-Voltage Lockout Threshold (On)	V_{V5V_UVLON}		4	4.2	4.4	V
V_{V5V} UVLO Off Threshold	V_{V5V_UVLOFF}		3.6	3.8	4	V
V_{V5V} UVLO Hysteresis	V_{V5V_HYS}		--	0.4	--	V
LDO Output for Internal Operation Voltage	V_{V1P8}		--	1.8	--	V
V_{V5V} Current at Operation Mode	I_{V5V_OPER}	20kHz PWM output	--	30	--	mA
V_{V5V} Current at Normal Sleep Mode	I_{V5V_NSLP}		--	9	--	mA
V_{V5V} Current at Deep Sleep Mode	I_{V5V_DSLP}		--	750	--	μA
ADC Section (0V to 3V, 10-bit, Single End Mode, Gain = 1) (Note 7)						
Minimum Conversion Voltage	V_{I_MIN}	Code 000h	--	0	--	V
Maximum Conversion Voltage	V_{I_MAX}	Code 3FFh	--	3	--	V
SCDAC Section (0V to 1.2V, 8-bit for Short Current) (Note 7)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	1.2	--	V
DAC Offset	V_{OFFSET}		--	4	--	LSB
CSUMDAC Section (0V to 0.6V, 8-bit for Current Sum) (Note 7)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	0.6	--	V
DAC Offset	V_{OFFSET}	4LSB	--	4	--	LSB
VDAC Section (0V to 3V, 8-bit for General Purposed Comparator) (Note 7)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	3	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DAC Offset	V_{OFFSET}		--	4	--	LSB
Output Resistance of DAC	R_O	(Note 8)	--	5.4	--	kΩ
Current Limit Comparator (Short Circuit) (Note 8)						
Input Voltage Range of Comparator	V_{IN}		0	--	1.2	V
Comparator Offset	V_{OFFSET}		–15	0	15	mV
Current Limit Comparator (Current Sum) (Note 8)						
Input Voltage Range of Comparator	V_{IN}		0	--	0.6	V
Comparator Offset	V_{OFFSET}		–15	0	15	mV
General Purposed Comparator (Level Comparator) (Note 8)						
Input Voltage Range of Comparator	V_{IN}		0.5	--	3	V
Comparator Offset	V_{OFFSET}		–20	0	20	mV
IO of P0_6 to P0_7						
Positive Going Threshold Voltage	V_{IH}		2.6	2.85	3.1	V
Negative Going Threshold Voltage	V_{IL}		1.6	1.85	2.1	V
Hysteresis (V_{IH} – V_{IL})	V_{HYS}		--	1	--	V
Pull-Down Resistor	R_{DOWN}		--	100	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of P0_8 to P0_9						
Input High Voltage	V_{IH}		2.6	2.85	3.1	V
Input Low Voltage	V_{IL}		1.6	1.85	2.1	V
Hysteresis (V_{IH} – V_{IL})	V_{HYS}		--	1	--	V
Pull-Up Resistor	R_{UP}		--	73	--	kΩ
Pull-Down Resistor	R_{DOWN}		--	40	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of P0_10 to P0_11						
Input High Voltage	V_{IH}		2.6	2.85	3.1	V
Input Low Voltage	V_{IL}		1.6	1.85	2.1	V
Hysteresis (V_{IH} – V_{IL})	V_{HYS}		--	1	--	V
Pull-Up Resistor	R_{UP}		--	73	--	kΩ
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of P0_15 (Open Drain)						
Input High Voltage	V_{IH}		2.1	2.3	2.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0.5	0.7	0.9	V
Hysteresis (V_{IH} – V_{IL})	V_{HYS}		--	1.6	--	V
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of RSTN						
Input High Voltage	V_{IH}		2	2.3	3	V
Input Low Voltage	V_{IL}		0.3	0.425	0.7	V
Hysteresis (V_{IH} – V_{IL})	V_{HYS}		--	1.875	--	V
IO of AD0 to AD5						
Time Constant of Input RC Filter	t_{AD0-5_RC}		--	60	--	ns
IO of AD6 to AD7						
Time Constant of Input RC Filter	t_{AD6-7_STEP1}	Set Registor AD6/7_FLT = 0, AD6/7_DIV = 0	--	6	--	µs
Time constant of 2-Steps Input RC Filter	t_{AD6-7_STEP2}	Set Registor AD6/7_FLT = 1, AD6/7_DIV = 0	--	125	--	µs
Voltage Divider of Input Resistor	D_{IV_RATIO}	(R_{UP} + R_{DOWN}) / R_{DOWN}	2.91	3	3.09	--
Positive Going Threshold Voltage	V_{IH}		2.5	2.75	3	V
Negative Going Threshold Voltage	V_{IL}		1.5	1.8	2.1	V
IO of AD8 to AD9						
Time Constant of Input RC Filter	t_{AD8-9_RC}		--	4.5	--	µs
Positive Going Threshold Voltage	V_{IH}		2.6	2.75	2.9	V
Negative Going Threshold Voltage	V_{IL}		1.6	--	2	V
Current Source for External Bias	I_{BIAS}		97	100	103	µA
I^2C Interface						
I^2C Clock	f_{I2C}		100	--	400	kHz
Buck Converter						
VIN Under-Voltage Lockout Threshold (On)	V_{IN_UVLON}		5.8	6.3	6.8	V
VIN Under-Voltage Lockout Threshold (Off)	V_{IN_UVLOFF}		5.3	5.8	6.3	V
VIN Under-Voltage Lockout Hysteresis	V_{IN_HYS}		--	500	--	mV
Rdson (High-Side)	$R_{DS(ON)\_H}$		1	3	5	Ω
Rdson (Low-Side)	$R_{DS(ON)\_L}$		1	3	5	Ω
FB UVP for Over Load or Short Circuit	V_{FB_UVP}		0.43	0.47	0.51	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVP Blanking Time	t_{BLK}		18.5	27	35.5	ms
High-Side Peak Current Limit	I_{PK_H}	VIN < 21V, VFB = 0.6V	--	225	--	mA
		VIN ≥ 23V, VFB = 0.6V	--	120	--	
Feedback Comparator Trip Voltage	V_{FB}		0.76	0.8	0.84	V
Feedback Comparator Hysteresis	V_{FB_HYS}		--	5	--	mV
High-Side and Low-Side Driver Section						
High-Side Under-Voltage Lockout Threshold (On)	V_{HS_UVLON}		2.9	3.2	3.5	V
High-Side Under-Voltage Lockout Threshold (Off)	V_{HS_UVLOFF}		2.7	3	3.3	V
Low-Side Under-Voltage Lockout Threshold (On)	V_{LS_UVLON}		4	4.25	4.5	V
Low-Side Under-Voltage Lockout Threshold (Off)	V_{LS_UVLOFF}		3.85	4.05	4.25	V
High/Low-side Under-Voltage Lockout Hysteresis	V_{H/LS_HYS}		--	200	--	mV
VDRV Operating Current	I_{VDRV_OP}	f_S = 20kHz (no load)	--	0.5	1	mA
VBSx Quiescent Current	I_{BSX_Q}	HOU/V/W = 0, 3-channels	--	375	600	μA
Bootstrap Diode Forward Voltage	V_{F_BOOT}	Id = 5mA	--	0.8	--	V
		Id = 0.1A	--	2.9	--	
High-Side Output Voltage	V_{OH}	IO = 0mA, VVBU/V/W - VHOU/V/W, VVDRV - VLOU/V/W	--	50	200	mV
Low-Side Output Voltage	V_{OL}	IO = 0mA, VHOU/V/W - VVSU/V/W, VLOU/V/W - VCOM	--	20	100	mV
HOU/V/W and LOU/V/W Sourcing Current	I_{O+}	Gate driver pull high, VBS = 7V VHOU/V/W = VLOU/V/W = 0V	--	200	--	mA
HOU/V/W and LOU/V/W Sinking Current	I_{O-}	Gate driver pull low, VHOU/V/W = VLOU/V/W = 7V	--	500	--	mA
Turn-On Propagation Delay	t_{ON}		50	115	250	ns
Turn-Off Propagation Delay	t_{OFF}		50	115	250	ns
Delay Matching	MT		--	--	150	ns
5V LDO Section						
VILDO Under-Voltage Lockout Threshold (On)	V_{ILDO_UVLON}		5.1	5.6	6.1	V
VILDO Under-Voltage Lockout Threshold (Off)	V_{ILDO_UVLOFF}		4.6	5.1	5.6	V
VILDO Under-Voltage Lockout Hysteresis	V_{ILDO_HYS}		--	500	--	mV
Output Short Current	I_{SC}	V5V connect to GND, V_{VILDO} = 7V	60	--	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (V5V)	V_{V5V}	V_{VILDO} = 7V, I_{LOAD} = 0 to 30mA	4.85	5	5.15	V

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. The programming may fail with under 8V V_{VPP}, and over 8.2V V_{VPP} may cause permanent damage to the device.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precaution is recommended.

Note 5. The device is not guaranteed to function outside its operating conditions.

Note 6. Characterized, not tested at manufacturing.

Note 7. This parameter is guaranteed by design.

Application Information

Buck Converter

The RT7083 contains a high-efficiency synchronous step-down (Buck) DC-DC converter with input range from 7V to 58V. This Buck converter implements Hysteresis Mode control adopting Boundary Conduction Mode (BCM) featuring the low quiescent current and high-side peak current limitation.

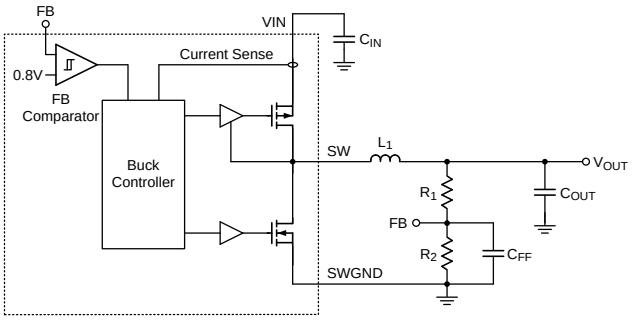


Figure 1. Buck Regulator

Table 1. Recommended Value for Buck Regulator

V_{OUT} (V)	7.3
C_{OUT} (μF)	4.7
R_1 (kΩ)	220
R_2 (kΩ)	27
C_{FF} (pF)	47

Output Voltage Setting for Feedback Network

The resistive feedback (FB) divider allows the Buck converter to regulate its output voltage.

Thus, the output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where V_{REF} is the reference voltage (0.8V typ.).

The selection of inductance value is suggested by Table 2 when use with different V_{IN} values.

Table 2. Inductor Selection

$V_{IN(MAX)}$ (V)	Under 30V	Over 30V
L (μH)	10	22
I_{sat} (mA)	> 400mA	

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-48L 6x6 package, the thermal resistance, θ_{JA}, is 26.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (26.8°C/W) = 3.73W for a WQFN-48L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 2 allows the designer to estimate the effect of rising ambient temperature on the maximum power dissipation.

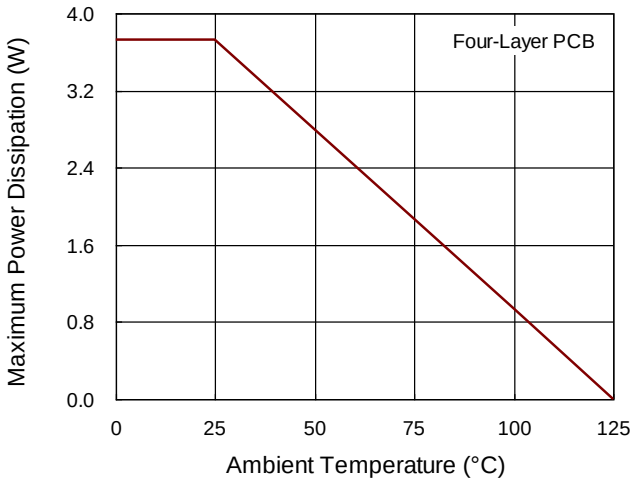
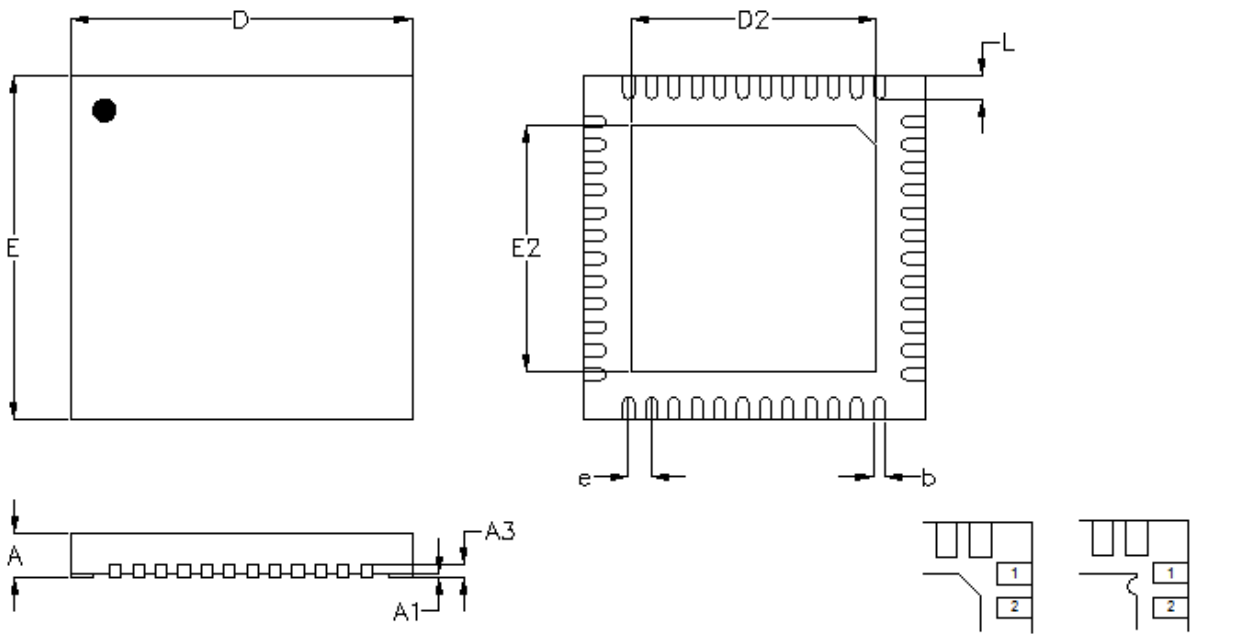


Figure 2. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

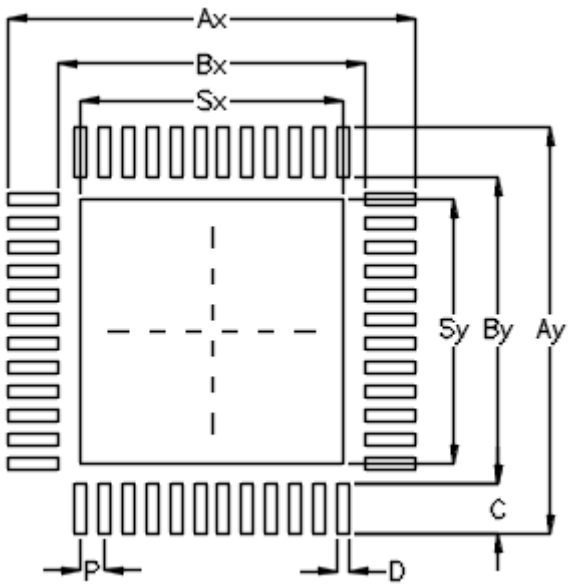
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		5.950	6.050	0.234	0.238
D2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
	Option 3	4.650	4.750	0.183	0.187
E		5.950	6.050	0.234	0.238
E2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
	Option 3	4.650	4.750	0.183	0.187
e		0.400		0.016	
L		0.350	0.450	0.014	0.018

W-Type 48L QFN 6x6 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN6x6-48	Option1	48	0.40	6.80	6.80	5.10	5.10	0.85	0.20	4.40	4.40	±0.05
	Option2									4.50	4.50	
	Option3									4.70	4.70	

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

单击下面可查看定价，库存，交付和生命周期等信息

>>Richtek(台湾立锜)