5.5A, 18V, 650kHz, ACOT™ Synchronous Step-Down Converter

General Description

The RT6206A is a synchronous step-down DC/DC converter with Advanced Constant On-Time (ACOT™) mode control. It achieves high power density to deliver up to 5.5A output current from a 4.5V to 18V input supply. The proprietary ACOT™ mode offers an optimal transient response over a wide range of loads and all kinds of ceramic capacitors, which allows the device to adopt very low ESR output capacitor for ensuring performance stabilization. In addition, RT6206A keeps an excellent constant switching frequency under line and load variation and the integrated synchronous power switches with the ACOT™ mode operation provides high efficiency in whole output current load range. Cycle-by-cycle current limit provides an accurate protection by a valley detection of low side MOSFET and external soft-start setting eliminates input current surge during startup. Protection functions include thermal shutdown for RT6206A.

The RT6206A are available in the TSSOP-14 (Exposed pad), SOP-8 (Exposed Pad) and WDFN-10L 3x3 packages.

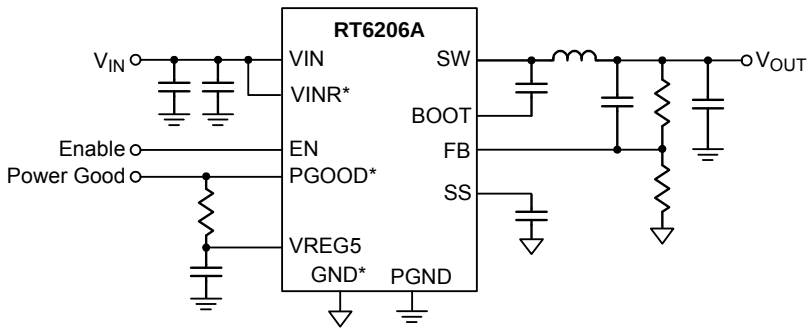
Features

- **ACOT™ Mode Enables Fast Transient Response**
- **4.5V to 18V Input Voltage Range**
- **5.5A Output Current**
- **35mΩ Internal Low Side N-MOSFET**
- **Advanced Constant On-Time Control**
- **Support All Ceramic Capacitors**
- **Up to 95% Efficiency**
- **Adjustable Output Voltage from 0.765V to 7V**
- **Adjustable Soft-Start**
- **Cycle-by-Cycle Current Limit**
- **Input Under-Voltage Lockout**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

Simplified Application Circuit



* : VINR, GND pin for TSSOP-14 (Exposed Pad) only.

* : PGOOD pin for TSSOP-14 (Exposed Pad) and WDFN-10L 3x3 only.

Ordering Information

RT6206A □□□

- Package Type
  CP : TSSOP-14 (Exposed Pad)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Trim Operation
  L : Latch-Off
- PWM/PSM Mode
  A : Force-PWM

RT6206A □□□

- Package Type
  SP : SOP-8 (Exposed Pad-Option 2)
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Trim Operation
  H : Hiccup
- PWM/PSM Mode
  A : Force-PWM

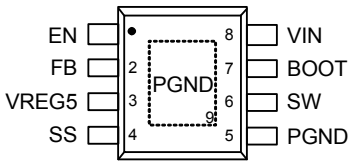
Note :

Richtek products are :

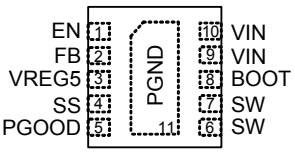
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

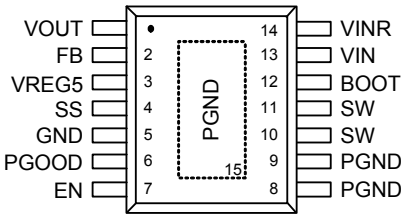
(TOP VIEW)



SOP-8 (Exposed Pad)



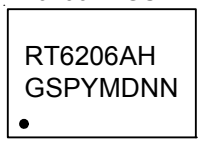
WDFN-10L 3x3



TSSOP-14 (Exposed Pad)

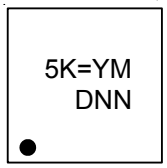
Marking Information

RT6206AHGSP



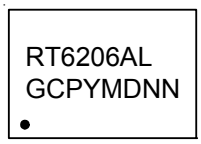
RT6206AHGSP : Product Number
YMDNN : Date Code

RT6206AHGQW



5K= : Product Code
YMDNN : Date Code

RT6206ALGCP

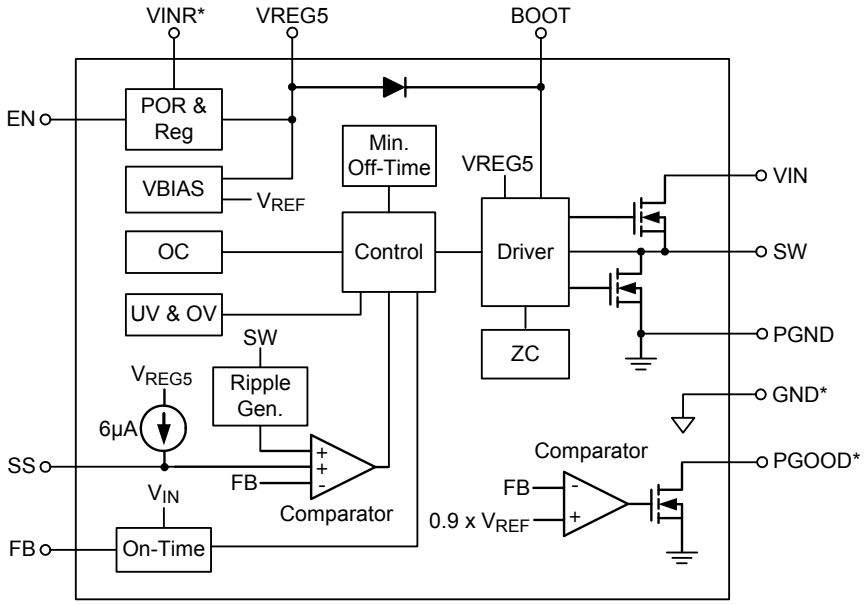


RT6206ALGCP : Product Number
YMDNN : Date Code

Functional Pin Description

Pin No.			Pin Name	Pin Function
TSSOP-14 (Exposed Pad)	SOP-8 (Exposed Pad)	WDFN-10L 3x3		
1	--	--	VOUT	Optional Output Voltage Discharge Connection. This open drain output connects to ground when the device is disabled. If output voltage discharge is desired, connect VOUT to the output voltage.
2	2	2	FB	Feedback Voltage Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback threshold voltage is 0.765V typically.
3	3	3	VREG5	Internal Regulator Output. Connect a 1μF capacitor to GND to stabilize output voltage.
4	4	4	SS	Soft-Start Time Setting. Connect an external capacitor between this pin and GND to set the soft- start time.
5	--	--	GND	Analog Ground.
6	--	5	PGOOD	Open Drain Power Good Indicator Output.
7	1	1	EN	Enable Control Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
8, 9, 15 (Exposed Pad)	5, 9 (Exposed Pad)	11 (Exposed Pad)	PGND	Power Ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.
10, 11	6	6, 7	SW	Switch Node. Connect this pin to an external L-C filter.
12	7	8	BOOT	Bootstrap Supply for High Side Gate Driver. Connect a 0.1μF capacitor between the BOOT and SW pin.
13	8	9, 10	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large (≥ 10μF x 2) ceramic capacitor.
14	--	--	VINR	Internal Linear Regulator Supply Input. For the TSSOP-14 (Exposed Pad) package, VINR supplies power for the internal linear regulator that powers the IC. Connect VIN to the input voltage and bypass to ground with a 0.1μF ceramic capacitor.

Function Block Diagram



* : VINR, GND pin for TSSOP-14 (Exposed Pad) only.

* : PGOOD pin for TSSOP-14 (Exposed Pad) and WDFN-10L 3x3 only.

Operation

The RT6206A is a synchronous step-down converter with advanced constant on-time control mode. Using the ACOT™ control mode can reduce the output capacitance and provide fast transient response. It can minimize the component size without additional external compensation network.

Internal Regulator

The regulator provides 5.1V power to supply the internal control circuit. Connecting a 1μF ceramic capacitor for decoupling and stability is required.

Soft-Start

In order to prevent the converter output voltage from overshooting during the startup period, the soft-start function is necessary. The soft-start time is adjustable and can be set by an external capacitor.

UVLO Protection

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage of VIN is lower than the UVLO falling threshold voltage, the device will be latch-off.

Thermal Shutdown

When the junction temperature exceeds the OTP threshold value, the IC will shut down the switching operation. Once the junction temperature cools down and is lower than the OTP lower threshold, the converter will automatically resume switching

Power Good (for TSSOP-14 (Exposed Pad) and WDFN-10L 3x3 only)

After soft-start is finished, the power good function will be activated. When the FB is activated, the PGOOD will become an open-drain output. If the FB is below, the PGOOD pin will be pulled low.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN, VINR ---------- –0.3V to 20V
- Switch Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
  < 10ns ---------- –5V to 25V
- BOOT to SW ---------- –0.3V to 6V
- EN, VOUT ---------- –0.3V to 20V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  TSSOP-14 (Exposed Pad) ---------- 2.5W
  SOP-8 (Exposed Pad) ---------- 2.041W
  WDFN-10L 3x3 ---------- 1.667W
- Package Thermal Resistance (Note 2)
  TSSOP-14 (Exposed Pad), θ_{JA} ---------- 40°C/W
  SOP-8 (Exposed Pad), θ_{JA} ---------- 49°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
  WDFN-10L 3x3, θ_{JA} ---------- 60°C/W
  WDFN-10L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

Recommended Operating Conditions (Note 3)

- Supply Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	1	10	μA
Quiescent Current		I_Q	V_{EN} = 5V, V_{FB} = 0.8V	--	1	1.3	mA
Logic Threshold							
EN Input Voltage	Logic-High			2	--	18	V
	Logic-Low			--	--	0.4	
V_{FB} Voltage							
Feedback Threshold Voltage		V_{FB}	T_A = 25°C	0.757	0.765	0.773	V
			T_A = –40°C to 85°C	0.755	--	0.775	
Feedback Input Current		I_{FB}	V_{FB} = 0.8V	--	0.01	0.1	μA
V_{REG5} Output							
V_{REG5} Output Voltage		V_{REG5}	6V ≤ V_{IN} ≤ 18V, 0 < I_{VREG5} < 5mA	4.8	5.1	5.4	V
Line Regulation			6V ≤ V_{IN} ≤ 18V, I_{VREG5} = 5mA	--	--	20	mV

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Load Regulation			$0 < I_{VREG5} < 5mA$	--	--	100	mV
Output Current		I_{VREG5}	V_{IN} = 6V, V_{REG5} = 4V, T_A = 25°C	--	70	--	mA
$R_{DS(ON)}$							
Switch On Resistance	High-Side	$R_{DS(ON)\_H}$	(V_{BOOT} – V_{SW}) = 5.5V	--	80	--	mΩ
	Low-Side	$R_{DS(ON)\_L}$		--	35	--	
Current Limit							
Current Limit		I_{LIM}		5.8	6.9	8.4	A
Thermal Shutdown							
Thermal Shutdown Threshold		T_{SD}	Shutdown Temperature	--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	
On-Time Timer Control							
On-Time		t_{ON}	V_{OUT} = 1.05V	--	135	--	ns
Minimum Off-Time		$t_{OFF(MIN)}$	V_{FB} = 0.7V	--	260	310	ns
Soft-Start							
SS Charge Current			V_{SS} = 0V	--	6	--	μA
SS Discharge Current			V_{SS} = 0.5V (Latch Mode)	0.1	0.2	--	mA
			V_{SS} = 0.5V (Hiccup Mode)	--	0.5	--	μA
UVLO							
UVLO Threshold			Wake Up V_{REG5}	3.6	3.85	4.1	V
Hysteresis				0.16	0.35	0.47	
Output Under Voltage and Over Voltage Protection							
OVP Trip Threshold			OVP Detect	115	120	125	%
OVP Prop Delay				--	5	--	μs
UVP Trip Threshold				65	70	75	%
UVP Hysteresis				--	10	--	
UVP Prop Delay				--	250	--	μs
UVP Enable Delay		t_{UVPEN}	Relative to Soft-Start Time	--	t_{SS} x 1.7	--	ms
Power Good							
PGOOD Threshold			V_{FB} Rising	85	90	95	%
			V_{FB} Falling	--	85	--	
PGOOD Sink Current			PGOOD = 0.5V	2.5	5	--	mA

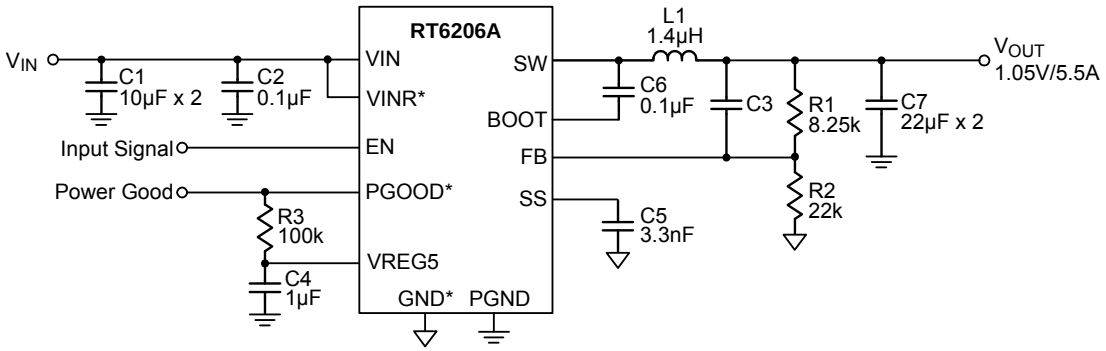
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



* : VINR, GND pin for TSSOP-14 (Exposed Pad) only.

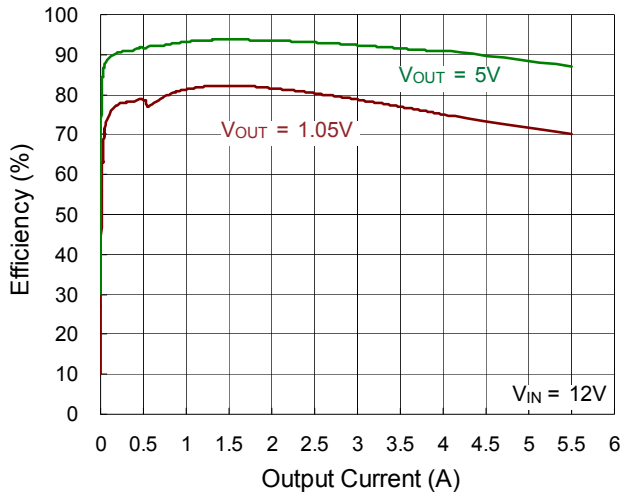
* : PGOOD pin for TSSOP-14 (Exposed Pad) and WDFN-10L 3x3 only.

Table 1. Suggested Component Values (V_{IN} = 12V)

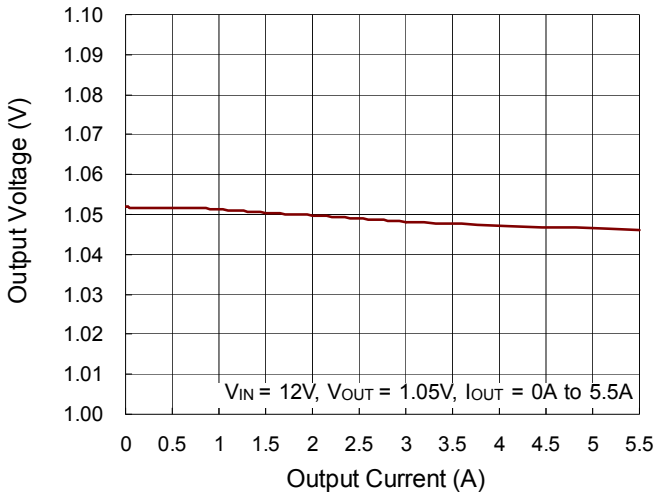
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C3 (pF)	L1 (µH)	C7 (µF)
1	6.81	22.1	--	1.4	22 to 68
1.05	8.25	22.1	--	1.4	22 to 68
1.2	12.7	22.1	--	1.4	22 to 68
1.8	30.1	22.1	5 to 22	2	22 to 68
2.5	49.9	22.1	5 to 22	2	22 to 68
3.3	73.2	22.1	5 to 22	2	22 to 68
5	124	22.1	5 to 22	3.3	22 to 68
7	180	22.1	5 to 22	3.3	22 to 68

Typical Operating Characteristics

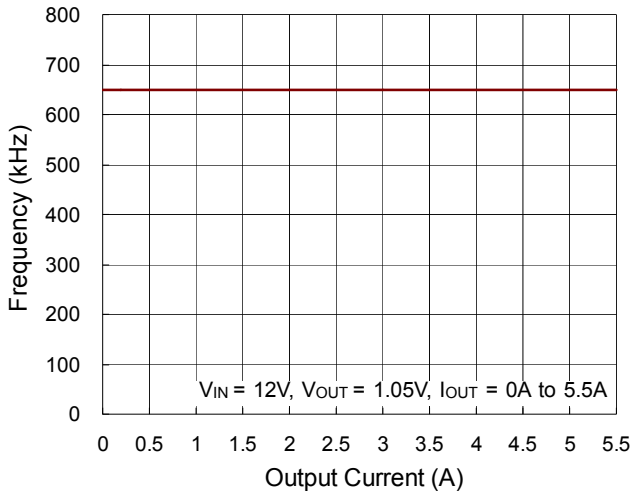
Efficiency vs. Output Current



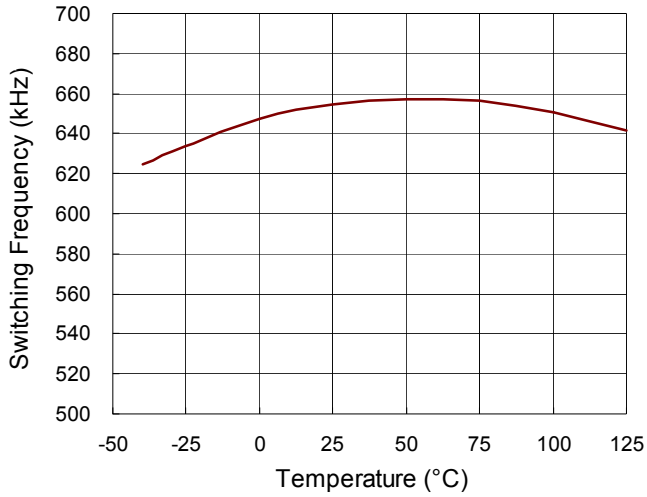
Output Voltage vs. Output Current



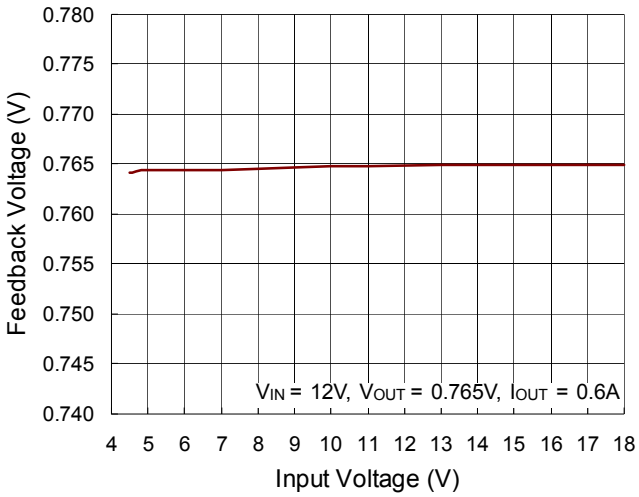
Switching Frequency vs. Output Current



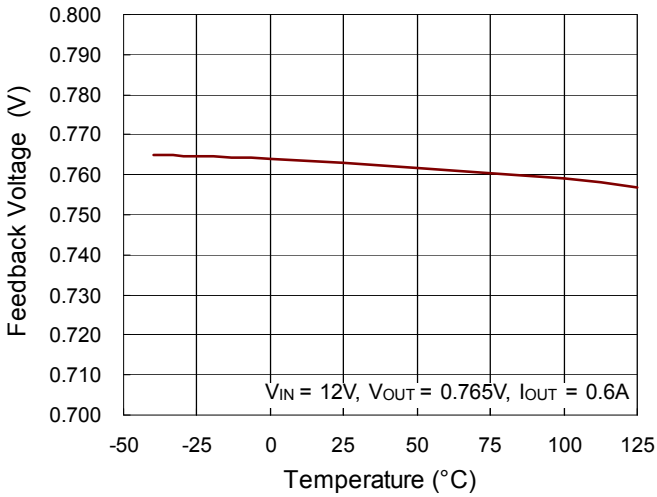
Switching Frequency vs. Temperature



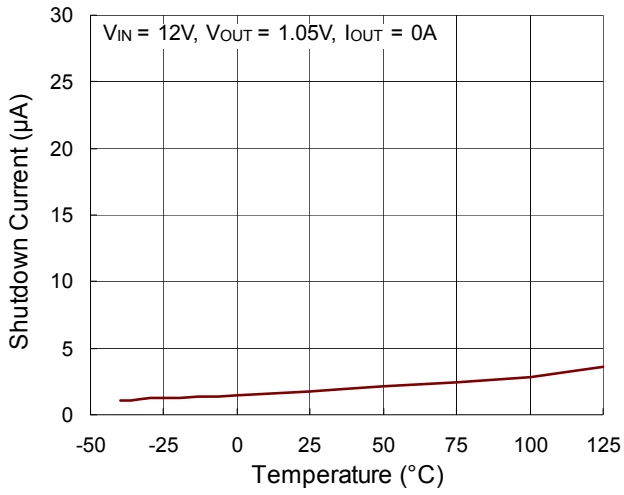
Feedback Voltage vs. Input Voltage



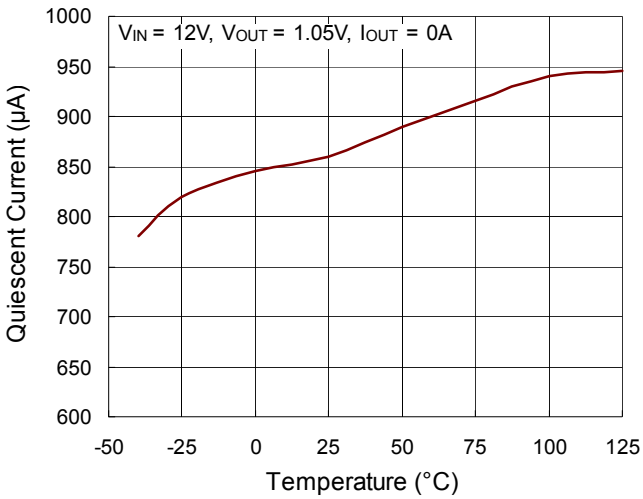
Feedback Voltage vs. Temperature



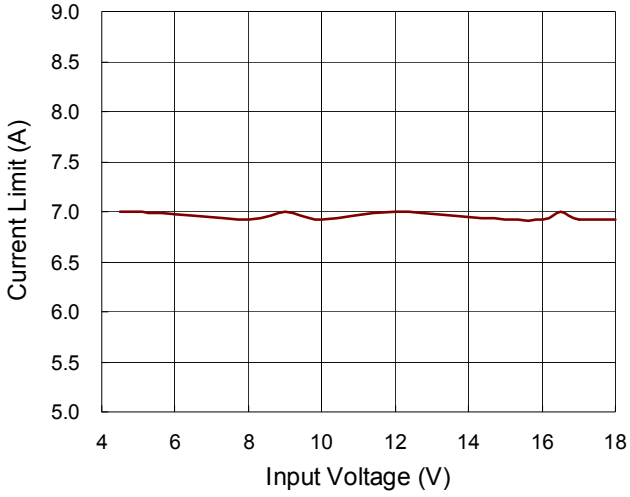
Shutdown Current vs. Temperature



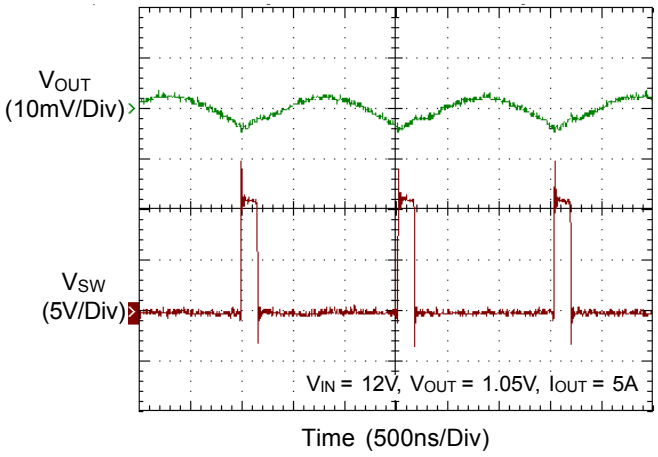
Quiescent Current vs. Temperature



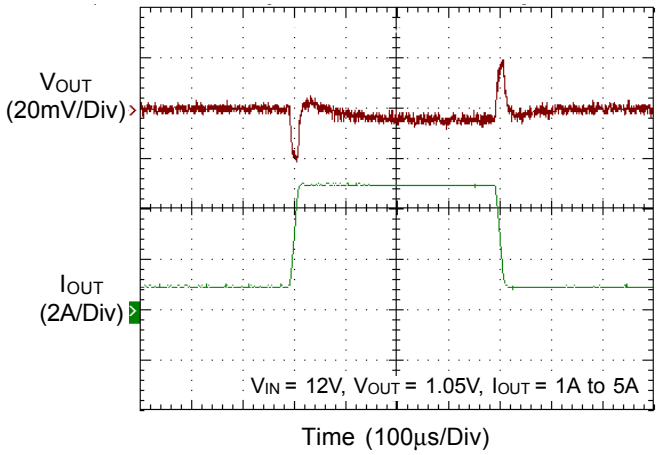
Current Limit vs. Input Voltage



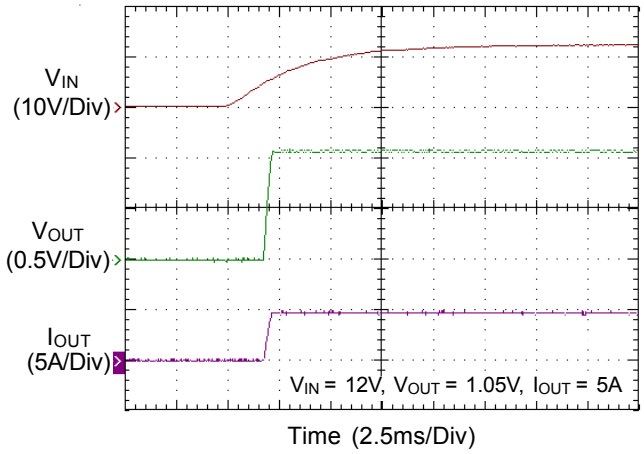
Output Ripple Voltage



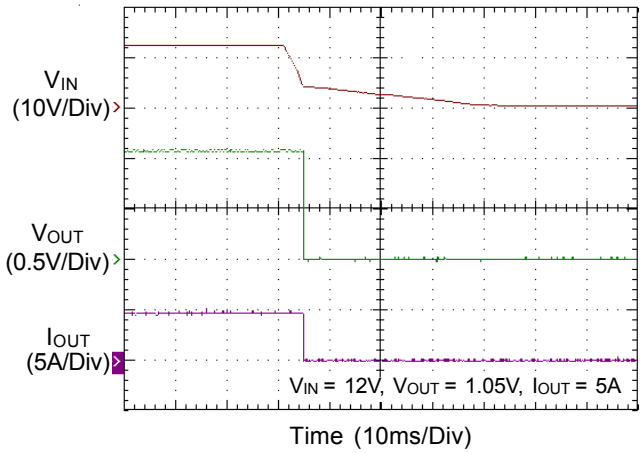
Load Transient Response



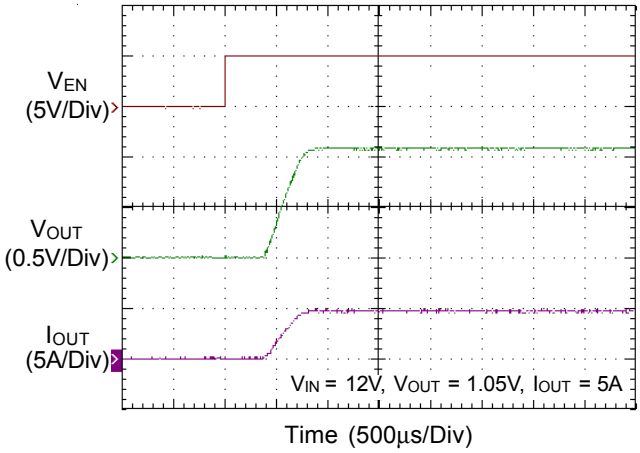
Power On from VIN



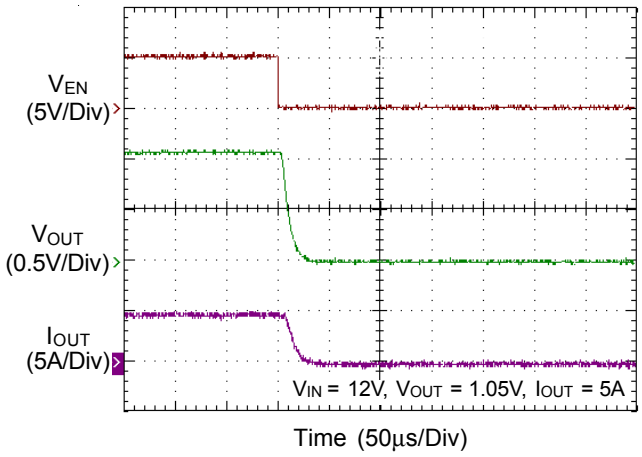
Power Off from VIN



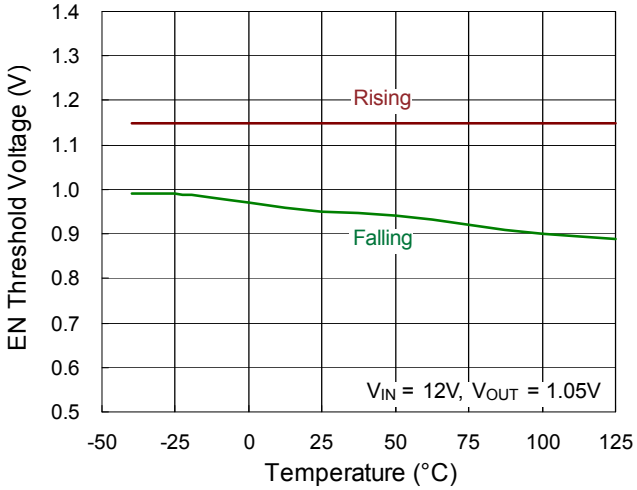
Power On from EN



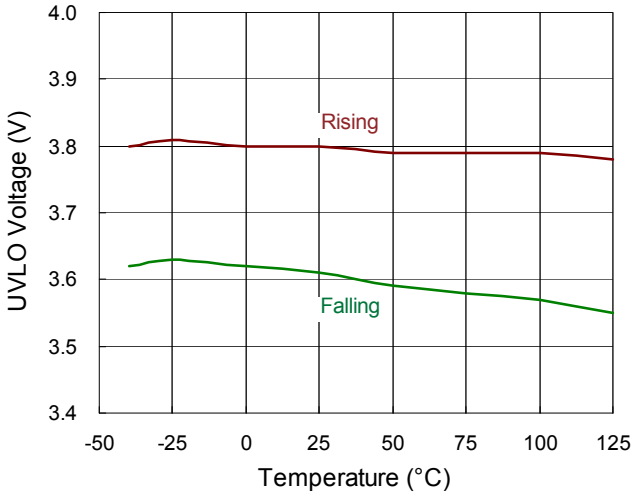
Power Off from EN



EN Threshold Voltage vs. Temperature



UVLO vs. Temperature



Application Information

The RT6206A is a synchronous high voltage Buck converter that can support the input voltage range from 4.5V to 18V and the output current up to 5.5A. It adopts ACOT™ mode control to provide a very fast transient response with few external compensation components.

PWM Operation

It is suitable for low external component count configuration with appropriate amount of Equivalent Series Resistance (ESR) capacitors at the output. The output ripple valley voltage is monitored at a feedback point voltage. The synchronous high side MOSFET is turned on at the beginning of each cycle. After the internal on-time expires, the MOSFET is turned off. The pulse width of this on-time is determined by the converter's input and output voltages to keep the frequency fairly constant over the entire input voltage range.

Advanced Constant On-Time Control

The RT6206A has a unique circuit which sets the on-time by monitoring the input voltage and SW signal. The circuit ensures the switching frequency operating at 650kHz over input voltage range and loading range.

Soft-Start

The RT6206A contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing is the output voltage rising time from 0V to settled level and can be programmed by the external capacitor between the SS and GND pins. The chip provides a 6μA charge current for the external capacitor. If a 3.9nF capacitor is used, the soft-start will be 0.5ms (typ.). The available capacitance range is from 2.7nF to 220nF.

$$t_{SS}\ (ms) = \frac{C5\ (nF) \times 0.765V}{I_{SS}\ (\mu A)}$$

Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the RT6206A's quiescent current drops to lower than 10μA. Driving the EN pin high (>2V, <18V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a R_{EN} resistor and C_{EN} capacitor from the VIN pin (see Figure 1).

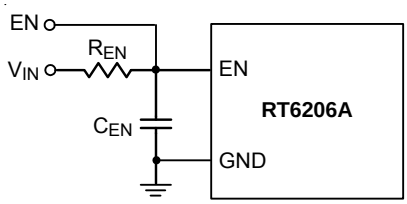


Figure 1. External Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2V is available, as shown in Figure 2. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between the V_{IN} and EN pins. MOSFET Q1 will be under logic control to pull down the EN pin.

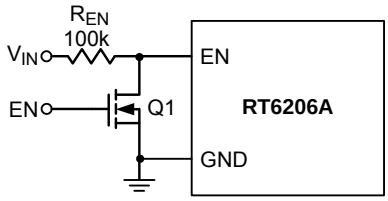


Figure 2. Digital Enable Control Circuit

To prevent enabling circuit when V_{IN} is smaller than the V_{OUT} target value, a resistive voltage divider can be placed between the input voltage and ground and connected to the EN pin to adjust IC lockout threshold, as shown in Figure 3. For example, if an 8V output voltage is regulated from a 12V input voltage, the resistor R_{EN2} can be selected to set input lockout threshold larger than 8V.

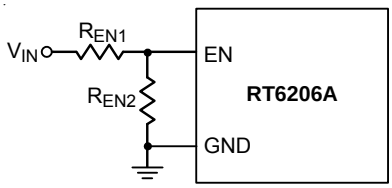


Figure 3. Resistor Divider for Lockout Threshold Setting

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 4.

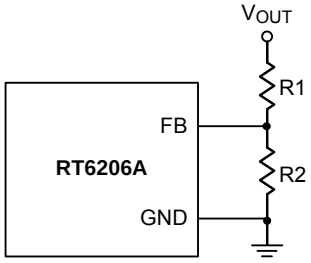


Figure 4. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation. It is recommended to use 1% tolerance or better divider resistors.

$$V_{OUT} = 0.765 \times (1 + \frac{R1}{R2})$$

Under Voltage Lockout Protection

The RT6206A has Under Voltage Lockout Protection (UVLO) that monitors the voltage of VIN pin. When the V_{IN} voltage is lower than UVLO threshold voltage, the RT6206A will be turned off in this state. This is non-latch protection.

Over Temperature Protection

The RT6206A equips an Over Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 25°C the main converter will resume operation. To keep operating at maximum, the junction temperature should be prevented from rising above 150°C.

Hiccup Mode UVP

A Hiccup Mode Under-Voltage Protection (UVP) function is provided for the SOP-8 (Exposed Pad) and WDFN-10L 3x3 packages. When the FB voltage drops below half of the feedback reference voltage, V_{FB}, the UVP function will be triggered and the RT6206A will shut down for a period of time before recovering automatically. The Hiccup Mode UVP can reduce input current in short-circuit conditions.

Latch off Mode UVP

The Latch off Under-Voltage Protection(UVP) function is provided for the TSSOP-14 (Exposed Pad) package. When the protection function is triggered, the IC will shutdown in Latch-Off Mode. The IC stops switching, leaving both switches open, and is latched off. To restart operation, toggle EN or power the IC off and then on again.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and an output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal. For the ripple current selection, the value of $\Delta I_L = 0.2(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Input and Output Capacitors Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. A low ESR input capacitor with larger ripple current rating should be used for the maximum RMS current. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the

input capacitor, two 10µF and 0.1µF low ESR ceramic capacitors are recommended.

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. The output ripple, ΔV_{OUT} , is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may need to meet the ESR and RMS current handling requirements.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. A sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

External Bootstrap Diode

Connect a 0.1µF low ESR ceramic capacitor between the BOOT and SW pins. This capacitor provides the gate driver voltage for the high side MOSFET. It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65%. The bootstrap diode can be a low cost one such as 1N4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT6206A. Note that the external boot voltage must be lower than 5.5V

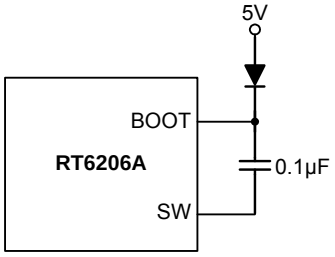


Figure 5. External Bootstrap Diode

Over Current Protection

When the output shorts to ground, the inductor current decays very slowly during a single switching cycle. An over current detector is used to monitor inductor current to prevent current runaway. The over current detector monitors the voltage between SW and GND during the low side MOS turn-on state. This is cycle-by-cycle protection.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TSSOP-14 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 40°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (40°C/W) = 2.5W for TSSOP-14 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (49°C/W) = 2.041W for SOP-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for WDFN-10L 3x3 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 6 allow the

designer to see the effect of rising ambient temperature on the maximum power dissipation.

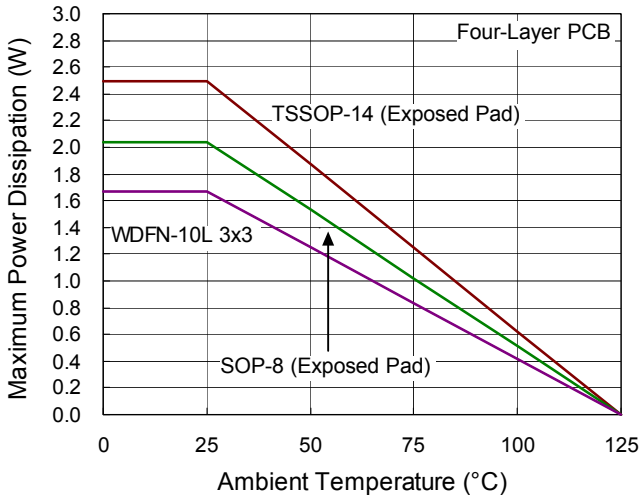


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT6206A

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT6206A FB pin.
- The GND and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

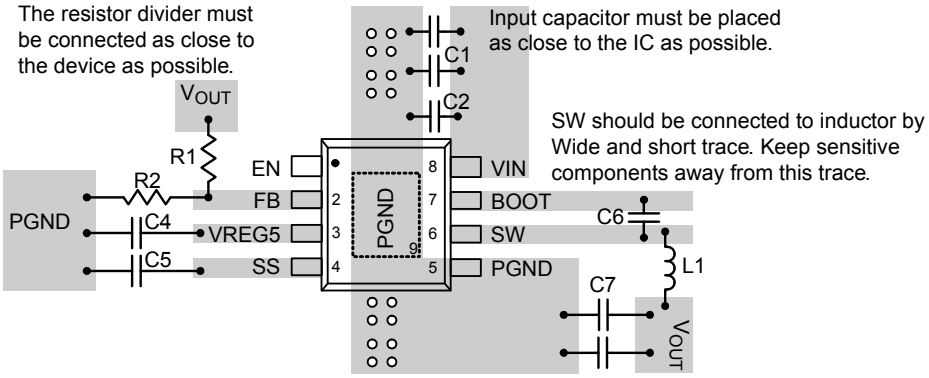


Figure 7. PCB Layout Guide for SOP-8 (Exposed Pad) Package

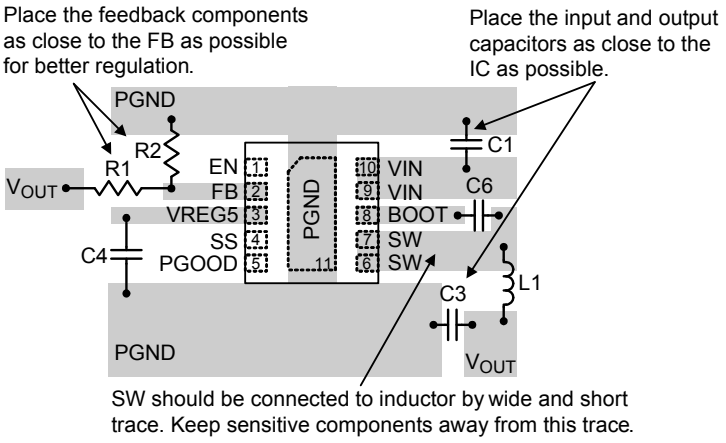


Figure 8. PCB Layout Guide for WDFN-10L 3x3 Package

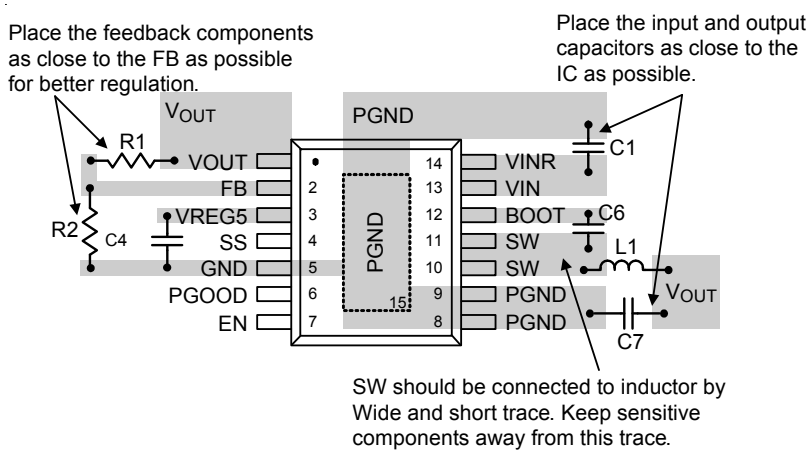
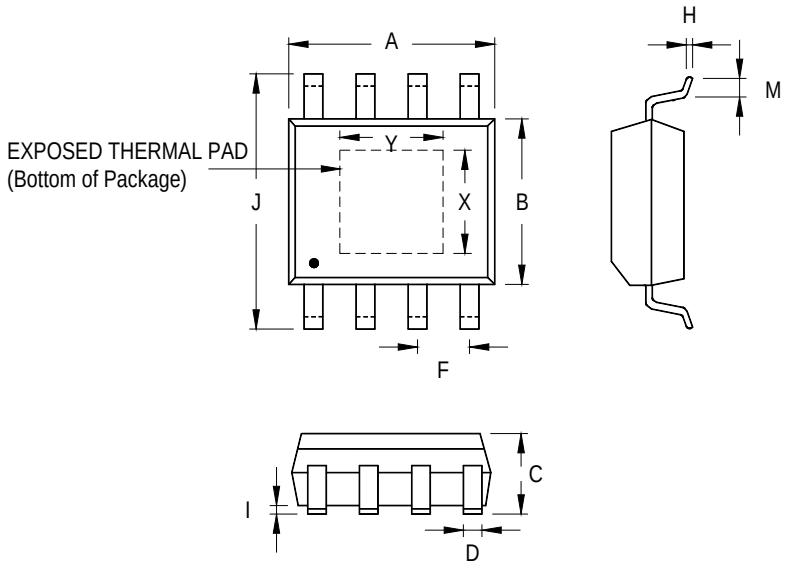


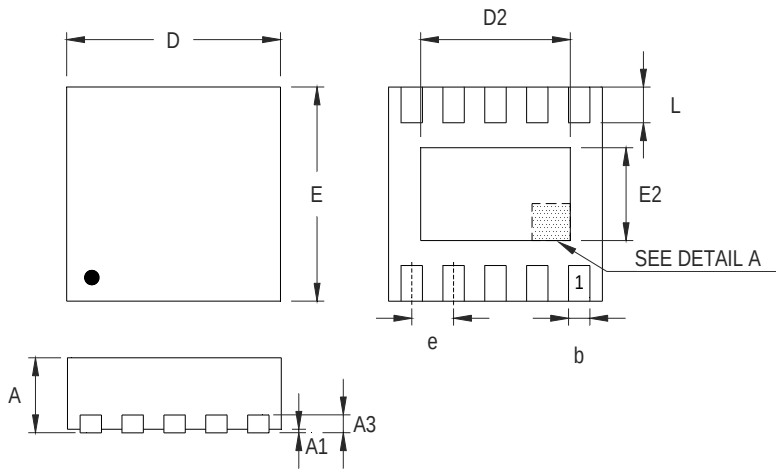
Figure 9. PCB Layout Guide for TSSOP-14 (Exposed Pad) Package

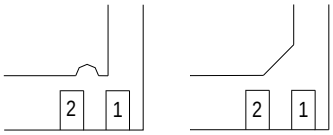
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package





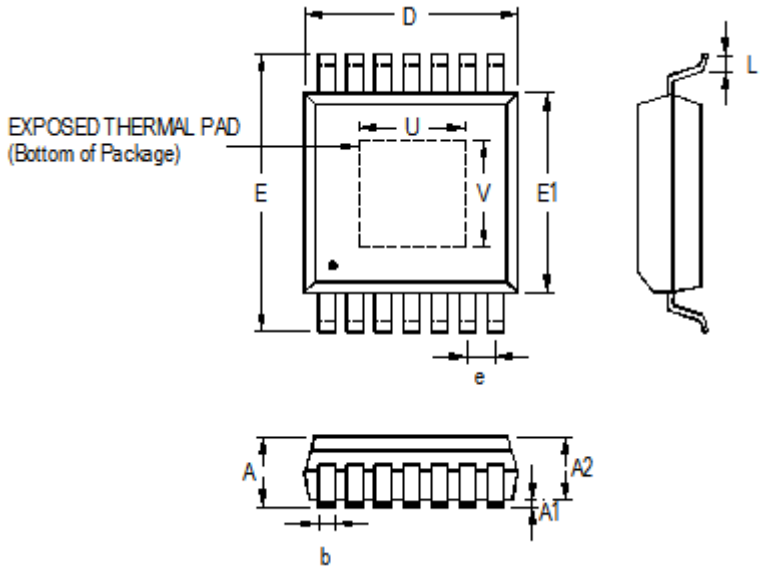
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.200	0.039	0.047
A1	0.000	0.150	0.000	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030
U	1.900	2.900	0.075	0.114
V	1.600	2.600	0.063	0.102

14-Lead TSSOP (Exposed Pad) Plastic Package

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单击下面可查看定价，库存，交付和生命周期等信息

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