Synchronous Rectified Buck MOSFET Drivers

General Description

The RT9611C/D is a high frequency, synchronous rectified, single phase dual MOSFET driver designed to adapt from normal MOSFET driving applications to high performance CPU VR driving capabilities.

The RT9611C/D can be utilized under both V_{CC} = 5V or V_{CC} = 12V applications. The RT9611C/D also builds in an internal power switch to replace external boot strap diode. The RT9611C/D can support switching frequency efficiently up to 500kHz. The RT9611C/D has the UGATE driving circuit and the LGATE driving circuit for synchronous rectified DC/DC converter applications. The driving rising/falling time capability is designed within 30ns and the shoot through protection mechanism is designed to prevent shoot through of high-side and low-side power MOSFETs. The RT9611C/D has PWM tri-state shut down and $\overline{OD}$ input shut down functions which can force driver output into high impedance.

The difference of the RT9611C and the RT9611D is the propagation delay, $t_{UGATEpdh}$. The RT9611D has comparatively larger $t_{UGATEpdh}$ than the RT9611D. Hence, the RT9611C is usually recommended to be utilized in performance oriented applications, such as high power density CPU VR or GPU VR.

The RT9611C/D is available in the small footprint WDFN-8L 3x3 package.

Features

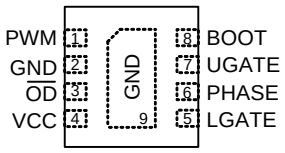
- **Drive Two N-MOSFETs**
- **Adaptive Shoot Through Protection**
- **Embedded Bootstrap Diode**
- **Support High Switching Frequency**
- **Fast Output Rising Time**
- **Tri-State Input for Bridge Shutdown**
- **Disable Control Input**
- **RoHS Compliant and Halogen Free**

Applications

- Core Voltage Supplies for Desktops, Motherboard CPUs
- High Frequency Low Profile DC/DC Converters
- High Current Low Voltage DC/DC Converters

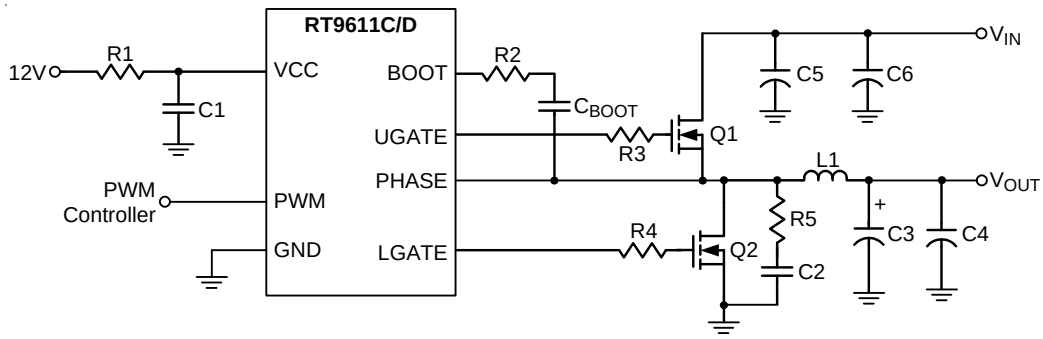
Pin Configurations

(TOP VIEW)



WDFN-8L 3x3

Simplified Application Circuit



Ordering Information

RT9611C/D□□

- Package Type
  QW : WDFN-8L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Long Dead Time
- Short Dead Time

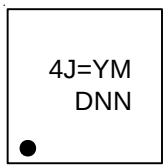
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

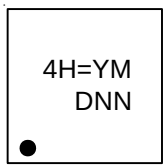
RT9611CGQW



4J= : Product Code

YMDNN : Date Code

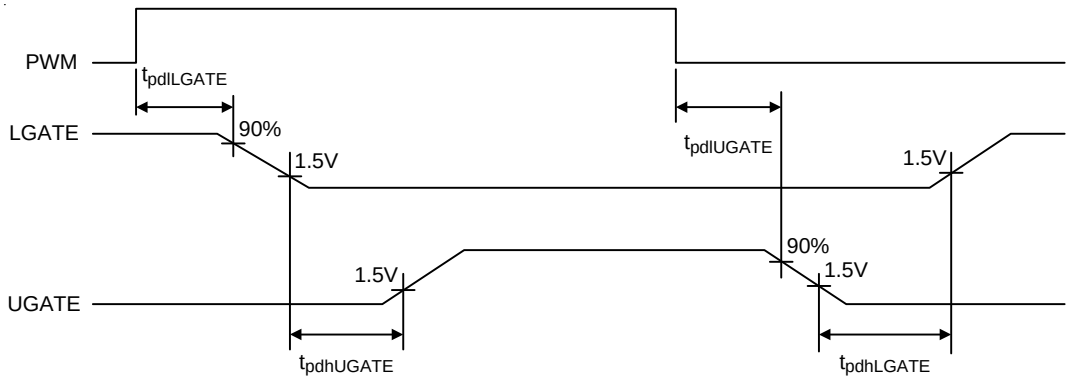
RT9611DGQW



4H= : Product Code

YMDNN : Date Code

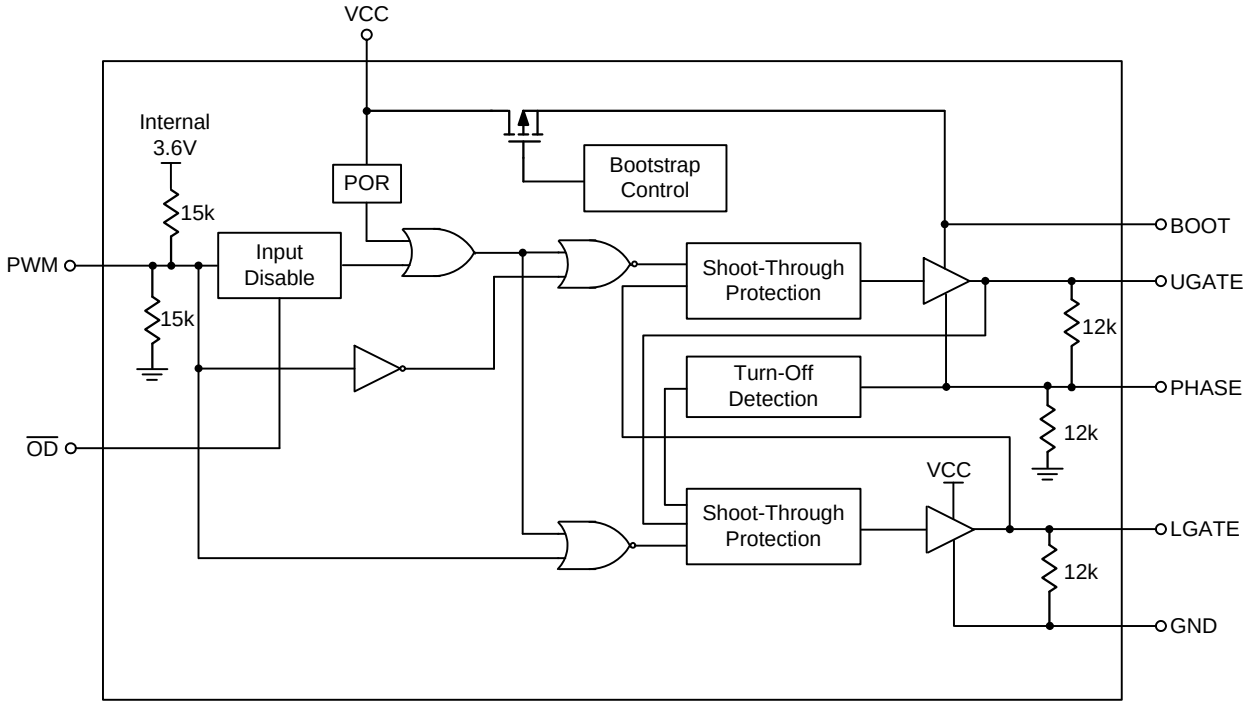
Timing Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PWM	Input PWM Signal for Controlling the Driver.
2, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	$\overline{OD}$	Output Disable. When pulled low, both UGATE and LGATE are driven low and the normal operation is disabled.
4	VCC	12V Supply Voltage Input.
5	LGATE	Low-Side Gate Driver Output. Connected to Gate of low-side power N-MOSFET.
6	PHASE	Switch Node. Connect this pin to the Source of the high-side MOSFET and the Drain of the low-side MOSFET.
7	UGATE	High-Side Gate Driver Output. Connected this pin to Gate of high-side power N-MOSFET.
8	BOOT	Bootstrap Supply for High-Side Gate Driver.

Function Block Diagram



Operation

POR (Power On Reset)

The POR block detects the voltage at the VCC pin. When the VCC pin voltage is higher than POR rising threshold, the POR block output is high. The POR output is low when VCC is not higher than POR rising threshold. When the POR block output is high, UGATE and LGATE can be controlled by PWM input voltage. If the POR block output is low, both UGATE and LGATE will be pulled to low.

Tri-State Detect

When both POR block output and EN pin voltages are high, UGATE and LGATE can be controlled by PWM input. There are three PWM input modes, which are high, low, and shutdown state. If PWM input is within the shutdown window, both UGATE and LGATE output are low. When PWM input is higher than its rising threshold, UGATE is high and LGATE is low. When PWM input is lower than its falling threshold, UGATE is low and LGATE is high.

Bootstrap Control

the Bootstrap Control block controls the integrated bootstrap switch. When LGATE is high (low-side MOSFET is turned on), the bootstrap switch is turned on to charge the bootstrap capacitor connected to the BOOT pin. When LGATE is low (low-side MOSFET is turned off), the bootstrap switch is turned off to disconnect the VCC pin and the BOOT pin.

Turn-Off Detection

The Turn-Off Detection block detects whether high-side MOSFET is turned off by monitoring the PHASE pin voltage. To avoid shoot-through between high-side and low-side MOSFETs, low-side MOSFET can be turned on only after high-side MOSFET is effectively turned off.

Shoot-Through Protection

The Shoot-Through Protection block implements the dead time when both high-side and low-side MOSFETs are turned off. With the Shoot-Through Protection block, high-side and low-side MOSFET are never turned on simultaneously. Thus, shoot-through between high-side and low-side MOSFETs is prevented.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VCC ---------- –0.3V to 15V
- BOOT to PHASE ---------- –0.3V to 15V
- PHASE to GND
  - DC ---------- –5V to 15V
  - < 200ns ---------- –10V to 30V
- LGATE
  - DC ---------- (GND – 0.3V) to (V_{CC} + 0.3V)
  - < 200ns ---------- –2V to (V_{CC} + 0.3V)
- UGATE ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - < 200ns ---------- (V_{PHASE} – 2V) to (V_{BOOT} + 0.3V)
- PWM Input Voltage ---------- (GND – 0.3V) to 7V
- $\overline{OD}$ ---------- (GND – 0.3V) to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-8L 3x3 ---------- 3.22W
- Package Thermal Resistance (Note 2)
  - WDFN-8L 3x3, θ_{JA} ---------- 31°C/W
  - WDFN-8L 3x3, θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 12V ±10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}		4.5	--	13.5	V
Power Supply Current	I_{VCC}	V_{BOOT} = 12V, PWM = 0V	--	1.2	--	mA
Power On Reset						
POR Threshold	V_{POR}	V_{CC} Rising	3	4	4.4	V
Hysteresis	V_{CC_hys}		--	0.5	--	V
PWM Input						
Maximum Input Current	I_{PWM}	PWM = 0V or 5V	--	300	--	µA
PWM Floating Voltage	V_{PWM_fl}		1.6	1.8	2	V
PWM Rising Threshold	V_{PWM_rth}		--	--	2.8	V
PWM Falling Threshold	V_{PWM_fth}		0.8	--	--	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Disable Input							
$\overline{OD}$ Rising Threshold		$V_{\overline{OD}\_rth}$		1	1.3	1.6	V
$\overline{OD}$ Hysteresis		$V_{\overline{OD}\_hys}$		--	0.3	--	V
Timing							
UGATE Rising Time		t_{UGATEr}	3nF load	--	25	--	ns
UGATE Falling Time		t_{UGATEf}	3nF load	--	12	--	ns
LGATE Rising Time		t_{LGATEr}	3nF load	--	24	--	ns
LGATE Falling Time		t_{LGATEf}	3nF load	--	10	--	ns
Propagation Delay	RT9611C	$t_{UGATEpdh}$	$V_{BOOT} - V_{PHASE}$ = 12V See Timing Diagram	--	22	--	ns
	RT9611D			--	60	--	
	RT9611C/D	$t_{UGATEpdl}$		--	22	--	
		$t_{LGATEpdh}$	See Timing Diagram	--	20	--	
		$t_{LGATEpdl}$		--	8	--	
Output							
UGATE Drive Source		$I_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$ = 12V $V_{UGATE} - V_{PHASE}$ = 12V	--	2	--	A
UGATE Drive Sink		$R_{UGATEsk}$	$V_{BOOT} - V_{PHASE}$ = 12V	--	1.4	--	Ω
LGATE Drive Source		$I_{LGATEsr}$	V_{LGATE} = 2V	--	2.2	--	A
LGATE Drive Sink		$R_{LGATEsk}$		--	1.1	--	Ω

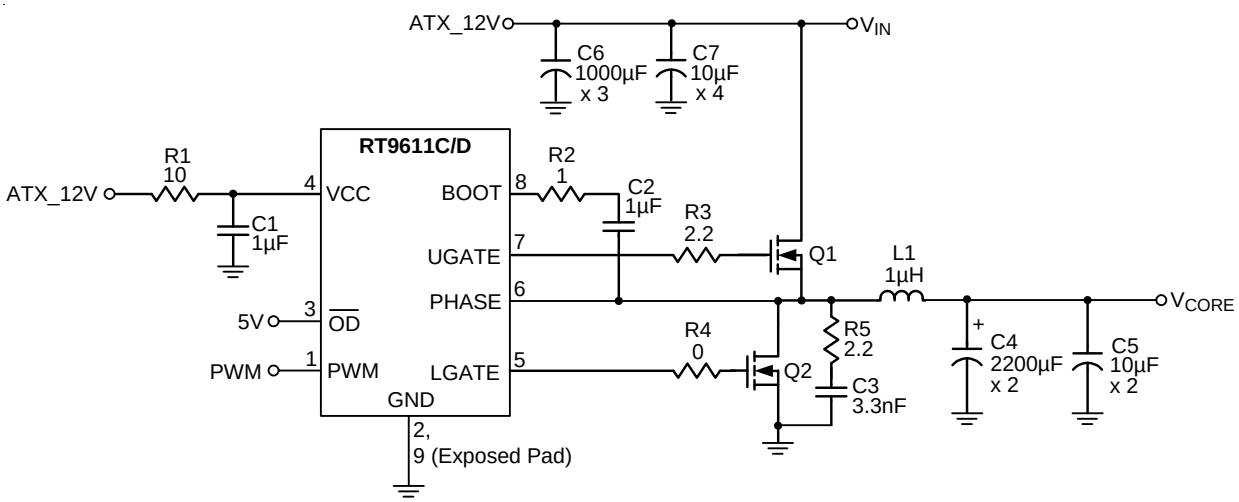
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

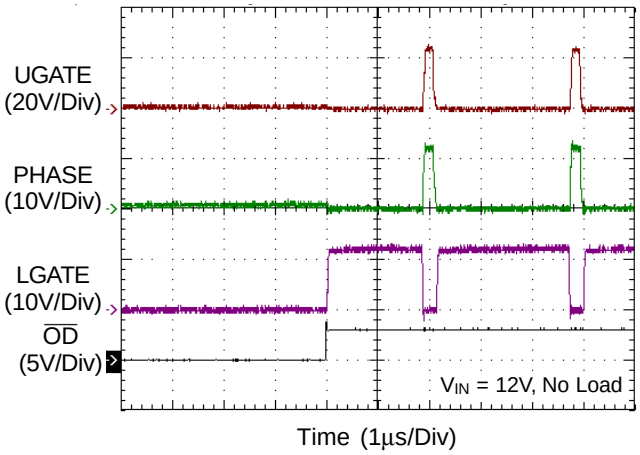
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

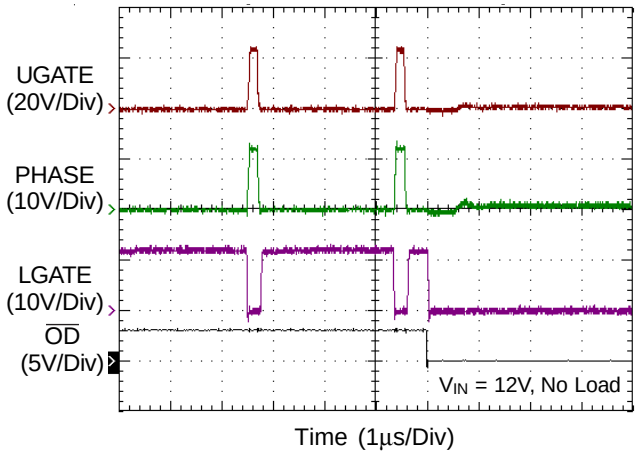


Typical Operating Characteristics

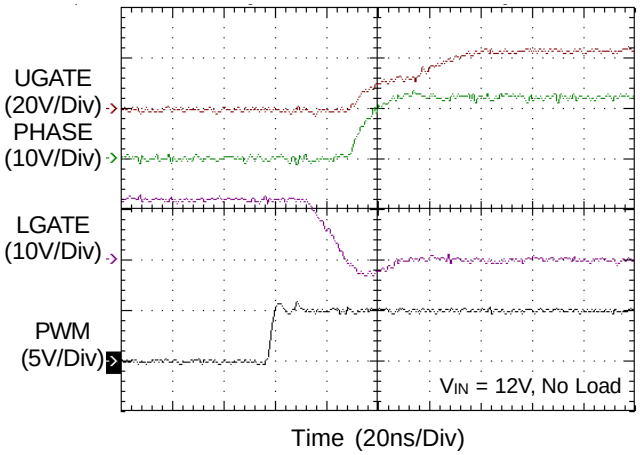
Drive Enable



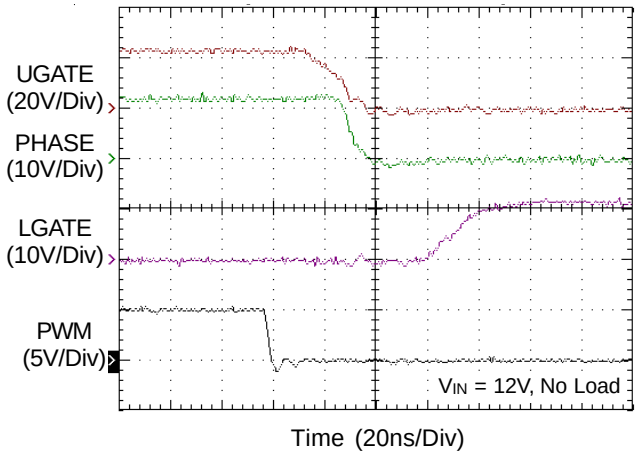
Drive Disable



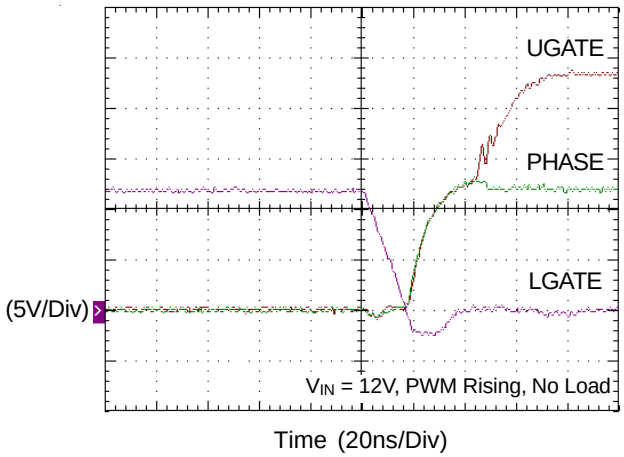
PWM Rising Edge



PWM Falling Edge



Dead Time



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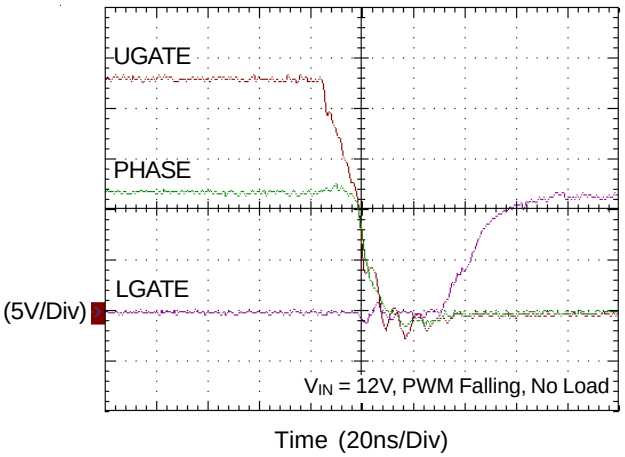
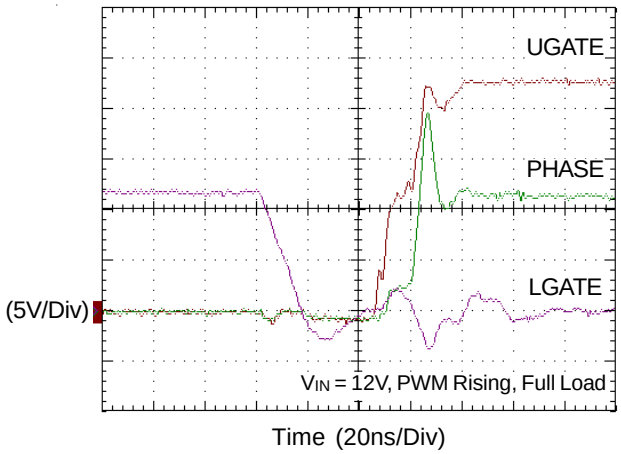
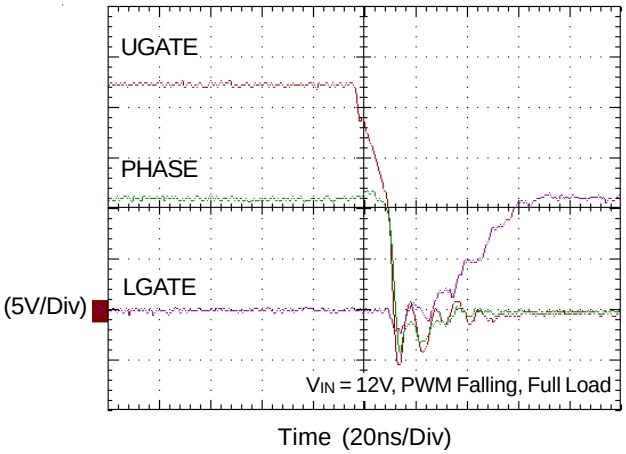


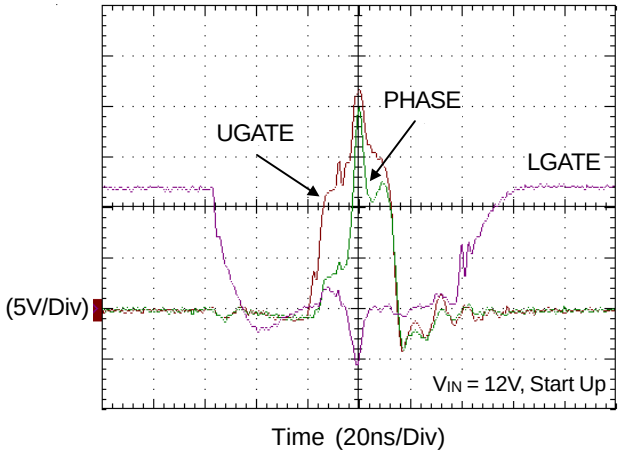
Dead Time



Dead Time



Short Pulse



Application Information

The RT9611C/D is a high frequency, synchronous rectified, single phase dual MOSFET driver containing Richtek's advanced MOSFET driver technologies. The RT9611C/D is designed to be able to adapt from normal MOSFET driving applications to high performance CPU VR driving capabilities. The RT9611C/D can be utilized under both V_{CC} = 5V or V_{CC} = 12V applications which may happen in different fields of electronics application circuits. In the efficiency point of view, higher VCC equals higher driving voltage of UG/LG which may result in higher switching loss and lower conduction loss of power MOSFETs. The choice of V_{CC} = 12V or V_{CC} = 5V can be a tradeoff to optimize system efficiency.

The RT9611C/D is designed to drive both high-side and low-side N-MOSFET through external input PWM control signal. It has power-on protection function which held UGATE and LGATE low before the VCC voltage rises to higher than rising threshold voltage. After the initialization, the PWM signal takes the control. The rising PWM signal first forces the LGATE signal turns low , and then UGATE signal is allowed to go high just after a non-overlapping time to avoid shoot through current. The falling of PWM signal first forces UGATE to go low. When UGATE and PHASE signal reach a predetermined low level, LGATE signal is allowed to turn high.

The PWM signal is acted as "High" if the signal is above the rising threshold and acted as "Low" if the signal is below the falling threshold. If any signal level enters and remains within the shutdown window is considered as "tri-state", the output drivers are disabled and both MOSFET gates are pulled and held low. If the PWM signal is left floating, the pin will be kept around 1.8V by the internal divider and provide the PWM controller with a recognizable level. $\overline{OD}$ pin will also turn off both high-/low-side MOSFETs when tied to GND.

The RT9611C/D builds in an internal bootstrap power switch to replace external bootstrap diode, and this can facilitate PCB design and reduce total BOM cost of the system. Hence, no external bootstrap diode is required in real applications.

The difference of the RT9611C and the RT9611D is the propagation delay, $t_{UGATEpdh}$. The RT9611D has comparatively larger $t_{UGATEpdh}$ to further prevent from shoot through when high-side power MOSFETs are going to be turned on. The long propagation delay of the RT9611D sacrifices efficiency for compromise of system safety. Hence, the RT9611C is usually recommended to be utilized in performance oriented applications, such as high power density CPU VR or GPU VR.

Non-overlap Control

To prevent the overlap of the gate drives during the UGATE pull low and the LGATE pull high, the non-overlap circuit monitors the voltages at the PHASE node and high-side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to pull low (after propagation delay). Before LGATE can pull high, the non-overlap protection circuit ensures that the monitored voltages have gone below 1.1V. Once the monitored voltages fall below 1.1V, LGATE begins to turn high. For short pulse condition, if the PHASE pin had not gone high after LGATE pulls low, the LGATE has to wait for 200ns before pull high. By waiting for the voltages of the PHASE pin and high-side gate drive to fall below 1.1V, the non-overlap protection circuit ensures that UGATE is low before LGATE pulls high.

Also, to prevent the overlap of the gate drives during LGATE pull low and UGATE pulls high, the non-overlap circuit monitors the LGATE voltage. When LGATE goes below 1.1V, UGATE is allowed to go high.

Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs1} or V_{gs2} is at 12V or 5V, the gate draws the current only for few nano-amperes. Thus, once the gate has been driven up to "ON" level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It is

also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

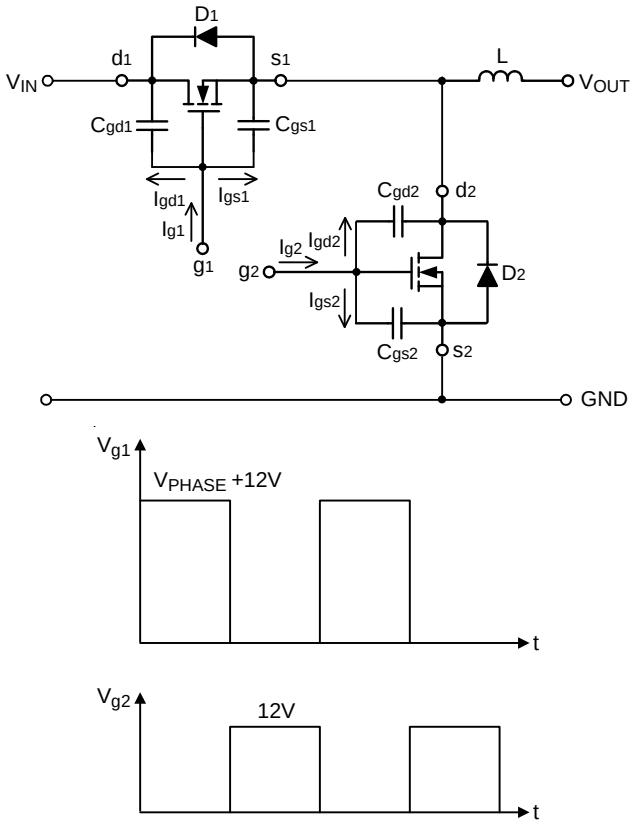


Figure1. Equivalent Circuit and Associated Waveforms

In Figure 1, the current I_{g1} and I_{g2} are required to move the gate up to 12V. The operation consists of charging C_{gd1}, C_{gd2} , C_{gs1} and C_{gs2}. C_{gs1} and C_{gs2} are capacitors from Gate to Source of the high-side and the low-side power MOSFETs, respectively. In general datasheets, the C_{gs1} and C_{gs2} are referred as "C_{iss}" which are the input capacitors. C_{gd1} and C_{gd2} are capacitors from Gate to Drain of the high-side and the low-side power MOSFETs, respectively and referred to the datasheets as "C_{rss}" the reverse transfer capacitance. For example, t_{r1} and t_{r2} are the rising time of the high-side and the low-side power MOSFETs, respectively. The required current I_{gs1} and I_{gs2}, are shown as below :

$$I_{gs1} = C_{gs1}\frac{dV_{g1}}{dt} = \frac{C_{gs1} \times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs1}\frac{dV_{g2}}{dt} = \frac{C_{gs1} \times 12}{t_{r2}} \quad (2)$$

Before driving the Gate of the high-side MOSFET up to 12V (or 5V), the low-side MOSFET has to be off. The high-side MOSFET is turned off before the low-side is turned on. In Figure 1, the body diode "D_2" had been turned on before high-side MOSFETs turned on.

$$I_{gd1} = C_{gd1}\frac{dV}{dt} = C_{gd1}\frac{12}{t_{r1}} \quad (3)$$

Before the low-side MOSFET is turned on, the C_{gd2} have been charged to V_{IN}. Thus, as C_{gd2} reverses its polarity and g_2 is charged up to 12V, the required current is :

$$I_{gd2} = C_{gd2}\frac{dV}{dt} = C_{gd2}\frac{Vi+12}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified Buck converter, input voltage V_{IN} = 12V, V_{g1} = V_{g2} = 12V. The high-side MOSFET is PHB83N03LT whose C_{iss} = 1660pF, C_{rss} = 380pF, and t_r = 14ns. The low-side MOSFET is PHB95N03LT whose C_{iss} = 2200pF, C_{rss} = 500pF and t_r = 30ns, from the equation (1) and (2) we can obtain :

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 1.428 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 12}{30 \times 10^{-9}} = 0.88 \quad (A) \quad (6)$$

from equation. (3) and (4)

$$I_{gd1} = \frac{380 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 0.326 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{500 \times 10^{-12} \times (12+12)}{30 \times 10^{-9}} = 0.4 \quad (A) \quad (8)$$

the total current required from the gate driving source can be calculated as following equations :

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.754 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28 \quad (A) \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

Select the Bootstrap Capacitor

Figure 2 shows part of the bootstrap circuit of the RT9611C/D. The V_{CB} (the voltage difference between BOOT and PHASE on RT9611C/D) provides a voltage to the Gate of the high-side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance C_B has to be selected properly. It is determined by the following constraints.

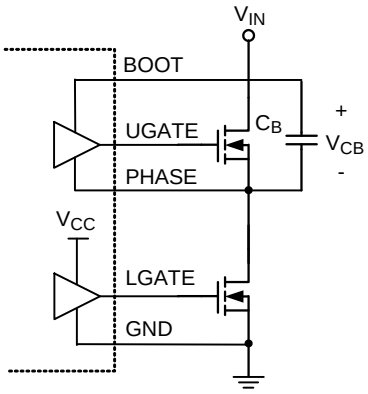


Figure 2. Part of Bootstrap Circuit of RT9611C/D

In practice, a low value capacitor C_B will lead to the over charging that could damage the IC. Therefore, to minimize the risk of overcharging and to reduce the ripple on V_{CB}, the bootstrap capacitor should not be smaller than 0.1µF, and the larger the better. In general design, using 1µF can provide better performance. At least one low ESR capacitor should be used to provide good local de-coupling. It is recommended to adopt a ceramic or tantalum capacitor.

Power Dissipation

To prevent driving the IC beyond the maximum recommended operating junction temperature of 125°C, it is necessary to calculate the power dissipation appropriately. This dissipation is a function of switching frequency and total gate charge of the selected MOSFET.

Figure 3 shows the power dissipation test circuit. C_L and C_U are the UGATE and LGATE load capacitors, respectively. The bootstrap capacitor value is 1µF.

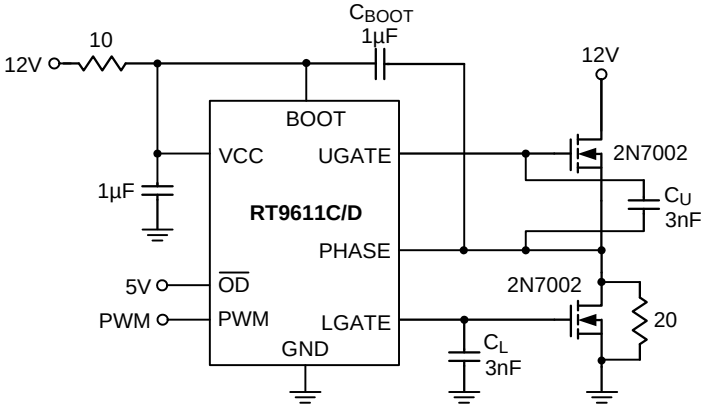


Figure 3. Test Circuit

Figure 4 shows the power dissipation of the RT9611C/D as a function of frequency and load capacitance. The value of C_U and C_L are the same and the frequency is varied from 100kHz to 1MHz.

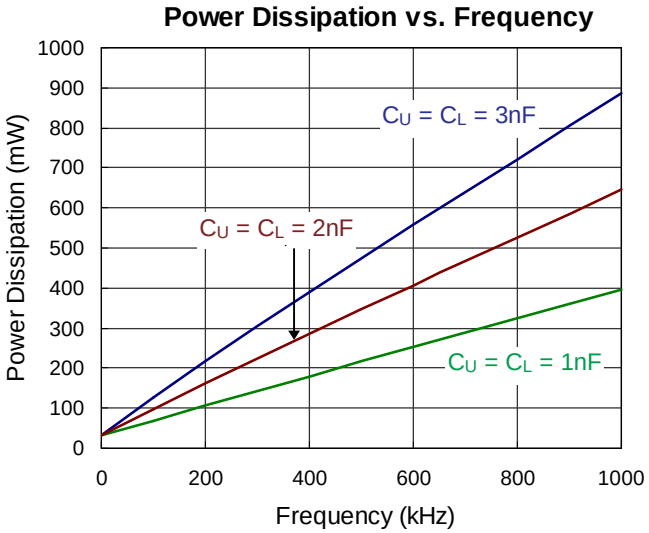


Figure 4. Power Dissipation vs. Frequency

The operating junction temperature can be calculated from the power dissipation curves (Figure 4). Assume V_{CC} = 12V, operating frequency is 200kHz and C_U = C_L = 1nF which emulate the input capacitances of the high-side and low-side power MOSFETs. From Figure 4, the power dissipation is 100mΩ. Thus, for example, with the WDFN-8L 3x3 package thermal resistance θ_{JA} is 31°C/W. The operating junction temperature is calculated as :

$$T_J = (31°C/W \times 100mW) + 25°C = 28.1°C \quad (11)$$

where the ambient temperature is 25°C.

Thermal Considerations

For recommended operating condition specifications of the RT9611C/D, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-8L 3x3 package, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (31°C/W) = 3.22W for WDFN-8L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 5 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

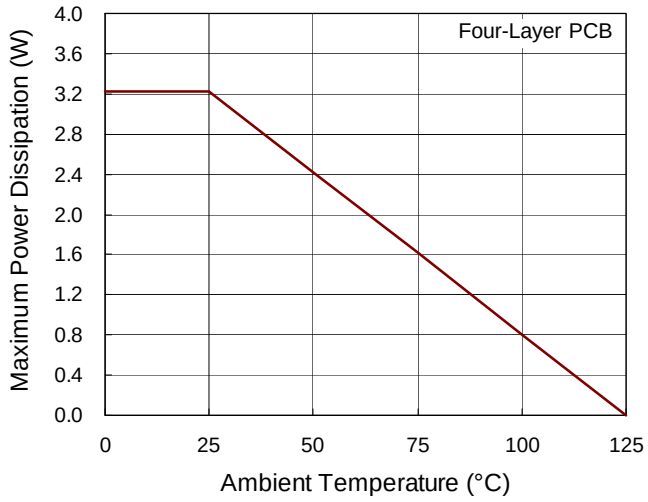


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Consideration

Figure 6 shows the schematic circuit of a synchronous Buck converter to implement the RT9611C/D. The converter operates from 5V to 12V of input Voltage.

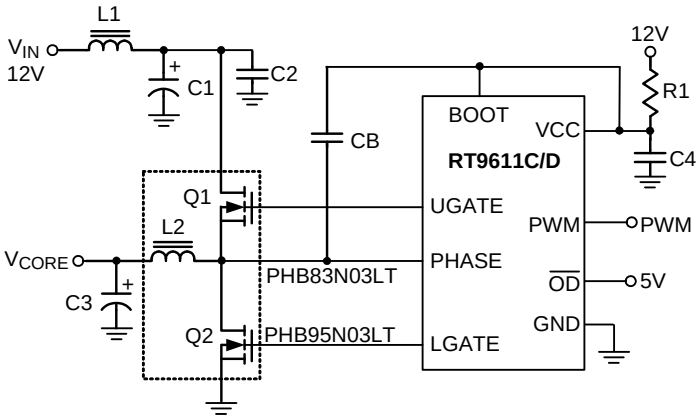
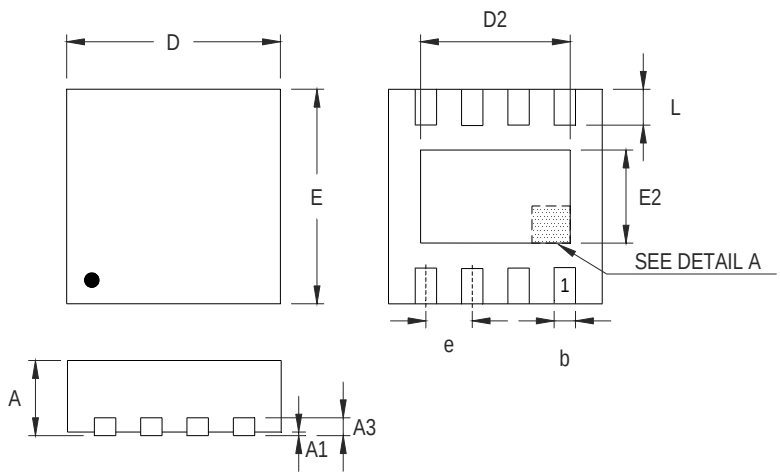


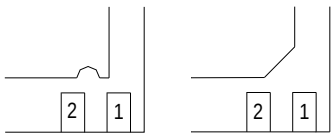
Figure 6. Synchronous Buck Converter Circuit

When layout the PCB, it should be very careful. The power circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The junction of Q1, Q2, L2 should be very close.

Next, the trace from UGATE and LGATE should also be short to decrease the noise of the driver output signals. the PHASE signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor C4 should be connected to GND directly. Furthermore, the bootstrap capacitors (C_B) should always be placed as close to the pins of the IC as possible.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

W-Type 8L DFN 3x3 Package

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单击下面可查看定价，库存，交付和生命周期等信息

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