

## Triple-Channel Synchronous Rectified Buck MOSFET Driver

### General Description

The RT9629A is a high frequency, triple-channel synchronous rectified buck MOSFET driver specifically designed to drive six power N-MOSFETs. The part is promoted to pair with Richtek's multiphase buck PWM controller family for high-density power supply implementation. The output drivers of RT9629A can efficiently switch power MOSFETs at frequency 300kHz typically. Operating in higher frequency should consider the thermal dissipation carefully. The device implements bootstrapping on the upper gate with only an external capacitor and a diode required. This reduces circuit complexity and allows the use of higher performance, cost effective N-MOSFETs. All drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. The RT9629A has also detected the fault condition during initial start-up before the multi-phase PWM controller takes control. As a result, the input supply will latch into the shutdown state. The RT9629A comes in a small footprint package with WQFN-24L 5x5 package.

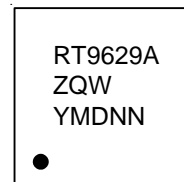
### Features

- Drive Six N-MOSFETs for 3-Phase Buck PWM Control
- Shoot Through Protection
- Embedded Bootstrap Diode
- Support High Switching Frequency
- Fast Output Rising Time
- Tri-State PWM Input for Output Shutdown
- Enable Control
- Small 24-Lead WQFN Package
- RoHS Compliant and Halogen Free

### Applications

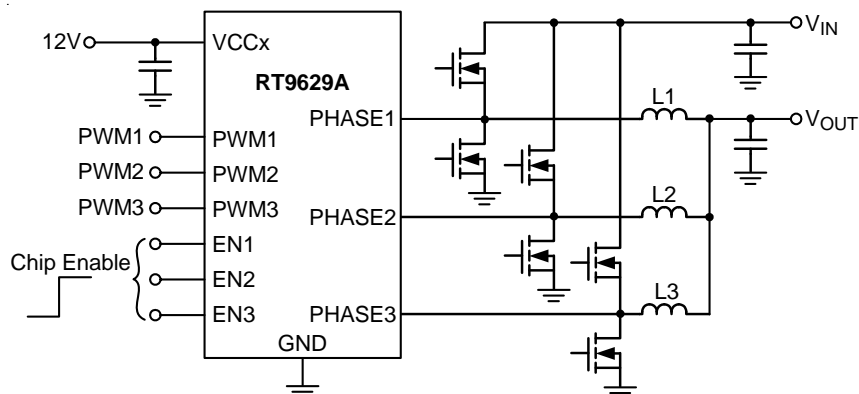
- Core Voltage Supplies for Desktop, Motherboard CPU
- High Frequency Low Profile DC/DC Converters
- High Current Low Voltage DC/DC Converters
- Core Voltage Supplies for GFX Card

### Marking Information



RT9629AZQW : Product Number  
YMDNN : Date Code

### Simplified Application Circuit



## Ordering Information

RT9629A □ □

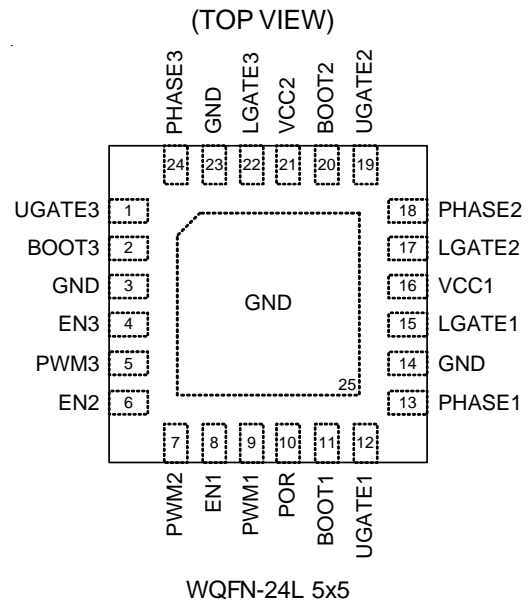
- Package Type  
QW : WQFN-24L 5x5 (W-Type)
- Lead Plating System  
Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

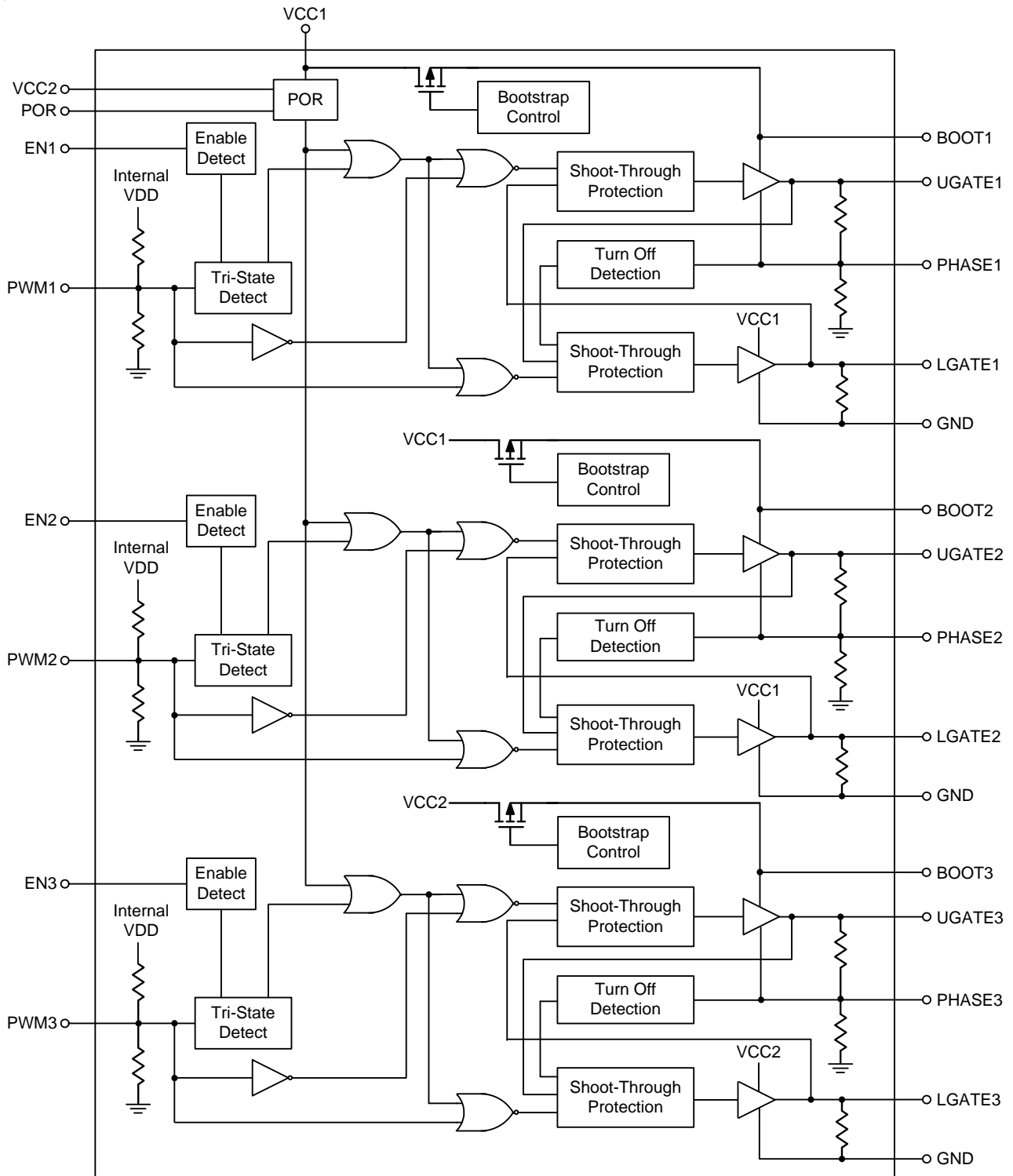
## Pin Configurations



## Function Pin Description

Pin No.	Pin Name	Pin Function
1, 12, 19	UGATE3, UGATE1, UGATE2	High Side Gate Drive Outputs for Phase 3, Phase 1, and Phase 2. Connect this pin to the Gate of high side power MOSFET.
2, 11, 20	BOOT3, BOOT1, BOOT2	Bootstrap Power Pins for Phase 3, Phase 1, and Phase 2. This pin powers the high side MOSFET driver. Connect this pin to the junction of the bootstrap capacitor and the cathode of the bootstrap diode.
3, 14, 23, 25 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4, 6, 8	EN3, EN2, EN1	Chip Enable (Active High). When this pin is low, both UGATE <sub>x</sub> and LGATE <sub>x</sub> are driven to low.
5, 7, 9	PWM3, PWM2, PWM1	PWM Signal Input. Connect this pin to the PWM output of the controller.
10	POR	Power On Reset Signal.
13, 18, 24	PHASE1, PHASE2, PHASE3	Switch Nodes of High Side Driver 1, Driver 2, and Driver 3. Connect this pin to the high side MOSFET Source together with the low side MOSFET Drain and the inductor.
15, 17, 22	LGATE1, LGATE2, LGATE3	Low Side Gate Drive Output for Phase 1, Phase 2, and Phase 3. This pin drives the Gate of low side MOSFET.
16, 21	VCC1, VCC2	Supply Input Pin. VCC1 supplies current for Channel 1 and Channel 2 gate drivers. VCC2 supplies current for Channel 3 gate driver.

**Function Block Diagram**



## Operation

### POR (Power On Reset)

POR block detects the voltage at VCC1 pin and VCC2 pin. When the VCC1 and VCC2 pin voltage is higher than POR rising threshold, POR pin output voltage (POR output) is high. POR output is low when VCC1 and VCC2 are not both higher than POR rising threshold. When the POR pin voltage is high, UGATE<sub>x</sub> and LGATE<sub>x</sub> can be controlled by EN<sub>x</sub> pin and PWM<sub>x</sub> pin voltage. With low POR pin voltage, both UGATE<sub>x</sub> and LGATE<sub>x</sub> will be pulled to low.

### Enable Detect

When EN<sub>x</sub> pin input voltage is higher/lower than EN rising threshold, MOSFET driver is enabled/disabled. When the EN<sub>x</sub> input and POR output are high, UGATE<sub>x</sub> and LGATE<sub>x</sub> can be controlled by PWM<sub>x</sub> input voltage. When EN<sub>x</sub> input is low, both UGATE<sub>x</sub> and LGATE<sub>x</sub> are pulled to low.

### Tri-State Detect

When both POR block output and EN<sub>x</sub> pin voltages are high, UGATE<sub>x</sub> and LGATE<sub>x</sub> can be controlled by PWM<sub>x</sub> input. There are three PWM<sub>x</sub> input modes, which are high, low, and shutdown state. If PWM<sub>x</sub> input is within the shutdown window, both UGATE<sub>x</sub> and LGATE<sub>x</sub> output are low. When PWM<sub>x</sub> input is higher than its rising threshold, UGATE<sub>x</sub> is high and LGATE<sub>x</sub> is low. When PWM<sub>x</sub> input is lower than its falling threshold, UGATE<sub>x</sub> is low and LGATE<sub>x</sub> is high.

### Bootstrap Control

Bootstrap control block controls the integrated bootstrap switch. When LGATE<sub>x</sub> is high (low side MOSFET is turned on), the bootstrap switch is turned on to charge the bootstrap capacitor connected to BOOT<sub>x</sub> pin. When LGATE<sub>x</sub> is low (low side MOSFET is turned off), the bootstrap switch is turned off to disconnect VCC<sub>x</sub> pin and BOOT<sub>x</sub> pin.

### Turn-Off Detection

Turn-off detection block detects whether high side MOSFET is turned off by monitoring PHASE<sub>x</sub> pin voltage. To avoid shoot through between high side and low side MOSFETs, low side MOSFET can be turned on only after high side MOSFET is effectively turned off.

### Shoot-Through Protection

Shoot-through protection block implements the dead time when both high side and low side MOSFETs are turned off. With shoot-through protection block, high side and low side MOSFET are never turned on simultaneously. Thus, shoot through between high side and low side MOSFETs is prevented.

**Absolute Maximum Ratings** (Note 1)

- Supply Voltage, VCC1, VCC2 ----- -0.3V to 15V
- BOOTx to PHASEx ----- -0.3V to 15V
- PHASEx to GND
  - DC ----- -0.3V to 30V
  - < 100ns ----- -10V to 35V
- LGATEx to GND
  - DC ----- -0.3V to (VCC + 0.3V)
  - < 100ns ----- -2V to (VCC + 0.3V)
- UGATEx to GND
  - DC ----- (V<sub>PHASE</sub> - 0.3V) to (V<sub>BOOT</sub> + 0.3V)
  - < 100ns ----- (V<sub>PHASE</sub> - 2V) to (V<sub>BOOT</sub> + 0.3V)
- ENx, PWMx to GND ----- -0.3V to 7V
- POR to GND ----- -0.3V to 5V
- Power Dissipation, P<sub>D</sub> @ T<sub>A</sub> = 25°C
  - WQFN-24L 5x5 ----- 2.778W
- Package Thermal Resistance (Note 2)
  - WQFN-24L 5x5, θ<sub>JA</sub> ----- 36°C/W
  - WQFN-24L 5x5, θ<sub>JC</sub> ----- 6°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ----- 2kV

**Recommended Operating Conditions** (Note 4)

- Supply Voltage, VCC1, VCC2 ----- 4.5V to 13.2V
- Input Voltage, (V<sub>IN</sub> + VCCx) ----- < 35V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

**Electrical Characteristics**

(V<sub>CCx</sub> = 12V, T<sub>A</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V <sub>CC</sub>		4.5	--	13.2	V
Power Supply Current	I <sub>VCC</sub>	V <sub>BOOTx</sub> = 12V, PWMx Floating	--	250	--	μA
<b>Power On Reset (POR)</b>						
POR Rising Threshold	V <sub>POR_r</sub>	V <sub>CCx</sub> Rising	--	4	4.4	V
POR Falling Threshold	V <sub>POR_f</sub>	V <sub>CCx</sub> Falling	3	3.5	--	V
POR Pin High Voltage	V <sub>POR_H</sub>		--	3.5	4	V
POR Pin Low Voltage	V <sub>POR_L</sub>		--	--	0.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>EN Input</b>						
ENx Rising Threshold	V <sub>ENH</sub>		--	1.3	1.6	V
ENx Falling Threshold	V <sub>ENL</sub>		0.7	1	--	V
<b>PWM Input</b>						
Maximum Input Current	I <sub>PWM</sub>	V <sub>PWMx</sub> = 0V or 5V	--	160	--	μA
PWMx Floating Voltage	V <sub>PWM_fl</sub>	PWMx = Open	--	1.8	--	V
PWMx Rising Threshold	V <sub>PWM_rth</sub>		2.3	2.8	3.2	V
PWMx Falling Threshold	V <sub>PWM_fth</sub>		0.7	1.1	1.4	V
<b>Timing</b>						
UGATEx Rising Time	t <sub>UGATEr</sub>	3nF load	--	25	--	ns
UGATEx Falling Time	t <sub>UGATEf</sub>	3nF load	--	12	--	ns
LGATEx Rising Time	t <sub>LGATEr</sub>	3nF load	--	24	--	ns
LGATEx Falling Time	t <sub>LGATEf</sub>	3nF load	--	10	--	ns
Propagation Delay	t <sub>UGATEpgh</sub>	V <sub>BOOTx</sub> – V <sub>PHASEx</sub> = 12V See Timing Diagram	--	60	--	ns
	t <sub>UGATEpdl</sub>		--	22	--	
	t <sub>LGATEpdh</sub>	See Timing Diagram	--	30	--	ns
	t <sub>LGATEpdl</sub>		--	8	--	
<b>Output</b>						
UGATEx Drive Source	R <sub>UGATEsr</sub>	V <sub>BOOT</sub> – V <sub>PHASE</sub> = 12V, I <sub>Source</sub> = 100mA	--	1.7	--	Ω
UGATEx Drive Sink	R <sub>UGATEsk</sub>	V <sub>BOOT</sub> – V <sub>PHASE</sub> = 12V, I <sub>Sink</sub> = 100mA	--	1.4	--	Ω
LGATEx Drive Source	R <sub>LGATEsr</sub>	I <sub>Source</sub> = 100mA	--	1.6	--	Ω
LGATEx Drive Sink	R <sub>LGATEsk</sub>	I <sub>Sink</sub> = 100mA	--	1.1	--	Ω

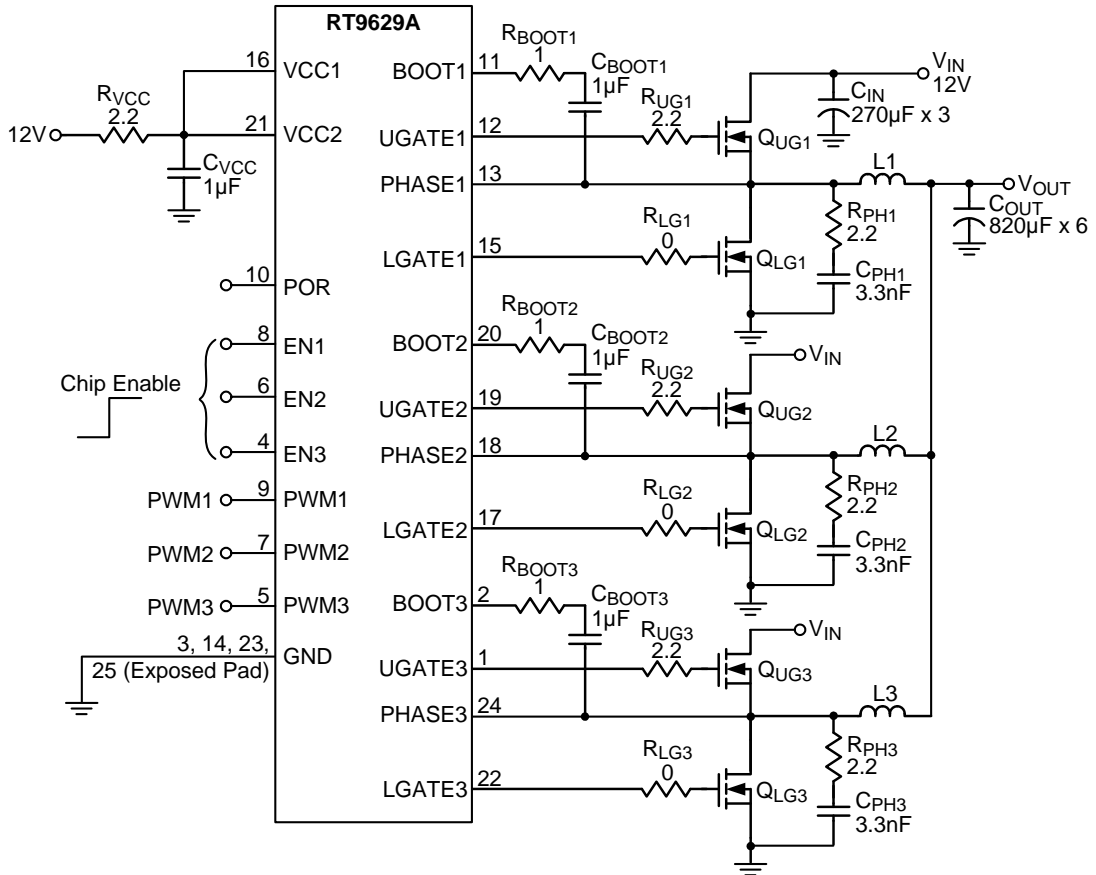
**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** θ<sub>JA</sub> is measured at T<sub>A</sub> = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ<sub>JC</sub> is measured at the exposed pad of the package.

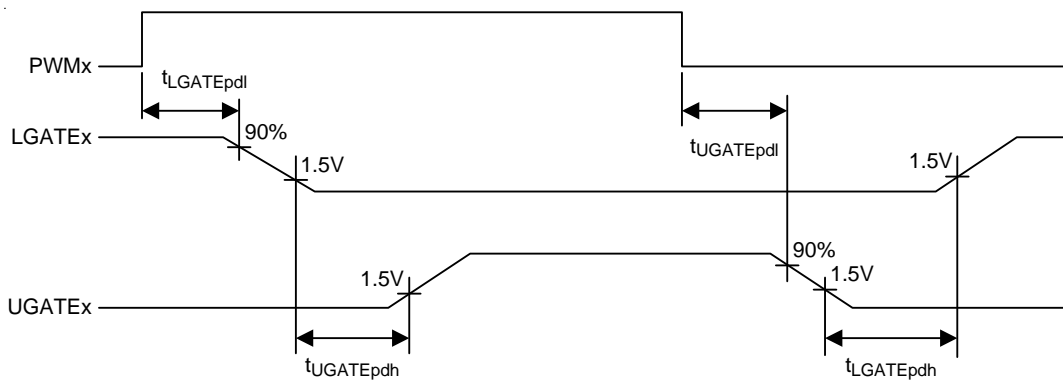
**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Typical Application Circuit**

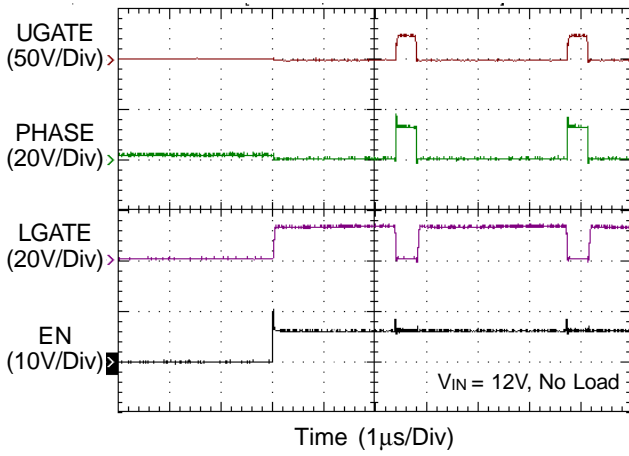


**Timing Diagram**

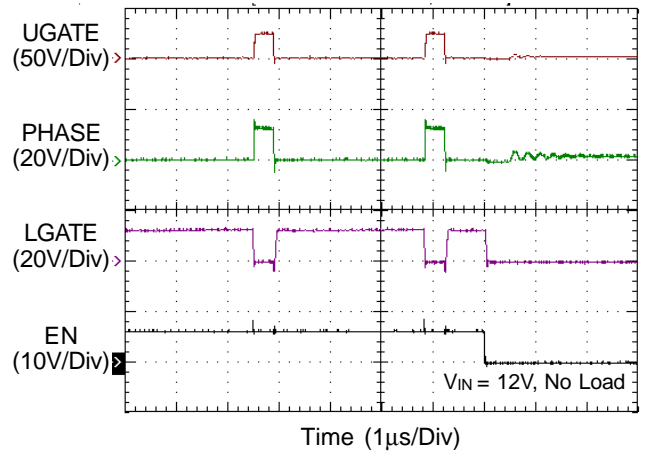


## Typical Operating Characteristics

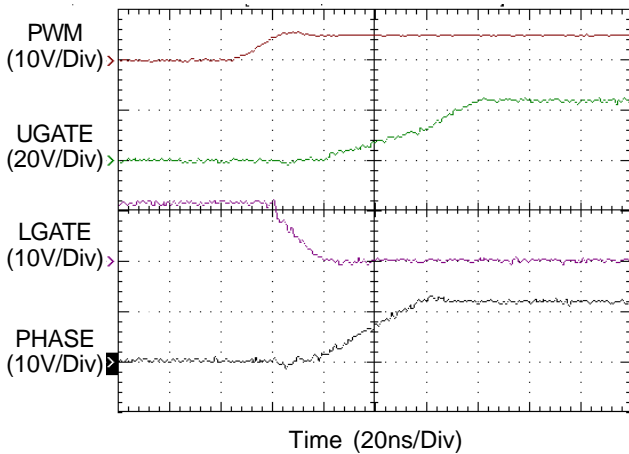
### Drive Enable



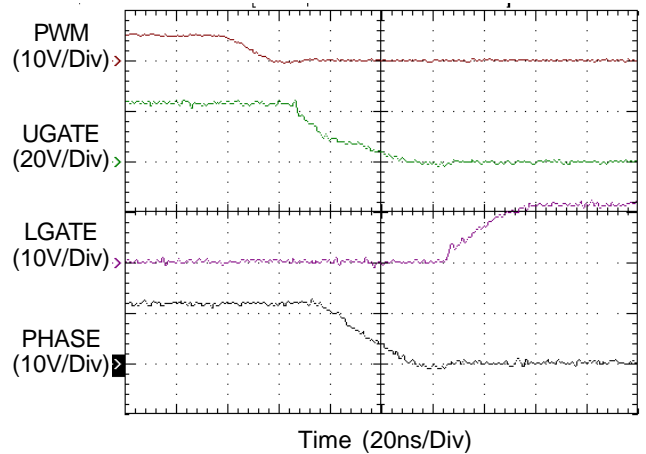
### Drive Disable



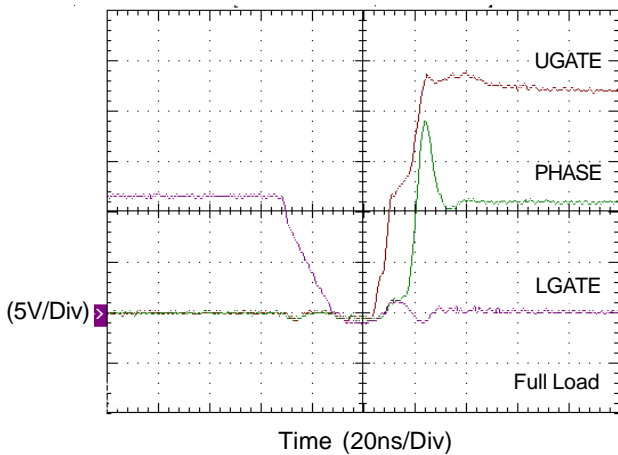
### PWM Rising Edge



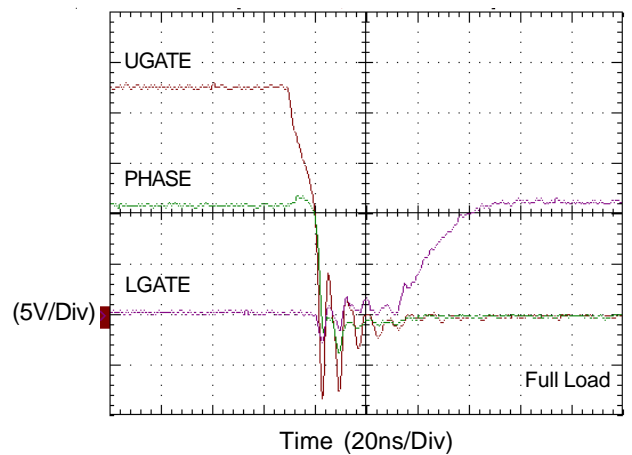
### PWM Falling Edge



### Dead Time

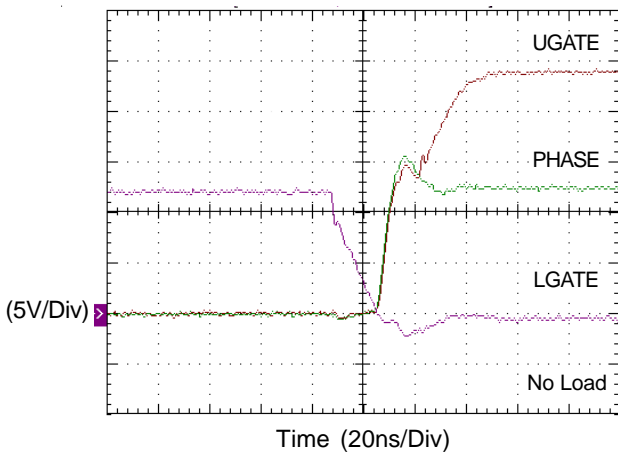


### Dead Time

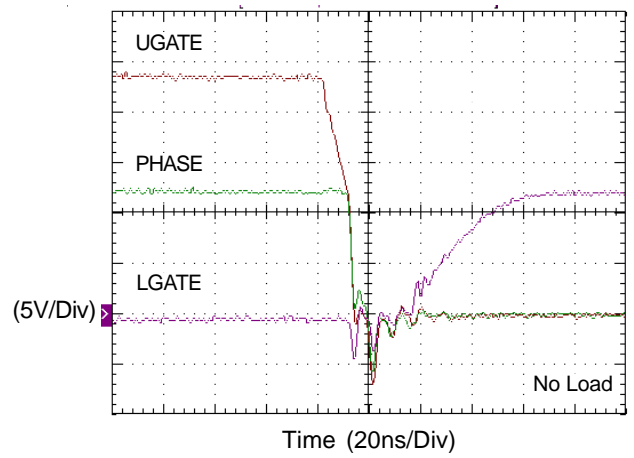




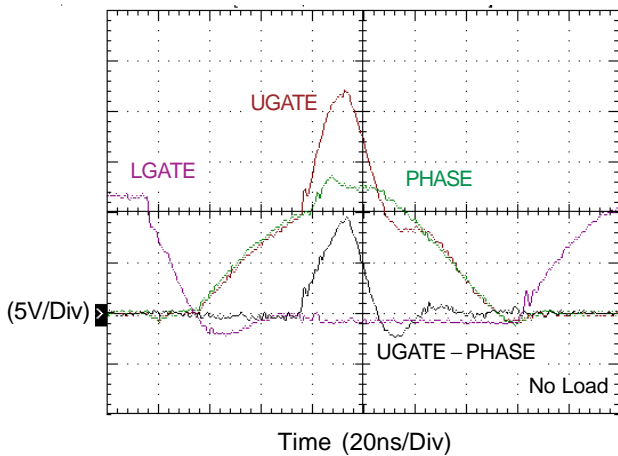
Dead Time



Dead Time



Short Pulse



## Application Information

The RT9629A is a high frequency, triple-channel synchronous rectified MOSFET driver containing Richtek's advanced MOSFET driver technologies. The RT9629A is designed to be able to adapt from normal MOSFET driving applications to high performance CPU VR driving capabilities.

### Supply Voltage and Power On Reset

The RT9629A can be utilized under both  $V_{CCx} = 5V$  or  $V_{CCx} = 12V$  applications which may happen in different fields of electronics application circuits. In terms of efficiency, higher  $V_{CCx}$  equals higher driving voltage of UGATEx/LGATEx which may result in higher switching loss and lower conduction loss of power MOSFETs. The choice of  $V_{CCx} = 12V$  or  $V_{CCx} = 5V$  can be a tradeoff to optimize system efficiency. And VCC1 pin must be directly connected to VCC2 pin.

The RT9629A controls both high side and low side N-MOSFETs of three half-bridge power according to three external input PWMx control signals. It has Power On Reset (POR) function which held UGATEx and LGATEx low before the VCCx voltage rises to higher than rising threshold voltage. When  $V_{CC1}$  and  $V_{CC2}$  exceed the POR threshold voltage, the voltage at the POR pin will be pulled high.

### Enable and Disable

The RT9629A includes an ENx pin for sequence control. When the ENx pin rises above the  $V_{ENH}$  trip point, the RT9629A begins a new initialization and follows the PWMx command to control the UGATEx and LGATEx. When the ENx pin falls below the  $V_{ENL}$  trip point, the RT9629A shuts down and keeps UGATEx and LGATEx low.

### Tri-state PWM Input

After the initialization, the PWMx signal takes the control. The rising PWMx signal first forces the LGATEx signal to turn low then UGATEx signal is allowed to go high just after a non-overlapping time to avoid shoot through current. The falling of PWMx signal first forces UGATEx to go low. When UGATEx and PHASEx signal reach a predetermined low level, LGATEx signal is allowed to turn high.

The PWMx signal is acted as "High" if the signal is above the rising threshold and acted as "Low" if the signal is below the falling threshold. When PWM signal level enters and remains within the shutdown window, the output drivers are disabled and both MOSFET gates are pulled and held low. If the PWMx signal is left floating, the pin will be kept around 1.8V by the internal divider and provide the PWMx controller with a recognizable level.

### Bootstrap Power Switch

The RT9629A builds in an internal bootstrap power switch to replace external bootstrap diode, and this can facilitate PCB design and reduce total BOM cost of the system. Hence, no external bootstrap diode is required in real applications.

### Non-overlap Control

To prevent the overlap of the gate drivers during the UGATEx pull low and the LGATEx pull high, the non-overlap circuit monitors the voltages at the PHASEx node and high side gate drive (UGATEx – PHASEx). When the PWMx input signal goes low, UGATEx begins to pull low (after propagation delay). Before LGATEx is pulled high, the non-overlap protection circuit ensures that the monitored voltages have gone below 1.1V. Once the monitored voltages fall below 1.1V, LGATEx begins to turn high. By waiting for the voltages of the PHASEx pin and high side gate driver to fall below 1.1V, the non-overlap protection circuit ensures that UGATEx is low before LGATEx pulls high.

Also to prevent the overlap of the gate drivers during LGATEx pull low and UGATEx pull high, the non-overlap circuit monitors the LGATEx voltage. When LGATEx goes below 1.1V, UGATEx goes high after propagation delay.

### Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When  $V_{gs1}$  or  $V_{gs2}$  is at 12V or 5V, the gate draws the current only for few nano-amperes. Thus once the gate has been driven up to "ON" level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It is also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

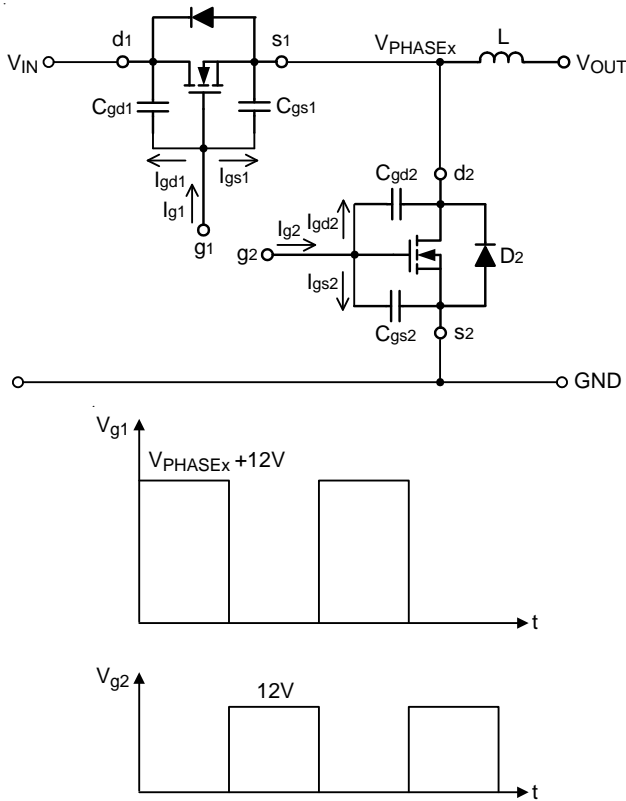


Figure 1. Equivalent Circuit and Waveforms (V<sub>CC</sub> = 12V)

In Figure 1, the current I<sub>g1</sub> and I<sub>g2</sub> are required to move the gate up to 12V. The operation consists of charging C<sub>gd1</sub>, C<sub>gd2</sub>, C<sub>gs1</sub> and C<sub>gs2</sub>. C<sub>gs1</sub> and C<sub>gs2</sub> are the capacitors from gate to source of the high side and the low side power MOSFETs, respectively. In general data sheets, the C<sub>gs1</sub> and C<sub>gs2</sub> are referred as “C<sub>iss</sub>” which are the input capacitors. C<sub>gd1</sub> and C<sub>gd2</sub> are the capacitors from gate to drain of the high side and the low side power MOSFETs, respectively and referred to the data sheets as “C<sub>rss</sub>” the reverse transfer capacitance. For example, t<sub>r1</sub> and t<sub>r2</sub> are the rising time of the high side and the low side power MOSFETs respectively, the required current I<sub>gs1</sub> and I<sub>gs2</sub>, are shown as below :

$$I_{gs1} = C_{gs1} \frac{dV_{g1}}{dt} = \frac{C_{gs1} \times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs2} \frac{dV_{g2}}{dt} = \frac{C_{gs2} \times 12}{t_{r2}} \quad (2)$$

Before driving the gate of the high side MOSFET up to 12V, the low side MOSFET has to be off; and the high side MOSFET will be turned off before the

low side is turned on. From Figure 1, the body diode “D<sub>2</sub>” will be turned on before high side MOSFETs turn on.

$$I_{gd1} = C_{gd1} \frac{dV}{dt} = C_{gd1} \frac{12}{t_{r1}} \quad (3)$$

Before the low side MOSFET is turned on, the C<sub>gd2</sub> have been charged to V<sub>IN</sub>. Thus, as C<sub>gd2</sub> reverses its polarity and g<sub>2</sub> is charged up to 12V, the required current is

$$I_{gd2} = C_{gd2} \frac{dV}{dt} = C_{gd2} \frac{V_{IN} + 12}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified Buck converter, input voltage V<sub>IN</sub> = 12V, V<sub>gs1</sub> = 12V, V<sub>gs2</sub> = 12V. The high side MOSFET is PHB83N03LT whose C<sub>iss</sub> = 1660pF, C<sub>rss</sub> = 380pF, and t<sub>r</sub> = 14ns. The low side MOSFET is PHB95N03LT whose C<sub>iss</sub> = 2200pF, C<sub>rss</sub> = 500pF and t<sub>r</sub> = 30ns, from the equation (1) and (2) we can obtain

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 1.428 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 12}{30 \times 10^{-9}} = 0.88 \quad (A) \quad (6)$$

from equation. (3) and (4)

$$I_{gd1} = \frac{380 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 0.326 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{500 \times 10^{-12} \times (12+12)}{30 \times 10^{-9}} = 0.4 \quad (A) \quad (8)$$

the total current required from the gate driving source can be calculated as following equations.

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.754 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28 \quad (A) \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

## Select the Bootstrap Capacitor

Figure 2 shows part of the bootstrap circuit of the RT9629A. The  $V_{CB}$  (the voltage difference between  $BOOTx$  and  $PHASEx$  on RT9629A) provides a voltage to the gate of the high side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance  $C_{BOOT}$  has to be selected properly. It is determined by the following constraints.

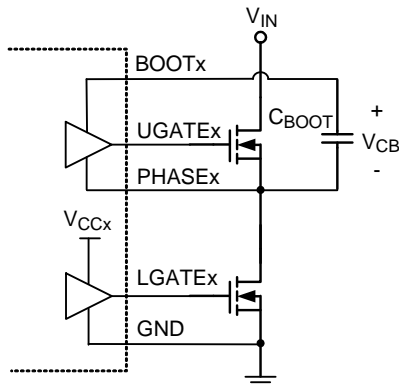


Figure 2. Part of Bootstrap Circuit of RT9629A

In practice, a low value capacitor  $C_{BOOT}$  will lead to the over charging that could damage the IC. Therefore, to minimize the risk of overcharging and to reduce the ripple on  $V_{CB}$ , the bootstrap capacitor should not be smaller than  $0.1\mu F$ , and the larger the better. In general design, using  $1\mu F$  can provide better performance. At least one low-ESR capacitor should be used to provide good local de-coupling. It is recommended to adopt a ceramic or tantalum capacitor.

## Power Dissipation

To prevent driving the IC beyond the maximum recommended operating junction temperature of  $125^{\circ}C$ , it is necessary to calculate the power dissipation appropriately. This dissipation is a function of switching frequency and total gate charge of the selected MOSFET.

Figure 3 shows the power dissipation test circuit.  $C_L$  and  $C_U$  are the  $UGATEx$  and  $LGATEx$  load capacitors, respectively. The bootstrap capacitor value is  $1\mu F$ .

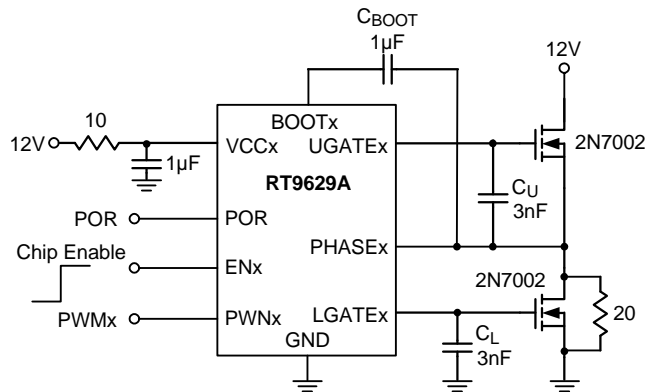


Figure 3. Power Dissipation Test Circuit

Figure 4 shows the power dissipation of the RT9629A as a function of frequency and load capacitance when  $V_{CC} = 12V$ . The value of  $C_U$  and  $C_L$  are the same and the frequency is varied from  $100kHz$  to  $1MHz$ .

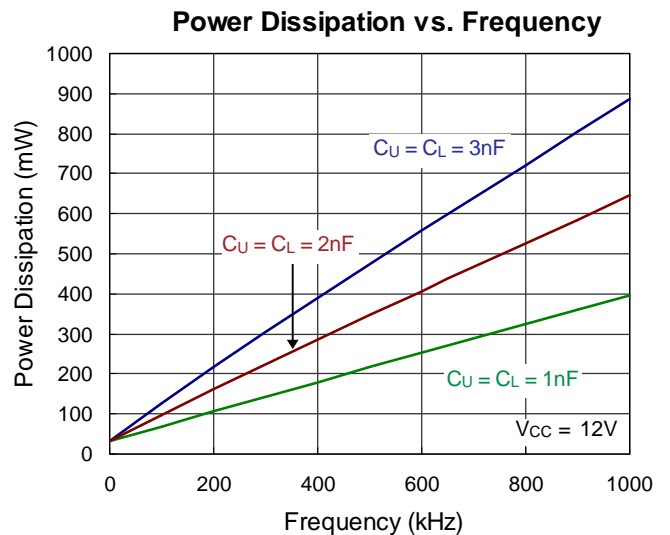


Figure 4. Power Dissipation vs. Frequency

The operating junction temperature can be calculated from the power dissipation curves (Figure 4). Assume  $V_{CCx} = 12V$ , operating frequency is  $200kHz$  and  $C_U = C_L = 1nF$  which emulate the input capacitances of the high side and low side power MOSFETs. From Figure 4, the power dissipation is  $100mW$ . Thus, for example, with the SOP-8 package, the package thermal resistance  $\theta_{JA}$  is  $120^{\circ}C/W$ . The operating junction temperature is then calculated as :

$$T_J = (120^{\circ}C/W \times 100mW) + 25^{\circ}C = 37^{\circ}C \quad (11)$$

where the ambient temperature is  $25^{\circ}C$ .

**Thermal Considerations**

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For WQFN-24L 5x5 package, the thermal resistance,  $\theta_{JA}$ , is 36°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (36^\circ\text{C/W}) = 2.778\text{W}$$

WQFN-24L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

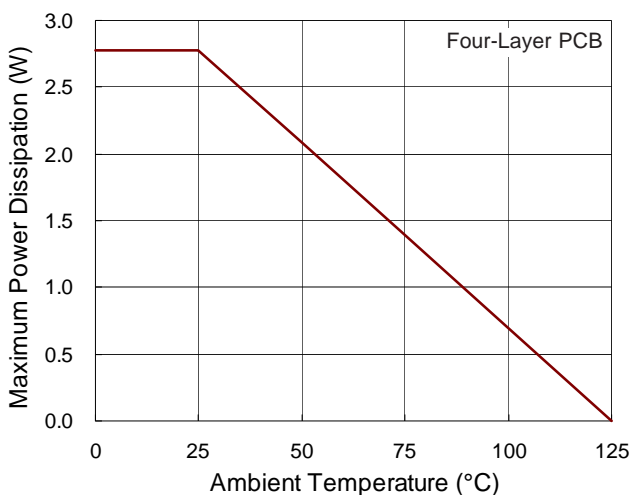


Figure 5. Derating Curve of Maximum Power Dissipation

**Layout Consideration**

Figure 6 shows the schematic circuit of a synchronous buck converter to implement the RT9629A. The converter operates from 5V to 12V of input Voltage.

For the PCB layout, it should be very careful. The power circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The location of  $Q_{UGx}$ ,  $Q_{LGx}$ ,  $L_x$  should be very close.

Next, the trace from  $UGATE_x$ , and  $LGATE_x$  should also be short to decrease the noise of the driver output signals.  $PHASE_x$  signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor  $C_{VCC}$  should be connected to GND directly. Furthermore, the bootstrap capacitors ( $C_{BOOTx}$ ) should always be placed as close to the pins of the IC as possible.

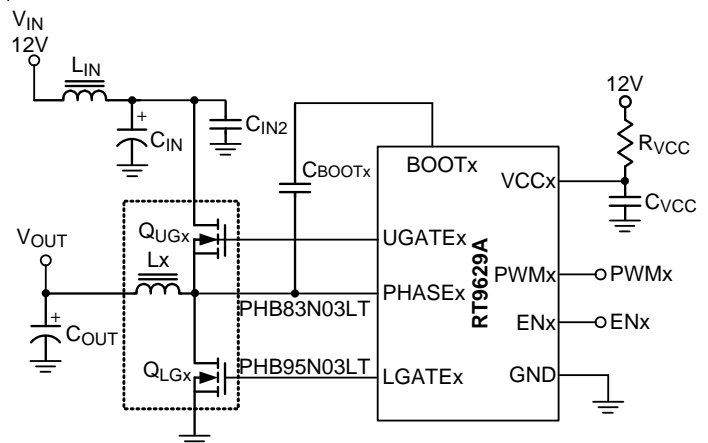
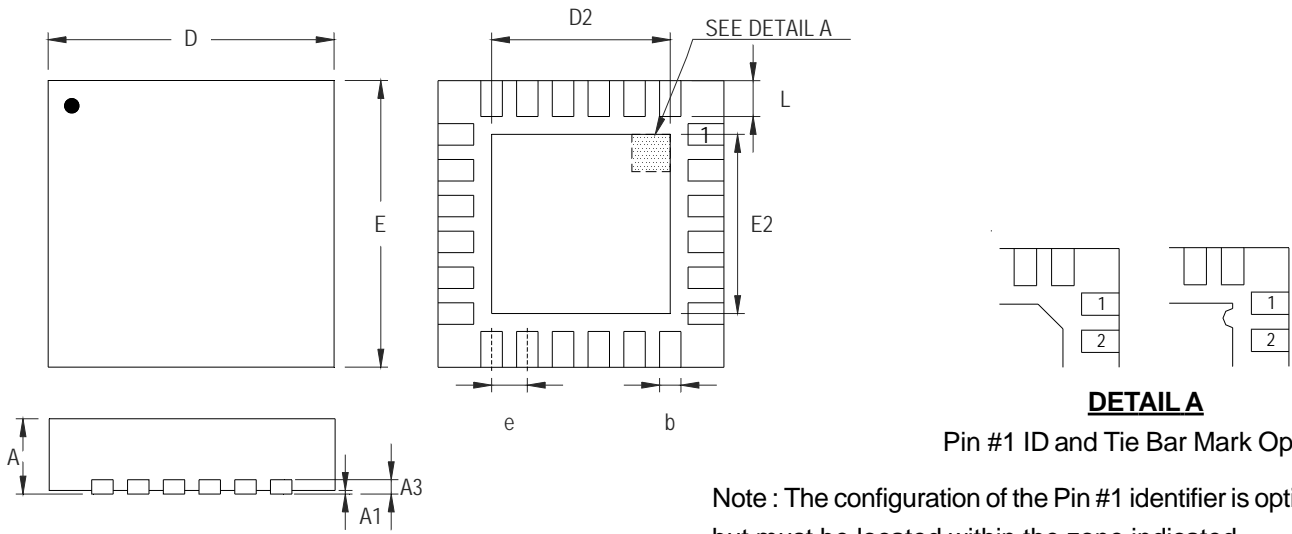


Figure 6. Synchronous Buck Converter Circuit

Outline Dimension



**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.350	0.010	0.014
D	4.950	5.050	0.195	0.199
D2	3.100	3.400	0.122	0.134
E	4.950	5.050	0.195	0.199
E2	3.100	3.400	0.122	0.134
e	0.650		0.026	
L	0.350	0.450	0.014	0.018

**W-Type 24L QFN 5x5 Package**

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