5.5V$_{IN}$, 2A, High Efficiency Synchronous Step-Down Converter with Low Quiescent Current

General Description

The RT5715 is a 2A, high-efficiency, Advanced Constant-On-Time (ACOT) synchronous step-down converter. The device operates with input voltages from 2.5V to 5.5V. The device can program the output voltage between 0.45V to VIN. The low quiescent current design with the integrated low $R_{DS(ON)}$ power MOSFETs achieves high efficiency over the wide load range. The advanced COT operation allows transient responses to be optimized over a wide range of loads, and output capacitors to efficiently reduce external component count. The RT5715 provides up to 2.7MHz switching frequency to minimize the size of output inductor and capacitors.

The RT5715 provides complete protection functions such as input under voltage lockout, output under voltage protection, over current protection, and thermal shutdown.

Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RT5715 is available in WDFN-8SL 2x2 package.

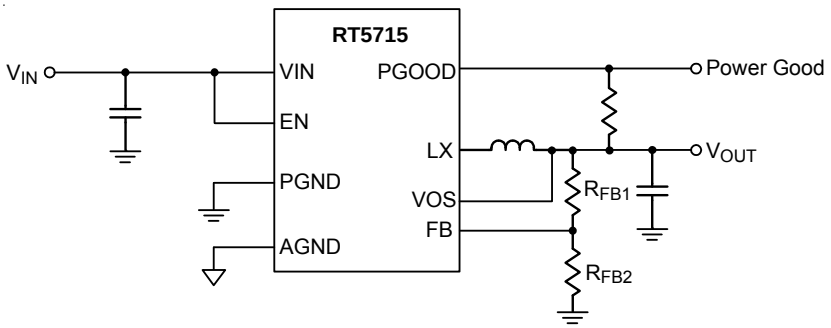
Applications

- Mobile Phones and Handheld Devices
- STB, Cable Modem, and xDSL Platforms
- WLAN ASIC Power / Storage (SSD and HDD)
- General Purpose for POL LV Buck Converter

Features

- **2A Converter Integrated 100mΩ and 80mΩ FETs in WDFN-8SL 2x2 Package**
- **Input Supply Voltage Range : 2.5V to 5.5V**
- **Output Voltage Range : 0.45V to V_{IN}**
- **Advanced Constant On-Time (ACOT™) Control**
  - **Ultrafast Transient Response**
  - **No Needs for External Compensations**
  - **Optimized for Low-ESR Ceramic Output Capacitors**
- **High Accuracy Feedback Reference Voltage : 0.45V ±1%**
- **Low Quiescent Current : 30μA**
- **Fixed Switching Frequency : 2.7MHz**
- **Internally Fixed Soft-Start (typ. 150μs)**
- **Safe Start-Up from Pre-biased Output**
- **Input Under-Voltage Lockout (UVLO)**
- **Output Under-Voltage Protection (UVP) with Hiccup Mode**
- **Over-Temperature Protection (OTP) (Thermal Shutdown)**
- **Enable Control**
- **Power Good Indication**
- **RoHS Compliant and Halogen Free**

Simplified Application Circuit



Ordering Information

RT5715 □□

Package Type
QW : WDFN-8SL 2x2 (W-Type)
(Exposed Pad-Option 2)

Lead Plating System
G : Green (Halogen Free and Pb Free)

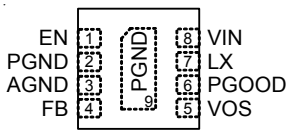
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

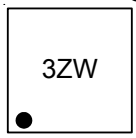
Pin Configuration

(TOP VIEW)



WDFN-8SL 2x2

Marking Information



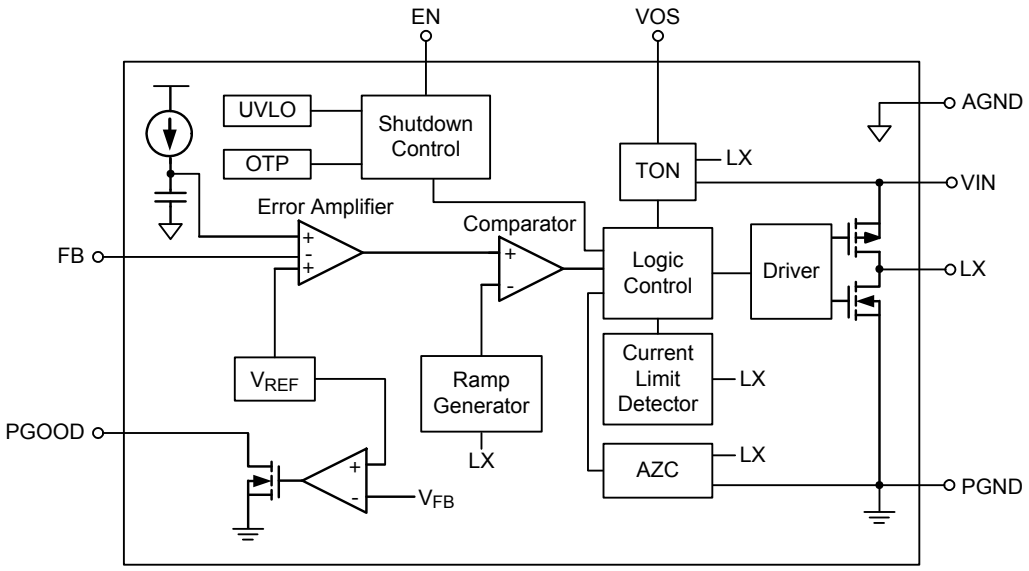
3Z : Product Code

W : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable control input. Connect this pin to logic high can enable the device and connect this pin to GND can disable the device.
2, 9 (Exposed Pad)	PGND	Power ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.
3	AGND	Analog ground. Should be electrically connected to GND close to the device.
4	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at Feedback Reference Voltage, typically 0.45V.
5	VOS	Output voltage sense pin for the internal control loop. Must be connected to output.
6	PGOOD	Power good open-drain output. This pin is pulled to low if the output voltage is below regulation limits. Can be left floating if not used.
7	LX	Switch node. The Source of the internal high-side power MOSFET, and Drain of the internal low-side (synchronous) rectifier MOSFET.
8	VIN	Power input supply voltage, 2.5V to 5.5V.

Functional Block Diagram



Operation

The RT5715 is a low voltage synchronous step-down converter that can support input voltage ranging from 2.5V to 5.5V and the output current can be up to 2A. The RT5715 uses ACOT™ mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation :

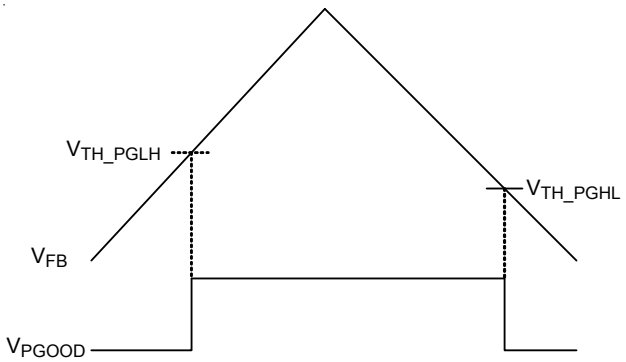
$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{OSC}}$$ where f_{OSC} is nominal 2.7MHz

Input Under-Voltage Lockout

In addition to the EN pin, the RT5715 also provides enable control through the VIN pin. If V_{EN} rises above V_{EN_H} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold voltage (V_{UVLO} - ΔV_{UVLO}), this switching will be inhibited; if VIN rises above the UVLO rising threshold (V_{UVLO}), the device will resume normal operation with a complete soft-start.

Power Good Indication

The RT5715 features an open-drain power-good output (PGOOD) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PGOOD with a resistor to VOUT or an external voltage below 5.5V. The power-good function is activated after soft start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above a power-good high threshold (V_{TH_PGLH}) (typically 95% of the reference voltage), the PGOOD pin will be in high impedance and V_{PG} will be held high. When V_{FB} falls short of power-good low threshold (V_{TH_PGHL}) (typically 90% of the reference voltage), the PGOOD pin will be pulled low. Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND. The internal open-drain pull-down device will pull the PGOOD pin low. The power good indication profile is shown below.



Output Under-Voltage Protection and Hiccup Mode

The RT5715 includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 66% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches. The RT5715 will enter output under-voltage protection with hiccup mode. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.

The Over-Current Protection

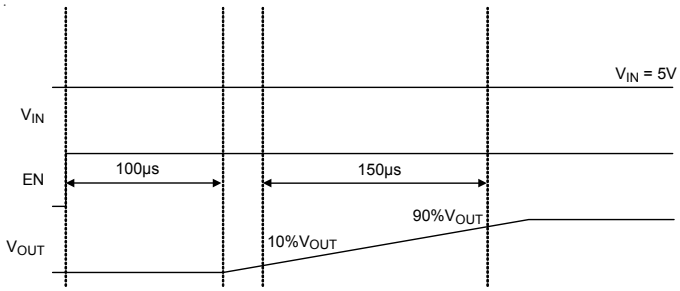
The RT5715 features cycle-by-cycle current-limit protection on both the high-side and low-side MOSFETs and prevents the device from the catastrophic damage in output short circuit, over current or inductor saturation.

The high-side MOSFET over-current protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET during each on-time. The switch current is compared with the high-side switch peak-current limit (I_{LIM_H}) after a certain amount of delay when the high-side switch being turned on each cycle. If an over-current condition occurs, the converter will immediately turns off the high-side switch and turns on the low-side switch to prevent the inductor current exceeding the high-side current limit.

The low-side MOSFET over-current protection is achieved by measuring the inductor current through the synchronous rectifier (low-side switch) during the low-side on-time. Once the current rises above the low-side switch valley current limit (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. If the output load current exceeds the available inductor current (clamped by the low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output under-voltage protection trip threshold, the IC will stop switching to avoid excessive heat.

Soft-Start (SS)

The RT5715 provides an internal soft-start feature for inrush control. At power up, the internal capacitor is charged by an internal current source to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB} to ensure the converters have a smooth start-up from pre-biased output. The output voltage starts to rise in 100µs from EN rising, and the soft-start ramp-up time (10%V_{OUT} to 90%V_{OUT}) is 150µs.



Thermal Shutdown

The RT5715 includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold (T_{SD}). Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Note that the over temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Maximum Duty Cycle Operation

The RT5715 is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off time becomes smaller than minimum off time, the RT5715 starts to enable skip off time function and keeps high-side MOSFET switch on continuously. The RT5715 implements skip off time function to achieve high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 6V
- Switch Voltage, LX ---------- –0.3V to 6V
  < 50ns ---------- –2.5V to 7V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8SL 2x2 ---------- 1.538W
- Package Thermal Resistance (Note 2)
  WDFN-8SL 2x2, θ_{JA} ---------- 65°C/W
  WDFN-8SL 2x2, θ_{JC} ---------- 8°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Under-Voltage Lockout Threshold		V_{UVLO}	V_{CC} rising	2.28	2.35	2.48	V
Under-Voltage Lockout Hysteresis		ΔV_{UVLO}		--	400	--	mV
Shutdown Supply Current		I_{SHDN}	EN = 0V	--	--	1	μA
Quiescent Current		I_Q	Active, V_{FB} = 0.5V, no switching	--	30	--	μA
Voltage Reference		V_{REF}		0.4455	0.45	0.4545	V
Current Limit	High-Side	I_{LIM_H}	Peak current	2.5	3.2	4	A
	Low-Side	I_{LIM_L}	Valley current	2	2.4	2.9	
Power Good High Threshold		V_{TH_PGLH}	V_{FB} rising, PGOOD goes high	90	95	100	%
Power Good High Hysteresis		ΔV_{TH_PGLH}	V_{FB} falling, PGOOD goes low	--	5	--	%
Power Good Leakage Current		I_{PG}	V_{PG} = 5V	--	0.01	0.1	μA
Power Good Low Level Voltage		V_{PGL}	I_{sink} = 500μA	--	--	0.3	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Enable Rising Threshold		V_{ENR}	Rising	1	--	--	V
Enable Falling Threshold		V_{ENF}	Falling	--	--	0.4	V
Soft-Start Time		t_{SS}	10%V_{OUT} to 90%V_{OUT}	--	150	--	μs
Switch On-Resistance	High-Side	$R_{P-MOSFET}$		--	100	--	mΩ
	Low-Side	$R_{N-MOSFET}$		--	80	--	
Minimum On-Time		t_{ON_MIN}		--	60	--	ns
Minimum Off-Time		t_{OFF_MIN}		--	90	--	ns
UVP Trip Threshold		V_{UVP}	Hiccup detect	--	66	--	%
Thermal Shutdown Temperature				--	150	--	°C
Thermal Shutdown Hysteresis				--	20	--	°C
Switching Frequency		f_{OSC}		--	2.7	--	MHz
Output Discharge Resistor				--	1	--	kΩ

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package. The copper area is 70mm^2 connected with IC exposed pad.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

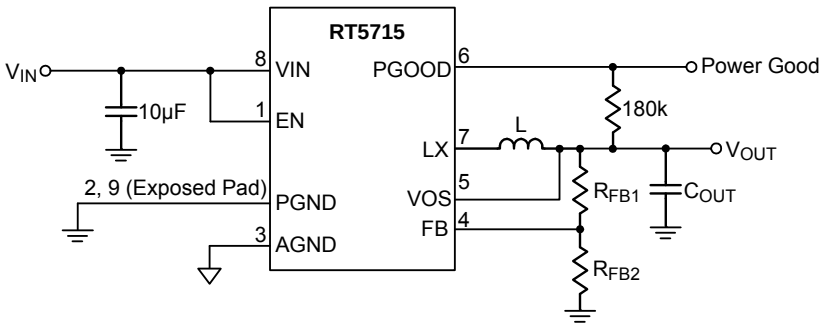
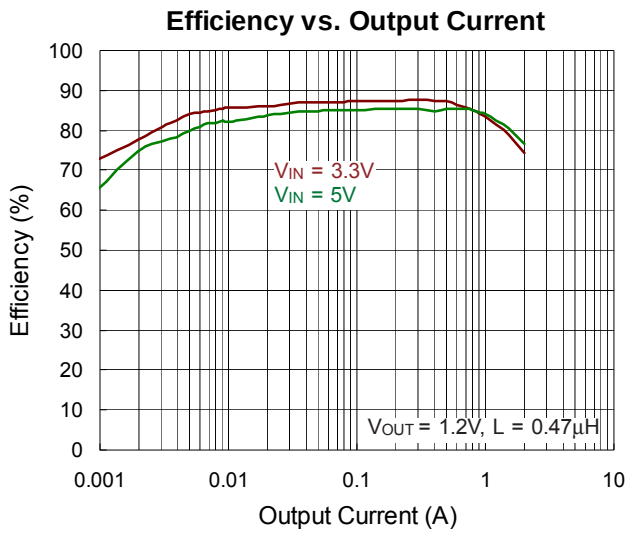
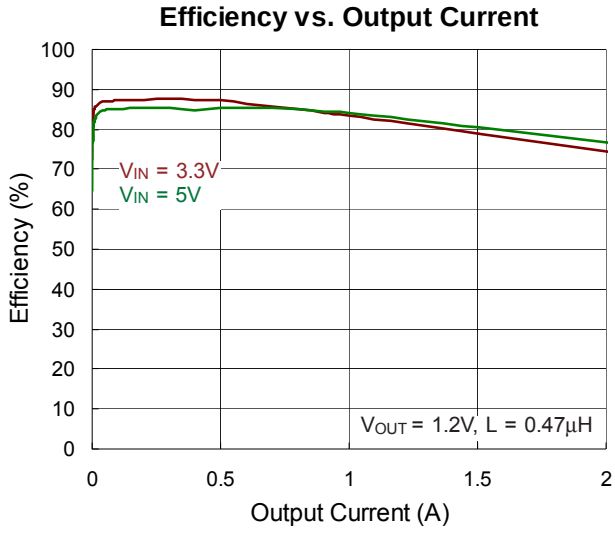


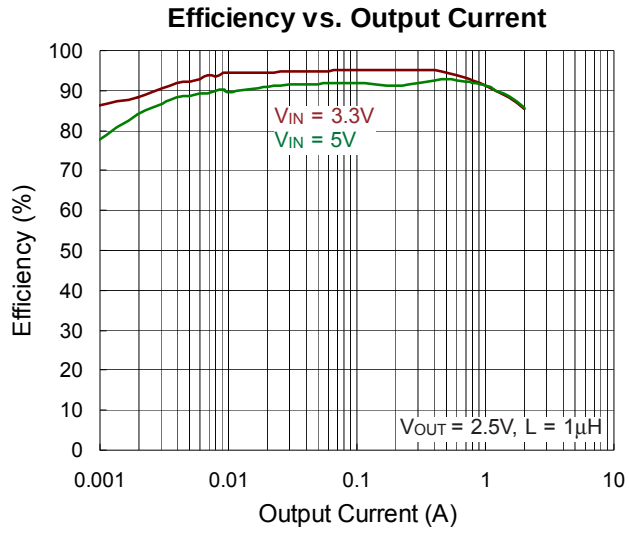
Table 1. Suggested Component Values

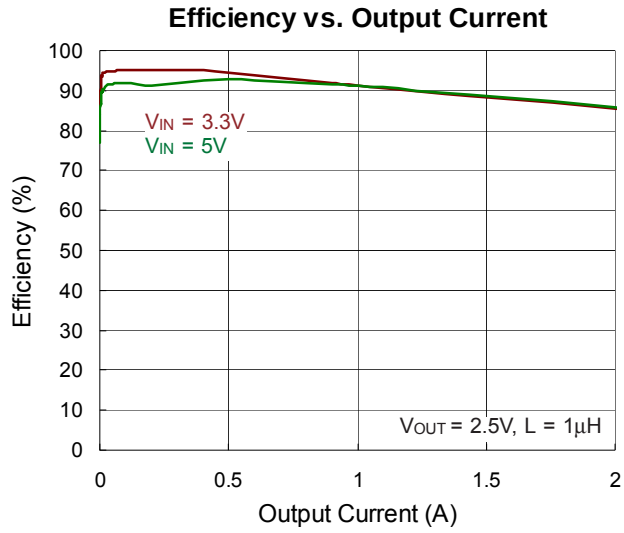
V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	L (µH)	C_{OUT} (µF)
1.2V	65.3	39.2	0.47	22
1.8V	117.6	39.2	1	22
2.5V	178.6	39.2	1	22
3.3V	248.3	39.2	1	22

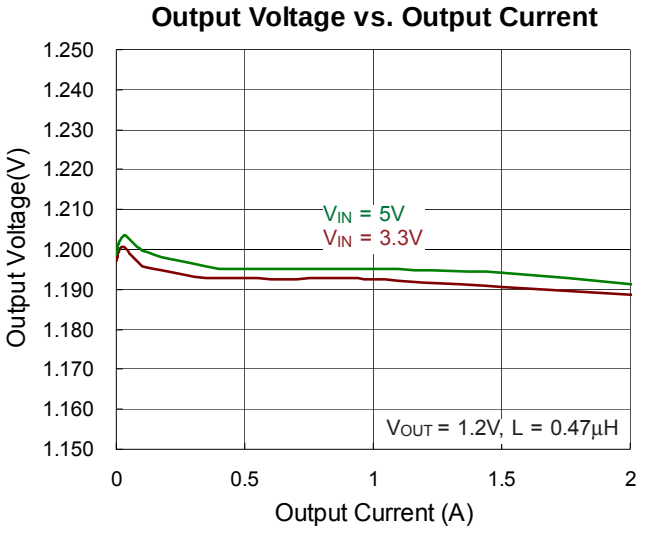
Typical Operating Characteristics

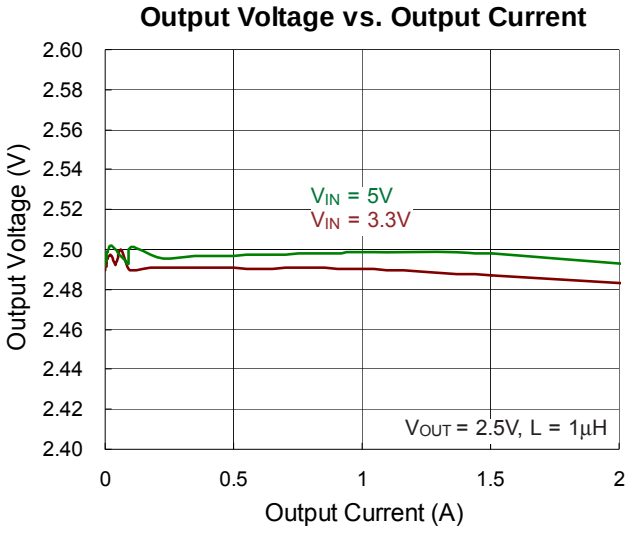




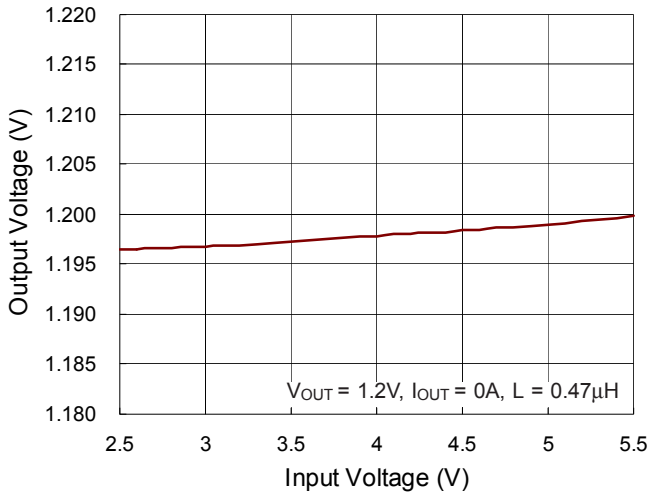








Output Voltage vs. Input Voltage



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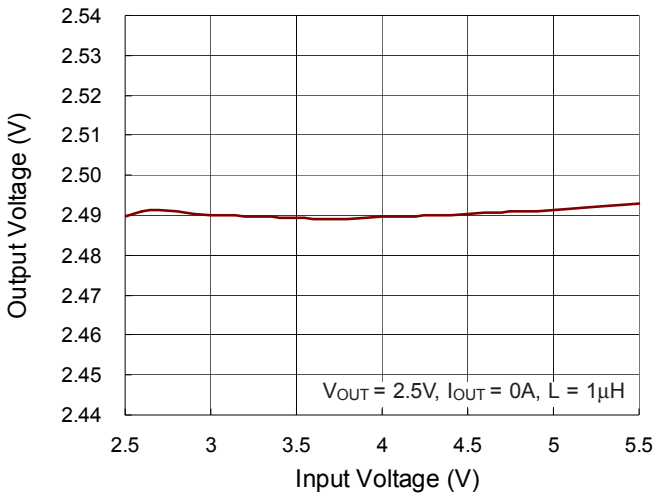
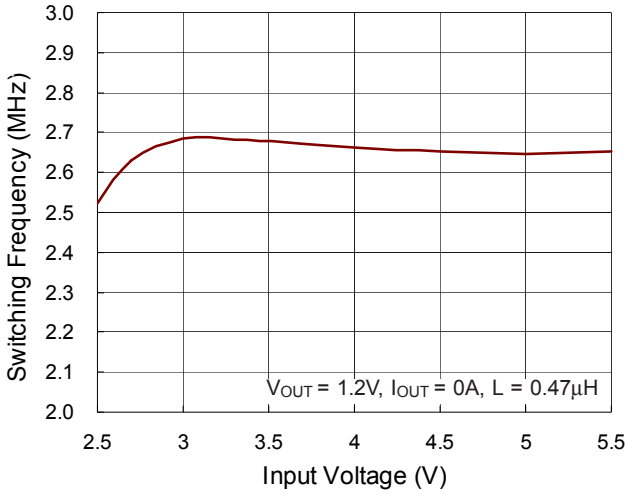
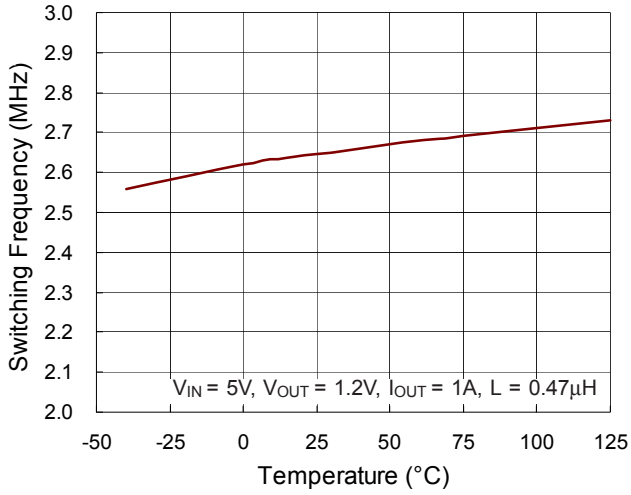


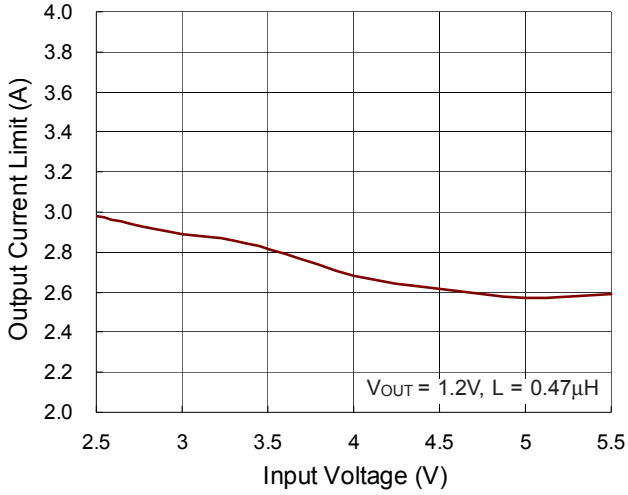
Switching Frequency vs. Input Voltage



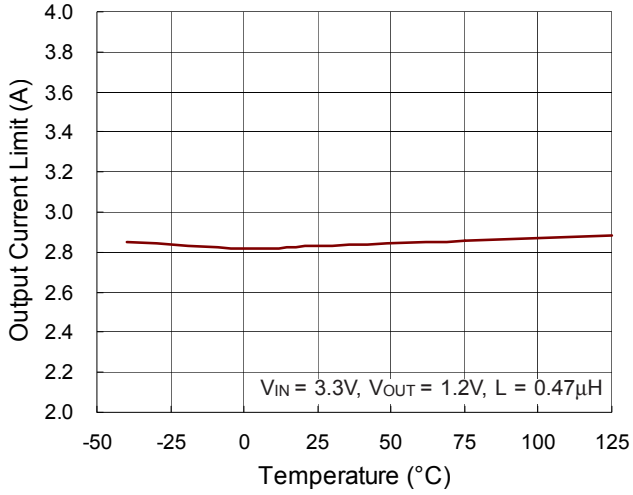
Switching Frequency vs. Temperature



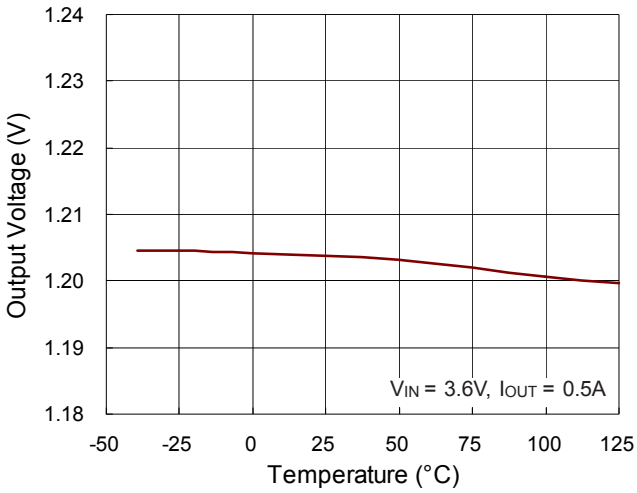
Output Current Limit vs. Input Voltage



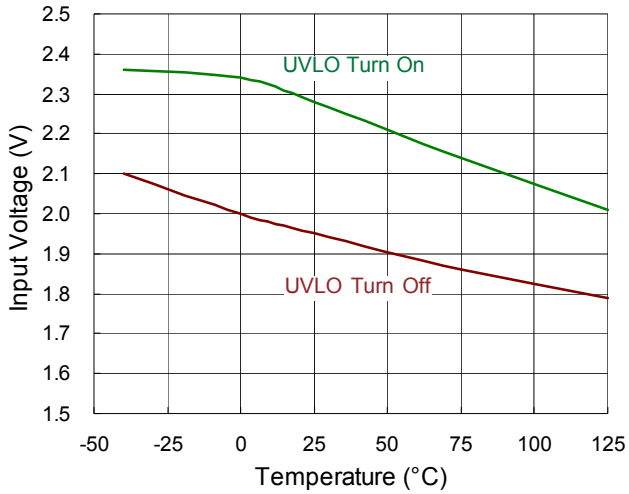
Output Current Limit vs. Temperature



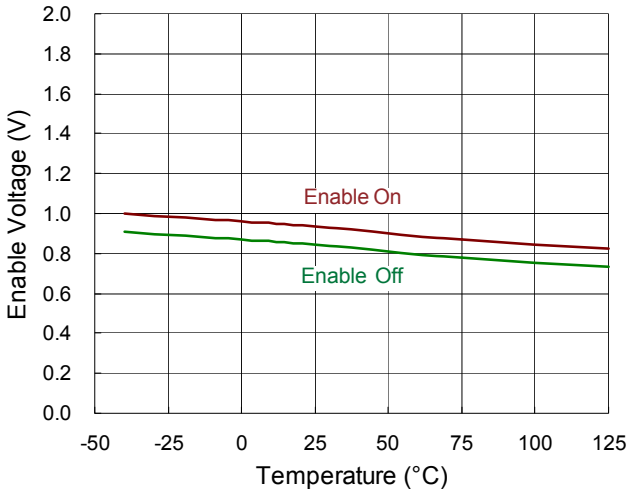
Output Voltage vs. Temperature



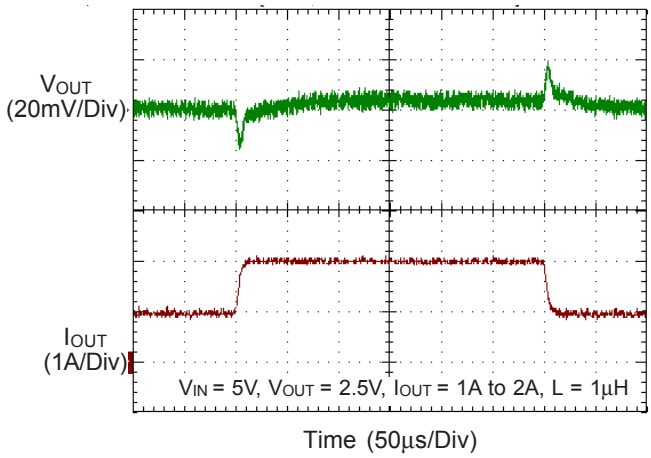
Input Voltage vs. Temperature



Enable Threshold vs. Temperature



Load Transient Response



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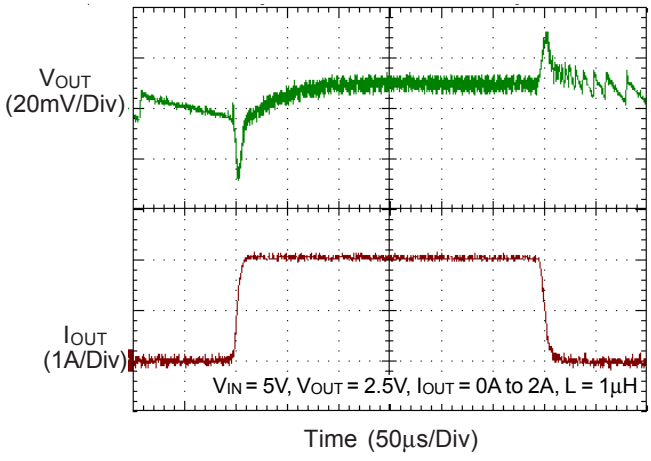

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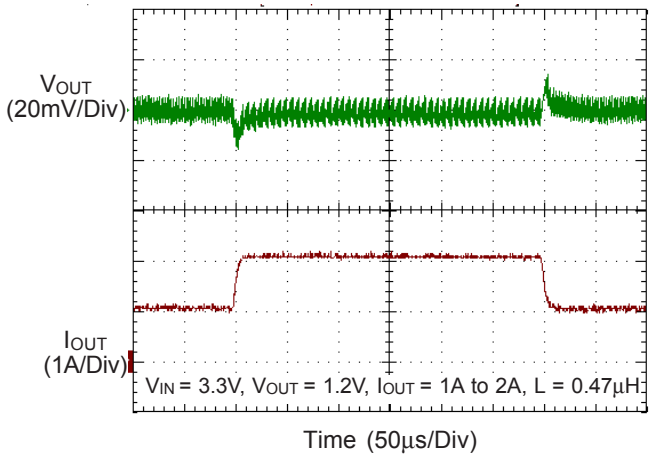

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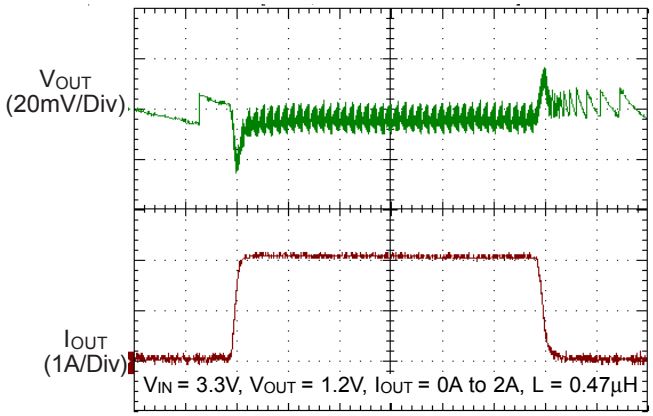
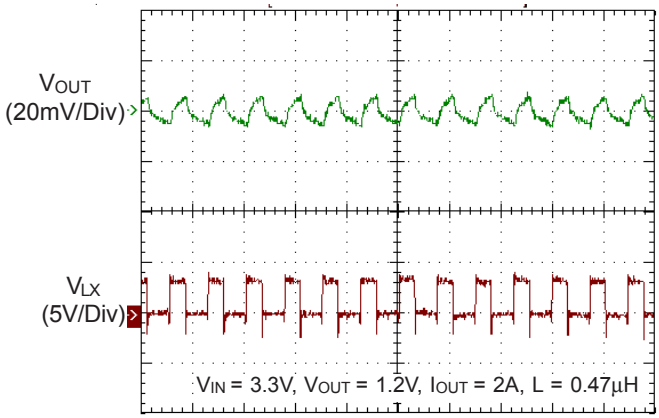
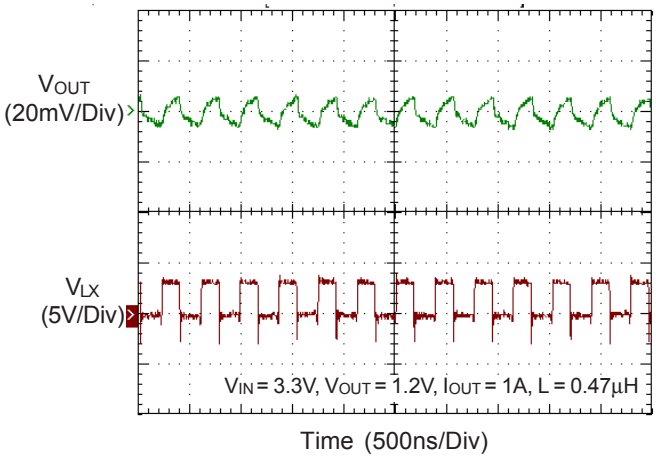


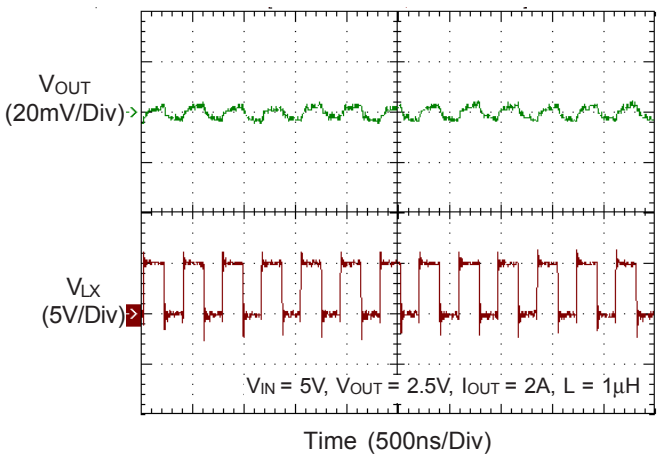
Voltage Ripple



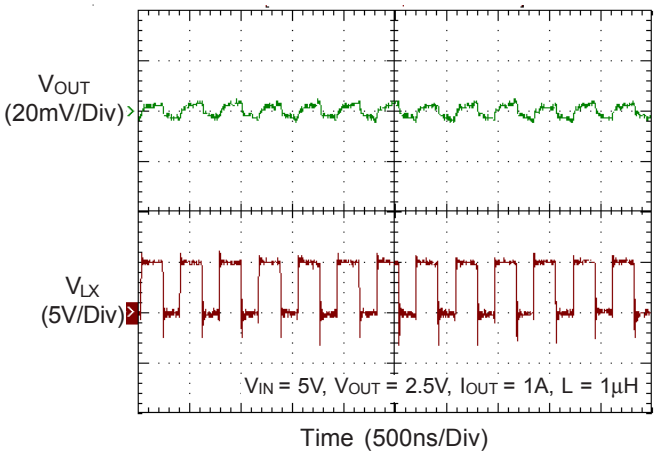
Voltage Ripple



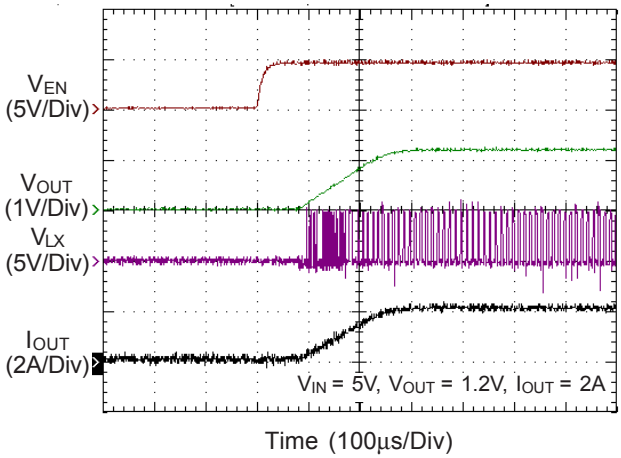
Voltage Ripple



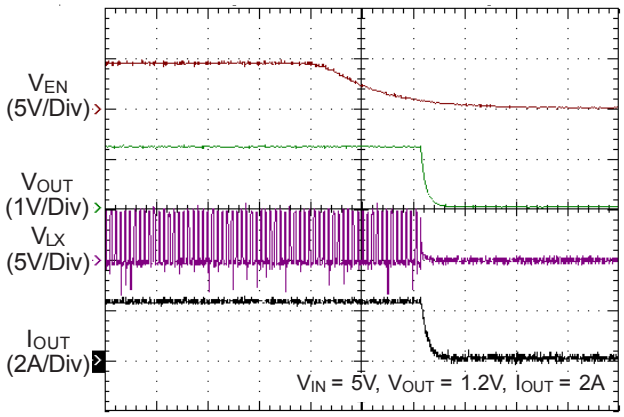
Voltage Ripple



Power On from VIN



Power Off from VIN



Application Information

The output stage of a synchronous buck converter is composed of an inductor and capacitor, which stores and delivers energy to the load, and forms a second-order low-pass filter to smooth out the switch node voltage to maintain a regulated output voltage.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 50% of the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

$I_{L(PEAK)}$ should not exceed the minimum value of IC's upper current limit level. Besides, the current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Considering the Typical Application Circuit for 1.2V output at 2A and an input voltage of 5V, using an inductor ripple of 0.8A (40% of the IC rated current), the calculated inductance value is :

$$L = \frac{1.2 \times (5 - 1.2)}{5 \times 2.7MHz \times 0.8A} = 0.42\mu H$$

For the typical application, a standard inductance value of 0.47µH can be selected.

$$\Delta I_L = \frac{1.2 \times (5 - 1.2)}{5 \times 2.7MHz \times 0.47\mu H} = 0.72A \text{ (36\% of the IC rated current)}$$

$$\text{and } I_{L(PEAK)} = 2A + \frac{0.72A}{2} = 2.36A$$

For the 0.47µH value, the inductor's saturation and thermal rating should exceed at least 2.36A. For more conservative, the rating for inductor saturation current must be equal to or greater than switch current limit of the device rather than the inductor peak current.

For EMI sensitive application, choosing shielding type inductor is preferred.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The waveform of C_{IN} ripple voltage and ripple current are shown in Figure 1. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1 - D}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum input capacitance can be estimated as equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1 - D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

Where $\Delta V_{CIN\_MAX} \leq 200mV$

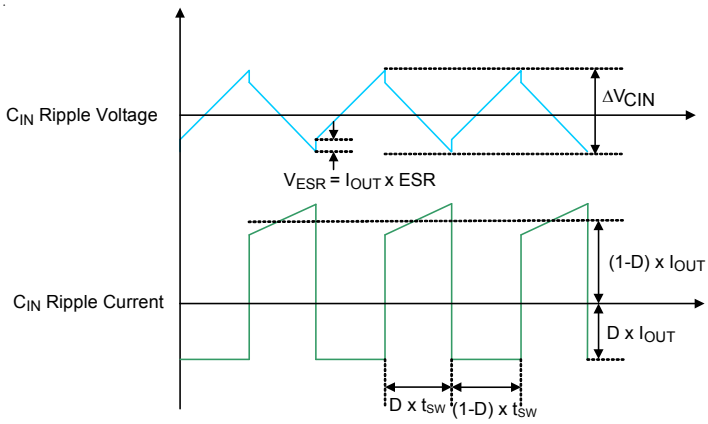


Figure 1. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of :

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is commonly to use the worse $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications due to its small, robust and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RT5715 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the GND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitors of 0.1μF should be placed close to the VIN and GND pin. This capacitor should be 0402 or 0603 in size.

Output Capacitor Selection

The RT5715 are optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on load apply) and soar (overshoot on load release).

Output Ripple

The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance, C_{OUT}, and its equivalent series resistance, R_{ESR}, must be taken into consideration. The output peak-to-peak ripple voltage V_{RIPPLE}, caused by the inductor current ripple ΔI_L, is characterized by two components, which are ESR ripple $V_{RIPPLE(ESR)}$ and capacitive ripple $V_{RIPPLE(C)}$, can be expressed as below :

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

If ceramic capacitors are used as the output capacitors, both the components need to be considered due to the extremely low ESR and relatively small capacitance.

For the RT5715's Typical Application Circuit for output voltage of 1.2V, and actual inductor current ripple (ΔI_L) of 0.72A, taking a 22μF ceramic capacitors of GRM188R60J226MEA0 from Murata as example, the output ripple of the output capacitor is as below :

The ripple caused by the ESR of about 5mΩ can be calculated as

$$V_{RIPPLE(ESR)} = 0.72A \times 5m\Omega = 3.6mV$$

Due to DC bias capacitance degrading, the effective capacitance at output voltage of 1.2V is about 14.8μF

$$V_{RIPPLE(C)} = \frac{0.72A}{8 \times 14.8\mu F \times 2.7MHz} = 2.25mV$$

$$V_{RIPPLE} = 3.6mV + 2.25mV = 5.85mV$$

Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT™ transient response is very quick and output transients are usually small. The following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components : the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasites) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Due to some modern digital loads can exhibit nearly instantaneous load changes, the amplitude of the ESR step up or down should be taken into consideration.

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB, as shown in Figure 2. The output voltage is set according to the following equation :

$V_{OUT} = 0.45V \times (1 + R_{FB1} / R_{FB2})$

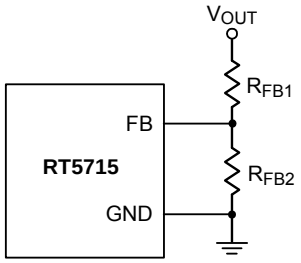


Figure 2. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. For output voltage accuracy, use divider resistors with 1% or better tolerance.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For

a WDFN-8SL 2x2 package, the thermal resistance, θ_{JA}, is 65°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (65°C/W) = 1.538W for a WDFN-8SL 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

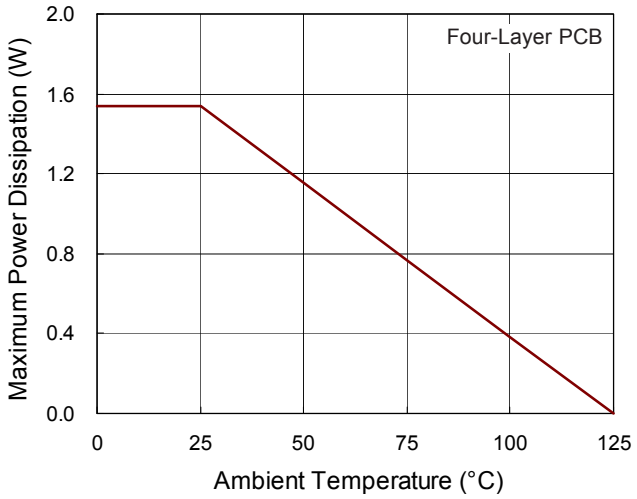


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and GND pins as possible. The major MLCC capacitors should be placed on the same layer as the RT5715.
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Place the feedback components next to the FB pin.
- For better thermal performance, to design a wide and thick plane for GND pin or to add a lot of vias to GND plane.

An example of PCB layout guide is shown from Figure 4.

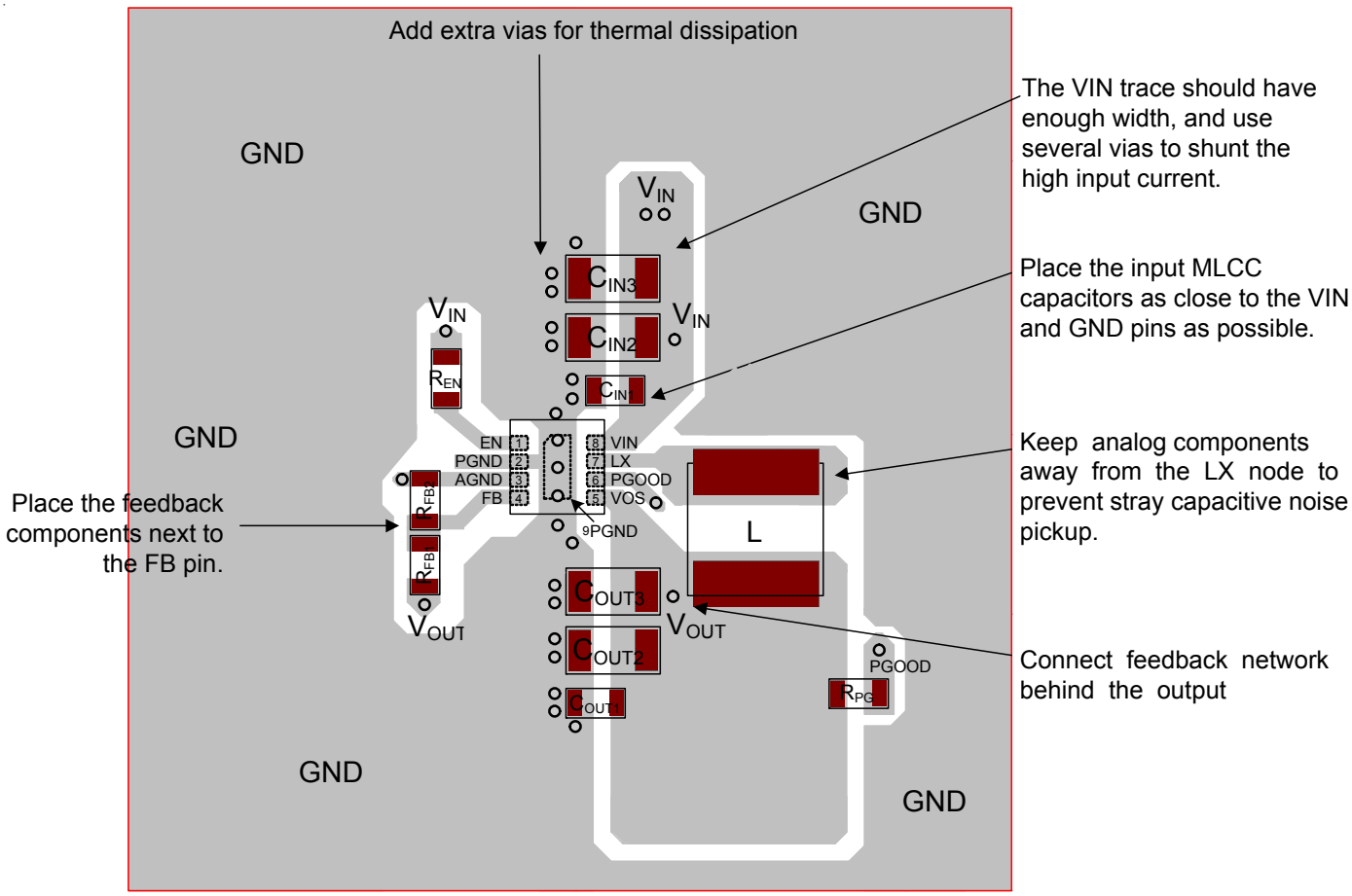
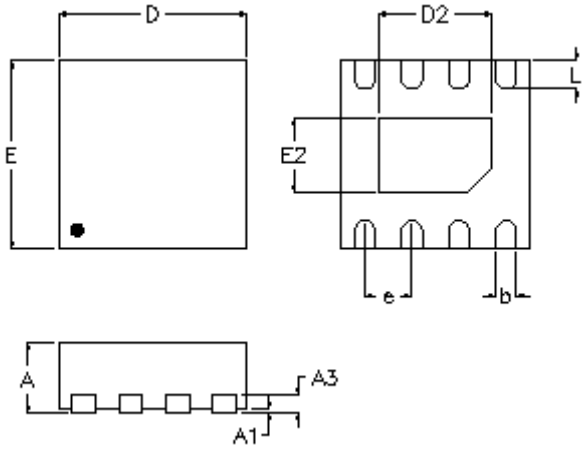
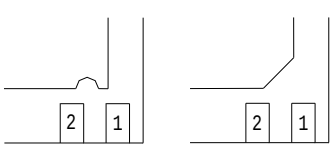


Figure 4. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.200	0.300	0.008	0.012
D		1.900	2.100	0.075	0.083
D2	Option1	1.150	1.250	0.045	0.049
	Option2	1.550	1.650	0.061	0.065
E		1.900	2.100	0.075	0.083
E2	Option1	0.750	0.850	0.030	0.033
	Option2	0.850	0.950	0.033	0.037
e		0.500		0.020	
L		0.250	0.350	0.010	0.014

W-Type 8SL DFN 2x2 Package

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单击下面可查看定价，库存，交付和生命周期等信息

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