Programmable USB Type-C PD Controller

General Description

The RT1711H is a USB Type-C controller that complies with the latest USB Type-C and PD standards. The RT1711H integrates a complete Type-C Transceiver including the Rp and Rd resistors. It does the USB Type-C detection including attach and orientation. The RT1711H integrates the physical layer of the USB BMC power delivery protocol to allow up to 100W of power and role swap. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

Ordering Information

RT1711H□

Package Type
WSC : WL-CSP-9B 1.38x1.34 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

4G : Product Code

W : Date Code

Features

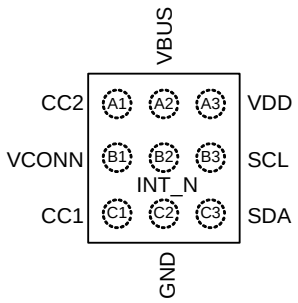
- **Dual-Role PD Compatible**
- **Attach/Detach Detection as Host, Device or DRP**
- **Current Capability Definition and Detection**
- **Cable Recognition**
- **Alternate Mode Support**
- **Supporting VCONN with Programmable OCP**
- **Dead Battery Support**
- **Low Power Mode for Attach Detection**
- **Simple I^2C Interface with AP or EC**
- **BIST Mode Supported**
- **e-fuse IP**
- **9-Ball WL-CSP Package**

Applications

- Smartphones
- Tablets
- Laptops

Pin Configuration

(TOP VIEW)

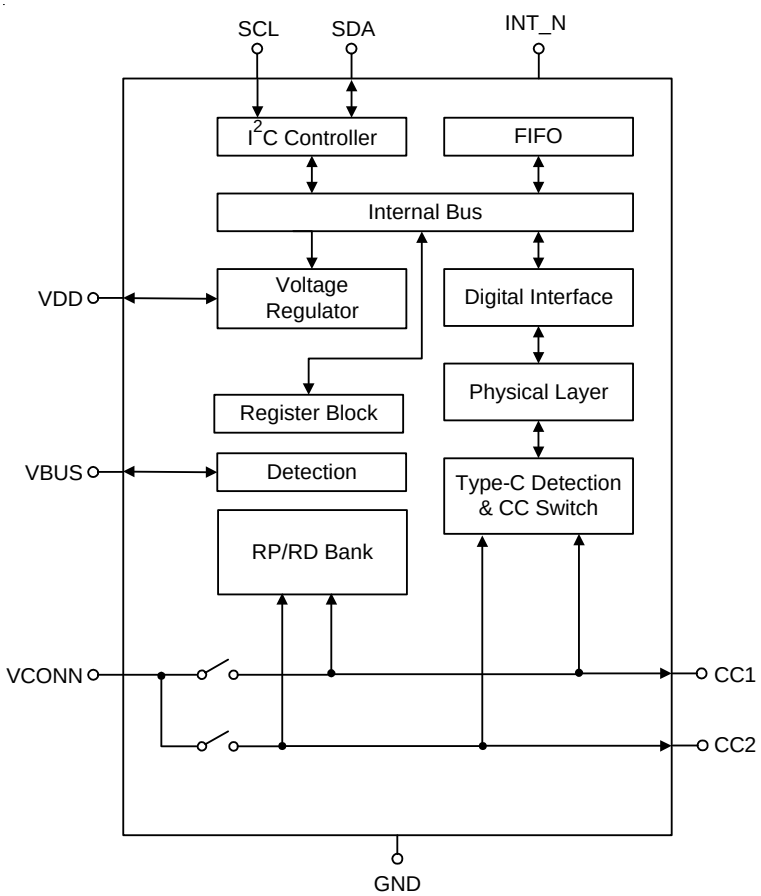


WL-CSP-9B 1.38x1.34 (BSC)

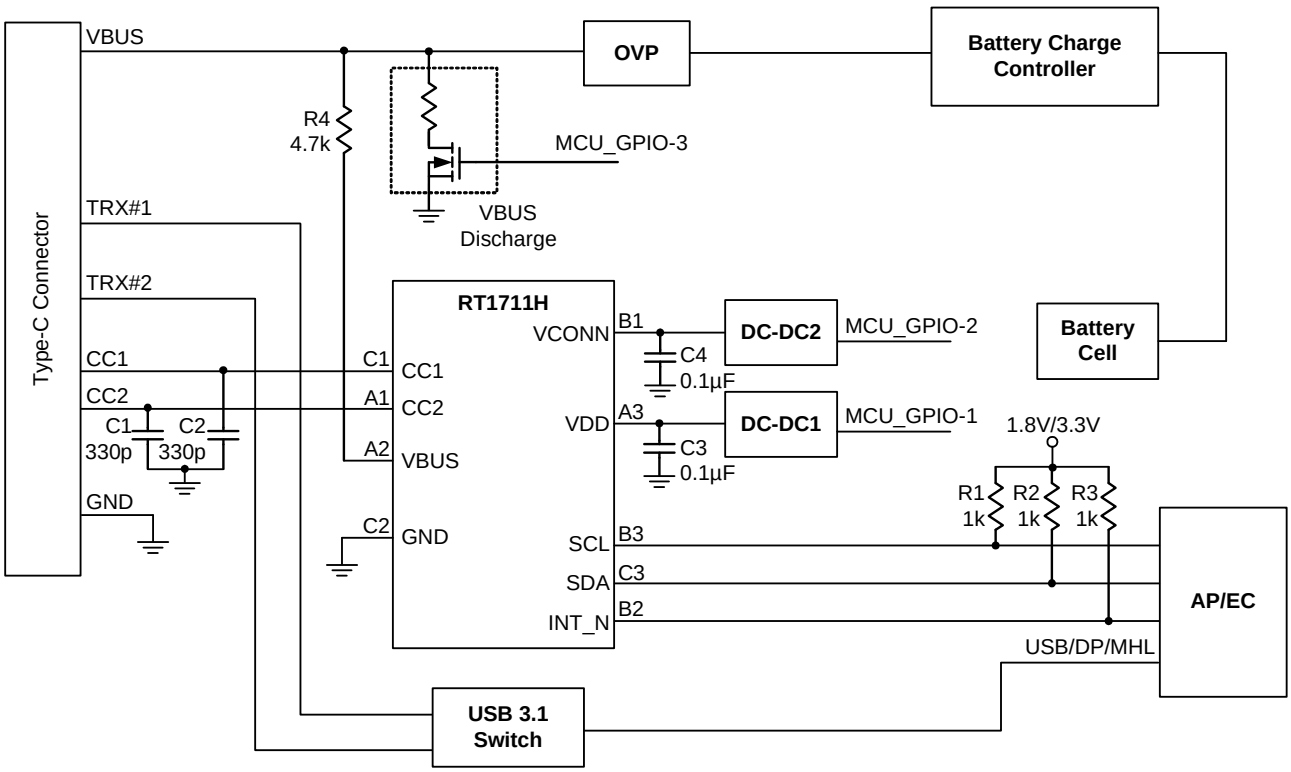
Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	CC2	Type-C Connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation detected.
A2	VBUS	VBUS input pin for attach and detach detection.
A3	VDD	Input supply voltage.
B1	VCONN	Regulated input pin to be switched to correct CC pin as VCONN to power Type-C full-featured cables and other accessories.
B2	INT_N	Open drain type interrupt output used to prompt the processor to read the registers.
B3	SCL	I^2C serial clock signal to be connected to the I^2C master.
C1	CC1	Type-C Connector Configuration Channel (CC) Pins. Initially used to determine when an attach has occurred and what the orientation detected.
C2	GND	Ground pin.
C3	SDA	I^2C serial data signal to be connected to the I^2C master.

Functional Block Diagram



Typical Application Circuit



Note :
VDD can not be powered directly by VBAT or VSYS.
MCU_GPIO-1/MCU_GPIO-2 control DC-DC power IC EN pin for power on/off sequence and phone shutdown mode.

Table 1. Recommended Components Information

Reference	Part Number	Description	Package	Manufacturer
R1, R2, R3	WR04X1001FTL	1kΩ 1%	0402	WALSIN
R4	CR-02FL6---4K7	4.7kΩ 1%	0402	VIKING
C1, C2	0402B331J250	330pF/25V/X7R	0402	WALSIN
C3, C4	0402B104K500CT	100nF/50V/X7R	0402	WALSIN

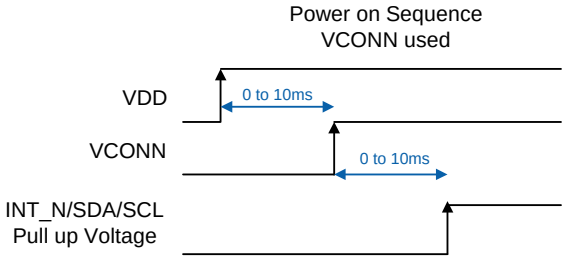
Table 2. Funtion Portfolio Information

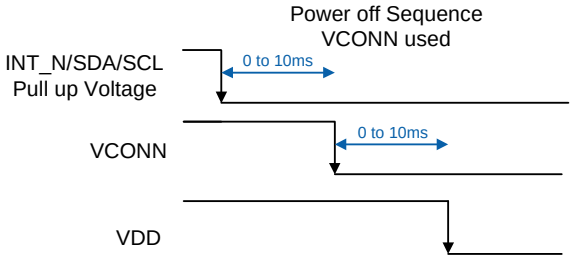
Function Portfolio	Pin Name	Pin Connection
Use VCONN	VBUS	Short to connector VBUS or 4.7k to connector VBUS (better for surge)
	CC1	Short to connector CC1
	CC2	Short to connector CC2
	VCONN	Short to DC-DC2
	INT_N	Pull-high to AP/EC
	SDA	Pull-high to AP/EC
	SCL	Pull-high to AP/EC
	VDD	Short to DC-DC1
Unused VCONN	VBUS	Short to connector VBUS or 4.7k to connector VBUS (better for surge)
	CC1	Short to connector CC1
	CC2	Short to connector CC2
	VCONN	1k to GND
	INT_N	Pull-high to AP/EC
	SDA	Pull-high to AP/EC
	SCL	Pull-high to AP/EC
	VDD	Short to DC-DC1

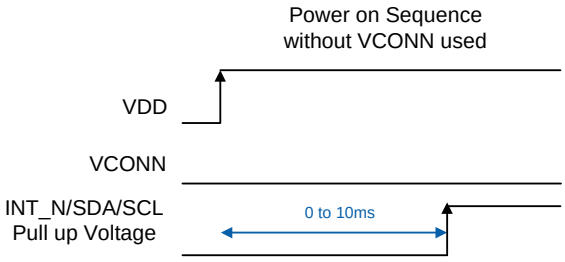
Note : If VBUS is shorted between the OVP and Battery Charge Controller, it will occur USB compliance testing failures and application issues.

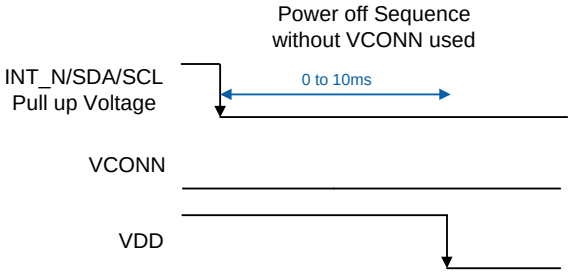
Operation

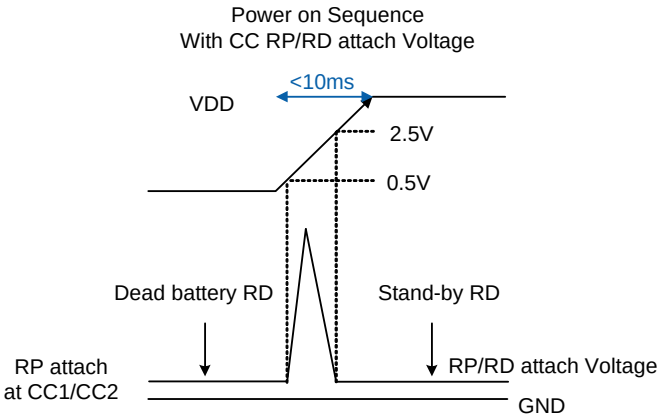
Power On/Off Sequence



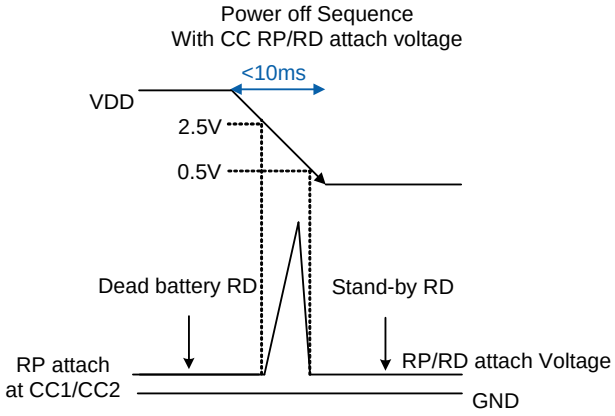








CC can't apply RD at VDD 0.5V to 2.5V
VDD rising timing needs less than 10ms
RP current is 64µA to 356µA.



CC can't apply RD at VDD 0.5V to 2.5V
VDD falling timing needs less than 10ms
RP current is 64µA to 356µA

Absolute Maximum Ratings (Note 1)

- VDD/VCONN ---------- –0.3V to 6V
- CC1/CC2 (Testing Condition : VDD ≥ 3V) ---------- –0.3V to 24V
- CC1/CC2 (Testing Condition : VDD < 3V) ---------- –0.3V to 6V
- VBUS ---------- –0.3V to 28V
- SDA/SCL/INT_N ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-9B 1.38x1.34 (BSC) ---------- 1.22W
- Package Thermal Resistance (Note 2)
  WL-CSP-9B 1.38x1.34 (BSC), θ_{JA} ---------- 81.5°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- VDD Input Voltage ---------- 3.0V to 5.5V
- VCONN Input Voltage ---------- 3.3V to 5.5V (Note 5)
- VCON Supply Current ---------- 200mA to 600mA
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Common Normative Signaling Requirements						
Bit Rate	$f_{BitRate}$	V_{DD} = 3V to 5.5V	270	300	330	Kbps
Common Normative Signaling Requirements for Transmitter						
Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate	$p_{BitRate}$	V_{DD} = 3V to 5.5V	--	--	0.25	%
Time from the end of last bit of a Frame until the start of the first bit of the next Preamble	$t_{InterFrameGap}$	V_{DD} = 3V to 5.5V	25	--	--	µs
Time before the start of the first bit of the Preamble when the transmitter shall start driving the line	$t_{StartDrive}$	V_{DD} = 3V to 5.5V	–1	--	1	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BMC Common Normative Requirements						
Time to cease driving the line after the end of the last bit of the Frame	$t_{EndDriveBMC}$	V_{DD} = 3V to 5.5V	--	--	23	μs
Fall Time	t_{Fall}	V_{DD} = 3V to 5.5V	300	--	--	ns
Time to cease driving the line after the final high-to-low transition	$t_{HoldLowBMC}$	V_{DD} = 3V to 5.5V	1	--	--	μs
Rise Time	t_{Rise}	V_{DD} = 3V to 5.5V	300	--	--	ns
Voltage Swing	V_{Swing}	V_{DD} = 3V to 5.5V	1.050	1.125	1.200	V
Transmitter Output Impedance	z_{Driver}	V_{DD} = 3V to 5.5V	33	--	75	Ω
BMC Receiver Normative Requirements						
Time Window for Detecting Non-Idle	$t_{TransitionWindow}$	V_{DD} = 3V to 5.5V	12	--	20	μs
Receiver Input Impedance	z_{BmcRx}	V_{DD} = 3V to 5.5V	1	--	--	MΩ
Power Consumption						
Stand-by Current	I_{SB_Sink}	Sink current consumption in cable attached V_{DD} = 3V to 5.5V V_{DD} (Typ.) = 3.8V	1.2	2.15	4.2	mA
Low Power Mode	I_{LP_DRP}	CC toggle at DRP mode when port is unconnected and waiting for connection V_{DD} = 3V to 5.5V V_{DD} (Typ.) = 3.8V	10	25	85	μA
VCONN power	I_{VCONN}	VCONN current consumption when VCONN without supply to CC V_{CONN} = 3V to 5.5V V_{CONN} (Typ.) = 5V	6	20	30	μA
Type-C Port Control						
Ron for VCONN Switch	R_{ON}	V_{CONN} = 3V to 5.5V	--	0.7	1	Ω
VCONN OCP Setting Range	I_{OCP}	V_{DD} = 3V to 5.5V, V_{CONN} = 3.3V to 5.5V	200	--	600	mA
VCONN OCP Range_200mA	$I_{OCP\_Range\_200mA}$	V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 200mA	135	205	275	mA
VCONN OCP Range_300mA	$I_{OCP\_Range\_300mA}$	V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 300mA	240	310	380	mA
VCONN OCP Range_400mA	$I_{OCP\_Range\_400mA}$	V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 400mA	345	415	485	mA
VCONN OCP Range_500mA	$I_{OCP\_Range\_500mA}$	V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 500mA	450	520	590	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCONN OCP Range_600mA	$I_{OCP\_Range\_600mA}$	V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 600mA	555	625	695	mA
Time for VCONN Switch to Turn-On State_3.3V	$t_{Soft\_VCCON\_3.3V}$	V_{DD} = 3.3V, V_{CONN} = 3.3V	350	450	620	µs
Time for VCONN Switch to Turn-On State_5V	$t_{Soft\_VCCON\_5V}$	V_{DD} = 3.3V, V_{CONN} = 5V	460	540	720	µs
DFP 80µA CC Current	$DFP_{80µ}$	V_{DD} = 3V to 5.5V	64	80	96	µA
DFP 180µA CC Current	$DFP_{180µ}$	V_{DD} = 3V to 5.5V	166	180	194	µA
DFP 330µA CC Current	$DFP_{330µ}$	V_{DD} = 3V to 5.5V	304	330	356	µA
UFP Rd	Rd	V_{DD} = 3V to 5.5V	4.59	5.10	5.61	kΩ
UFP Pull-Down Voltage in Dead Battery Under DFP80µ and DFP180µA	V_{DBL}	V_{DD} = 0V	--	--	1.6	V
UFP Pull-Down Voltage in Dead Battery Under DFP330µA	V_{DBH}	V_{DD} = 0V	--	--	2.6	V
I^2C Electrical Characteristics						
I^2C Bus Supply Voltage	I^2C_VDD	V_{DD} = 3V to 5.5V	1.5	--	3.6	V
LOW-Level Input Voltage	V_{IL}	V_{DD} = 3V to 5.5V	--	--	0.4	V
HIGH-Level Input Voltage	V_{IH}	V_{DD} = 3V to 5.5V	1.3	--	--	V
LOW-Level Output Voltage	V_{OL}	V_{DD} = 3V to 5.5V, Open-drain	--	--	0.4	V
Input Current Each IO Pin	I_I	V_{DD} = 3V to 5.5V, $0.1V_{DD} < V_I < 0.9V_{DDMAX}$	–10	--	10	µA
SCL Clock Frequency	f_{SCL}	V_{DD} = 3V to 5.5V	0	--	3400	kHz
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	V_{DD} = 3V to 5.5V	--	--	50	ns
Data Hold Time	$t_{HD:DAT}$	V_{DD} = 3V to 5.5V	30	--	--	ns
Data Set-Up Time	$t_{SU:DAT}$	V_{DD} = 3V to 5.5V	70	--	--	ns

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

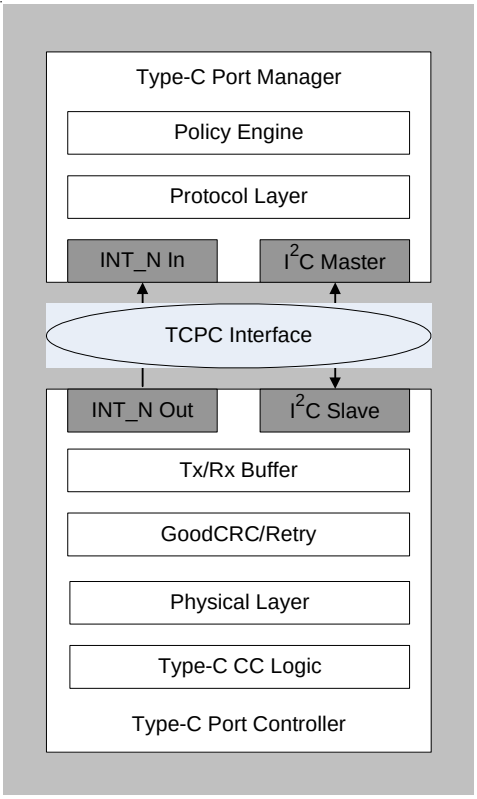
Note 5. When VCONN doesn't use, VCONN short to GND.

Application Information

Abbreviations :

Term	Description
BMC	Biphase Mark Coding
TCPC	Type-C Port Controller
TCPCI	Type-C Port Controller Interface
TCPM	Type-C Port Manager

Type-C Port Controller (TCPC) Interface :



The Type-C Port Controller Interface, TCPCI, is the interface between a Type-C Port Manager and a Type-C Port Controller.

The Controller Interface uses the I^2C protocol :

- The TCPM is the only master on this I^2C bus
- The TCPC is a slave device on this I^2C bus
- Each Type-C port has its own unique I^2C slave address. The TCPC shall have equal numbers of unique I^2C slave addresses and supported Type-C ports
- The TCPC supports Fast-mode bus speed
- The TCPC has an open drain output, active low INT_N Pin. This pin is used to indicate change of state, where INT_N pin is asserted when any Alert Bits are set
- The TCPCI supports an I/O nominal voltage range of 1.8V and 3.3V
- The TCPC can auto-increment the I^2C internal register address of the last byte transferred during a read independent of an ACK/NACK from the master
- The default I^2C address shows below

1	0	0	1	1	1	0	RW
MSB							LSB

BMC TC Mask Definition, X Values						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Left Edge of Mask	X1Tx			0.015		UI
X2Tx point	X2Tx			0.07		UI
X3Tx point	X3Tx			0.15		UI
X4Tx point	X4Tx			0.25		UI
X5Tx point	X5Tx			0.35		UI
X6Tx point	X6Tx			0.43		UI
X7Tx point	X7Tx			0.485		UI
X8Tx point	X8Tx			0.515		UI
X9Tx point	X9Tx			0.57		UI
X10Tx point	X10Tx			0.65		UI
X11Tx point	X11Tx			0.75		UI
X12Tx point	X12Tx			0.85		UI
X13Tx point	X13Tx			0.93		UI
Right Edge of Mask	X14Tx			0.985		UI

BMC TC Mask Definition, Y Values						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Lower bound of Outer mask	Y1Tx			–0.075		V
Lower bound of inner mask	Y2Tx			0.075		V
Y3Tx point	Y3Tx			0.15		V
Y4Tx point	Y4Tx			0.325		V
Inner mask vertical midpoint	Y5Tx			0.5625		V
Y6Tx point	Y6Tx			0.8		V
Y7Tx point	Y7Tx			0.975		V
Y8Tx point	Y8Tx			1.04		V
Upper Bound of Outer mask	Y9Tx			1.2		V

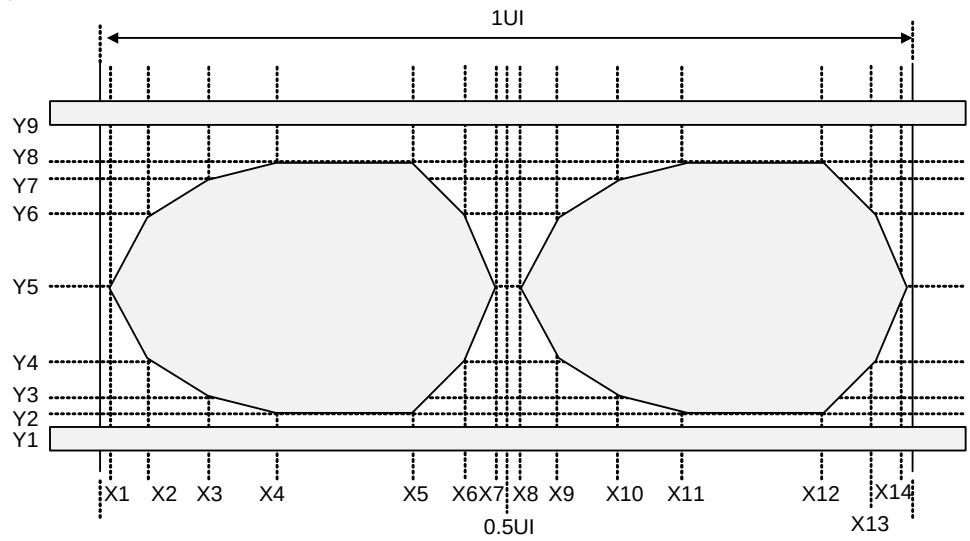


Figure 1. BMC T_X "ONE" Mask

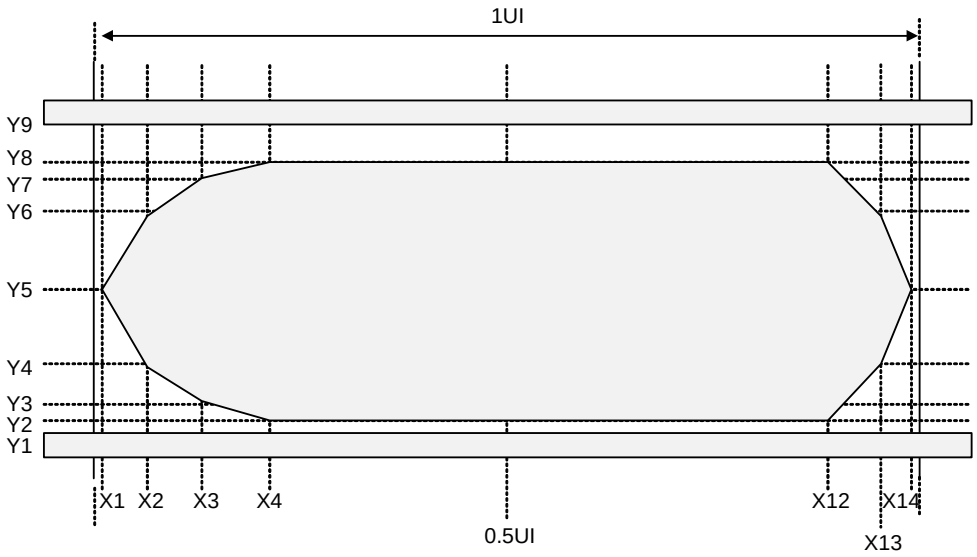


Figure 2. BMC T_X "ZERO" Mask

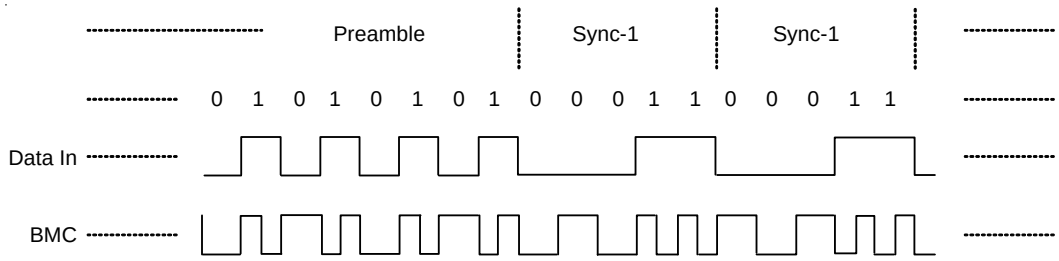


Figure 3. BMC Example

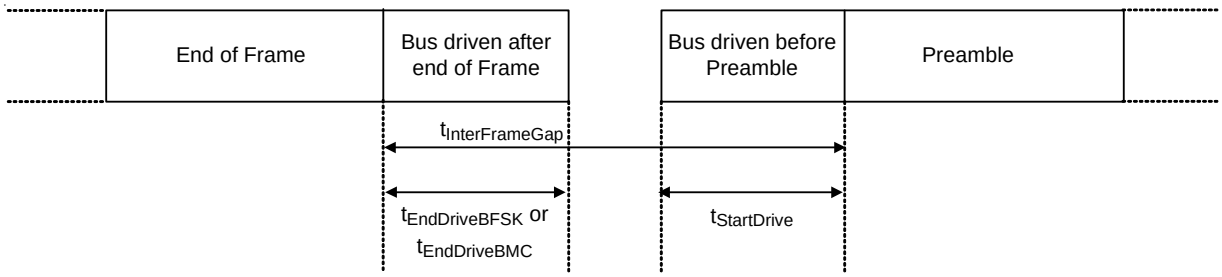


Figure 4. Inter-Frame Gap Timings

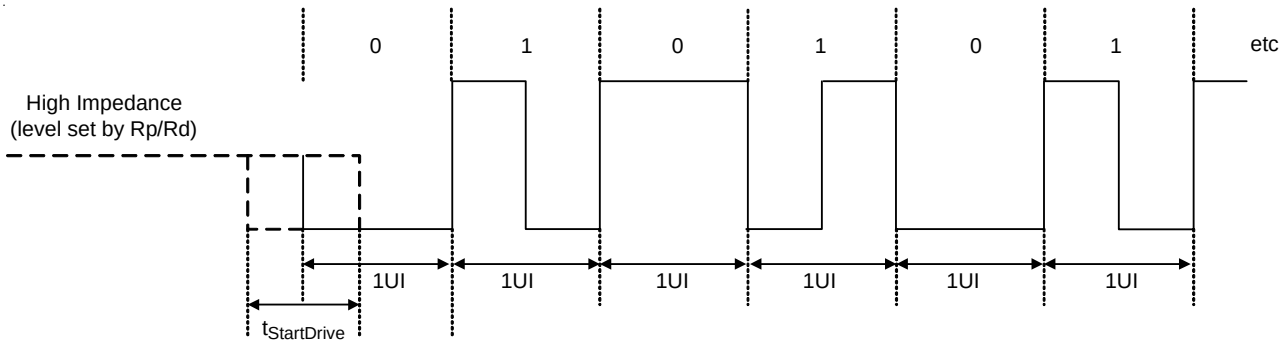


Figure 5. BMC Encoded Start of Preamble

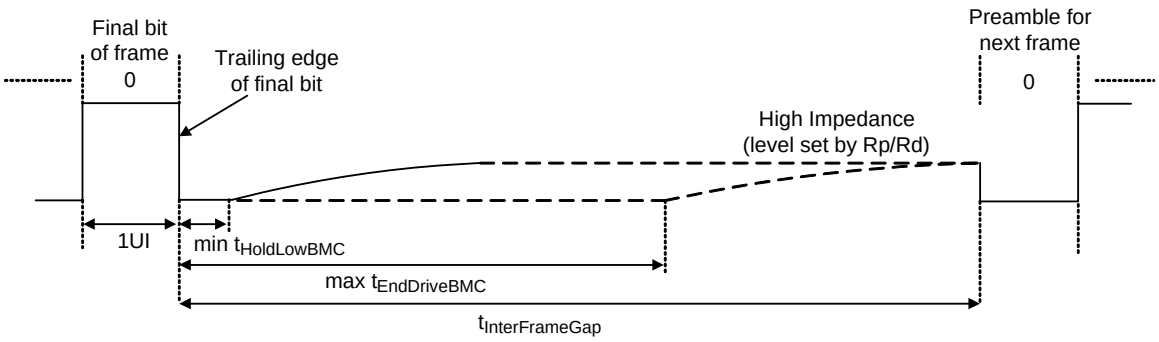


Figure 6. Transmitting or Receiving BMC Encoded Frame Terminated

USB_PD

The PD function of the RT1711H complies with USB Power Delivery spec 2.0 and Type-C Port Controller Interface spec 1.0. Some "Not support" functions are listed in the register table.

Type-C Detection

The USB_PD implements multiple comparators which can be used by software to determine the state of the CC1, CC2 pins. This status information provides the host processor all of the information required to determine attach and detach status of the cable.

The USB_PD has three threshold comparators, which match the USB Type-C specification for the three charge current levels, which can be detected by a Type-C device. These comparators can automatically trigger interrupts to occur when there is a state change.

Detection through Autonomous DRP Toggles

The USB_PD has the capability to do autonomous DRP toggles. In DRP toggles, the RT1711H implements DRP toggle between SRC (source) and SNK (sink). It can also present as a SRC or SNK only and monitor CC1, CC2 status.

Dead Battery Mode

RT1711H that supports being charged by USB whose VDD's DC-DC is off shall apply Rd to both CC1 and CC2 and follow all Sink rules. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default VBUS. Circuitry to present Rd in this case only needs to guarantee the voltage on CC is pulled within the same range as the voltage clamp implementation of Rd in order for a Source to recognize the Sink and provide VBUS.

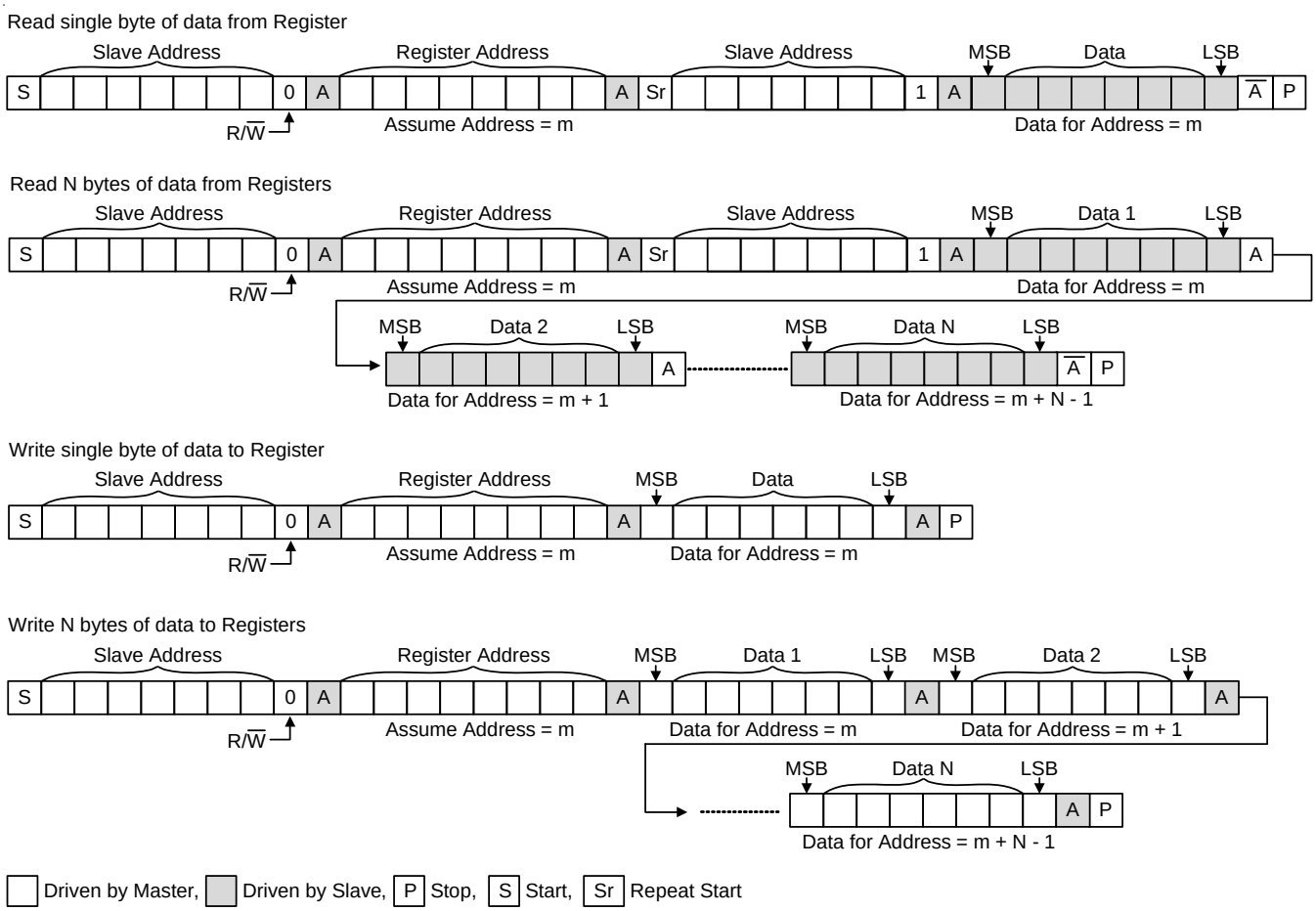
I²C Interface

The following table shows the RT1711H unique address as below.

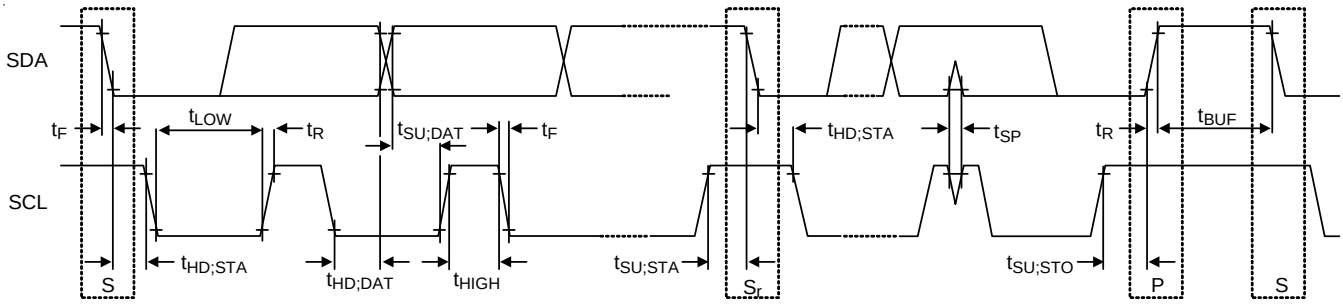
RT1711H I²C Slave Address			
MSB	**LSB**	**R/W bit**	**R/W**
100111	0	1/0	9D/9C

The I²C interface bus must be connect a resistor 1kΩ to power node and independent connection to processor, individually. The I²C timing diagrams are listed below.

Read and Write Function



I²C Waveform Information



Register Map :

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x00	1	VENDOR_ID	7:0	VID[7:0]	0xCF	R	A unique 16-bit unsigned integer. Assigned by the USB-IF to the Vendor.
0x01	1		7:0	VID[15:8]	0x29	R	
0x02	1	PRODUCT_ID	7:0	PID[7:0]	0x11	R	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC.
0x03	1		7:0	PID[15:8]	0X17	R	
0x04	1	DEVICE_ID	7:0	DID[7:0]	0x71	R	A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the TCPC.
0x05	1		7:0	DID[15:8]	0x21	R	
0x06	1	USBTYPEC_REV	7:0	USBTYPEC_REV	0x11	R	Byte 0 of a 16-bit USB Type-C Revision. Revision 1.1
0x07	1		7:0	Reserved	0	R	
0x08	1	USBPD_REV_VER	7:0	USBPD_VER	0x11	R	Byte 0 of a 16-bit USB PD version. Version 1.1.
0x09	1		7:0	USBPD_REV	0x20	R	Byte 1 of a 16-bit USB PD Revision. Revision 2.0.
0x0A	1	PD_INTERFACE_REV	7:0	PDIF_VER	0x10	R	Byte 0 of a 16-bit PD Interface (TCPC) Version. Version 1.0
0x0B	1		7:0	PDIF_REV	0x10	R	Byte 1 of a 16-bit PD Interface (TCPC) Revision. Revision 1.0

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x10	1	ALERT	7	ALARM_VBUS_VOLTAGE_H	0	R	Not support.
			6	TX_SUCCESS	0	RW	0b: Cleared (default) 1b : Reset or SOP* message transmission successful.
			5	TX_DISCARD	0	RW	0b : Cleared (default) 1b : Reset or SOP* message transmission not sent due to incoming receive message.
			4	TX_FAIL	0	RW	0b : Cleared (default) 1b : SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission.
			3	RX_HARD_RESET	0	RW	0b : Cleared (default) 1b : Received Hard Reset message
			2	RX_SOP_MSG_STATUS	0	RW	0b : Cleared (default) 1b : Receive status register changed
			1	POWER_STATUS	1	RW	0b : Cleared 1b : Port status changed (default)
			0	CC_STATUS	0	RW	0b : Cleared (default) 1b : CC status changed
0x11	1	ALERT	7	Reserved	0	R	Reserved
			6	Reserved	0	R	Reserved
			5	Reserved	0	R	Reserved
			4	Reserved	0	R	Reserved
			3	VBUS_SINK_DISCNT	0	R	Not support.
			2	RXBUF_OVFLOW	0	RW	0b : TCPC Rx buffer is functioning properly. (default) 1b : TCPC Rx buffer has overflowed.
			1	FAULT	0	RW	0b : No Fault. (default) 1b : A Fault has occurred. Read the FAULT_STATUS register.
			0	ALARM_VBUS_VOLTAGE_L	0	R	Not support.

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x12	1	ALERT_ MASK	7	M_ALARM_ VBUS_ VOLTAGE_H	1	R	Not support.
			6	M_TX_ SUCCESS	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			5	M_TX_ DISCARD	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			4	M_TX_FAIL	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			3	M_RX_HARD_ RESET	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			2	M_RX_SOP_ MSG_STATUS	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			1	M_POWER_ STATUS	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			0	M_CC_ STATUS	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
0x13	1	ALERT_ MASK	7	Reserved	0	R	Reserved
			6	Reserved	0	R	Reserved
			5	Reserved	0	R	Reserved
			4	Reserved	0	R	Reserved
			3	M_VBUS_ SINK_DISCNT	1	R	Not support.
			2	M_RXBUF_ OVFLOW	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			1	M_FAULT	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			0	M_ALARM_ VBUS_ VOLTAGE_L	1	R	Not support.
0x14	1	POWER_ STATUS_ MASK	7	Reserved	1	R	Not support.
			6	M_TCPC_ INITIAL	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			5	M_SRC_HV	1	R	Not support.
			4	M_SRC_VBUS	1	R	Not support.
			3	M_VBUS_PRE SENT_DETC	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			2	M_VBUS_ PRESENT	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			1	M_VCONN_ PRESENT	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			0	M_SINK_VBUS	1	R	Not support.

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x15	1	FAULT_STATUS_MASK	7	M_VCON_OV	0	RW	0b : Interrupt masked (default) 1b : Interrupt unmasked
			6	M_FORCE_OFF_VBUS	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			5	M_AUTO_DISC_FAIL	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			4	M_FORCE_DISC_FAIL	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			3	M_VBUS_OC	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			2	M_VBUS_OV	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			1	M_VCON_OC	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
			0	M_I2C_ERROR	1	RW	0b : Interrupt masked 1b : Interrupt unmasked (default)
0x18	1	CONFIG_STANDARD_OUTPUT	7	H_IMPEDENCE	0	R	Not support.
			6	DBG_ACC_CONNECT_O	0	R	Not support.
			5	AUDIO_ACC_CONNECT	0	R	Not support.
			4	ACTIVE_CABLE_CONNECT	0	R	Not support.
			3:2	MUX_CTRL	00	R	Not support.
			1	CONNECT_PRESENT	0	R	Not support.
			0	CONNECT_ORIENT	0	R	Not support.

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x19	1	TCPC_CONTROL	7:5	Reserved	000	R	Reserved
			4	Reserved	0	R	Reserved
			3:2	I2C_CK_STRETCH	00	R	Not support.
			1	BIST_TEST_MODE	0	RW	0b : Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. (default) 1b : BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.
			0	PLUG_ORIENT	0	RW	0b : When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. (default) 1b : When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. Required
0x1A	1	ROLE_CONTROL	7	Reserved	0	R	Reserved
			6	DRP	0	RW	0b : No DRP. Bits B3..0 determine Rp/Rd/Ra settings (default) 1b: DRP
			5:4	RP_VALUE	00	RW	00b : Rp default (default) 01b : Rp 1.5A 10b : Rp 3.0A 11b : Reserved
			3:2	CC2	10	RW	00b : Reserved 01b : Rp (Use Rp definition in B5..4) 10b : Rd (default) 11b : Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6
			1:0	CC1	10	RW	00b : Reserved 01b : Rp (Use Rp definition in B5..4) 10b : Rd (default) 11b : Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x1B	1	FAULT_CONTROL	7	DIS_VCON_OV	0	RW	0b: Fault detection circuit enabled (default) 1b: Fault detection circuit disabled
			6:5	Reserved	00	R	Reserved
			4	DIS_FORCE_OFF_VBUS	0	R	Not support.
			3	DIS_VBUS_DISC_FAULT_TIMER	0	R	Not support.
			2	DIS_VBUS_OC	0	R	Not support.
			1	DIS_VBUS_OV	0	R	Not support.
			0	DIS_VCON_OC	0	RW	0b : Fault detection circuit enabled (default) 1b : Fault detection circuit disabled
0x1C	1	POWER_CONTROL	7	Reserved	0	R	Reserved
			6	VBUS_VOL_MONITOR	0	R	Not support.
			5	DIS_VOL_ALARM	0	R	Not support.
			4	AUTO_DISC_DISCNCT	0	R	Not support.
			3	BLEED_DISC	0	R	Not support.
			2	FORCE_DISC	0	R	Not support.
			1	VCONN_POWER_SPT	0	RW	0b : TCPC delivers at least 1W on VCONN (default) 1b : TCPC delivers at least the power indicated in DEVICE_CAPABILITIES.VCONNPowerSupported
			0	EN_VCONN	0	RW	0b : Disable VCONN Source (default) 1b : Enable VCONN Source to CC Required

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x1D	1	CC_ STATUS	7:6	Reserved	00	R	Reserved
			5	DRP_ STATUS	0	R	0b : the TCPC has stopped toggling or (ROLE_CONTROL.DRP = 00) (default) 1b : the TCPC is toggling
			4	DRP_ RESULT	0	R	0b : the TCPC is presenting Rp (default) 1b : the TCPC is presenting Rd

			3:2	CC2_ STATUS	00	R	If (ROLE_CONTROL.CC2 = Rp) or (DrpResult = 0)
							00b : SRC.Open (Open, Rp) (default)
							01b : SRC.Ra (below maximum vRa)
							10b : SRC.Rd (within the vRd range)
							11b : reserved
							
							If (ROLE_CONTROL.CC2 = Rd) or (DrpResult = 1)
							00b: SNK.Open (Below maximum vRa) (default)
							01b: SNK.Default (Above minimum vRd-Connect)
							10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A
							11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A
							
							If ROLE_CONTROL.CC2 = Ra, this field is set to 00b
							If ROLE_CONTROL.CC2 = Open, this field is set to 00b
							
							This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVCONN = 1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

Address	Length	Register Name	Bit	BitName	Default	Type	Description

0x1D	1	CC_ STATUS	1:0	CC1_STATUS	00	R	If (ROLE_CONTROL.CC1 = Rp) or (DrpResult = 0)
							00b : SRC.Open (Open, Rp) (default)
							01b : SRC.Ra (below maximum vRa)
							10b : SRC.Rd (within the vRd range)
							11b : reserved
							
							If (ROLE_CONTROL.CC1 = Rd) or DrpResult = 1)
							00b : SNK.Open (Below maximum vRa)
							(default)
							01b: SNK.Default (Above minimum vRd-Connect)
							10b : SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A
							11b : SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A
							
							If ROLE_CONTROL.CC1 = Ra, this field is set to 00b
							If ROLE_CONTROL.CC1 = Open, this field is set to 00b
							
							This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVCONN = 1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x1E	1	POWER_ STATUS	7	DBG_ACC_ CONNECT	0	R	Not support.
			6	TCPC_INITIAL	0	R	0b : The TCPC has completed initialization and all registers are valid (default) 1b : The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh
			5	SRC_HV	0	R	Not support.
			4	SRC_VBUS	0	R	Not support.
			3	VBUS_PRESE NT_DETC	1	R	0b : VBUS present detection disabled 1b : VBUS present detection enabled (default)
			2	VBUS_PRESE NT	0	R	0b : VBUS Disconnected (default) 1b : VBUS Connected
			1	VCONN_PRE SENT	0	R	0b : VCONN is not present (default) 1b : This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4V
			0	SINK_VBUS	0	R	Not support.
0x1F	1	FAULT_ STATUS	7	VCON_OV	0	RW	0b : Not in an over-voltage protection state (default) 1b : Over-voltage fault latched.
			6	FORCE_OFF_ VBUS	0	R	Not support.
			5	AUTO_DISC_ FAIL	0	R	Not support.
			4	FORCE_DISC _FAIL	0	R	Not support.
			3	VBUS_OC	0	R	Not support.
			2	VBUS_OV	0	R	Not support.
			1	VCON_OC	0	RW	0b : No fault detected (default) 1b : Over-current VCONN fault latched
			0	I2C_ERROR	0	RW	0b : No Error (default) 1b : I^2C error has occurred.

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x23	1	COMMAND	7:0	COMMAND	0x00	RW	0010 0010b : DisableVbusDetect: Disable Vbus present and vSafe0V detection. 0011 0011b : EnableVbusDetect: Enable Vbus present and vSafe0V detection. 1001 1001b : Start DRP Toggling if ROLE_CONTROL.DRP = 1b. If ROLE_CONTROL.CC1/CC2= 01b start with Rp, if ROLE_CONTROL.CC1/CC2 =10b start with Rd.
0x24	1	DEVICE_ CAPABILITIES_1L	7:5	ROLES_ SUPPORT	110	R	000b : Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b : Source only 010b : Sink only 011b : Sink with accessory support (optional) 100b : DRP only 101b : Adapter or Cable (Ra) only 110b : Source, Sink, DRP, Adapter/Cable all supported (default) 111b : Not valid
			4	ALL_SOP_ SUPPORT	1	R	0b : All SOP* except SOP'_DBG/SOP"_DBG 1b : All SOP* messages are supported (default)
			3	SOURCE_ VCONN	1	R	0b : TCPC is not capable of switching VCONN 1b : TCPC is capable of switching VCONN (default)
			2	CPB_SINK_ VBUS	0	R	0b : TCPC is not capable controlling the sink path to the system load (default) 1b : TCPC is capable of controlling the sink path to the system load
			1	SOURCE_ HV_VBUS	0	R	0b : TCPC is not capable of controlling the source high voltage path to VBUS (default) 1b : TCPC is capable of controlling the source high voltage path to VBUS
			0	SOURCE_ VBUS	0	R	0b : TCPC is not capable of controlling the source path to VBUS (default) 1b : TCPC is capable of controlling the source path to VBUS

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x25	1	DEVICE_CAPABILITIES_1H	7	Reserved	0	R	Reserved
			6	CPB_VBUS_OC	0	R	0b: VBUS OCP is not reported by the TCPC (default) 1b: VBUS OCP is reported by the TCPC
			5	CPB_VBUS_OV	0	R	0b : VBUS OVP is not reported by the TCPC (default) 1b : VBUS OVP is reported by the TCPC
			4	CPB_BLEED_DISC	0	R	0b : No Bleed Discharge implemented in TCPC (default) 1b : Bleed Discharge is implemented in the TCPC
			3	CPB_FORCE_DISC	0	R	0b : No Force Discharge implemented in TCPC (default) 1b : Force Discharge is implemented in the TCPC
			2	VBUS_MEASURE_ALARM	0	R	0b : No VBUS voltage measurement nor VBUS Alarms (default) 1b : VBUS voltage measurement and VBUS Alarms
			1:0	SOURCE_RP_SUPPORT	10	R	00b : Rp default only 01b : Rp 1.5A and default 10b : Rp 3.0A, 1.5A, and default (default) 11b : Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x26	1	DEVICE_CAPABILITIES_2L	7	SINK_DISCONNECT_DET	0	R	0b : VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default: Use POWER_STATUS.VbusPresent = 0b to indicate a Sink disconnect) (default) 1b : VBUS_SINK_DISCONNECT_THRESHOLD implemented
			6	STOP_DISC_THD	0	R	0b : VBUS_STOP_DISCHARGE_THRESHOLD not implemented (default) 1b : VBUS_STOP_DISCHARGE_THRESHOLD implemented
			5:4	VBUS_VOL_ALARM_LSB	11	R	00b : TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01b : TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC. 10b : TCPC has 100mV LSB for its voltage alarm and uses only 8 bits. VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. 11b : Not support this function. (default)
			3:1	VCONN_POWER	010	R	000b : 1.0W 001b : 1.5W 010b : 2.0W (default) 011b : 3W 100b : 4W 101b : 5W 110b : 6W 111b : External
			0	VCONN_OCF	1	R	0b : TCPC is not capable of detecting a VCONN fault 1b : TCPC is capable of detecting a VCONN fault (default)
0x27	1	DEVICE_CAPABILITIES_2H	7:0	Reserved	0x00	R	Reserved

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x28	1	STANDARD_INPUT_CAPABILITIES	7:3	Reserved	00000	R	Reserved
			2	VBUS_EXT_OVF	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
			1	VBUS_EXT_OCF	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
			0	FORCE_OFF_VBUS_IN	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
0x29	1	STANDARD_OUTPUT_CAPABILITIES	7	Reserved	0	R	Reserved
			6	CPB_DBG_ACC_IND	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
			5	CPB_VBUS_PRESENT_MNT	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
			4	CPB_AUDIO_ADT_ACC_IND	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
			3	CPB_ACTIVE_CABLE_IND	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
			2	CPB_MUX_CFG_CTRL	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
			1	CPB_CONNECT_PRESENT	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
			0	CPB_CONNECT_ORIENT	0	R	0b : Not present in TCPC (default) 1b : Present in TCPC
0x2E	1	MESSAGE_HEADER_INFO	7:5	Reserved	000	R	Reserved
			4	CABLE_PLUG	0	RW	0b : Message originated from Source, Sink, or DRP (default) 1b : Message originated from a Cable Plug
			3	DATA_ROLE	0	RW	0b : Sink (default) 1b : Source
			2:1	USBPD_SPECREV	01	RW	00b : Revision 1.0 01b : Revision 2.0 (default) 10b : Revision 3.0 11b : Reserved
			0	POWER_ROLE	0	RW	0b : Sink (default) 1b : Source

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x2F	1	RECEIVE_DETECT	7	Reserved	0	R	Reserved
			6	EN_CABLE_RST	0	RW	0b : TCPC does not detect Cable Reset signaling (default) 1b : TCPC detects Cable Reset signaling
			5	EN_HARD_RST	0	RW	0b: TCPC does not detect Hard Reset signaling (default) 1b : TCPC detects Hard Reset signaling
			4	EN_SOP2DB	0	RW	0b: TCPC does not detect SOP_DBG'' message (default) 1b : TCPC detects SOP_DBG'' message
			3	EN_SOP1DB	0	RW	0b : TCPC does not detect SOP_DBG' message (default) 1b : TCPC detects SOP_DBG' message
			2	EN_SOP2	0	RW	0b : TCPC does not detect SOP'' message (default) 1b : TCPC detects SOP'' message
			1	EN_SOP1	0	RW	0b : TCPC does not detect SOP' message (default) 1b : TCPC detects SOP' message
			0	EN_SOP	0	RW	0b : TCPC does not detect SOP message (default) 1b : TCPC detects SOP message
0x30	1	RX_BYTE_COUNT	7:0	RX_BYTE_COUNT	0x00	RW	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register.
0x31	1	RX_BUF_FRAME_TYPE	7:3	Reserved	0000	R	Reserved
			2:0	RX_FRAME_TYPE	000	R	Type of received frame 000b : Received SOP (default) 001b : Received SOP' 010b : Received SOP" 011b : Received SOP_DBG' 100b : Received SOP_DBG'' 110b : Received Cable Reset All others are reserved.
0x32	1	RX_BUF_HEADER_BYTE_0	7:0	RX_HEAD_0	0x00	R	Byte 0 (bits 7..0) of message header
0x33	1	RX_BUF_HEADER_BYTE_1	7:0	RX_HEAD_1	0x00	R	Byte 1 (bits 15..8) of message header
0x34	1	RX_BUF_OBJ1_BYTE_0	7:0	RX_OBJ1_0	0x00	R	Byte 0 (bits 7..0) of 1st data object

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x35	1	RX_BUF_OBJ1_BYTE_1	7:0	RX_OBJ1_1	0x00	R	Byte 1 (bits 15..8) of 1st data object
0x36	1	RX_BUF_OBJ1_BYTE_2	7:0	RX_OBJ1_2	0x00	R	Byte 2 (bits 23..16) of 1st data object
0x37	1	RX_BUF_OBJ1_BYTE_3	7:0	RX_OBJ1_3	0x00	R	Byte 3 (bits 31..24) of 1st data object
0x38	1	RX_BUF_OBJ2_BYTE_0	7:0	RX_OBJ2_0	0x00	R	Byte 0 (bits 7..0) of 2st data object
0x39	1	RX_BUF_OBJ2_BYTE_1	7:0	RX_OBJ2_1	0x00	R	Byte 1 (bits 15..8) of 2st data object
0x3A	1	RX_BUF_OBJ2_BYTE_2	7:0	RX_OBJ2_2	0x00	R	Byte 2 (bits 23..16) of 2st data object
0x3B	1	RX_BUF_OBJ2_BYTE_3	7:0	RX_OBJ2_3	0x00	R	Byte 3 (bits 31..24) of 2st data object
0x3C	1	RX_BUF_OBJ3_BYTE_0	7:0	RX_OBJ3_0	0x00	R	Byte 0 (bits 7..0) of 3st data object
0x3D	1	RX_BUF_OBJ3_BYTE_1	7:0	RX_OBJ3_1	0x00	R	Byte 1 (bits 15..8) of 3st data object
0x3E	1	RX_BUF_OBJ3_BYTE_2	7:0	RX_OBJ3_2	0x00	R	Byte 2 (bits 23..16) of 3st data object
0x3F	1	RX_BUF_OBJ3_BYTE_3	7:0	RX_OBJ3_3	0x00	R	Byte 3 (bits 31..24) of 3st data object
0x40	1	RX_BUF_OBJ4_BYTE_0	7:0	RX_OBJ4_0	0x00	R	Byte 0 (bits 7..0) of 4st data object
0x41	1	RX_BUF_OBJ4_BYTE_1	7:0	RX_OBJ4_1	0x00	R	Byte 1 (bits 15..8) of 4st data object
0x42	1	RX_BUF_OBJ4_BYTE_2	7:0	RX_OBJ4_2	0x00	R	Byte 2 (bits 23..16) of 4st data object
0x43	1	RX_BUF_OBJ4_BYTE_3	7:0	RX_OBJ4_3	0x00	R	Byte 3 (bits 31..24) of 4st data object

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x44	1	RX_BUF_OBJ5_BYTE_0	7:0	RX_OBJ5_0	0x00	R	Byte 0 (bits 7..0) of 5st data object
0x45	1	RX_BUF_OBJ5_BYTE_1	7:0	RX_OBJ5_1	0x00	R	Byte 1 (bits 15..8) of 5st data object
0x46	1	RX_BUF_OBJ5_BYTE_2	7:0	RX_OBJ5_2	0x00	R	Byte 2 (bits 23..16) of 5st data object
0x47	1	RX_BUF_OBJ5_BYTE_3	7:0	RX_OBJ5_3	0x00	R	Byte 3 (bits 31..24) of 5st data object
0x48	1	RX_BUF_OBJ6_BYTE_0	7:0	RX_OBJ6_0	0x00	R	Byte 0 (bits 7..0) of 6st data object
0x49	1	RX_BUF_OBJ6_BYTE_1	7:0	RX_OBJ6_1	0x00	R	Byte 1 (bits 15..8) of 6st data object
0x4A	1	RX_BUF_OBJ6_BYTE_2	7:0	RX_OBJ6_2	0x00	R	Byte 2 (bits 23..16) of 6st data object
0x4B	1	RX_BUF_OBJ6_BYTE_3	7:0	RX_OBJ6_3	0x00	R	Byte 3 (bits 31..24) of 6st data object
0x4C	1	RX_BUF_OBJ7_BYTE_0	7:0	RX_OBJ7_0	0x00	R	Byte 0 (bits 7..0) of 7st data object
0x4D	1	RX_BUF_OBJ7_BYTE_1	7:0	RX_OBJ7_1	0x00	R	Byte 1 (bits 15..8) of 7st data object
0x4E	1	RX_BUF_OBJ7_BYTE_2	7:0	RX_OBJ7_2	0x00	R	Byte 2 (bits 23..16) of 7st data object
0x4F	1	RX_BUF_OBJ7_BYTE_3	7:0	RX_OBJ7_3	0x00	R	Byte 3 (bits 31..24) of 7st data object

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x50	1	TX_BUF_FRAME_TYPE	7:6	Reserved	00	R	Reserved
			5:4	TX_RETRY_CNT	00	RW	00b : No message retry is required (default) 01b : Automatically retry message transmission once 10b : Automatically retry message transmission twice 11b : Automatically retry message transmission three times
			3	Reserved	0	R	Reserved
			2:0	TX_FRAME_TYPE	000	RW	000b : Transmit SOP (default) 001b : Transmit SOP' 010b : Transmit SOP" 011b : Transmit SOP_DBG' 100b : Transmit SOP_DBG'' 101b : Transmit Hard Reset 110b : Transmit Cable Reset 111b : Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max)
0x51	1	TX_BYTE_COUNT	7:0	TX_BYTE_COUNT	0x00	RW	The number of bytes the TCPM will write
0x52	1	TX_BUF_HEADER_BYTE_0	7:0	TX_HEAD_0	0x00	RW	Byte 0 (bits 7..0) of message header
0x53	1	TX_BUF_HEADER_BYTE_1	7:0	TX_HEAD_1	0x00	RW	Byte 1 (bits 15..8) of message header
0x54	1	TX_BUF_OBJ1_BYTE_0	7:0	TX_OBJ1_0	0x00	RW	Byte 0 (bits 7..0) of 1st data object
0x55	1	TX_BUF_OBJ1_BYTE_1	7:0	TX_OBJ1_1	0x00	RW	Byte 1 (bits 15..8) of 1st data object
0x56	1	TX_BUF_OBJ1_BYTE_2	7:0	TX_OBJ1_2	0x00	RW	Byte 2 (bits 23..16) of 1st data object
0x57	1	TX_BUF_OBJ1_BYTE_3	7:0	TX_OBJ1_3	0x00	RW	Byte 3 (bits 31..24) of 1st data object
0x58	1	TX_BUF_OBJ2_BYTE_0	7:0	TX_OBJ2_0	0x00	RW	Byte 0 (bits 7..0) of 2st data object
0x59	1	TX_BUF_OBJ2_BYTE_1	7:0	TX_OBJ2_1	0x00	RW	Byte 1 (bits 15..8) of 2st data object

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x5A	1	TX_BUF_OBJ2_BYTE_2	7:0	TX_OBJ2_2	0x00	RW	Byte 2 (bits 23..16) of 2st data object
0x5B	1	TX_BUF_OBJ2_BYTE_3	7:0	TX_OBJ2_3	0x00	RW	Byte 3 (bits 31..24) of 2st data object
0x5C	1	TX_BUF_OBJ3_BYTE_0	7:0	TX_OBJ3_0	0x00	RW	Byte 0 (bits 7..0) of 3st data object
0x5D	1	TX_BUF_OBJ3_BYTE_1	7:0	TX_OBJ3_1	0x00	RW	Byte 1 (bits 15..8) of 3st data object
0x5E	1	TX_BUF_OBJ3_BYTE_2	7:0	TX_OBJ3_2	0x00	RW	Byte 2 (bits 23..16) of 3st data object
0x5F	1	TX_BUF_OBJ3_BYTE_3	7:0	TX_OBJ3_3	0x00	RW	Byte 3 (bits 31..24) of 3st data object
0x60	1	TX_BUF_OBJ4_BYTE_0	7:0	TX_OBJ4_0	0x00	RW	Byte 0 (bits 7..0) of 4st data object
0x61	1	TX_BUF_OBJ4_BYTE_1	7:0	TX_OBJ4_1	0x00	RW	Byte 1 (bits 15..8) of 4st data object
0x62	1	TX_BUF_OBJ4_BYTE_2	7:0	TX_OBJ4_2	0x00	RW	Byte 2 (bits 23..16) of 4st data object
0x63	1	TX_BUF_OBJ4_BYTE_3	7:0	TX_OBJ4_3	0x00	RW	Byte 3 (bits 31..24) of 4st data object
0x64	1	TX_BUF_OBJ5_BYTE_0	7:0	TX_OBJ5_0	0x00	RW	Byte 0 (bits 7..0) of 5st data object
0x65	1	TX_BUF_OBJ5_BYTE_1	7:0	TX_OBJ5_1	0x00	RW	Byte 1 (bits 15..8) of 5st data object
0x66	1	TX_BUF_OBJ5_BYTE_2	7:0	TX_OBJ5_2	0x00	RW	Byte 2 (bits 23..16) of 5st data object
0x67	1	TX_BUF_OBJ5_BYTE_3	7:0	TX_OBJ5_3	0x00	RW	Byte 3 (bits 31..24) of 5st data object
0x68	1	TX_BUF_OBJ6_BYTE_0	7:0	TX_OBJ6_0	0x00	RW	Byte 0 (bits 7..0) of 6st data object

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x69	1	TX_BUF_OBJ6_BYTE_1	7:0	TX_OBJ6_1	0x00	RW	Byte 1 (bits 15..8) of 6st data object
0x6A	1	TX_BUF_OBJ6_BYTE_2	7:0	TX_OBJ6_2	0x00	RW	Byte 2 (bits 23..16) of 6st data object
0x6B	1	TX_BUF_OBJ6_BYTE_3	7:0	TX_OBJ6_3	0x00	RW	Byte 3 (bits 31..24) of 6st data object
0x6C	1	TX_BUF_OBJ7_BYTE_0	7:0	TX_OBJ7_0	0x00	RW	Byte 0 (bits 7..0) of 7st data object
0x6D	1	TX_BUF_OBJ7_BYTE_1	7:0	TX_OBJ7_1	0x00	RW	Byte 1 (bits 15..8) of 7st data object
0x6E	1	TX_BUF_OBJ7_BYTE_2	7:0	TX_OBJ7_2	0x00	RW	Byte 2 (bits 23..16) of 7st data object
0x6F	1	TX_BUF_OBJ7_BYTE_3	7:0	TX_OBJ7_3	0x00	RW	Byte 3 (bits 31..24) of 7st data object
0x90	1		7	Reserved	0	R	Reserved
			6	Reserved	0	RW	Reserved
			5	VCONN DISCHARGE_EN	0	RW	VCONN OVP occurs and discharge path turn-on 0b : No discharge (default) 1b : Discharge
			4	BMCIO_LPRPRD	0	RW	Low power mode enable 0b : Low power mode RD (default) 1b : Low power mode RP
			3	BMCIO_LPEN	0	RW	Low power mode enable 0b : Standby mode (default) 1b : Low power
			2	BMCIO_BG_EN	1	RW	BMCIO BandGap enable 0b : BandGap off CC pin function disable 1b : BandGap on (default) CC pin function enable
			1	VBUS_DETEN	1	RW	VBUS detection enable 0b : Measure off 1b : Operation (default)
			0	BMCIO_OSC_EN	1	RW	24M oscillator for BMC communication 0b : Disable 24M oscillator 1b : Enable 24M oscillator (default) Note : 24M oscillator will be enabled automatically when INT occur.

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0x93	1		7:5	BMCIO_VCONOCP[2:0]	100	RW	VCONN over-current control selection 000b : Current level = 200mA 001b : Current level = 300mA 010b : Current level = 400mA 011b : Current level = 500mA 100b : Current level = 600mA (default) 101 to 111b : Reserved If VCONN OCP trigger, the switch turn off timing under 55μs.
			4:1	Reserved	0000	R	Reserved
			0	Reserved	1	RW	Reserved
0x97	1	RT_ST	7:2	Reserved	000000	R	Reserved
			1	VBUS_80	0	R	0b : VBUS over 0.8V (default) 1b : VBUS under 0.8V
			0	Reserved	0	R	Reserved
0x98	1	RT_INT	7:6	Reserved	00	R	Reserved
			5	INT_RA_DETACH	0	RW	0b : Cleared (default) 1b : Ra detach
			4:2	Reserved	000	RW	Reserved
			1	INT_VBUS_80	0	RW	0b : VBUS without under 0.8V (default) 1b : VBUS under 0.8V
			0	INT_WAKEUP	0	RW	0b : Cleared (default) 1b : Low power mode exited
0x99	1	RT_MASK	7:6	Reserved	00	R	Reserved
			5	M_RA_DETACH	0	RW	0b : Interrupt masked (default) 1b : Interrupt unmasked
			4:2	Reserved	000	RW	Reserved
			1	M_VBUS_80	0	RW	0b : Interrupt masked (default) 1b : Interrupt unmasked
			0	M_WAKEUP	0	RW	0b : Interrupt masked (default) 1b : Interrupt unmasked
0x9F	1		7	WAKEUP_EN	1	RW	0 : Wakeup function disable 1 : Wakeup function enable (default)
			6:4	Reserved	000	R	Reserved
			3:0	Reserved	0000	RW	Reserved

Address	Length	Register Name	Bit	BitName	Default	Type	Description
0xA0	1		7:1	Reserved	0000000	R	Reserved
			0	SOFT_RESET	0	W	Write 1 to trigger software reset.
0xA2	1		7:4	Reserved	0000	R	
			3:0	TDRP	0011	RW	The period a DRP will complete a Source to Sink and back advertisement. (Period = TDRP * 6.4 + 51.2ms) 0000 : 51.2ms 0001 : 57.6ms 0010 : 64ms 0011 : 70.4ms (default) … 1110 : 140.8ms 1111 : 147.2ms
0xA3	1		7:0	DCSRCDRP [7:0]	01000111	RW	The percent of time that a DRP will advertise Source during tDRP. (DUTY = (DCSRCDRP[9:0] + 1) / 1024) 0000000000 : 1/1024 0000000001 : 2/1024 … 0101000111 : 328/1024 (default) … 1111111110 : 1023/1024 1111111111 : 1024/1024 Note : Setting with 0xA4[9:8]
0xA4	1		7:2	Reserved	000000	R	
			1:0	DCSRCDRP [9:8]	01	RW	The percent of time that a DRP will advertise Source during tDRP. (DUTY = (DCSRCDRP[9:0] + 1) / 1024) 0000000000 : 1/1024 0000000001 : 2/1024 … 0101000111 : 328/1024 (default) … 1111111110 : 1023/1024 1111111111 : 1024/1024 Note : Setting with 0xA4[9:8]

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-9B 1.38x1.34 (BSC) package, the thermal resistance, θ_{JA}, is 81.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (81.5°C/W) = 1.22W for a WL-CSP-9B 1.38x1.34 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

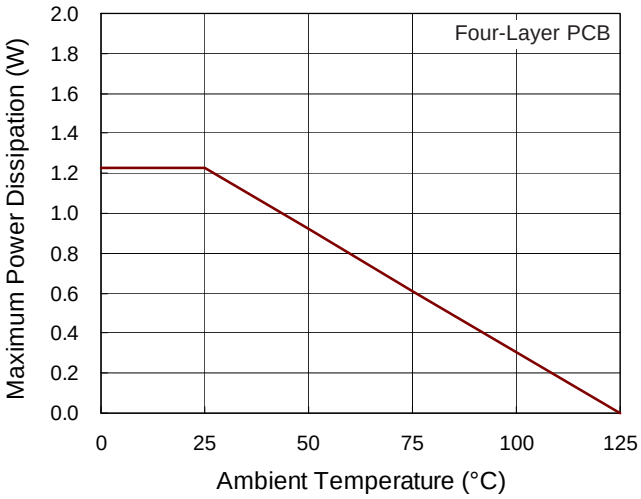
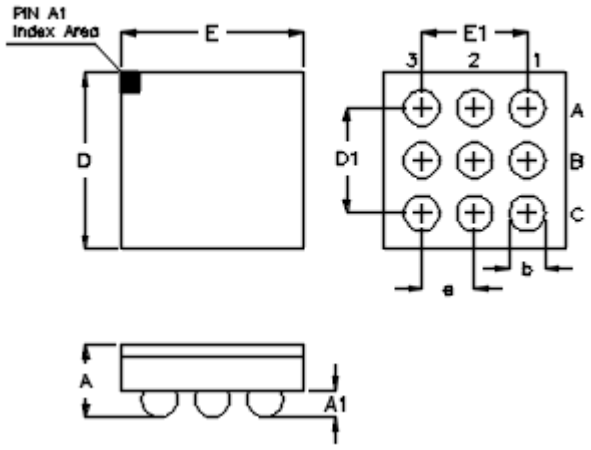


Figure 7. Derating Curve of Maximum Power Dissipation

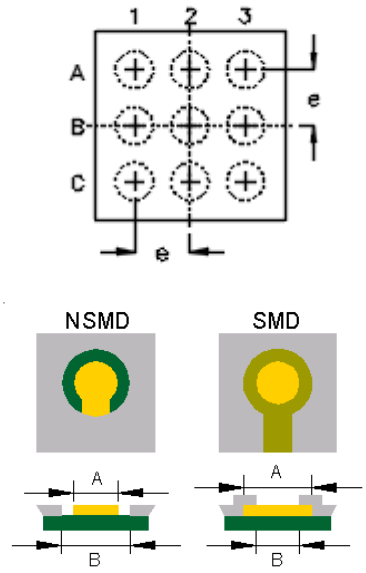
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.300	1.380	0.051	0.054
D1	0.800		0.031	
E	1.340	1.420	0.053	0.056
E1	0.800		0.031	
e	0.400		0.016	

9B WL-CSP 1.38x1.34 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.38*1.34-9(BSC)	9	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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