TFT LCD Integrated Power Module for Automotive

General Description

The RTQ6749 is an I2C interface programmable power management IC. The IC includes two synchronous boost converters for PAVDD and VGH, one synchronous NAVDD buck-boost, one VGL charge pump, one high performance VCOM with 8-bit Calibrator and one RESET voltage detector. With available in a WQFN-32L 5x5 package, this device is suitable for automotive TFT-LCD panel.

The IC can operate from 2.5V to 5.5V input voltages. High switching frequency operation prevent that the switching noise to interfere AM band. Current-limit functions are provided for all internal- switch converters, and output-fault shutdown protects all converters against output-fault conditions, and output the FAULT signal to communicate with automotive computer. Programmable soft-start functions for all output voltage to limit input inrush current during startup.

Ordering Information

RTQ6749□□-QT-A2

Package Type
QW : WQFN-32L 5x5 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RTQ6749GQW-QT : Product Number
YMDNN : Date Code

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Features

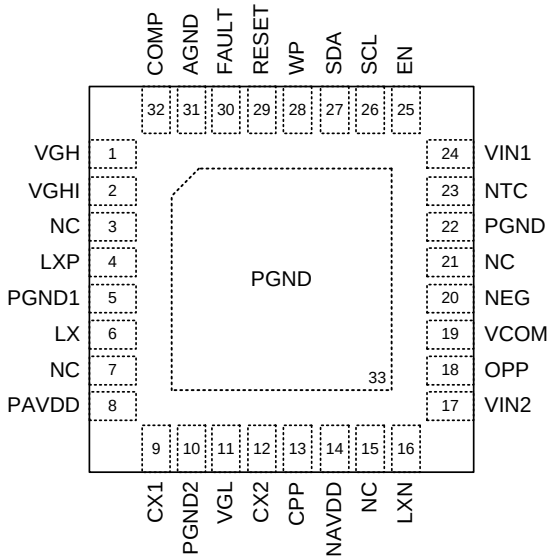
- **2.5V to 5.5V Input Supply Voltage**
- **I2C Interface**
- **Power-on and Power-off Sequence Free**
- **PAVDD Programmable Output Voltage 5V to 7.3V**
- **PAVDD Output Current Capability up to 200mA**
- **NAVDD Programmable Output Voltage –5V to –7.3V**
- **NAVDD Output Current Capability up to 200mA**
- **VGH Programmable Output Voltage 7V to 30V**
- **VGH Output Current Capability up to 60mA**
- **VGH Output Voltage Temperature Compensation**
- **VGL Programmable Output Voltage –6V to –18V**
- **VGL Output Current Capability up to 60mA**
- **VCOM 8bits Programmable Output Voltage**
- **Outputs Power-off Discharge Function**
- **Programmable Voltage Detector**
- **AEC-Q100 Grade 2 Qualified**
- **Built in UVLO, UVP, OVP, SCP and OTP Protection**

Applications

- **Infotainment LCD panel**

Pin Configuration

(TOP VIEW)



WQFN-32L 5x5

Typical Application Circuit

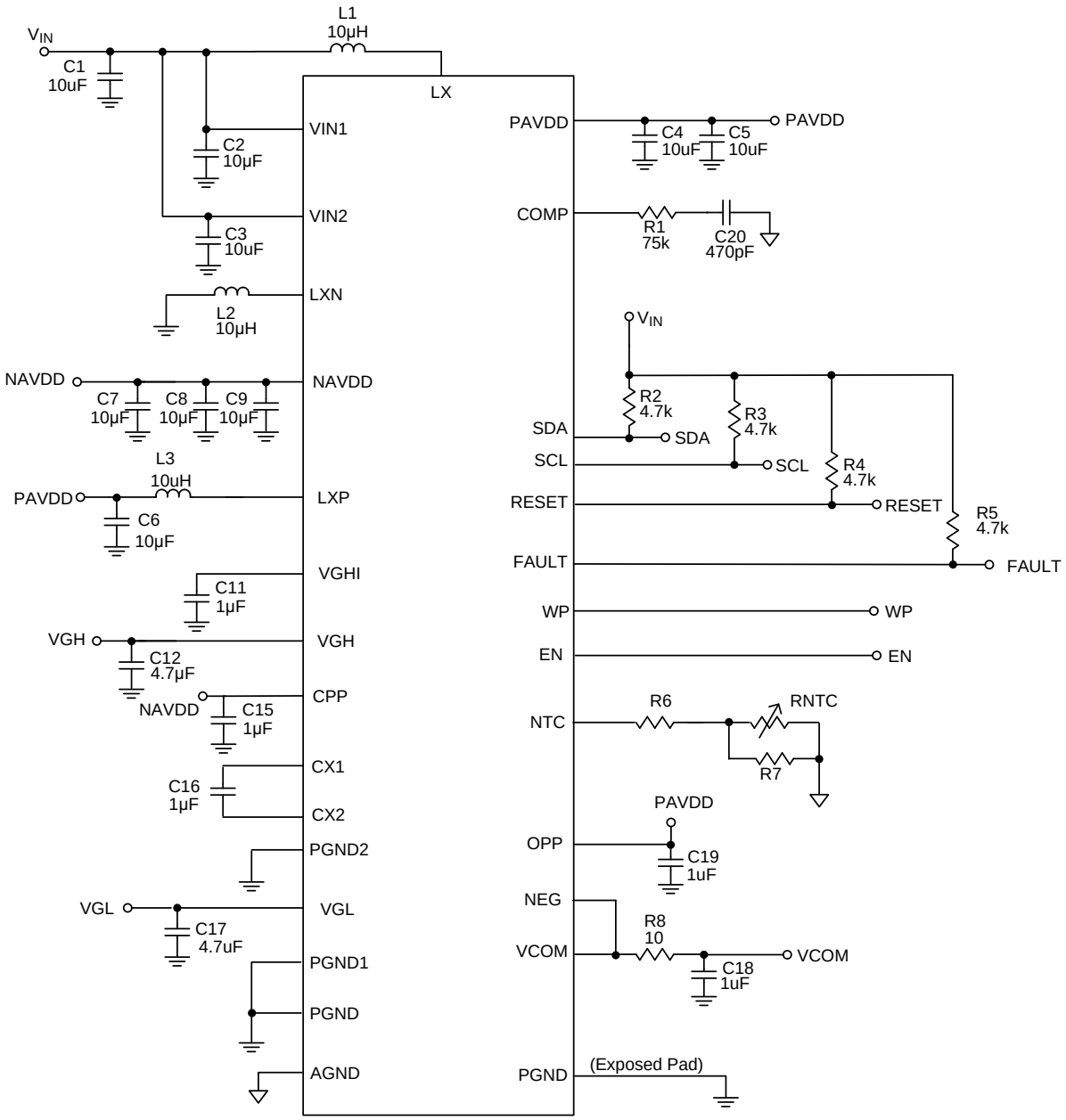


Figure 1. Typical Application Circuit with Internal Topology of VGL (PAVDD<|VGL|<PAVDD+|NAVDD|)

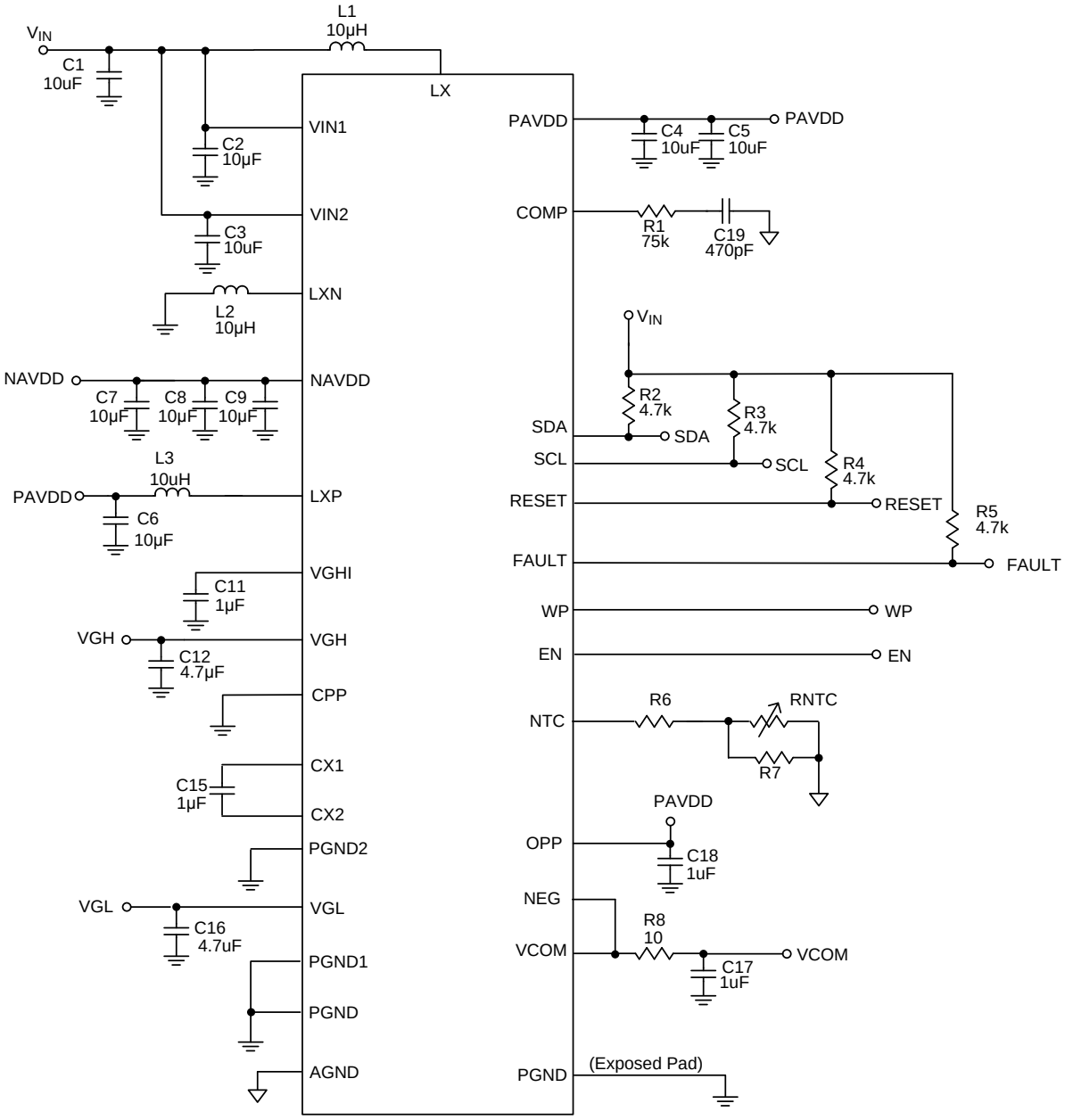


Figure 2. Typical Application Circuit with Internal Topology of VGL (|VGL|<PAVDD)

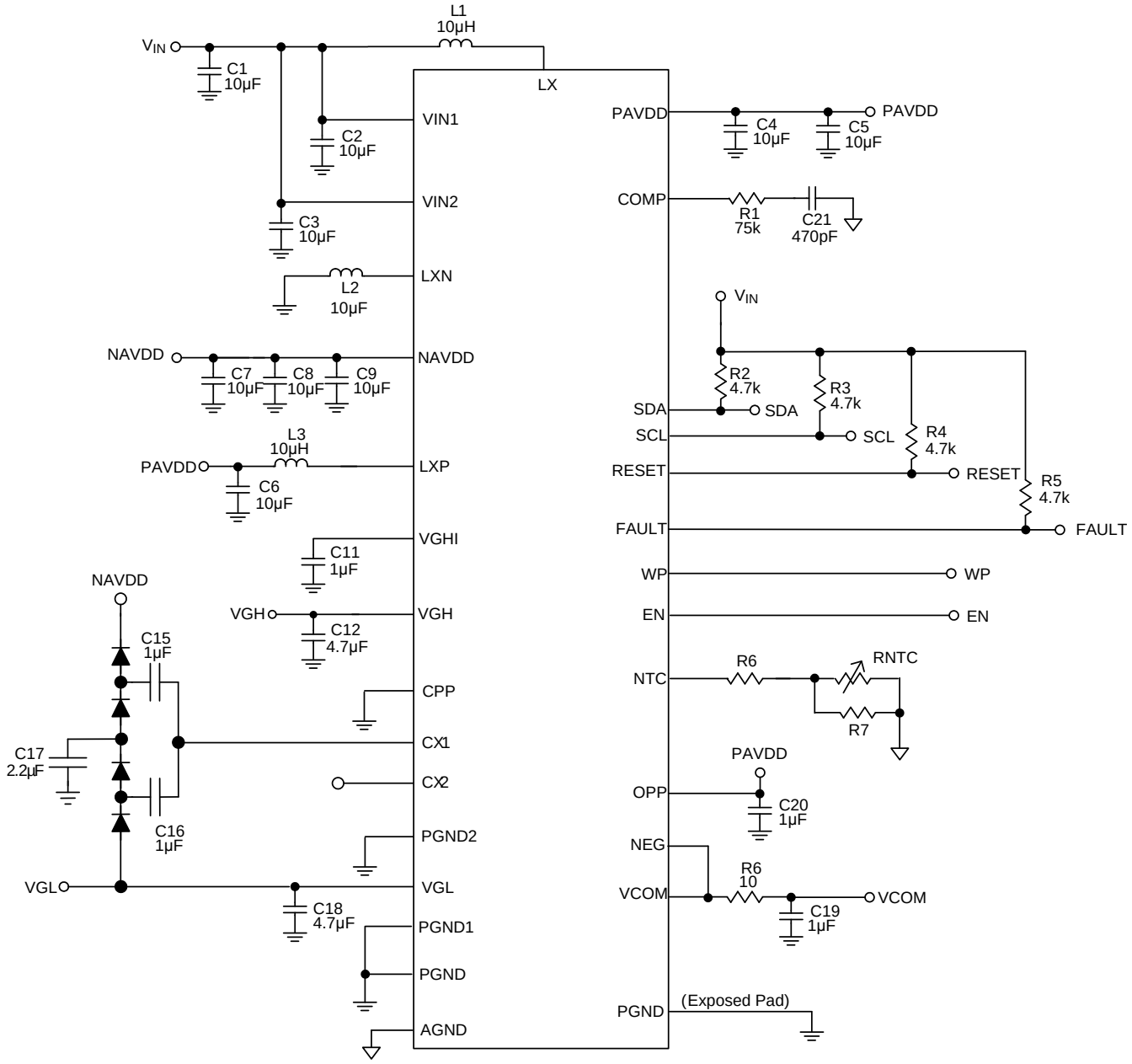


Figure 3. Typical Application Circuit with External Topology of VGL (|VGL|>PAVDD+|NAVDD|)

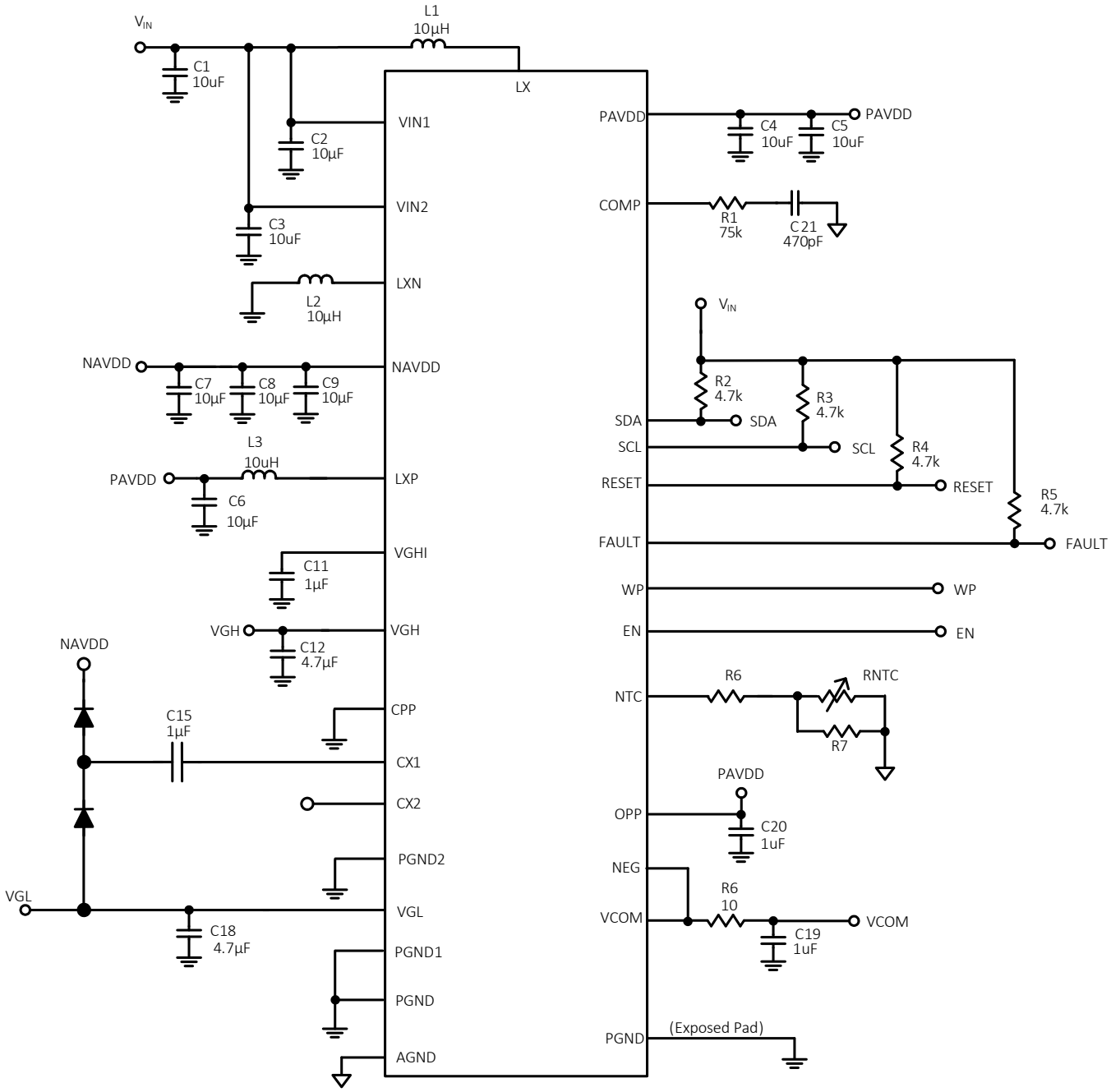


Figure 4. NAVDD Power Sequence Leading VGL Application Circuit with External Topology of VGL (PAVDD<|VGL|<PAVDD+|NAVDD|)

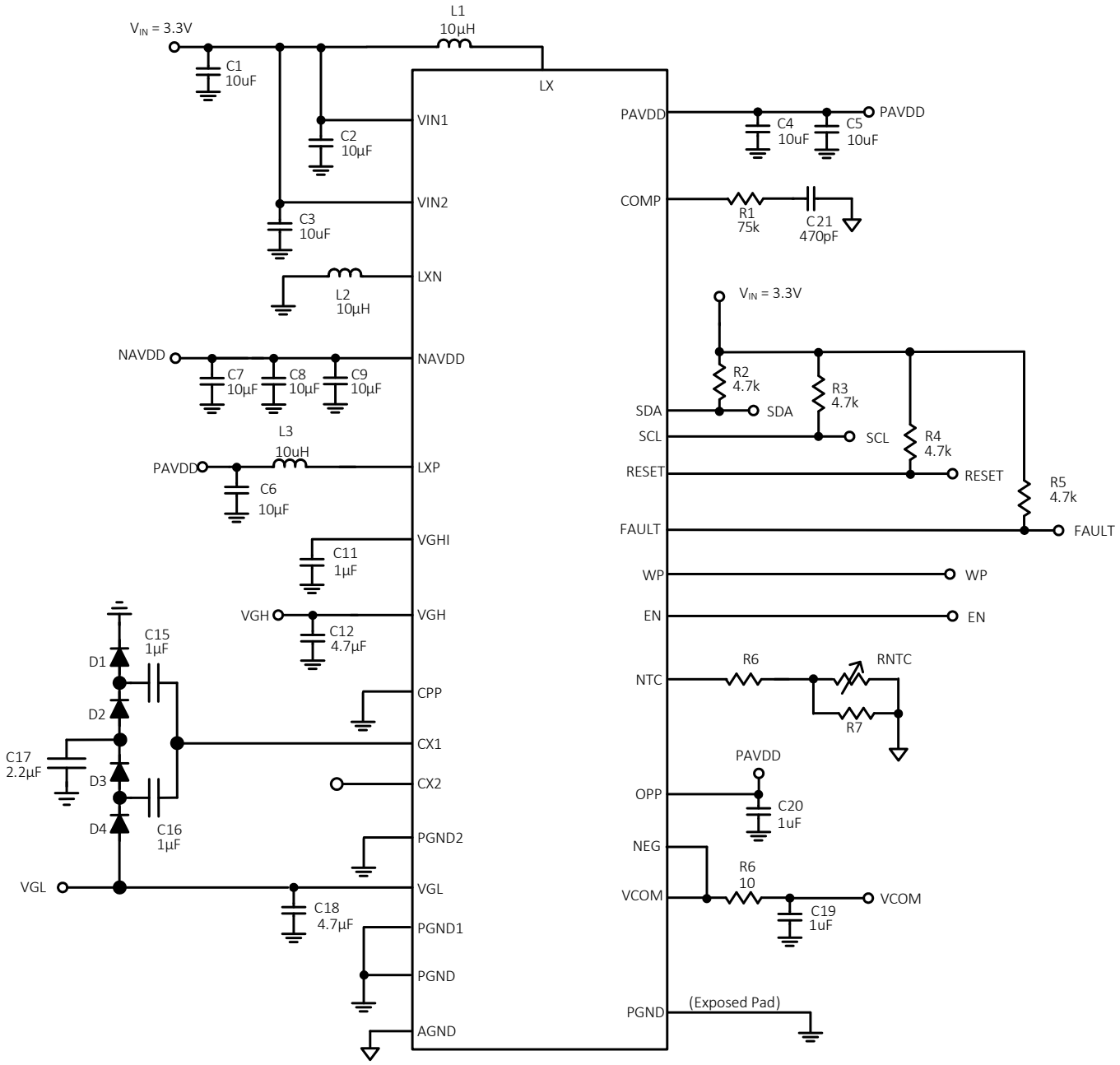


Figure 5. NAVDD Power Sequence Leading VGL and VGL Discharge Function Enabling Application Circuit with External Topology of VGL (PAVDD<|VGL|< 2 x PAVDD)

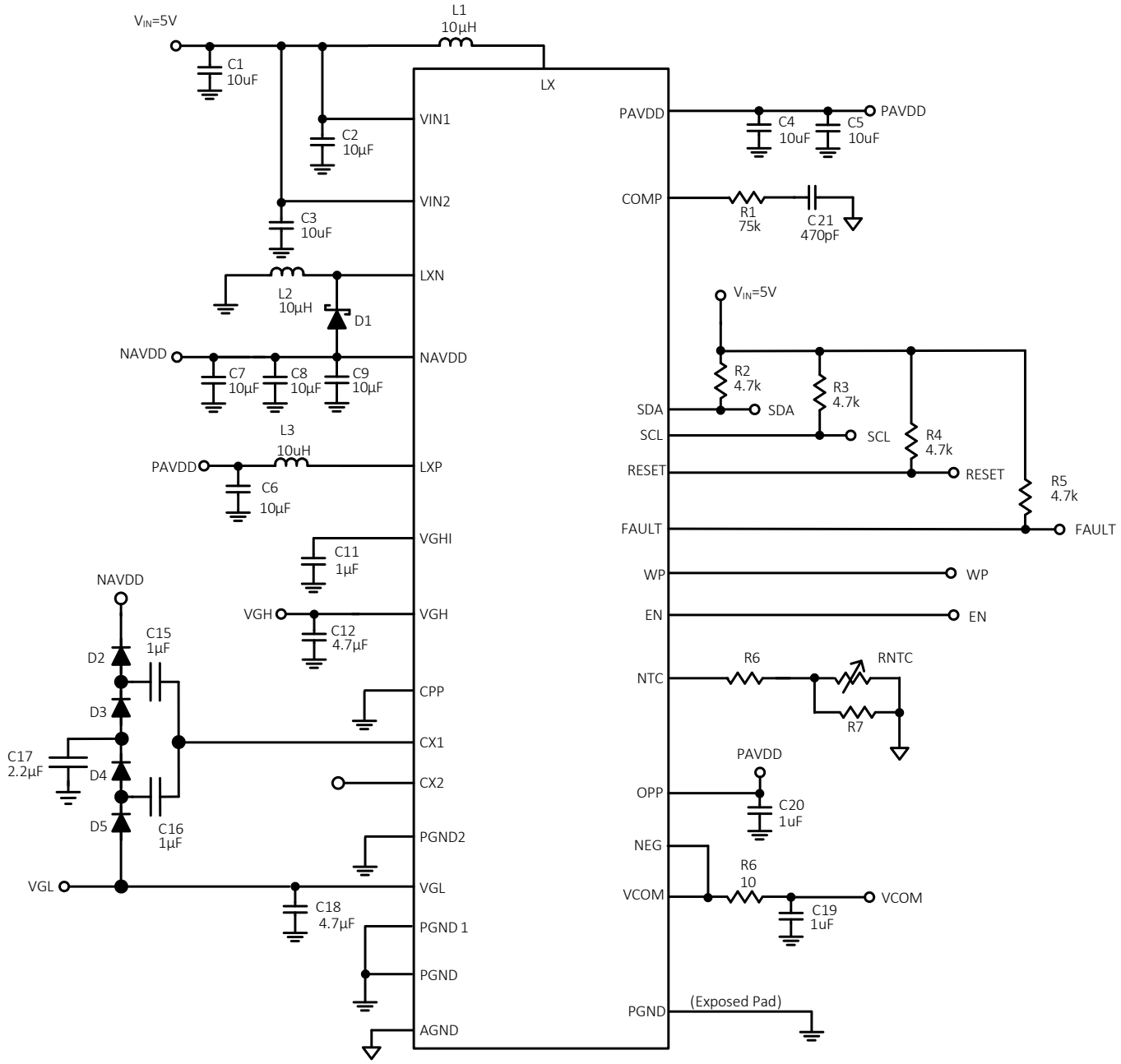


Figure 6. Typical Application Circuit with VIN > 4V Application

Table 1. Component List of Figure 1 Recommended

Components	Part Number	Description	Package	Supplier
C1~C9	GRT21BC71C106KE13	10uF/16V/X7S/0805	2mmx1.25mmx1.25mm	MURATA
C11	GRT21BR71H105KE01	1uF/50V/X7R/0805	2mmx1.25mmx1.25mm	MURATA
C12	GRT32ER71H475KE01	4.7uF/50V/X7R/1210	3.2mmx2.5mmx2.5mm	MURATA
C15, C16, C18, C19	GRT188R71E105KE13	1uF/25V/X7R/0603	1.6mmx0.8mmx0.8mm	MURATA
C17	GRT32ER71H475KE01	4.7uF/50V/X7R/1210	3.2mmx2.5mmx2.5mm	MURATA
C20	GRT155R71H471KE01	470pF/50V/X7R/0402	1.0mmx0.5mmx0.5mm	MURATA
L1, L2, L3	VCHA042A-100MS6	10uH	4.5mmx4.3mmx2.1mm	CYNTEC

Table 1. VGL Application Condition with Circuit

VIN	VGL Conditions	Power Sequence	Circuit No.	LXN-NAVDD Schottky	14[5]	VGL D/C	CPP Connection	VGL follow NAVDD at power up
2.5V~4V (3.3V)	|VGL| < PAVDD	VGL → NAVDD	Fig 2	X	0	V	GND	X
		NAVDD → VGL			0	V	GND	X
	PAVDD < |VGL| < (PAVDD+|NAVDD|)	VGL → NAVDD	Fig 1		0	V	NAVDD	X
			Fig 4		1	V	GND	X
		NAVDD → VGL			1	X	GND	V
	PAVDD < |VGL| < 2 x PAVDD	VGL → NAVDD	Fig 5		1	V	GND	X
		NAVDD → VGL			1	V	GND	X
	|VGL| > (PAVDD + |NAVDD|)	VGL → NAVDD	Fig 3		1	V	GND	X
		NAVDD → VGL			1	X	GND	V
4V~5.5V (5V)	|VGL| < PAVDD	VGL → NAVDD	Fig 2 + Schottky	V	0	V	GND	X
		NAVDD → VGL			0	V	GND	X
	PAVDD < |VGL| < (PAVDD+|NAVDD|)	VGL → NAVDD	Fig 1 + Schottky		0	V	NAVDD	X
			Fig 4 + Schottky		1	V	GND	X
		NAVDD → VGL			1	X	GND	V
	PAVDD < |VGL| < 2 x PAVDD	VGL → NAVDD	Fig 5 + Schottky		1	V	GND	V
		NAVDD → VGL			1	V	GND	V
	|VGL| > (PAVDD + |NAVDD|)	VGL → NAVDD	Fig 6		1	V	GND	X
		NAVDD → VGL			1	X	GND	V

Timing Diagram

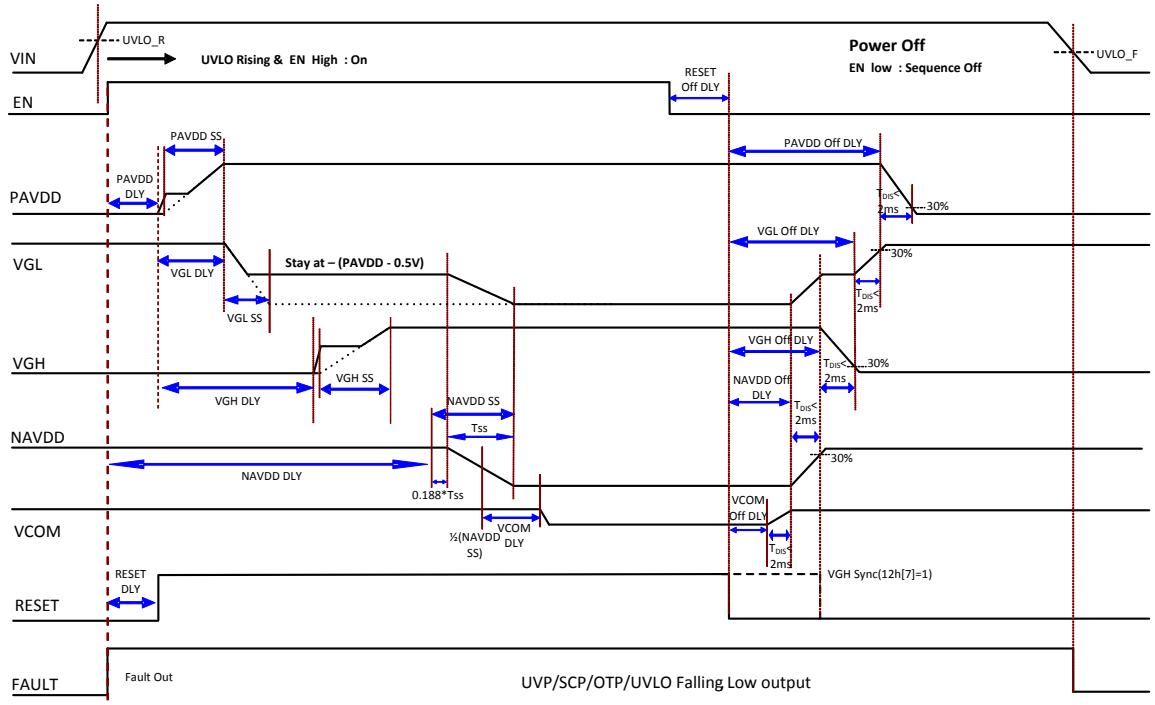


Figure 7. Power Sequence with Sequence Power-Off

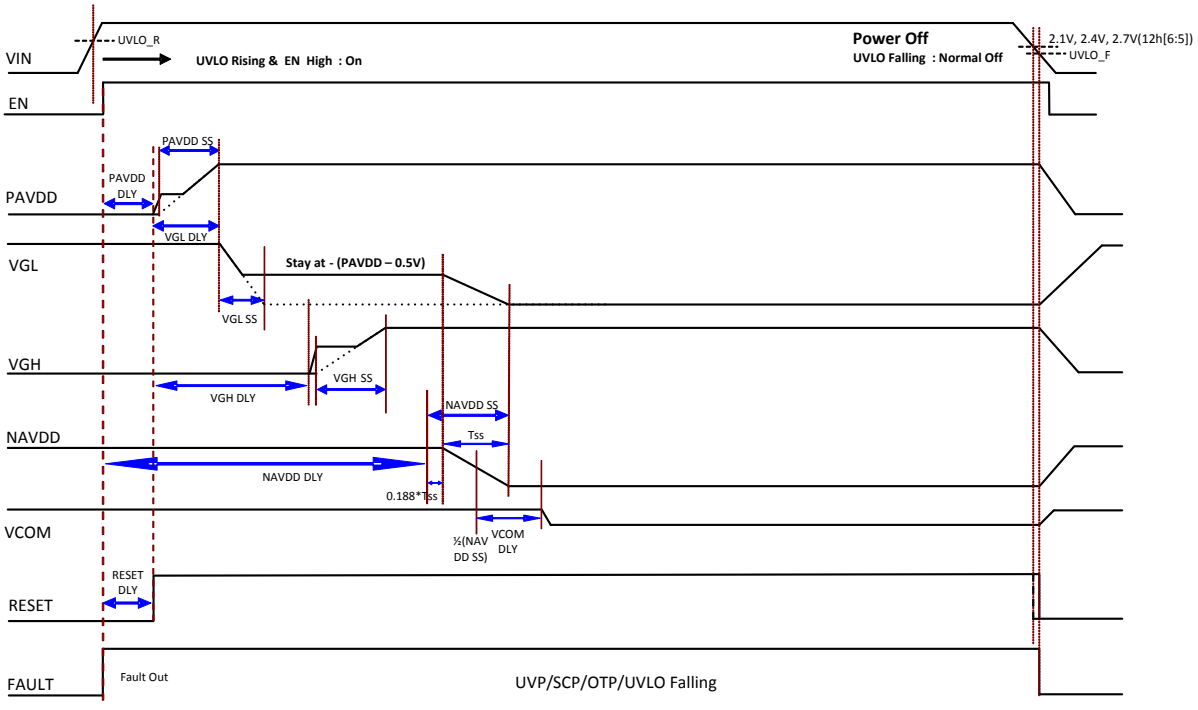


Figure 8. Power Sequence with Normal Power-Off

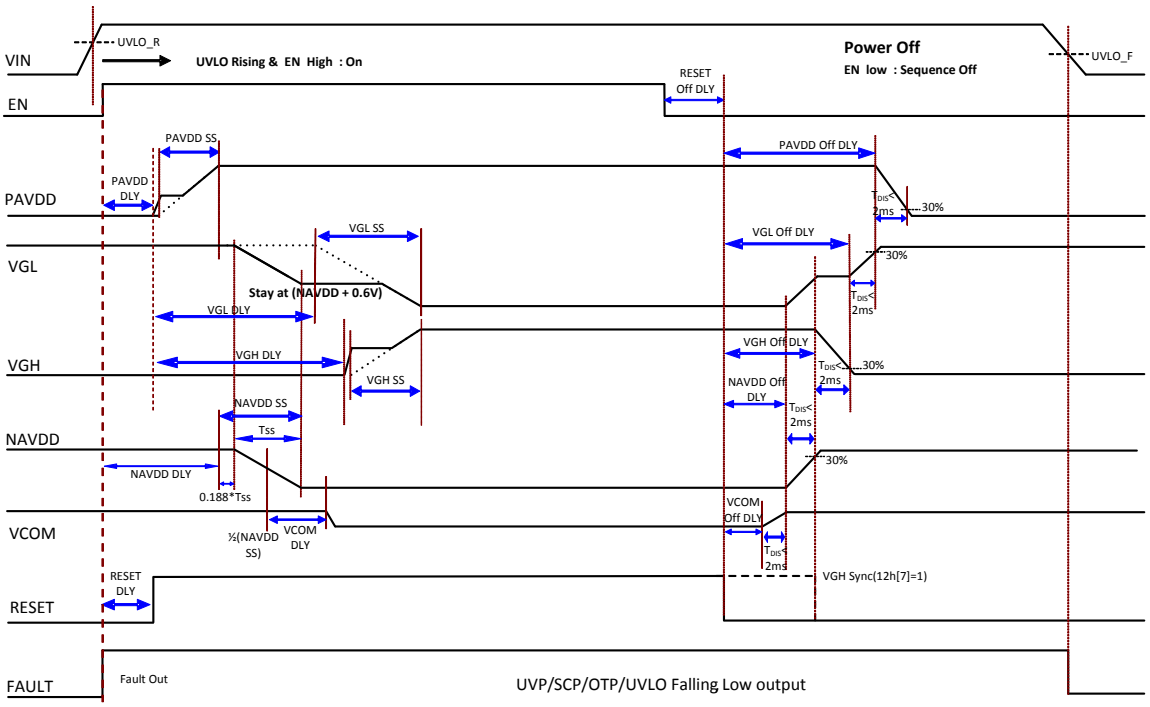


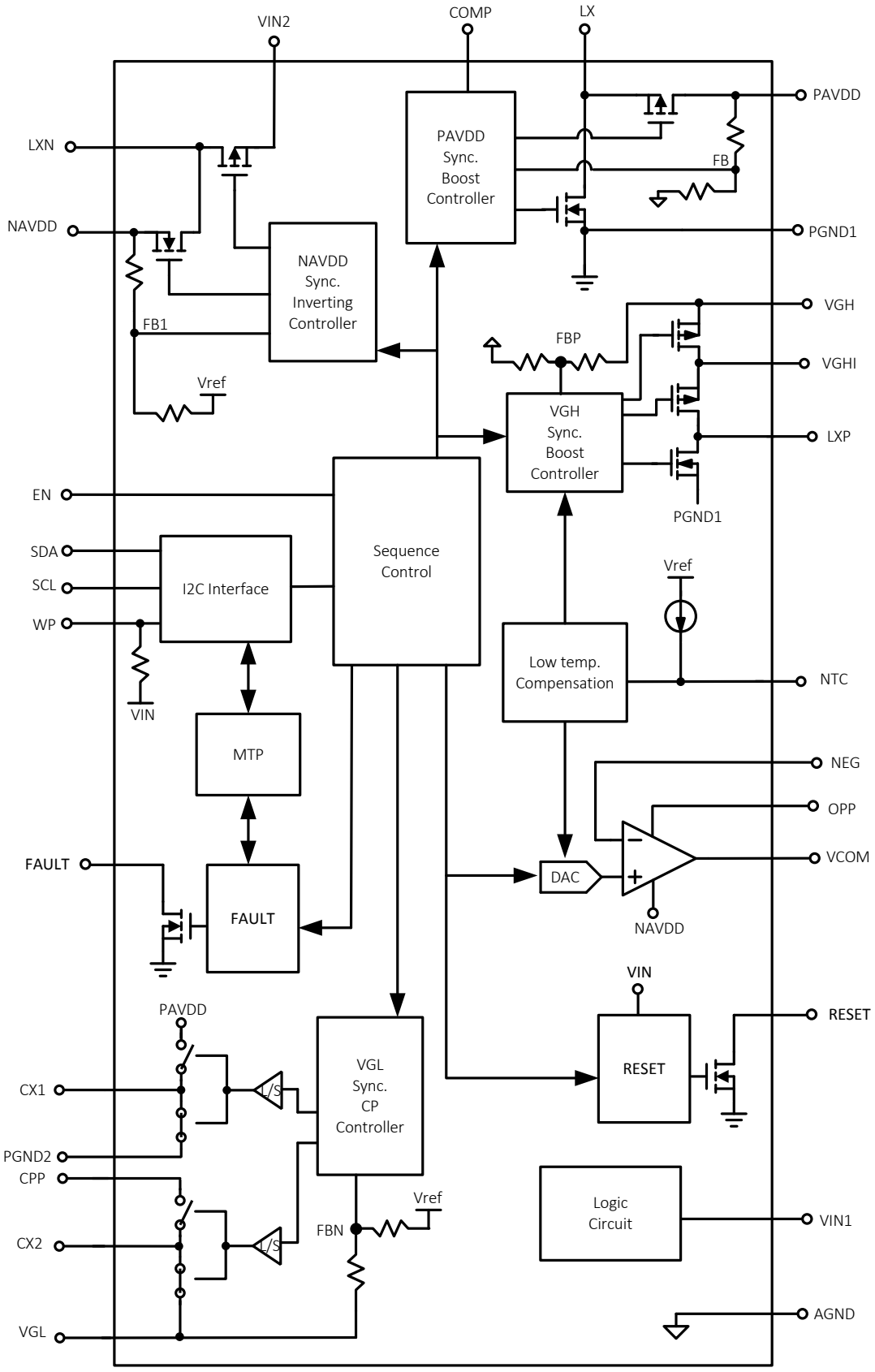
Figure 9. Power Sequence with NAVDD leading VGL (External Topology)

Note 1. Before IC power-up, the output voltage of each channel will be detected. If the one of outputs voltage is not below the SCP level, IC will wait the output voltage fall below the SCP level, then power up with sequence.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VGH	VGH boost converter output.
2	VGHI	VGH boost converter output without sequence control. The output is not isolated from input.
3	NC	No internal connection.
4	LXP	Switching node of VGH boost converter.
5	PGND1	Power Ground of PAVDD and VGH boost converter.
6	LX	Switching node of PAVDD boost converter.
7	NC	No internal connection.
8	PAVDD	PAVDD boost converter output.
9	CX1	VGL charge pump flying cap node1.
10	PGND2	Power ground of VGL charge pump.
11	VGL	VGL charge pump output.
12	CX2	VGL charge pump flying cap node2.
13	CPP	VGL charge pump power input.
14	NAVDD	NAVDD inverting converter output.
15	NC	No internal connection.
16	LXN	Switching node of NAVDD inverting converter.
17	VIN2	NAVDD supply voltage input.
18	OPP	VCOM OP-Amp positive power supply.
19	VCOM	VCOM Op-Amp output.
20	NEG	Inverting input of VCOM calibrator.
21	NC	No internal connection.
22	PGND	Power ground.
23	NTC	Thermistor network connection for temperature compensation.
24	VIN1	IC supply voltage input.
25	EN	Enable control input.
26	SCL	I2C clock input.
27	SDA	I2C data input.
28	WP	MTP write protection. When WP = 1, MTP is protected, but register still can be written. WP = 0, register and MTP can be written.
29	RESET	Output of voltage detection function
30	FAULT	Fault signal output.
31	AGND	Analog ground.
32	COMP	AVDD boost converter compensation input.
33 (Exposed Pad)	PGND	The exposed pad must be soldered to a large PCB and connected to PGND for maximum thermal dissipation.

Functional Block Diagram



Absolute Maximum Ratings (Note 2)

- VIN1, VIN2 to AGND ---------- –0.3 to 6V
- CPGND, PGND1, AGND to PGND ---------- –0.3 to 0.3V
- COMP, RESET, FAULT, WP, SDA, SCL, EN, NTC to AGND ---------- –0.3 to 6V
- LX, PAVDD to PGND ---------- –0.3 to 10V
- VIN2 to LXN ---------- –0.3 to 13V
- NAVDD to PGND ---------- –12 to 0.3V
- PAVDD to CX1 ---------- –0.3 to 10V
- CX1 to CPGND ---------- –0.3 to 10V
- CX2 to CPP ---------- –0.3 to 10V
- CX2 to VGL ---------- –0.3 to 20V
- CPP to PGND ---------- NAVDD to 0.3V
- VGL to PGND ---------- –20 to 0.3V
- LXP, VGHI, VGH to PGND ---------- –0.3 to 35V
- OPP to VCOM, NEG ---------- –0.3 to 16V
- VCOM, NEG to NAVDD ---------- –0.3 to 16V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN 32L 5x5 ---------- 3.63W
- Package Thermal Resistance (Note 3)

  WQFN 32L 5x5, θ_{JA} ---------- 27.5°C/W

  WQFN 32L 5x5, θ_{JC} ---------- 6°C/W
- Lead Temperature (Soldering, 10 sec) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –60°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 5)

- Supply Input Voltage, VIN1 ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(VIN1 = 2.5V to 5.5V, T_A = –40°C to 105°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
VIN1 Range	V_{IN1}		2.5	--	5.5	V
VIN1 Under-Voltage-Lockout Threshold	V_{UVLO_R}	VIN1 rising, turn-on IC	2.16	2.33	2.5	V
	V_{UVLO_H}	$V_{UVLO\_H} = V_{UVLO\_R} - V_{UVLO\_F}$	0.01	0.15	0.3	V
EN/WP Input Threshold	V_{IH}		1.5	--	--	V
	V_{IL}		--	--	0.8	V
VIN1 Quiescent Current	I_{VIN1}	SW not switching	0	2	4.5	mA
		SW switching	0	2.35	5	mA
VIN1 Shutdown Current		EN = Low, VIN1 = 3.3V	0	200	400	μA
Switch Frequency Range	f_{OSC}		600	--	2200	kHz
Switch Frequency Accuracy			–15	--	15	%
UVP Voltage Percentage	UVP		58	70	78	%
UVP Fault Delay Duration to IC Shutdown	t_{UVP}		30	50	70	ms
SCP Voltage percentage	SCP		23	30	37	%
SCP Delay	t_{SCP}		85	100	115	μs
Power Off Delay Time	t_{D_poff}	3ms/step, 16 steps	0	--	45	ms
Thermal Shutdown	T_{SD}	Temperature rising	--	150	--	°C
	ΔT_{SD}	Hysteresis	--	20	--	°C
PAVDD Sync. Boost Converter						
Output Voltage Range	V_{PAVDD}	0.05V/step, f_{OSC} = 2.2MHz	5.0 or VIN + 2.2	--	7.3	V
		0.05V/step, f_{OSC}≤1MHz	5.0 or VIN + 1.3	--	7.3	V
Output Voltage Tolerance		T_A = 25°C, (V_O – V_S) / V_S x 100%, no load	–1	--	1	%
		T_A = –40°C to 105°C, (V_O –V_S) / V_S x 100%, no load	–2	--	2	%
On Delay Time	t_{D_PAVDD}	5ms/step, 16 steps	0	--	75	ms
Soft-start Time	t_{SS_PAVDD}	5ms/step, 8 steps	5	--	40	ms
Delay/Soft-start Time Tolerance			–15	--	15	%
Max. Duty	D_{MAX_PAVDD}		83	90	97	%
OVP Voltage percentage	V_{OVP_PAVDD}	PAVDD rising	110	120	130	%
Current Limit	I_{LIM_PAVDD}		1.5	1.8	2.3	A
R_{ON} Low-Site	$R_{DSON\_LS\_PAVDD}$		0.05	0.2	0.4	Ω
R_{ON} High-Site	$R_{DSON\_HS\_PAVDD}$		0.05	0.3	0.4	Ω
Power On/Off Discharge R_{ON}	PAVDD_R_{DIS}		3	5	7	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pre-charge Threshold	V_{PC}	V_{IN} = 3.3V, V_{PC} = V_{IN} – V_{PAVDD}	--	0.2	--	V
PAVDD SCP level	PAVDD_SCP_2	Before PAVDD Soft-start finish	1.134	1.26	1.386	V
NAVDD Sync. Buck-Boost Converter						
Output Voltage Range	V_{NAVDD}	0.05V/step	–5	--	–7.3	V
Output Voltage Tolerance		T_A = 25°C, (V_O - V_S) / V_S x 100%, no load	–1	--	1	%
		T_A = –40°C to 105°C, (V_O – V_S) / V_S x 100%, no load	–2	--	2	%
On Delay Time	t_{D_NAVDD}	5ms/step, 16 steps	0	--	75	ms
Soft-Start Time	t_{SS_NAVDD}	5ms/step, 8 steps	5	--	40	ms
Delay/Soft-start Time Tolerance			–15	--	15	%
Max. Duty	D_{MAX_NAVDD}		83	90	97	%
OVP Voltage percentage	V_{OVP_NAVDD}	NAVDD falling	110	120	130	%
R_{ON} High-Site	$R_{DSON\_HS\_NAVDD}$		0.05	0.14	0.4	Ω
R_{ON} Low-Site	$R_{DSON\_LS\_NAVDD}$		0.05	0.23	0.4	Ω
Power On/Off Discharge R_{ON}	NAVDD_R_{DIS}		6	10	14	Ω
Current Limit	I_{LIM_NAVDD}		1.5	1.9	2.5	A
VGL Charge-Pump Regulator						
Output Voltage Range	V_{GL}	0.25V/step	–6	--	–18	V
Output Voltage Tolerance		T_A = –40°C to 105°C, (V_O – V_S) / V_S x 100%, no load	–3	--	3	%
On Delay Time	t_{D_VGL}	5ms/step, 16 steps	0	--	75	ms
Soft-start Time	t_{SS_VGL}	3ms/step, 8 steps	3	--	24	ms
Delay/Soft-start Time Tolerance			–15	--	15	%
PMOS R_{ON}	$R_{DSON\_PMOS\_VGL}$		0.15	0.5	1.5	Ω
NMOS_1 R_{ON}	$R_{DSON\_NMOS1\_VGL}$		0.15	0.32	1.5	Ω
NMOS_2 R_{ON}	$R_{DSON\_NMOS2\_VGL}$		0.15	0.9	1.5	Ω
NMOS_3 R_{ON}	$R_{DSON\_NMOS3\_VGL}$		0.15	0.4	1.5	Ω
Power On/Off Discharge R_{ON}	VGL_R_{DIS}		50	175	300	Ω
VGH Sync. Boost Converter						
Output Voltage Range	VGH		7 or PAVDD + 2	--	30	V
Output Voltage Tolerance		T_A = 25°C, (V_O – V_S) / V_S x 100%, no load	–3	--	3	%
		T_A = –40°C to 105°C, (V_O – V_S) / V_S x 100%, no load	–4.5	--	4.5	%
VGH Low Temperature Compensation Output Voltage Range	VGH_LT	2V/step, 4 steps. VGH = VGH + VGH_LT @ Low temperature compensation. (VGH + VGH_LT) > 30V, VGH is limited on 30V at low temperature.	2	--	8	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On Delay Time	t_{D_VGH}	5ms/step, 16 steps	0	--	75	ms
Soft-start Time	t_{SS_VGH}	5ms/step, 4 steps	5	--	20	ms
Delay/Soft-start Time Tolerance			–15	--	15	%
Max. Duty	D_{MAX_VGH}		83	90	97	%
OVP Voltage percentage	V_{OVP_VGH}	(VGH + VGH_LT)*120%	105	120	135	%
Max OVP Voltage Threshold	$V_{OVP\_VGH\_Max}$	(VGH + VGH_LT) > 28.5V	32.5	34.5	34.5	V
R_{ON} Low-Site	$R_{DSON\_LS\_VGH}$		0.2	0.36	0.6	Ω
R_{ON} High-Site	$R_{DSON\_HS\_VGH}$		0.3	0.6	1	Ω
R_{ON} High-Site_GD	$R_{DSON\_HS\_GD\_VGH}$		0.3	0.65	1	Ω
Power On/Off Discharge R_{ON}	VGH_R_{DIS}		150	200	250	Ω
Current Limit	I_{LIM_VGH}		0.56	0.7	0.88	A
VCOM Operational Amplifier						
VCOM_C Output Voltage Range	V_{COM_C}	20mV/step, 251 steps	-3	--	2	V
VCOM_F Output Voltage Range	V_{COM_F}	10mV/step, 256 steps	V_{COM_C} – 1.27	--	V_{COM_C} + 1.28	V
On Delay Time	t_{D_VCOM}	5ms/step, 16 steps	0	--	75	ms
Slew Rate	SR		1	15	40	V/μs
Short Circuit Current	I_{VCOM_SC}	Unit Gain,VCOM = –1V,	±100	±350	±600	mA
RESET Function						
On Delay Time	t_{D_RESET}	5ms/step, 16 steps	0	--	75	ms
I2C Interface						
Logic-Input High Input	V_{IH}	SCL, SDA	1.05	--	--	V
Logic-Input Low Input	V_{IL}	SCL, SDA	--	--	0.4	V
SCL Clock Frequency	f_{SCL}		15	400	1000	kHz

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

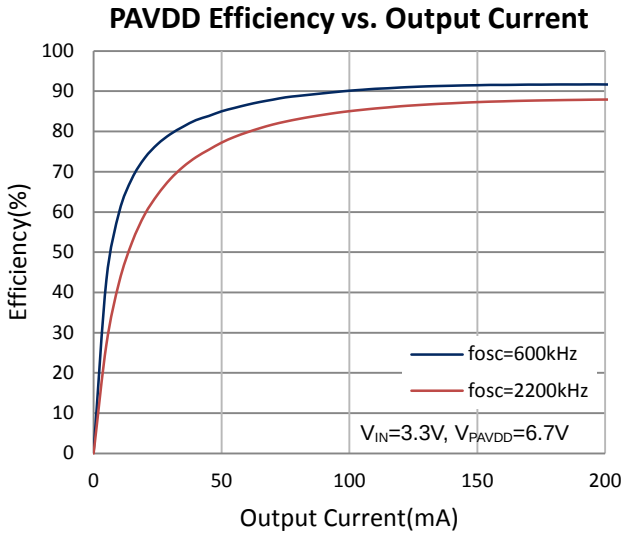
Note 4. Devices are ESD sensitive. Handling precaution is recommended.

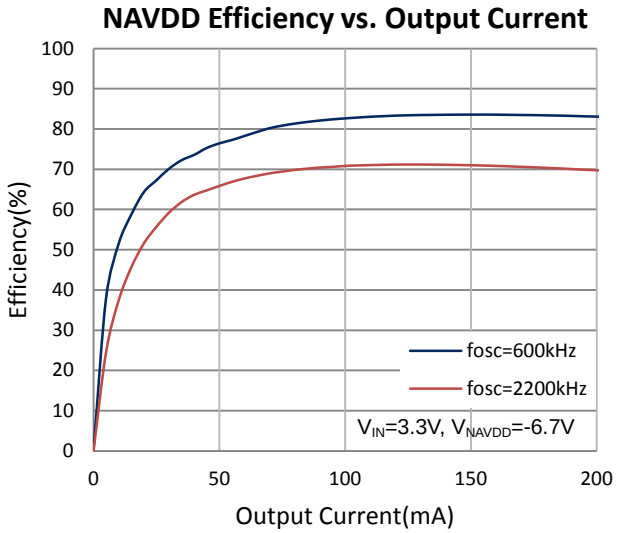
Note 5. The device is not guaranteed to function outside its operating conditions.

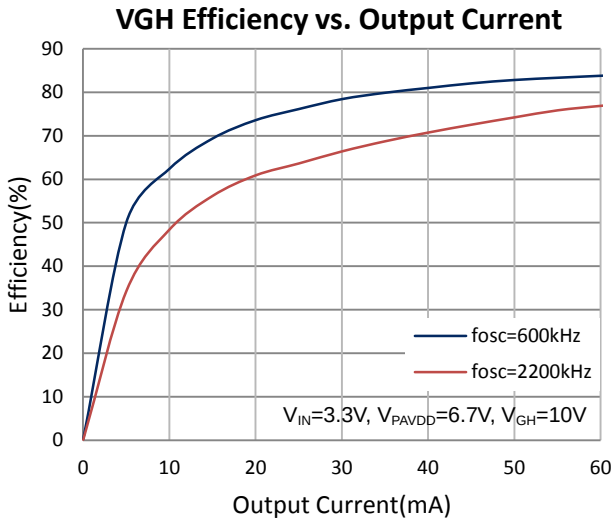
Note 6. Limits apply to the recommended operating temperature range of –40°C to 105°C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN1 = 2.5V to 5.5V.

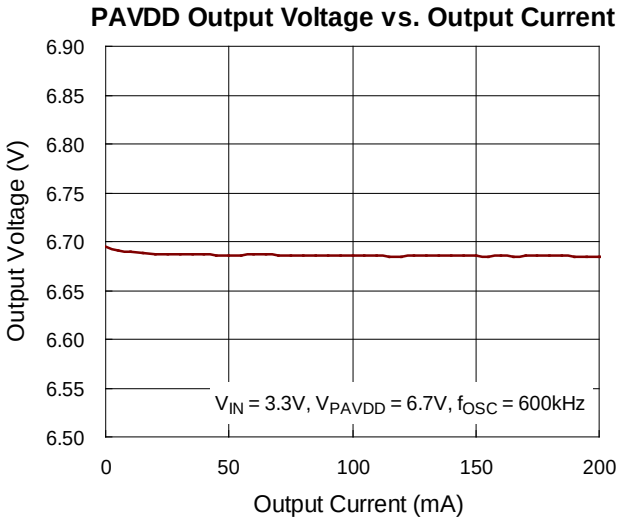
Note 7. In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R\theta_{JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX} - (R\theta_{JA} \times P_{D\text{-}MAX})$.

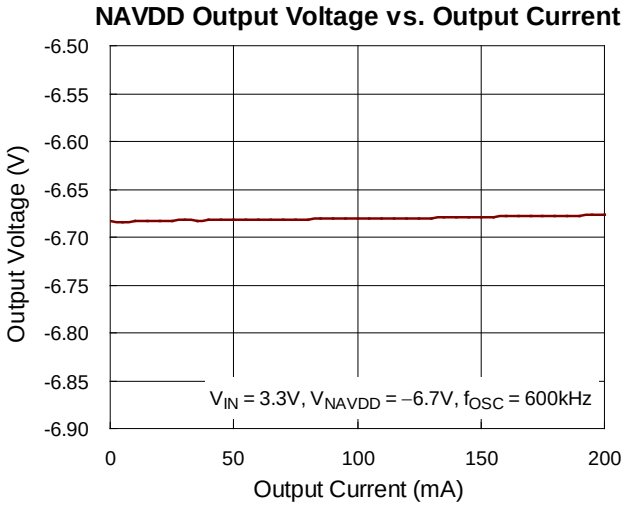
Typical Operating Characteristics

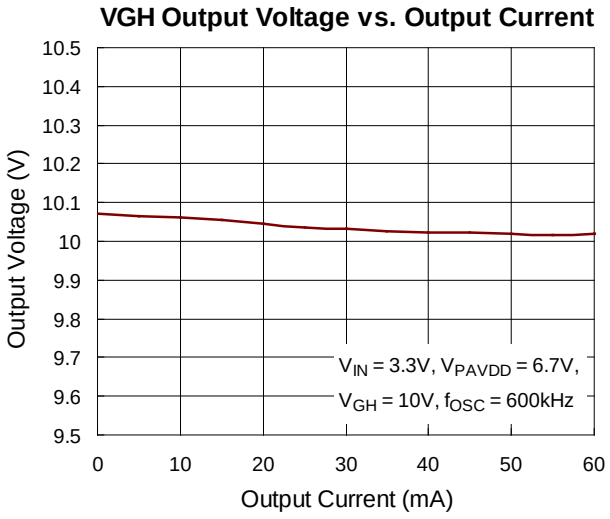




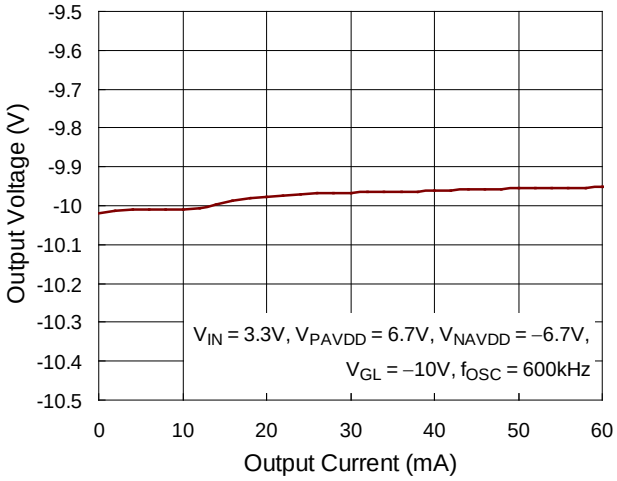




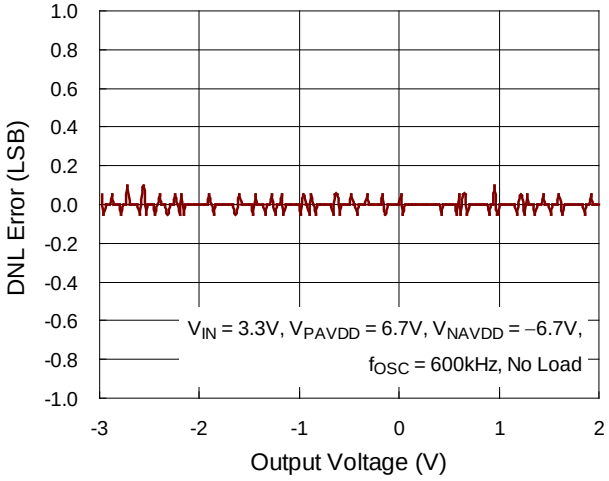




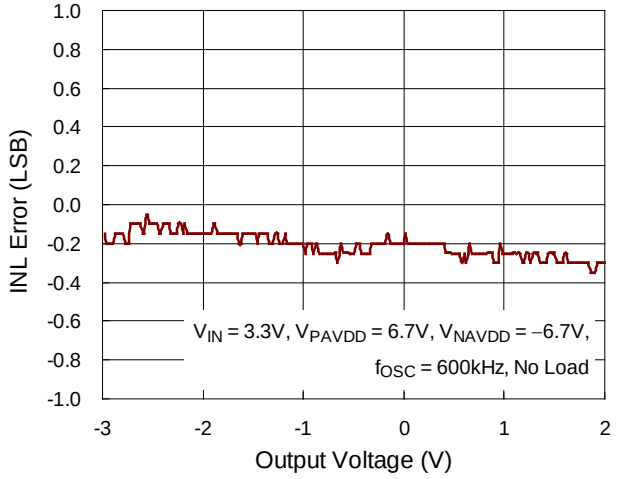
VGL Output Voltage vs. Output Current



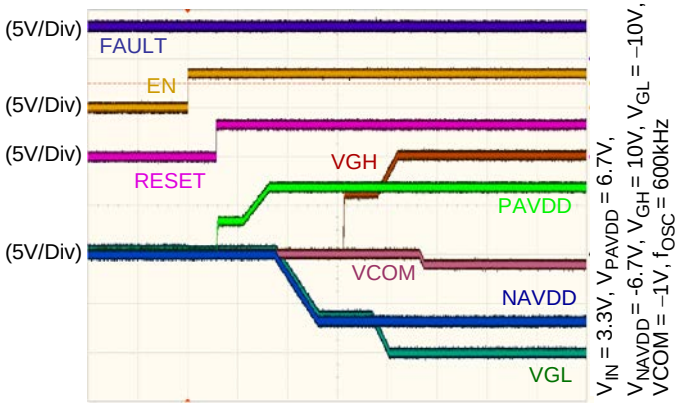
VCOM_C DNL Error vs. Output Voltage



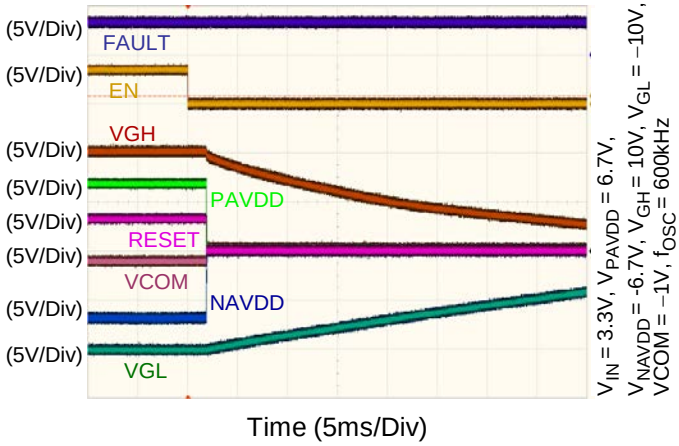
VCOM_C INL Error vs. Output Voltage



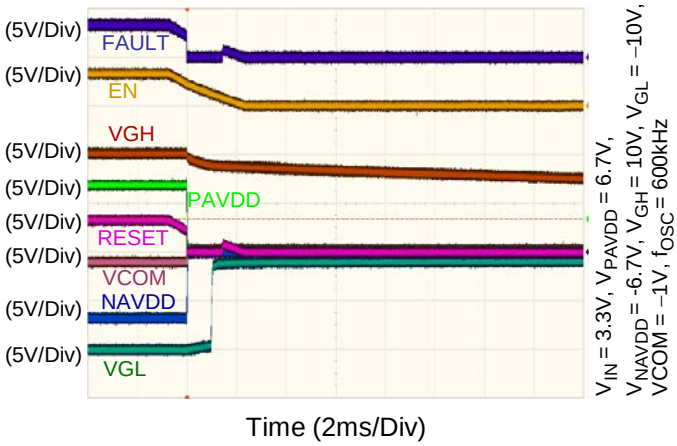
Power On



Power Off with Sequence-Off



Power Off with Normal-Off



Applications Information

The RTQ6749 is an integrated solution for automotive TFT LCD panel, including PMIC and memory system. The RTQ6749 application mechanism is introduced in later sections. The RTQ6749's slave address is 1101110.

PMIC - Power management system provides 2 sync-boost converters for PAVDD and VGH, one synchronous inverting converter for NAVDD, one negative charge-pump for VGL, and one operational amplifier for VCOM. Power-On and Power-Off sequences are control by EN input pin. Detail time sequence control is described in “Timing Diagram”. The I^2C interface can program each output channel as well as sequence control and voltage setting.

Switching Frequency Setting

The each channel switching frequency is set by the I^2C interface. It has a 2-bit register as 4 steps, the setting options are 600kHz, 800kHz, 1MHz and 2.2MHz. The switching frequency default value is 600kHz (0x00). Please refer to the register map for details.

Under Voltage Protection (UVP)

The RTQ6749 equip a fault conditions to shut down IC. Once the output voltage is below the 70% output voltage, the internal timer starts counting and the fault condition continued about 50ms, the IC will shut down. After the UVLO or EN started again, the fault protection would be released. The protection start detecting at the soft-start finish of the outputs channel, the voltage of outputs has to large than the UVP level after soft-start finish and within 50ms. And an option is provided for user to enable or disable, the option can set by the register 14h[1].

Short Circuit Protection (SCP)

The RTQ6749 equip a fault conditions to shut down IC. In the power-on sequence, before the each channel power-up, the outputs voltage of each channel have to smaller than the SCP level of the channel. Or IC would wait the all of outputs voltage fall below the SCP level, then do the power-on sequence as the Figure 10 shown. The PAVDD_SCP_2 of PAVDD is 1.26V(typ) before PAVDD Soft-start, after soft-start finish the SCP will become 30% of voltage setting. the other channels are the 30% of voltage setting. The judgement point of the output voltage below SCP is from UVLO_R and plus 1ms.

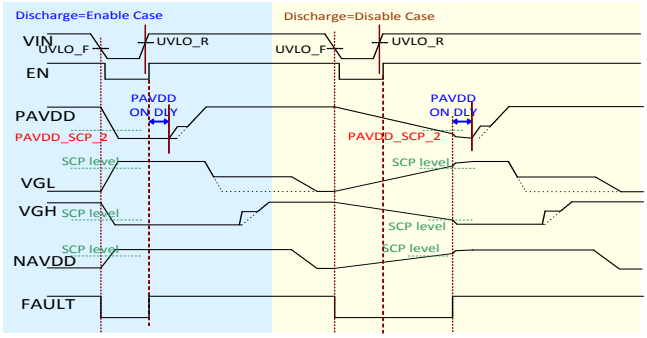


Figure 10. The Power-up Limitation of The Outputs Voltage must below the SCP level

In PAVDD pre-charge stage, the PAVDD SCP will be also checked after PAVDD power-on delay counting finish and plus 4ms. The SCP function also work during the soft-start period. If the PAVDD voltage is below the PAVDD_SCP_2 (1.26V_typ), IC will be protected at the delay counting finish and plus 4ms as the point “c” in the Figure 11 shown.

The pre-charging finish is going to judge the difference between PAVDD and VIN. When the difference is smaller than 0.2V(typ) that will be judged to pre-charge finished, and entry the soft-start stage. The SCP of the other channels is enabled after the soft-start of the channels is finished.

In another one case, If the PAVDD voltage is above PAVDD_SCP_2, but not satisfy the condition of pre-charging finish. Then IC will keep in pre-charge stage, until the condition is satisfied and then to entry soft-start stage as the Figure 12 shown.

Once the output voltage is below the 30% output voltage during operation stage, the high/low side MOSFET will stop switching immediately as the point “a” in the Figure 13 shown. The other channels will be stopped switching after 100us and the FAULT pin go low as the point “b”.

After the UVLO or EN started again, the protection would be released. There is an option as 14h[0] for user to disable or enable this function. the first PAVDD_SCP_2 detection during new power on in

Figure 10 cannot be disable by 14h[0].

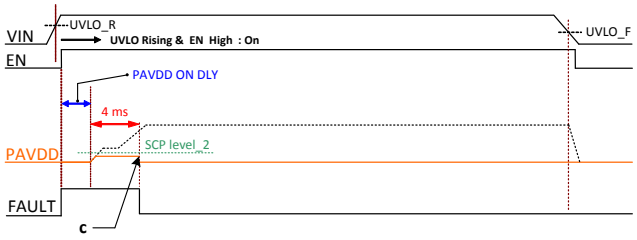


Figure 11. SCP Mechanism at PAVDD pre-charge when PAVDD with the Abnormal Heavy Load

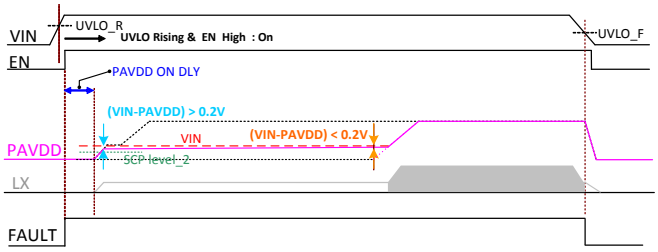


Figure 12. SCP Mechanism when PAVDD between SCP Level and Pre-charge Finish

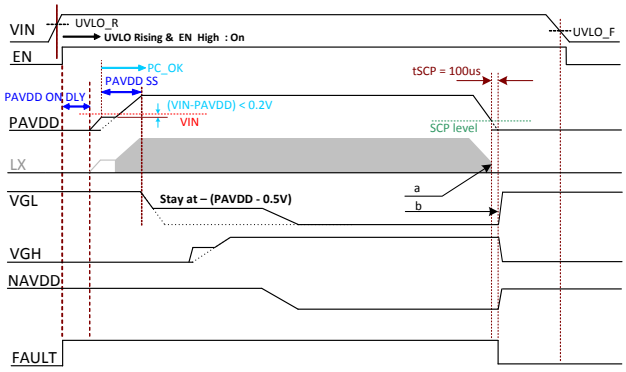


Figure 13. SCP Mechanism during Normal Operating

Over Temperature Protection (OTP)

The RTQ6749 equips an over temperature protection (OTP) to prevent the excessive power dissipation from overheating. The OTP will shut down switching operation while junction temperature exceeds approximately 150°C. All of output channel starting work while junction temperature is cooled by approximately 20°C. Prevent the maximum junction temperature over around 150℃ and maintain continuous operation. The protection provided an option for user to enable or disable, the option can set by the register 14h[2].

PAVDD Synchronous Boost Converter

The PAVDD synchronous Boost converter is high efficiency PWM architecture with programmable switching frequency. It performs fast transient responses to meet the requirement of source driver supplies for TFT-LCD display. The high operation frequency can prevent that switching frequency influence AM band range. The output voltage is controlled by a 6-bit register with 47 steps. The error amplifier varies the COMP voltage by sensing the PAVDD pin to regulate the output voltage.

PAVDD Slew Rate Setting

The PAVDD LX falling slew rate can be controlled by I^2C interface, to optimize the efficiency and EMI performance. The adjustable options are slowest, slow, normal and fast. The default value is normal option. Please refer to the register map for details.

PAVDD Output Voltage Setting

The PAVDD output voltage is set by I^2C interface. User can write the 00h[5:0] register to set PAVDD output voltage. It has 6 bits for output voltage adjustable, the setting range is from 5V to 7.3V, and each voltage step is about 50mV. The default voltage of PAVDD is 6.7V(0x22). Please refer the register map for detail on how to adjust the output voltage.

PAVDD Soft-start time Setting

The PAVDD soft-start time could be adjusted by the register 08h[2:0]. There are 3 bits and 8 steps. The soft-start time setting range is from 5ms to 40ms, and each step is about 5ms. The soft-start time default value is 10ms (0x01). The soft- start mechanism is following the reference voltage to soft-start, the soft-start starting point is from the slope of the soft-start down to the point of crosses 0V. The soft-start finish point is PAVDD output voltage ready. Please refer to Figure 7 and register map for details.

PAVDD Power-on Delay Time Setting

The PAVDD power-on delay time is adjustable by I^2C interface. There are 16 steps within 3 bits register of 07h. The delay time setting range is from 0ms to 75ms, and each steps time is about 5ms. The delay time default value is 5ms (0x01). The delay time is from the MTP load data finish to PAVDD output voltage starting rising. Please refer the Figure 7, and register map for detail.

PAVDD Current Limit

The RTQ6749 can limit the peak current to achieve over-current protection. The IC senses the inductor current of on period that is flowing into LX pin. The minimum value of the current limit is 1.5A. The internal N-MOSFET will be turned off if the peak inductor current achieve current limitation level, so that the output current at current limit boundary is denoted as $I_{OUT(CL)}$ and can be calculated as shown in the following equation :

$$I_{OUT(CL)} = \eta \times \frac{V_{IN}}{V_{OUT}} \times \left(I_{CL} - \frac{1}{2} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{T_S}{L} \right)$$

where η is the efficiency of the PAVDD sync-boost converter, I_{CL} is the value of the current limit and T_S is the switching period.

PAVDD Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of R1 and C18. Choose R1 to set high frequency integrator gain for fast transient response and C18 to set the integrator zero to maintain stability. The recommended values are 75kΩ and 470pF for most applications.

Sync-Boost Inductor Selection

The inductance depends on the maximum input current. The inductor ripple current range is 20% to 40% of maximum input current that is a general rule. If 40% is selected as an example, the inductor ripple current can be calculated as following equation :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

Where η is the efficiency of the synchronous boost converter, $I_{IN(MAX)}$ is the maximum input current and I_{RIPPLE} is the inductor ripple current. Besides, the input peak current can be calculated by maximum input current plus half of inductor ripple current shown as following equation :

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of inductor must be greater than I_{PEAK}. The inductance can be eventually determined as following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

Where f_{OSC} is the PAVDD switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Sync-Boost Output Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of two parts, one is the product of $(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT})$ and ESR of output capacitor, another part is formed by charging and discharging process of output capacitor. Refer to Figure 14, evaluate ΔV_{OUT1} by ideal energy equalization. According to the definition of Q, the Q value can be calculated as following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2}\Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

Where T_S is the inverse of switching frequency and the ΔI_L is the inductor ripple current. Move C_{OUT} to left side to estimate the value of ΔV_{OUT1} as following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

Then take the ESR into consideration, the ESR voltage can be determined as the following equation :

$$\Delta V_{ESR} = \left(\frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D \times T_{OSC}}{2L} \right) \times R_{ESR}$$

Finally, the output ripple voltage ΔV_{OUT} is combined from theΔV_{OUT1} and ΔV_{ESR} as following equation :

$$\Delta V_{OUT} = \Delta V_{OUT1} + \Delta V_{ESR}$$

In the general application, the PAVDD output capacitor is recommended that to use three 10μF/X7R/1206 capacitors and the effective capacitance value of output capacitance needs 13μF at least. In addition, The VGH effective output capacitance should be at least 2.1μF. It is recommended to use a 4.7μF/50V/X7R/1210 for

general applications. To reduce VGH ripple, higher values for VGH capacitance are allowed, but the designer should consider the worst case input inrush current when using larger VGH capacitance as shown in Figure 14.

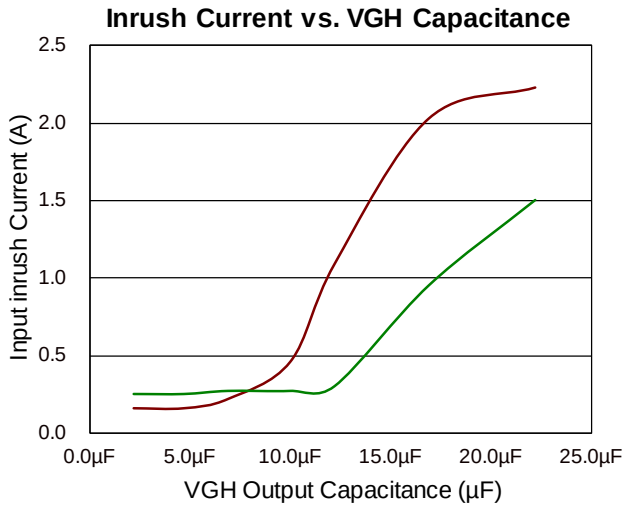


Figure 14. Inrush current vs. VGH capacitance

Higher inrush current in combination with increased input power trace resistance could result in input voltage drop which could trigger IC input UVLO.

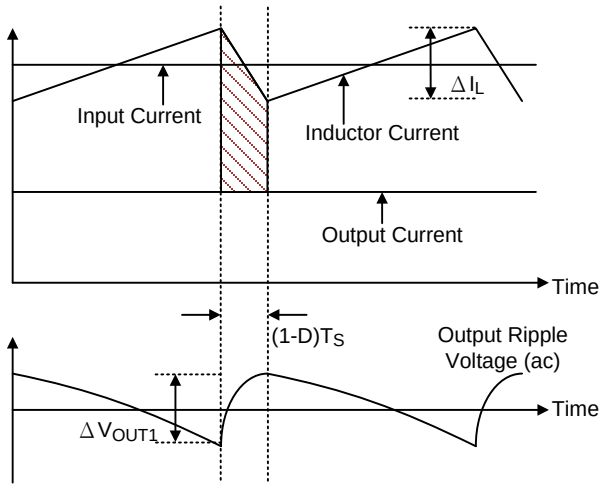


Figure 15. The Output Ripple Voltage without the Contribution of ESR

VGH Sync-Boost Converter

The VGH synchronous boost converter is high efficiency PWM architecture with programmable switching frequency, output voltage, power-on delay time and soft-start time by I^{2}C interface. The VGH integrate a GD MOSFET at output for sequence control.

VGH Soft-start Time Setting

The VGH sync-boost converter has an integrated soft-start function to reduce the input inrush current of power on. The soft-start time can be set through the 0Ch[1:0] register by the I^{2}C interface. It has a 2-bit register with 4 steps. The soft-start time options as 5ms, 10ms, 15ms and 20ms, the each step is about 5ms. The soft- start mechanism is following the reference voltage to start up. The soft-start starting point is from the slope of the soft-start down to the point of crosses 0V. The soft-start finish point is VGH output voltage ready. Please refer to Figure 7, and register map for details.

VGH Power-on Delay Time Setting

The VGH boost converter has integrated a power-on delay function. The delay time can be adjusted by I^{2}C interface, to write data into the 0Bh[3:0] register. There are 16 options within 3 bits. The delay time setting range is from 0ms to 75ms, and each step is about 5ms and the default value is 25ms (0x05). The delay time period is from the start point of PAVDD soft-start to VGH output voltage starts rising. If the VGH delay time set 0ms, the VGH need to wait PAVDD pre-charge finish, then go do pre-charge. Please refer the Figure 7 and register map for detail.

VGH Current Limit

The RTQ6749 can limit the peak current to achieve over current protection. The IC senses the inductor current of on period that is flowing into LXP pin. The typical value of the current limit is 0.7A. The internal N-MOSFET will be turned off if the peak inductor current reaches 0.7A. So that, the output current at current limit boundary is denoted as $I_{OUT(CL)}$ and can be calculated as following equation :

$$I_{OUT(CL)} = \eta_P \times \frac{V_{IN}}{V_{OUT}} \times \left(I_{CL} - \frac{1}{2} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{T_S}{L} \right)$$

Where η_P is the efficiency of the VGH boost converter, I_{CL} is the value of the current limit and T_S is the switching period.

VGH Sync-Boost Loop Compensation

The VGH boost converter's loop compensation network is built-in inside the RTQ6749 and the compensation setting is fixed.

VGH Voltage Setting

The VGH voltage is programmable by I^2C interface. User can write data into 02h[5:0] register to set VGH voltage. The 02h register is for the VGH voltage of TH. The TH is the temperature point of started compensated temperature. Please refer the Figure 11 for clarity.

The voltage setting range is from 7V to 30V. The default value of VGH is 10V (0x06). The each voltage step is about 0.5V. It is integrated a protection when VGH too close PAVDD, VGH will automatically adjust the output voltage to keep the difference equal or large than 2V between PAVDD and VGH. Please refer the register map for detail.

VGH_LT Voltage Setting

The VGH_LT voltage is programmable by I^2C interface. User can write the 06h[4:0] register to set VGH_LT voltage. The 06h register is for VGH voltage of TL. TL is the temperature point of stopped compensated temperature. The VGH voltage of TL is equal to VGH+VGH_LT, the VGH_LT setting is only for difference. The setting range is from 2V to 8V. The default value of VGH_LT is 2V (0x00). The each voltage step is about 2V. Please refer the Figure 11 and register map for detail.

VGH Temperature Compensation

There is a temperature compensation feature in the RTQ6749. The VGH output voltage of TH will be change slowly from VGH of TH to VGH of TL if temperature is below TH, until the temperature is equal to TL, the VGH output voltage will be equal to VGH of TL.

The compensation is achieved by controlling the feedback voltage .The feedback voltage (V_{FBP}) of VGH is sensed by VGH pin, from the VGH output voltage through the internal divider to get the feedback voltage. The V_{FBP} can be compensated by external thermal sensing element (R_{NTC}) and resistors (R6, R7), which set at what temperature the compensation starts and the slope of the compensation. The R_{NTC}, R6 and R7 are shown in the “Typical Application Circuit”, and temperature compensation curve is shown in Figure 16 :

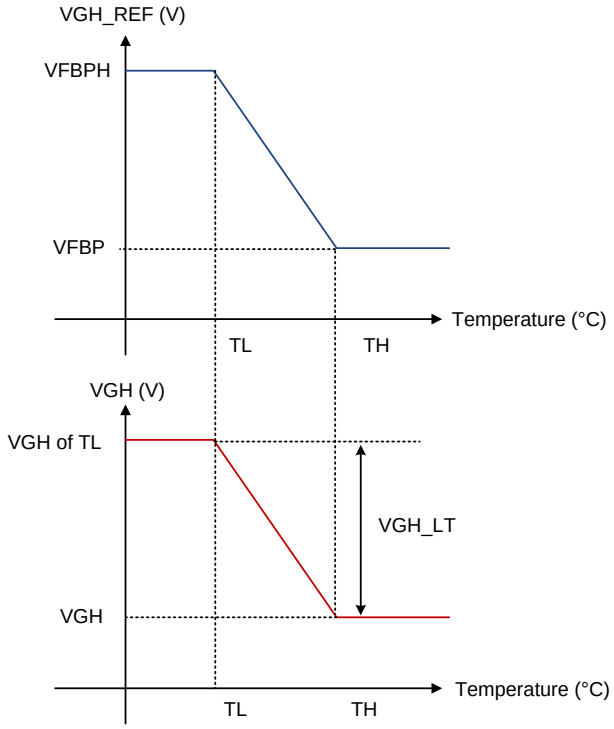


Figure 16. VGH Temperature Compensation Curve

Where V_{FBPH} is the feedback voltage at TL, the TH is the temperature point of started compensated temperature; TL is the temperature point of stopped compensated temperature.

The NTC pin will provide a current about 20μA(I_{NTC}), from IC internal constant current source. Then the R_{ENTC} can be calculated by the 20μA. The R_{ENTC} is equivalent resistance of R_{NTC}, R_6 and R_7.

$$V_{FBP} = I_{NTC} \times R_{ENTC\_H} \quad (1)$$

$$V_{FBPH} = I_{NTC} \times R_{ENTC\_L} \quad (2)$$

By the above-descript relationship, the R6 and R7 can be determined by the below equation :

$$R7 = \frac{-B+\sqrt{B-4AC}}{2A}$$

$$R6 = R_{ENTC\_H} - \frac{R7 \times R_{ENTC\_H}}{R7+R_{ENTC\_H}}$$

$$A = R_{ENTC\_H} - R_{ENTC\_L} - R_{NTC\_H} + R_{NTC\_L}$$

$$B = (R_{ENTC\_H} - R_{ENTC\_L}) \times (R_{NTC\_H} + R_{NTC\_L})$$

$$C = (R_{ENTC\_H} - R_{ENTC\_L}) \times R_{NTC\_H} \times R_{NTC\_L}$$

Where R_{ENTC_H} is the equivalent resistance value of R_{NTC}, R6 and R7 at TH, The R_{ENTC_L} is the equivalent resistance value of R_{NTC}, R6 and R7 at TL, R_{NTC_H} is the resistance value of R_{NTC} at TH, R_{NTC_L} is the resistance value of R_{NTC} at TL.

VGL Negative Charge Pump Regulator

The negative charge pump regulator is programmable for soft-start time, the output voltage, switching frequency and power-on delay time by I^2C interface. Moreover, it also equips a fault protection to prevent the output sudden overload.

VGL Output Voltage Setting

The VGL output voltage is adjusted by I^2C interface. User can write a data into the 03h[5:0] register for setting VGL output voltage. There are 7 bits for output voltage adjustable, the setting range is from -6V to -18V, and each voltage step is about -250mV. The default output voltage is about -10V(0x10). Please refer the register map for detail.

Because the VGL voltage is supplied by PAVDD and NAVDD, the VGL maximum output voltage is limited by PAVDD + |NAVDD|, the VGL provides 3 options for user. If |VGL| < PAVDD, it is recommended that the CPP should be connected to GND as Figure 2 shown. But if the NAVDD power-on sequence lead VGL, the VGL topology should be used external mode (14h[5] = 1). The CPP should be connected to GND as the Figure 4. The definition of NAVDD leading VGL is (VGL – NAVDD) ≥ 0.3V during soft-start stage. If PAVDD < |VGL| < (PAVDD + |NAVDD|), the CPP should be connected to NAVDD as Figure 1 shown. If |VGL| > (PAVDD + |NAVDD|), changing internal mode to be external mode and using external diode structure as Figure 3 shown.

In addition, if VGL uses internal mode, it needs enough headroom to regulate the output voltage. The headroom could be calculated by below equation :

$$\text{Headroom} \geq I_{OUT\_Max} \times 12mV$$

$$|V_{GL}| < V_{PVDD} + |V_{NVDD}| - \text{Headroom}$$

Where the V_{PAVDD} is PAVDD output voltage, the V_{NAVDD} is NAVDD output voltage.

If |VGL| voltage is higher than PAVDD + |NAVDD|, it is recommended to use external mode. The register 14h[5] should be changed from 0 to 1. The VGL output voltage is also limited by PAVDD, NAVDD and V_F of external diode. The V_F of external diode is not a constant, the forward current and ambient temperature will influence the V_F, it is recommended to choose a maximum V_F value to calculate. Therefore, the VGL voltage setting should be met the below equation :

$$\text{Headroom} \geq I_{OUT\_Max} \times 12mV$$

$$|V_{GL}| < 2 \times V_{PVDD} + |V_{NVDD}| - \text{Headroom} - (V_{F\_max} \times 4)$$

Where the V_{F_max} is maximum forward voltage of diode.

VGL Soft-Start Time Setting

The VGL negative charge pump regulator has integrated soft-start function to reduce the input inrush current at power on. The soft-start time cab be adjusted by register 0Ah[2:0]. There are 8 steps for setting. The soft-start time setting range is from 3ms to 24ms and each step is about 3ms. The soft-start time default value is 9ms (0x02). The soft-start time start from the VGL voltage starting falling to the slope of soft-start cross the setting level, the period is the VGL soft-start time. Please refer to Figure 7, and register map for details.

VGL Power-on Delay Time Setting

The negative charge pump regulator has integrated a power-on sequence control. The VGL power-on delay time is adjustable by I^2C interface, there are 4 bits within register 0Ah[3:0] for setting. The setting range is from 0ms to 75ms and each step is about 5ms. The default setting is 25ms (0x05). The delay time start from the start point of PAVDD soft-start to VGL output voltage starting falling. If the VGL delay time set 0ms, the VGL soft-start need to wait PAVDD pre-charge finish, then go do soft-start. Please refer the Figure 7, and register map for detail.

VGL Output Capacitor Selection

For the best output voltage filtering, low ESR ceramic capacitors are recommended. One 4.7μF/X7R/1206 capacitors in parallel and the effective capacitance needs 4μF at least that are afford most applications. Additional capacitors can be added to improve output voltage ripple.

NAVDD Synchronous Buck-Boost Converter

The NAVDD synchronous Buck-Boost converter is high efficiency PWM architecture with programmable switching frequency. It performs fast transient responses to meet the requirement of source driver supplies for TFT-LCD display. The high operation frequency can prevent that switching frequency influence AM band range. The output voltage is controlled by a 6-bit register with 47 steps.

For VIN > 4V application, the an-synchronous topology should be applied as the Figure 6 shown. To get a better performance.

NAVDD Power-on Delay Time Setting

The NAVDD power-on delay time is adjustable by I^2C interface. There are 16 steps within 4 bits register of 0Dh. The power-on delay time setting range is from 0ms to 75ms, and each steps time is about 5ms. The delay time default value is 15ms (0x03). The delay time is from the MTP load data finish to NAVDD output voltage starting falling. Please refer the Figure 7, and register map for detail.

NAVDD Soft-Start Time Setting

The NAVDD has an internal soft-start mechanism to reduce the input inrush current. The NAVDD soft-start time can be adjusted by the register 0Eh[2:0]. There are 3 bits and 8 steps for setting. The soft-start time setting range is from 5ms to 40ms, and each step is about 5ms. The soft-start time default value is 10ms (0x01). The soft-start time starts from the NAVDD delay time counting finish. The stop point of soft-start time is NAVDD output voltage ready. Please refer to Figure 3 and register map for details.

NAVDD Output Voltage Setting

The NAVDD output voltage is adjusted by I^2C interface. User can write data into the register 01h[5:0]. There are 6 bits for output voltage adjustable, the setting range is from -5V to -7.3V, and each voltage step is about -50mV. The default value is -6.7V(0x22). Please refer the register map for detail on how to adjust the output voltage.

NAVDD Inductor Selection

The first step in design procedure is to verify whether the maximum possible output current of the buck-boost converter support the specific application requirements. To simplify the calculation, the fastest approach is to estimate converter efficiency by taking the efficiency numbers from provided efficiency curves or to use a worst case assumption for the expected efficiency, ex 75%. The calculation must be performed for the minimum assumed input voltage where the peak switch current is the highest. The inductor and internal switch have to be able to handle this current.

- Converter duty cycle :

$$D = \frac{|V_{OUT}|}{V_{IN} \times \eta \times |V_{OUT}|}$$

- Maximum output current :

$$I_{OUT} = \left(I_{PEAK} - \frac{V_{IN} \times D}{2 \times f_{OSC} \times L} \right) \times (1\text{-}D)$$

- Inductor peak current :

$$I_{PEAK} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D}{2 \times f_{OSC} \times L}$$

As for inductance, we are going to derive the transition point, there the converter toggle from CCM to DCM. We need to define the point at which the inductor current ripple touches zero, and as the power switch SW is immediately reactivated, the current ramps up again. Figure 17 portrays the input current activity of the buck-boost converter.

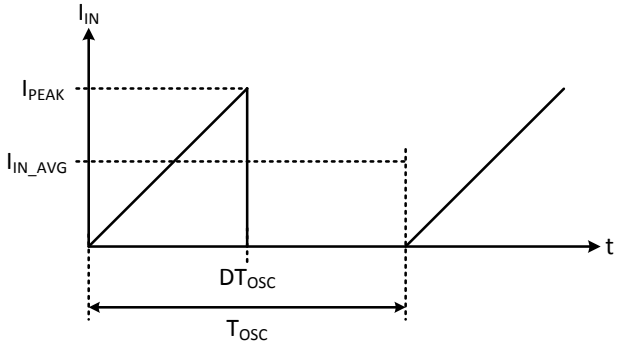


Figure 17. The Buck-boost Input Signature in BCM

The inductance can eventually be determined according to the following equation :

$$L_{critical} = \frac{|V_{OUT}| \times \eta}{2 \times f_{OSC} \times I_{OUT}} + \left(\frac{V_{IN}}{V_{IN} + |V_{OUT}|} \right)^2$$

NAVDD Output Capacitor Selection

For the best output voltage filtering, low ESR ceramic capacitors are recommended. Three 10μF/X7R/1206 capacitors in parallel and the effective capacitance needs 13μF at least that are afford most applications. Additional capacitors can be added to improve output voltage ripple.

NAVDD Current Limitation

The RTQ6749 can limit the peak current to achieve over current protection. The IC senses the inductor current during an on period. The internal P-MOSFET will be turned off if the peak inductor current reaches 1.5A (min.)

Programmable VCOM

The RTQ6749 provides the ability to reduce the flicker of an LCD Panel by adjusting the VCOM voltage during production test and alignment. The output voltage is adjusted by the I^2C interface. There are two registers to adjust the VCOM voltage, one is VCOM_C for coarse tune, and another one is VCOM_F for fine tune. It is suggested to connect a resistor 10 ohm between output pin and output capacitor for better stability.

In general application, VCOM should not be set 0V. If user don't want to use this channel, please disable it.

VCOM Power-On Delay Time Setting

The VCOM is integrated power-on sequence control. The delay time is adjustable by I^2C interface, there are 4 bits within register 0Fh[3:0]. The delay time setting range is from 0ms to 75ms, and each step is about 5ms. The default value is 25ms (0x05). The delay time start from half of PAVDD and NAVDD soft-start to VCOM output voltage starting falling. Please refer the Figure 7, and register map for detail.

VCOM_C Voltage Setting

The VCOM_C voltage is adjusted by the register 04h[7:0], it is provided 8bits resolution and 256 steps for user setting. The setting range is from 2V to −3V, each step is about 20mV. The default value is −1V (0x64). Please refer the register map for detail.

VCOM_F Voltage Setting

The VCOM_F voltage is programmable by I^2C interface, but the slave ID is different to VCOM_C, the slave ID is 0x60 and user can adjust it with "VCOM_F I^2C Write Timing Sequence". The VCOM_F is also provided 256 steps and 8 bits resolution. The default value is equal to VCOM_C setting (0x7F). From the 0x7F of VCOM_F to go up means VCOM_F voltage will be from VCOM_C voltage setting to increase with steps and each step is about 10mV. On the contrary, from the 0x7F to go down means VCOM_F voltage will be from VCOM_C voltage setting to decrease with steps. The setting range is from (VCOM_C + 1.28V) to (VCOM_C – 1.27V). Please refer the register map for detail.

RESET Voltage Detector

The voltage detector monitors the VIN voltage to generate a RESET signal from RESET pin while V_{IN} is lower than the detecting level and not latched. Both detecting level and power-on delay time could be set by I^2C interface. The detecting level could be adjusted by the register (0x12 [6:5]), it provided 4 options such as UVLO falling, 2.1V, 2.4V and 2.7V. The delay time could be set by register (0x10[3:0]), the setting range is from 0ms to 75ms, the each step is about 5ms. The delay time start from that the two conditions are achieved, one is VIN over UVLO threshold, and another one is the EN over VIH threshold, the stop point is that RESET signal goes to high.

In addition, the voltage detector also provided an option, user can chose which RESET goes low following power-off delay time or VGH channel turn off. The options can be set by the register 12h[7].

Discharge Function

The PAVDD, NAVDD, VGH, VGL and VCOM outputs voltage is integrated a discharge function. The each output voltage discharged from 100% to 30% rapidly

within 2ms at power-off, preventing phenomena such as residual image on the display at power-off. If user want to make the outputs voltage were discharged to GND level, user should add discharging resistances on the outputs. The discharge function also provided an option for user to enable or disable, the option can set by the register 12h[4:0] individually for each channel.

If the discharge function is enabled, except discharge is worked at power-off, it also be discharge at power-on. The power-on discharge start to work from UVLO and plus 1ms, until the delay time of the channel be counting finish. If the discharge function is disabled, except the power-off without discharge function, the power-on also does not have. However, the period still has discharge function from UVLO_R to MTP_LOAD_OK. The mechanism is shown in Figure 18. Beside the discharging function should be turned off at same time if the channels are unused.

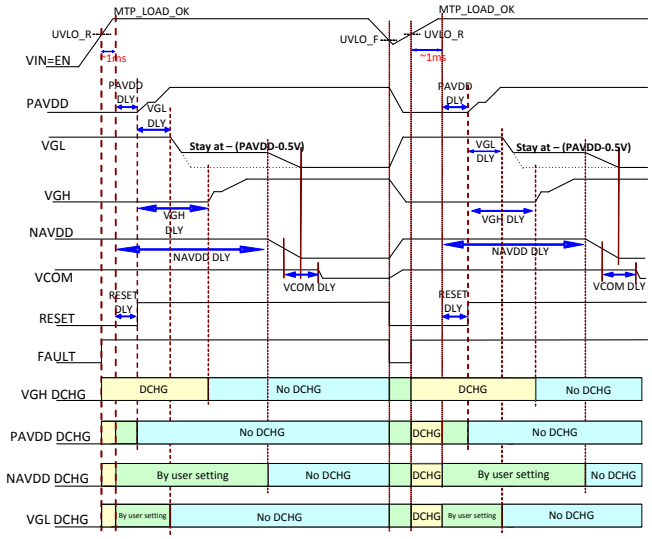


Figure 18. Discharge Function Enable Operation Mechanism

In addition, the VGL discharge function is related to the VGL topology and power-off sequence. Once VGL discharge enable, the VGL topology is recommended to use external mode as Figure 5, or the power sequence of VGL must be leading NAVDD.

Slew Rate Control

The RTQ6749 provided options for switching node slew rate adjustment with I^{2}C interface. The slew rate can be adjusted by the register 13h[7:0]. The register 13h[7:6] is for PAVDD LX falling slew rate control and there are 4 options for setting such as fast, normal, slow and slowest. The register 13h[5:4] is for NAVDD LXN rising slew rate control, the options are same as PAVDD. The register 13h[3:2] is for VGL CX1 slew rate control. The register 13h[1:0] is for VGH LXP falling slew rate control.

Power-off Delay Time Setting

The PAVDD (18h[2:0]), NAVDD (19h[2:0]), VGH (1Ah[2:0]), VGL (1Bh[2:0]) and VCOM (1Ch[2:0]) power-off delay time are adjustable by I^{2}C interface. The each output channels 8 steps within 3 bits register. The delay time setting range is from 0ms to 14ms, and each steps time is about 2ms. The each output power-off delay time default value is 0ms. The power-off delay time is from the RESET goes low to the delay counting finish. Please refer the Figure 7, and register map for detail.

Frequency Spread

The RTQ6749 is integrated a frequency spread of switching frequency function, it can reduce the noise level of the switching frequency point, it is good for EMI performance. There are 3 options for adjustment such as disabled, 3% and 6%. User can write data into the register 14h[4:3] to control the frequency spread.

FAULT Analysis Function

The RTQ6749 has provided a fault recording register that can help quickly user to know which output channel is UVP fault. If one of the output channels triggered UVP, the fault record will be saved into register 1Dh[3:0]. Then user can use I^{2}C interface to read the data of 1Dh register during the UVP is triggered. The 1Dh register will show which channel is fault.

In addition, there is an option (1Ch[3]) for clearing the record of the fault register. Users can choice that the fault record be cleared by EN going low, or VIN fall below the VIN1 UVLO_F that also can be cleared fault record.

Control Register (FFH)

The RTQ6749 provides a register for user choosing that write/read data into MTP or register. User can set the MSB of the register FFH goes to high, it means the data is written into MTP. But writing data into register don't

need to set the register FFH. In addition, reading data from MTP need to set the LSB of register FFH to high. On the contrary, reading data from register need to set LSB to low. Please refer the "I^{2}C Write/Read Timing Sequence" for detail.

Auto Refresh Functions

The RTQ6749 has integrated registers code auto recovery function if the registers code is changed abnormally. The issue could be detected with Auto Refresh Function that has provided an option to enable and disable by setting 17h[0]. The refreshing time also can be adjusted with 17h[2:1]. In addition, the FAULT pin also can be choosing pull low or not, to adjusted by 17h[3]. Please refer the register map for detail.

Table 2. Protection Behavior of Each Output Channels

Block	Protection	Work Condition	Behavior	Recovery
PAVDD	OVP	PAVDD > PAVDD x 120%	LX Stop Switching	Vout < OVP - Hys, Hys=0.5V(typ), LX switch at next clk.
	UVP	PAVDD < PAVDD x 70% and duration time is about 50ms	IC shut down and latch	1. VIN re-power up. (Duration time ≥ 50ms) 2. EN toggle again. (Duration time ≥ 50ms)
	SCP	PAVDD < PAVDD x 30%	LX stop switching, IC shutdown and latch	1. VIN re-power up. 2. EN toggle again.
NAVDD	OVP	NAVDD x120%	LXN Stop Switching	Vout < OVP-Hys, Hys=0.6V(typ), LXN switch at next clk.
	UVP	NAVDD < NAVDD x 70% and duration time is about 50ms	IC shut down and latch	1. VIN re-power up. (Duration time ≥ 50ms) 2. EN toggle again. (Duration time ≥ 50ms)
	SCP	NAVDD < NAVDD x 30%	LXN stop switching, IC shutdown and latch	1. VIN re-power up. 2. EN toggle again.
VGH	OVP	VGH > VGH x 120% VGH=30V > 36V	LXP Stop Switching	Vout < OVP-Hys, Hys=0.3V(typ), LXP switch at next clk.
	UVP	VGH < VGH x 70% and duration time is about 50ms	IC shut down and latch	1. VIN re-power up. (Duration time ≥ 50ms) 2. EN toggle again. (Duration time ≥ 50ms)
	SCP	VGH < VGH x 30%	LXP stop switching, IC shutdown and latch	1. VIN re-power up. 2. EN toggle again.
VGL	UVP	VGL < VGL x 70% and duration time is about 50ms	IC shut down and latch	1. VIN re-power up. (Duration time ≥ 50ms) 2. EN toggle again. (Duration time ≥ 50ms)
	SCP	VGL > VGL x 30%	CX1/CX2 stop switching, IC shutdown and latch	1. VIN re-power up. 2. EN toggle again.
VCOM	OCP	VCOM source/sink current > ±350mA(typ)	Clamping the output current at OCP level	After the abnormal load is removed.

Table 3. FAULT Behavior and Protections

Block	Triggering Protection	FAULT Pin Behavior	Recovery
PAVDD	OVP	High(Normal state)	--
	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low (Fault pin toggle one time)	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hys, Hys=20°C(typ)
NAVDD	OVP	High(Normal state)	--
	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hys, Hys=20°C(typ)
VGH	OVP	High(Normal state)	--
	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hys, Hys=20°C(typ)
VGL	OVP	High(Normal state)	--
	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low (The short-circuit condition needs to keep until IC re-power up at next time)	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hys, Hys=20°C(typ)
VCOM	OCP	High(Normal state)	--
	OTP	Low	IC Temperature < OTP - Hys, Hys=20°C(typ)

I²C Command

PMIC Slave Address

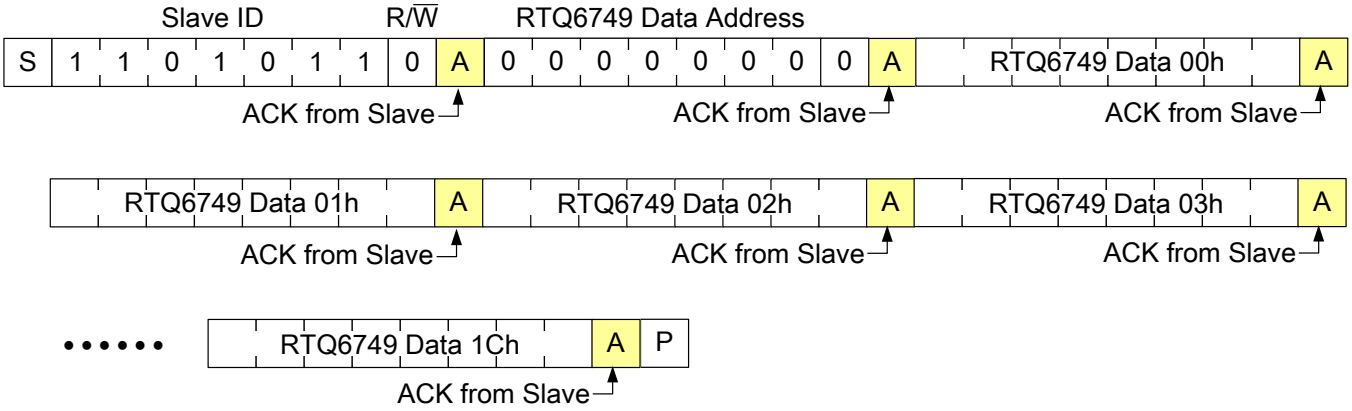
7	6	5	4	3	2	1	0 = R/W	
1	1	0	1	0	1	1	0	D6H
1	1	0	1	0	1	1	1	D7H

VCOM_F Slave Address

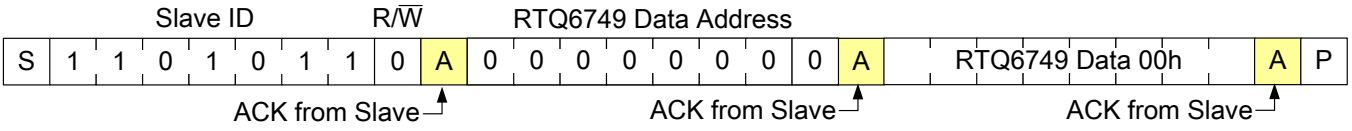
7	6	5	4	3	2	1	0 = R/W	
0	1	1	0	0	0	0	0	60H
0	1	1	0	0	0	0	1	61H

PMIC I2C Write Timing Sequence (To DAC Register)

Write Multiple Data (00h~1Ch)

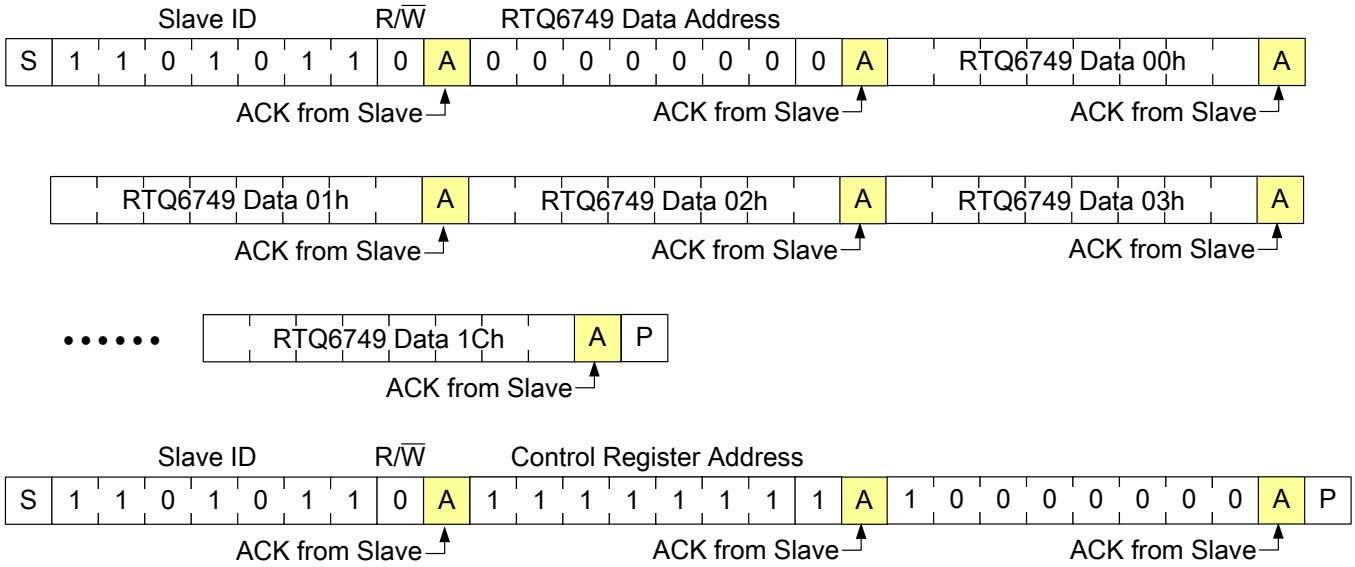


Write Single Data (00h)

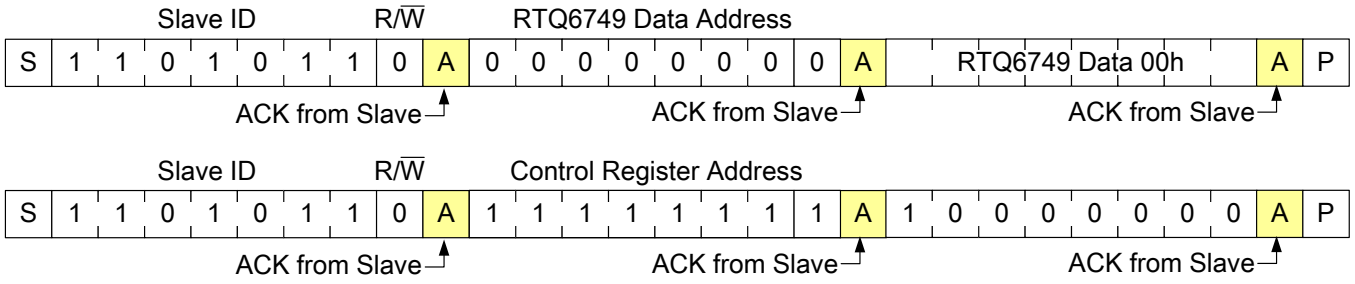


PMIC I2C Write Timing Sequence (To MTP)

Write Multiple Data (00h~1Ch)

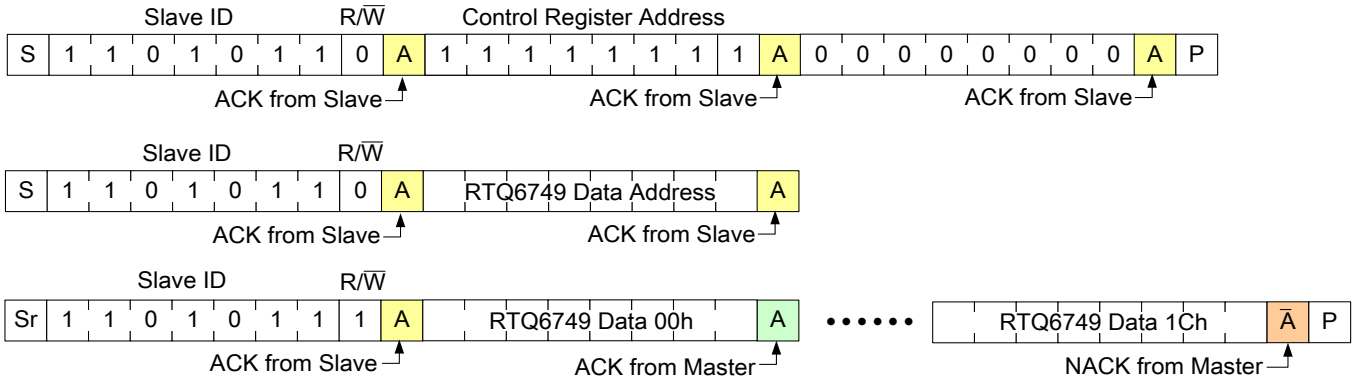


Write Single Data (00h)

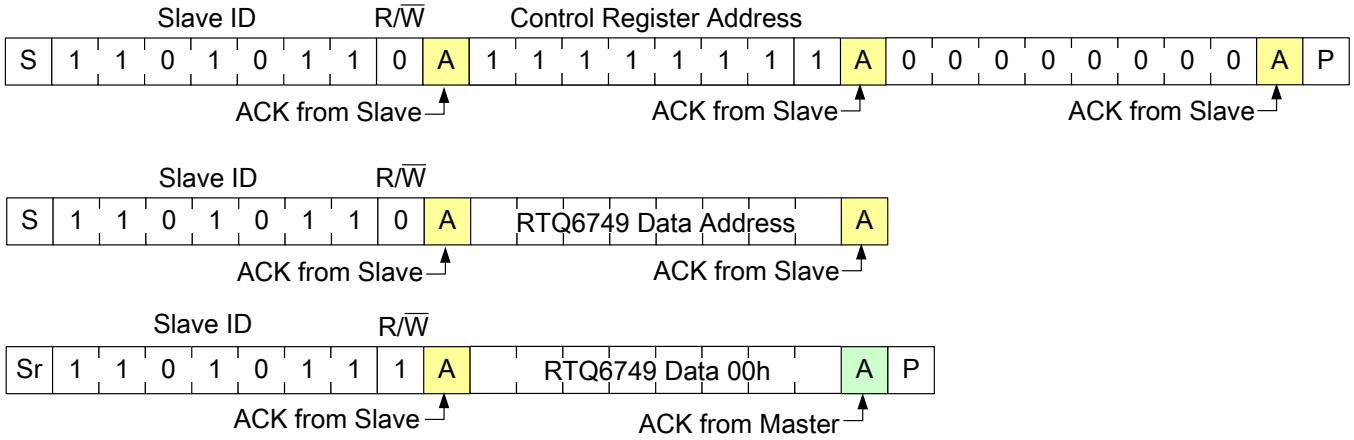


PMIC I2C Read Timing Sequence (From DAC Register)

Read Multiple Data (00h~1Ch)

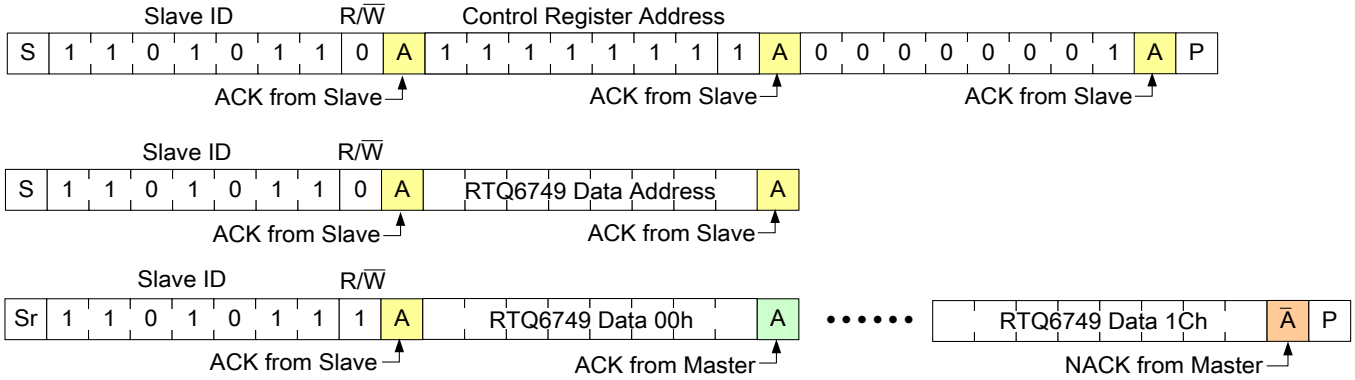


Read Single Data (00h)

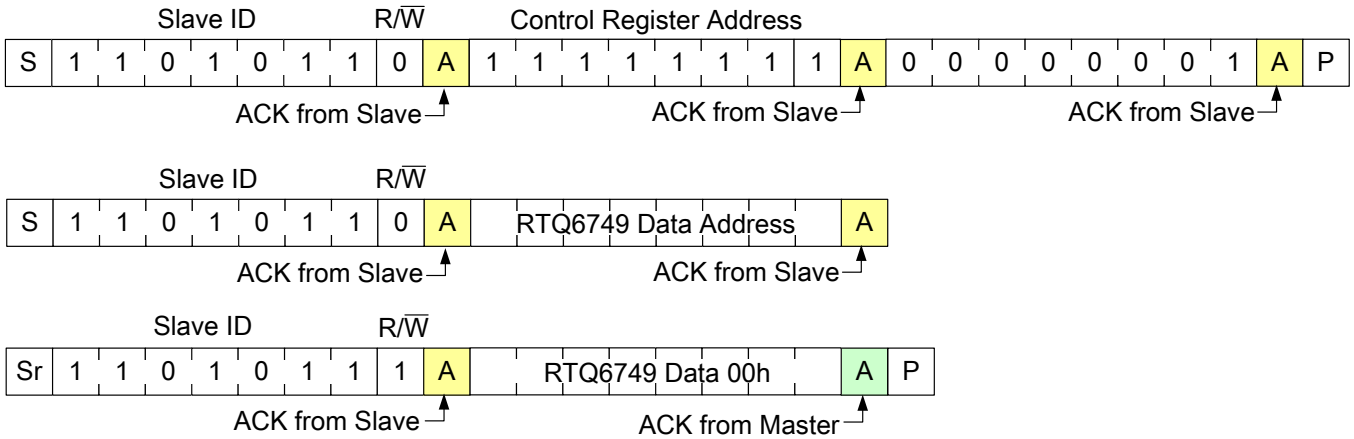


PMIC I2C Read Timing Sequence (From MTP)

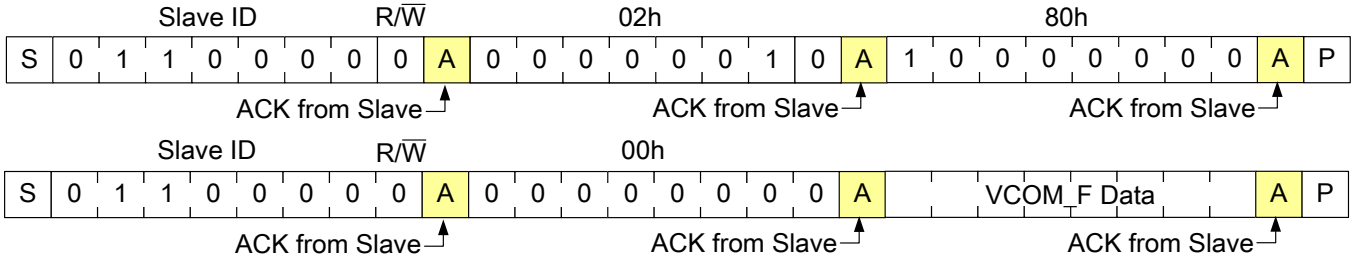
Read Multiple Data (00h~1Ch)



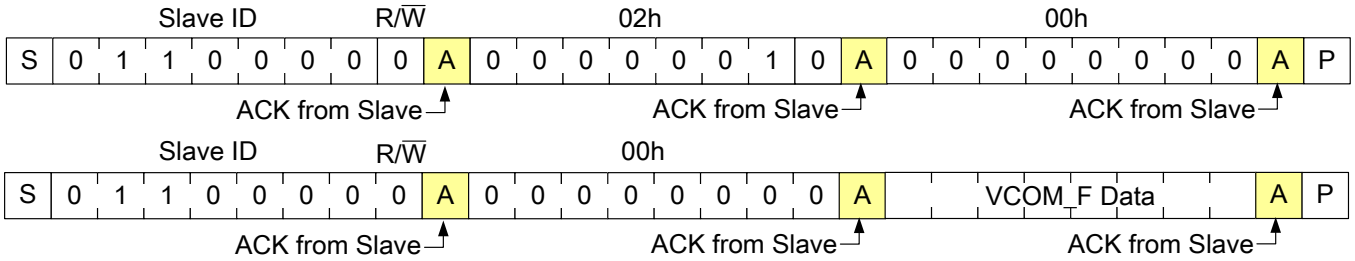
Read Single Data (00h)



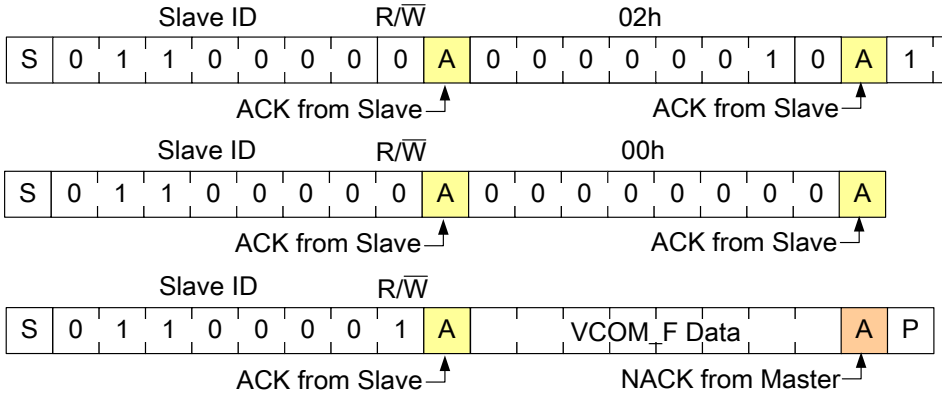
VCOM_F I2C Write Timing Sequence (To DAC Register)



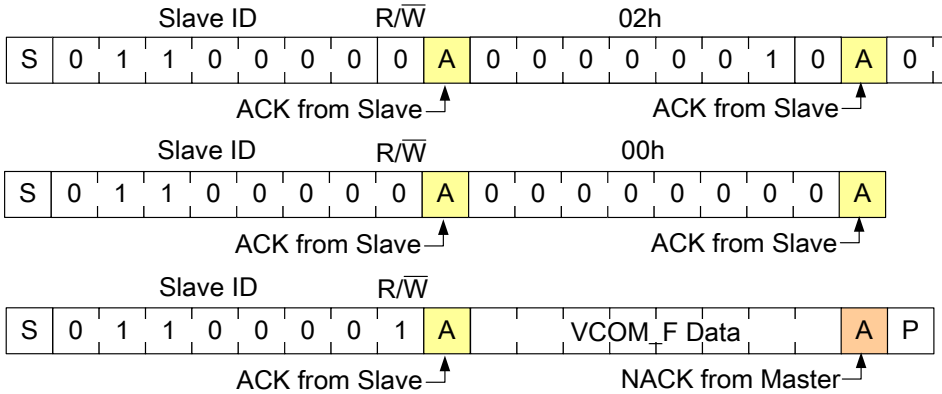
VCOM_F I2C Write Timing Sequence (To MTP & DAC Register)



VCOM_F I2C Read Timing Sequence (From DAC Register)

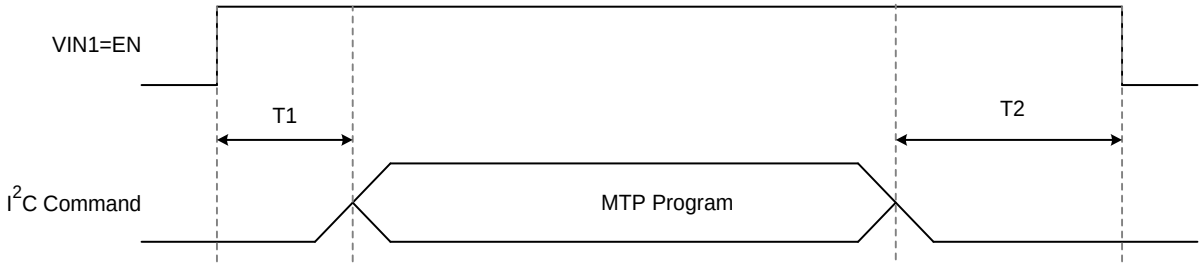


VCOM_F I2C Read Timing Sequence (From MTP)



MTP Program Sequence for Single Chip

MTP program timing sequence



Write Timing :

T1 = 50ms, T2 = 500ms

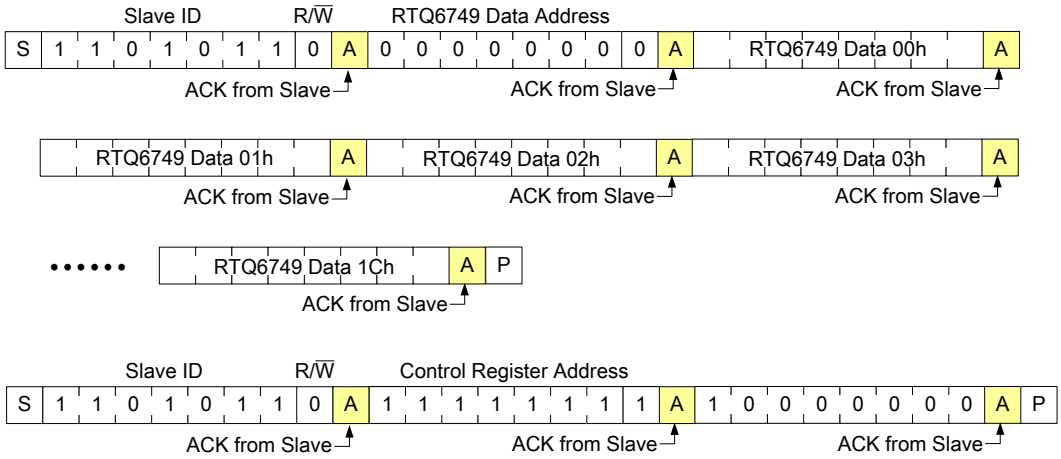
Read Timing:

T1=50ms, T2=10ms

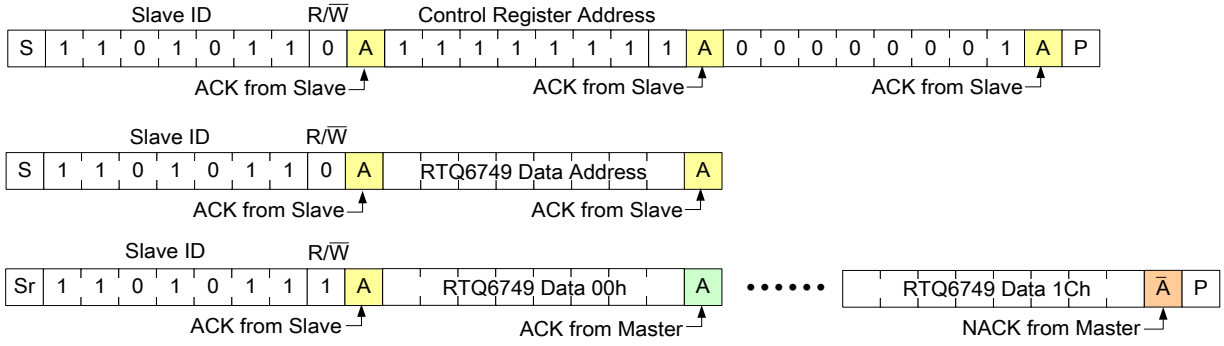
f_{SCL}=400kHz

I²C Protocol for MTP Program

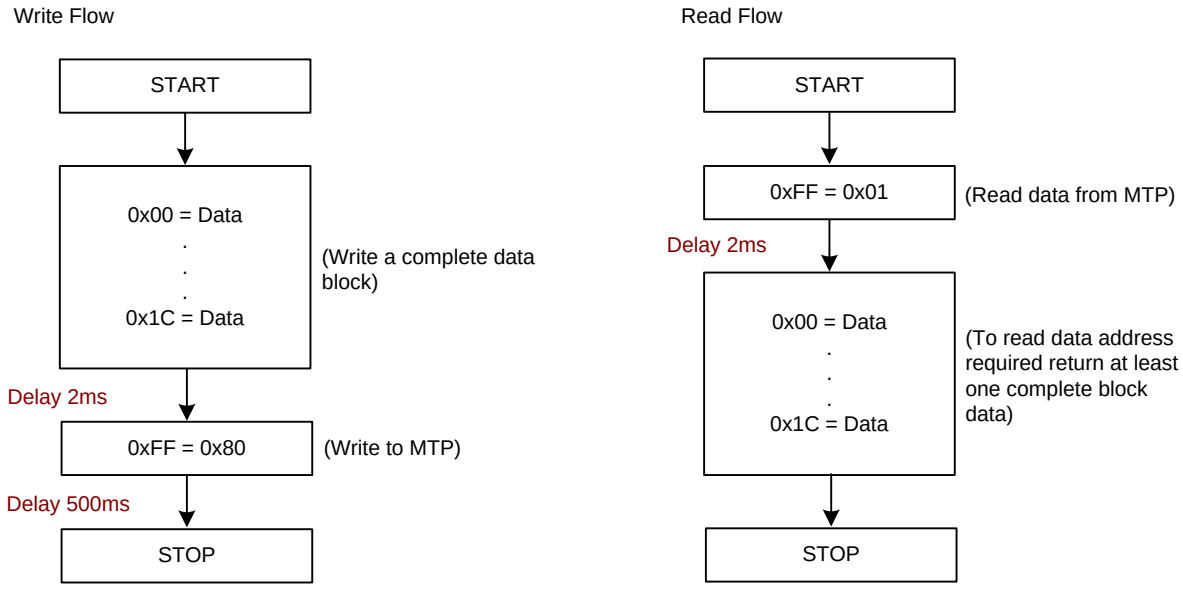
I²C Write Timing Sequence



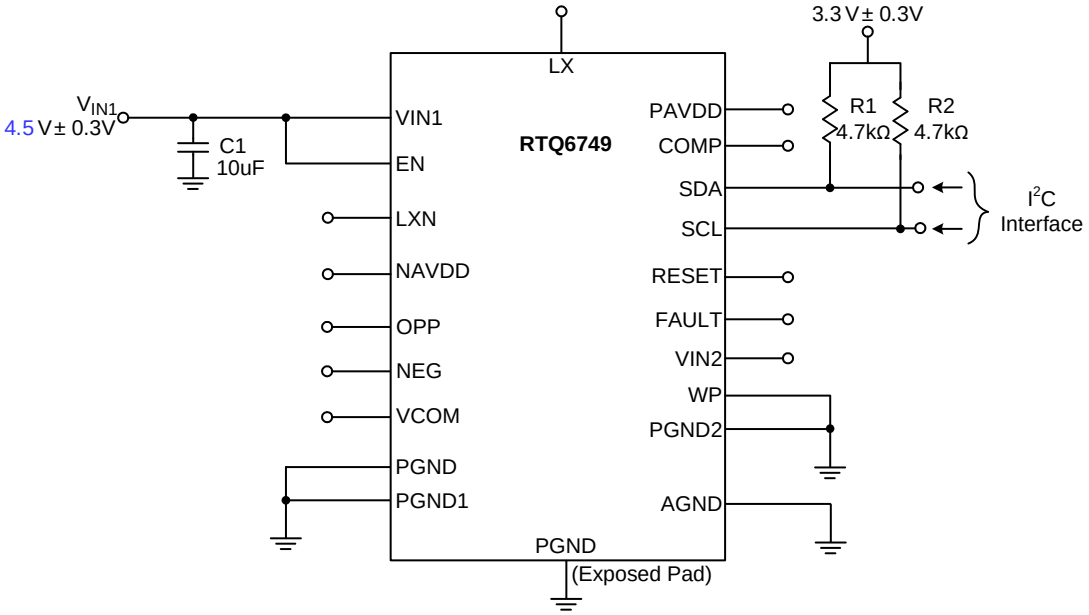
I²C Read Timing Sequence



I²C Read / Write Flow Chat

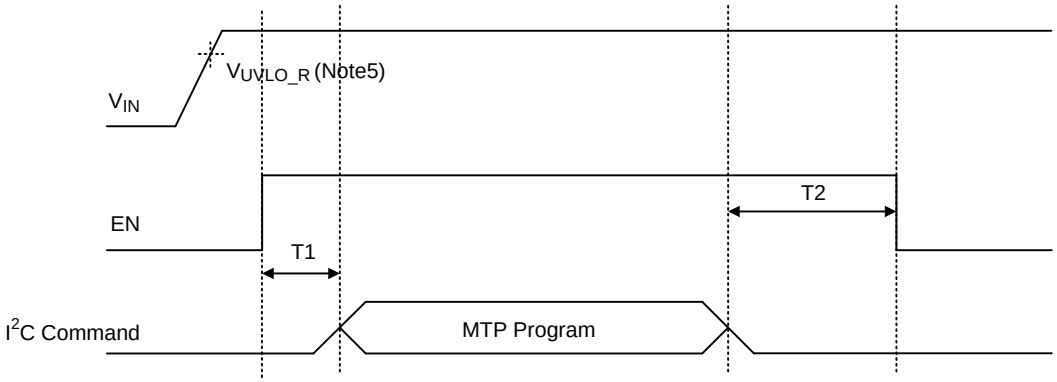


MTP Program Application Circuit for Single Chip



MTP Program Sequence on Board

MTP program timing sequence



I^2C Writing Conditions : (Note.2)

1. VIN = 3.3V ± 0.3V
2. EN = H
3. WP = L
4. All of output power ready(Note.6)

Write Timing :

VCOM_F：T1 = 60ms(Default code), T2 = 15ms (15ms wait time is required regardless of the number of rewrite bits.) (Note.1)

00h~1Ch：T1 = 60ms(Default code), T2 > 150ms (150ms wait time is required regardless of the number of rewrite bits.) (Note.1)

Read Timing :

T1 = 60ms, T2 = 10ms

MTP Program function (Note.4)

Program time

1 page = 4 bytes

MTP page program = 1 * ERASE (4 bytes) + 2 * PROGRAM (2 bytes) = 5ms + 2 * 5ms = 15ms

VCOM_F = 1 page ： 1 * 15ms = 15ms

0x00~0x1C = 10 pages ： 10 * 15ms = 150ms (Note.3)

Note.1 : T2: Add a margin according to the writing environment.

Note.2 : RTQ6749 reads default data from internal memory (MTP) at startup, and run. The customer can change the data in the internal memory via external I2C communication, but I2C communication is not possible until VIN over UVLO_R and EN = H are satisfied.

When VIN over UVLO_R, EN = H, All of output power ready, and T1 are satisfied, settings such as output voltage and delay time can be changed.

Note.3 : All data in the DAC register (existing data and rewritten data) is written to the MTP by the control register (FFH) command, so a 150ms wait time is required.

Note.4 : If the setting conditions are fixed, an IC with the setting conditions written to the MTP can be provided.

Note.5 : UVLO_R = UVLO_F + UVLO_H

Note.6 : Once the power on sequence is changed, the T1 waiting time should be changed to be PAVDD_DLY + PAVDD_SS + VGL_DLY + VGL_SS + VGH_DLY + VGH_SS + NAVDD_DLY + NAVDD_SS + VCOM_DLY + VCOM_SS(5ms)

Register Map

Items		Register Address	Resolution	Range	Default value	Step	Bit
PMIC	PAVDD[5:0]	00h	0.05V	5.0~7.3V	6.7V	47 Step	6 Bit
	NAVDD[5:0]	01h	0.05V	-5.0~-7.3V	-6.7V	47 Step	6 Bit
	VGH[5:0]	02h	0.5V	7~30V	10V	31 Step	6 Bit
	VGL[5:0]	03h	0.25V	-6V~ -18V	-10V	49 Step	6 Bit
	VCOM_C [7:0]	04h	20mV	2V~-3V	-1V	251 step	8 Bit
	VGH Low Temp. [1:0]	05h	2V	2V / 4V / 6V / 8V	2V	4 Step	2 Bit
	SW Freq.[1:0]	06h	--	600k/800k/1M/2.2M	600kHz	4 Step	2 Bit
Power On Sequence (Conrol by 2Ah[0])	PAVDD On Delay[3:0]	07h	5ms	0ms ~ 75ms	5ms	16 Step	4 Bit
	PAVDD Soft Start[2:0]	08h	5ms	5ms ~ 40ms	10ms	8 Step	3 Bit
	VGL On Delay[3:0]	09h	5ms	0ms ~ 75ms	10ms	16 Step	4 Bit
	VGL Soft Start[2:0]	0Ah	3ms	3ms ~ 24ms	6ms	8 Step	3 Bit
	VGH On Delay[3:0]	0Bh	5ms	0ms ~ 75ms	5ms	16 Step	4 Bit
	VGH Soft Start[1:0]	0Ch	5ms	5 / 10 / 15 / 20ms	10ms	4 Step	2 Bit
	NAVDD On Delay[3:0]	0Dh	5ms	0ms ~ 75ms	5ms	16 Step	4 Bit
	NAVDD Soft Start[2:0]	0Eh	5ms	5ms ~ 40ms	10ms	8 Step	3 Bit
	VCOM On Delay[3:0]	0Fh	5ms	0ms ~ 75ms	0ms	16 Step	4 Bit
	RESET On Delay[3:0]	10h	5ms	0ms ~ 75ms	5ms	16 Step	4 Bit
	Power Off Delay[3:0]	11h	3ms	0ms ~ 45ms	18ms	16 Step	4 Bit
Option1	RESET Sync option[7]	12h	--	Power Off Delay/ VGH Sync	Power Off Delay	2 Step	1 Bit
	Vin Detection[6:5]		--	UVLO Falling /2.1V/2.4V/2.7V	UVLO Falling	4 Step	2 Bit
	PAVDD D/C function[4]		--	On (0) / Off (1)	On	2 Step	1 Bit
	NAVDD D/C function[3]		--	On (0) / Off (1)	On	2 Step	1 Bit
	VGH D/C function[2]		--	On (0) / Off (1)	Off	2 Step	1 Bit
	VGL D/C function[1]		--	On (0) / Off (1)	On	2 Step	1 Bit
	VCOM D/C function[0]		--	On (0) / Off (1)	On	2 Step	1 Bit
Option2	PAVDD Slew rate[7:6]	13h	--	Fast/normal/Slow/Slowest	Normal	4 Step	2 Bit
	NAVDD Slew rate[5:4]		--	Fast/normal/Slow/Slowest	Normal	4 Step	2 Bit
	VGL Slew rate[3:2]		--	Fast/normal/Slow/Slowest	Normal	4 Step	2 Bit
	VGH Slew rate[1:0]		--	Fast/normal/Slow/Slowest	Normal	4 Step	2 Bit

Items		Register Address	Resolution	Range	Default value	Step	Bit
Option3	VGL Internal/External[5]	14h	--	Internal/External	Internal	2 Step	1 Bit
	Freq. Spread Option(EMI)[4:3]		--	Off/ +3% / +6%	Off	3 Step	2 Bit
	OTP On / Off[2]		--	On (0) / Off (1)	On	2 Step	1 Bit
	UVP On / Off[1]		--	On (0) / Off (1)	On	2 Step	1 Bit
	SCP On / Off[0]		--	On (0) / Off (1)	On	2 Step	1 Bit
	VCOM_F [7:0]	X	10mV	VCOM_C-1.27V~VCOM_C+1.28V	VCOM_C	256 step	8 Bit
Channel ON/OFF Option	RESET EN[5]	16h	--	On (1) / Off (0)	On	2 Step	1 Bit
	VCOM EN[4]		--	On (1) / Off (0)	On	2 Step	1 Bit
	NAVDD EN[3]		--	On (1) / Off (0)	On	2 Step	1 Bit
	VGH EN[2]		--	On (1) / Off (0)	On	2 Step	1 Bit
	VGL EN[1]		--	On (1) / Off (0)	On	2 Step	1 Bit
	PAVDD EN[0]		--	On (1) / Off (0)	On	2 Step	1 Bit
Auto Refresh Option	FAULT Behavior[3]	17h	--	Pull Low(0)/Not Pull Low(1)	Pull Low	2 Step	1 Bit
	Refreshing Time[2:1]		--	0.25s/0.5s/1s/2s	0.5s	4 Step	2 Bit
	AR EN[0]		--	Off (0) / On (1)	Off	2 Step	1 Bit
Power Off Sequence	PAVDD Off Delay[2:0]	18h	2ms	0ms ~ 14ms	0ms	7 step	3 Bit
	NAVDD Off Delay[2:0]	19h	2ms	0ms ~ 14ms	0ms	7 step	3 Bit
	VGH Off Delay[2:0]	1Ah	2ms	0ms ~ 14ms	0ms	7 step	3 Bit
	VGL Off Delay[2:0]	1Bh	2ms	0ms ~ 14ms	0ms	7 step	3 Bit
	FAULT Analysis Clear Option[3]	1Ch	--	Not Clear by EN go low(0) / Clear by EN go low(1)	Not Clear	2 Step	1 Bit
	VCOM Off Delay[2:0]		2ms	0ms ~ 14ms	0ms	7 step	3 Bit
Fault Analysis	PAVDD Fault[3]	1Dh	--	No Fault (0) / Fault Happen (1)	No Fault	2 Step	1 Bit
	VGL Fault[2]		--	No Fault (0) / Fault Happen (1)	No Fault	2 Step	1 Bit
	VGH Fault[1]		--	No Fault (0) / Fault Happen (1)	No Fault	2 Step	1 Bit
	NAVDD Fault[0]		--	No Fault (0) / Fault Happen (1)	No Fault	2 Step	1 Bit

Register Table

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
Data Address	00h	01h	02h	03h	04h	05h	06h
Bits	[5:0]	[5:0]	[5:0]	[5:0]	[7:0]	[1:0]	[1:0]
Min	5V	-7.3V	7V	-18V	-3V	2V	600kHz
Max	7.3V	-5V	30V	-6V	2V	8V	2.2MHz
Default	22h	22h	06h	10h	64h	00h	00h
Resolution	50mV	50mV	0.5V	0.25V	20mV	2V	-
0H	5.00V	-5.00V	7.0V	-6.00V	-3.00V	2.0V	600kHz
1H	5.05V	-5.05V	7.5V	-6.25V	-2.98V	4.0V	800kHz
2H	5.10V	-5.10V	8.0V	-6.50V	-2.96V	6.0V	1MHz
3H	5.15V	-5.15V	8.5V	-6.75V	-2.94V	8.0V	2.2MHz
4H	5.20V	-5.20V	9.0V	-7.00V	-2.92V		
5H	5.25V	-5.25V	9.5V	-7.25V	-2.90V		
6H	5.30V	-5.30V	10.0V	-7.50V	-2.88V		
7H	5.35V	-5.35V	10.5V	-7.75V	-2.86V		
8H	5.40V	-5.40V	11.0V	-8.00V	-2.84V		
9H	5.45V	-5.45V	11.5V	-8.25V	-2.82V		
AH	5.50V	-5.50V	12.0V	-8.50V	-2.80V		
BH	5.55V	-5.55V	12.5V	-8.75V	-2.78V		
CH	5.60V	-5.60V	13.0V	-9.00V	-2.76V		
DH	5.65V	-5.65V	13.5V	-9.25V	-2.74V		
EH	5.70V	-5.70V	14.0V	-9.50V	-2.72V		
FH	5.75V	-5.75V	14.5V	-9.75V	-2.70V		
10H	5.80V	-5.80V	15.0V	-10.00V	-2.68V		
11H	5.85V	-5.85V	15.5V	-10.25V	-2.66V		
12H	5.90V	-5.90V	16.0V	-10.50V	-2.64V		
13H	5.95V	-5.95V	16.5V	-10.75V	-2.62V		
14H	6.00V	-6.00V	17.0V	-11.00V	-2.60V		
15H	6.05V	-6.05V	17.5V	-11.25V	-2.58V		
16H	6.10V	-6.10V	18.0V	-11.50V	-2.56V		
17H	6.15V	-6.15V	18.5V	-11.75V	-2.54V		
18H	6.20V	-6.20V	19.0V	-12.00V	-2.52V		
19H	6.25V	-6.25V	19.5V	-12.25V	-2.50V		
1AH	6.30V	-6.30V	20.0V	-12.50V	-2.48V		
1BH	6.35V	-6.35V	20.5V	-12.75V	-2.46V		
1CH	6.40V	-6.40V	21.0V	-13.00V	-2.44V		
1DH	6.45V	-6.45V	21.5V	-13.25V	-2.42V		
1EH	6.50V	-6.50V	22.0V	-13.50V	-2.40V		
1FH	6.55V	-6.55V	22.5V	-13.75V	-2.38V		
20H	6.60V	-6.60V	23.0V	-14.00V	-2.36V		
21H	6.65V	-6.65V	23.5V	-14.25V	-2.34V		
22H	6.70V	-6.70V	24.0V	-14.50V	-2.32V		
23H	6.75V	-6.75V	24.5V	-14.75V	-2.30V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
24H	6.80V	-6.80V	25.0V	-15.00V	-2.28V		
25H	6.85V	-6.85V	25.5V	-15.25V	-2.26V		
26H	6.90V	-6.90V	26.0V	-15.50V	-2.24V		
27H	6.95V	-6.95V	26.5V	-15.75V	-2.22V		
28H	7.00V	-7.00V	27.0V	-16.00V	-2.20V		
29H	7.05V	-7.05V	27.5V	-16.25V	-2.18V		
2AH	7.10V	-7.10V	28.0V	-16.50V	-2.16V		
2BH	7.15V	-7.15V	28.5V	-16.75V	-2.14V		
2CH	7.20V	-7.20V	29.0V	-17.00V	-2.12V		
2DH	7.25V	-7.25V	29.5V	-17.25V	-2.10V		
2EH	7.30V	-7.30V	30.0V	-17.50V	-2.08V		
2FH				-17.75V	-2.06V		
30H				-18.00V	-2.04V		
31H					-2.02V		
32H					-2.00V		
33H					-1.98V		
34H					-1.96V		
35H					-1.94V		
36H					-1.92V		
37H					-1.90V		
38H					-1.88V		
39H					-1.86V		
3AH					-1.84V		
3BH					-1.82V		
3CH					-1.80V		
3DH					-1.78V		
3EH					-1.76V		
3FH					-1.74V		
40H					-1.72V		
41H					-1.70V		
42H					-1.68V		
43H					-1.66V		
44H					-1.64V		
45H					-1.62V		
46H					-1.60V		
47H					-1.58V		
48H					-1.56V		
49H					-1.54V		
4AH					-1.52V		
4BH					-1.50V		
4CH					-1.48V		
4DH					-1.46V		
4EH					-1.44V		
4FH					-1.42V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
50H					-1.40V		
51H					-1.38V		
52H					-1.36V		
53H					-1.34V		
54H					-1.32V		
55H					-1.30V		
56H					-1.28V		
57H					-1.26V		
58H					-1.24V		
59H					-1.22V		
5AH					-1.20V		
5BH					-1.18V		
5CH					-1.16V		
5DH					-1.14V		
5EH					-1.12V		
5FH					-1.10V		
60H					-1.08V		
61H					-1.06V		
62H					-1.04V		
63H					-1.02V		
64H					-1.00V		
65H					-0.98V		
66H					-0.96V		
67H					-0.94V		
68H					-0.92V		
69H					-0.90V		
6AH					-0.88V		
6BH					-0.86V		
6CH					-0.84V		
6DH					-0.82V		
6EH					-0.80V		
6FH					-0.78V		
70H					-0.76V		
71H					-0.74V		
72H					-0.72V		
73H					-0.70V		
74H					-0.68V		
75H					-0.66V		
76H					-0.64V		
77H					-0.62V		
78H					-0.60V		
79H					-0.58V		
7AH					-0.56V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
7BH					-0.54V		
7CH					-0.52V		
7DH					-0.50V		
7EH					-0.48V		
7FH					-0.46V		
80H					-0.44V		
81H					-0.42V		
82H					-0.40V		
83H					-0.38V		
84H					-0.36V		
85H					-0.34V		
86H					-0.32V		
87H					-0.30V		
88H					-0.28V		
89H					-0.26V		
8AH					-0.24V		
8BH					-0.22V		
8CH					-0.20V		
8DH					-0.18V		
8EH					-0.16V		
8FH					-0.14V		
90H					-0.12V		
91H					-0.10V		
92H					-0.08V		
93H					-0.06V		
94H					-0.04V		
95H					-0.02V		
96H					0.00V		
97H					0.02V		
98H					0.04V		
99H					0.06V		
9AH					0.08V		
9BH					0.10V		
9CH					0.12V		
9DH					0.14V		
9EH					0.16V		
9FH					0.18V		
A0H					0.20V		
A1H					0.22V		
A2H					0.24V		
A3H					0.26V		
A4H					0.28V		
A5H					0.30V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
A6H					0.32V		
A7H					0.34V		
A8H					0.36V		
A9H					0.38V		
AAH					0.40V		
ABH					0.42V		
ACH					0.44V		
ADH					0.46V		
AEH					0.48V		
AFH					0.50V		
B0H					0.52V		
B1H					0.54V		
B2H					0.56V		
B3H					0.58V		
B4H					0.60V		
B5H					0.62V		
B6H					0.64V		
B7H					0.66V		
B8H					0.68V		
B9H					0.70V		
BAH					0.72V		
BBH					0.74V		
BCH					0.76V		
BDH					0.78V		
BEH					0.80V		
BFH					0.82V		
C0H					0.84V		
C1H					0.86V		
C2H					0.88V		
C3H					0.90V		
C4H					0.92V		
C5H					0.94V		
C6H					0.96V		
C7H					0.98V		
C8H					1.00V		
C9H					1.02V		
CAH					1.04V		
CBH					1.06V		
CCH					1.08V		
CDH					1.10V		
CEH					1.12V		
CFH					1.14V		
D0H					1.16V		

	PMIC						
	PAVDD	NAVDD	VGH	VGL	VCOM_C	VGH Low Temp	Switching Frequency
D1H					1.18V		
D2H					1.20V		
D3H					1.22V		
D4H					1.24V		
D5H					1.26V		
D6H					1.28V		
D7H					1.30V		
D8H					1.32V		
D9H					1.34V		
DAH					1.36V		
DBH					1.38V		
DCH					1.40V		
DDH					1.42V		
DEH					1.44V		
DFH					1.46V		
E0H					1.48V		
E1H					1.50V		
E2H					1.52V		
E3H					1.54V		
E4H					1.56V		
E5H					1.58V		
E6H					1.60V		
E7H					1.62V		
E8H					1.64V		
E9H					1.66V		
EAH					1.68V		
EBH					1.70V		
ECH					1.72V		
EDH					1.74V		
EEH					1.76V		
EFH					1.78V		
F0H					1.80V		
F1H					1.82V		
F2H					1.84V		
F3H					1.86V		
F4H					1.88V		
F5H					1.90V		
F6H					1.92V		
F7H					1.94V		
F8H					1.96V		
F9H					1.98V		
FAH					2.00V		

		Power On Sequence										
		PAVDD On Delay Time	PAVDD Soft-start Time	VGL On Delay Time	VGL Soft-start Time	VGH On Delay Time	VGH Soft-start Time	NAVDD On Delay Time	NAVDD Soft-start Time	VCOM On Delay Time	RESET On Delay Time	Power Off Delay Time
Data Address		07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h
Bits		[3:0]	[2:0]	[3:0]	[2:0]	[3:0]	[1:0]	[3:0]	[2:0]	[3:0]	[3:0]	[3:0]
Min		0ms	5ms	0ms	3ms	0ms	5ms	0ms	5ms	0ms	0ms	0ms
Max		75ms	40ms	75ms	24ms	75ms	20ms	75ms	40ms	75ms	75ms	45ms
Default		01h	01h	02h	01h	04h	01h	08h	01h	02h	01h	06h
Resolution		5ms	5ms	5ms	3ms	5ms	5ms	5ms	5ms	5ms	5ms	3ms
0H		0ms	5ms	0ms	3ms	0ms	5ms	0ms	5ms	0ms	0ms	0ms
1H		5ms	10ms	5ms	6ms	5ms	10ms	5ms	10ms	5ms	5ms	3ms
2H		10ms	15ms	10ms	9ms	10ms	15ms	10ms	15ms	10ms	10ms	6ms
3H		15ms	20ms	15ms	12ms	15ms	20ms	15ms	20ms	15ms	15ms	9ms
4H		20ms	25ms	20ms	15ms	20ms		20ms	25ms	20ms	20ms	12ms
5H		25ms	30ms	25ms	18ms	25ms		25ms	30ms	25ms	25ms	15ms
6H		30ms	35ms	30ms	21ms	30ms		30ms	35ms	30ms	30ms	18ms
7H		35ms	40ms	35ms	24ms	35ms		35ms	40ms	35ms	35ms	21ms
8H		40ms		40ms		40ms		40ms		40ms	40ms	24ms
9H		45ms		45ms		45ms		45ms		45ms	45ms	27ms
AH		50ms		50ms		50ms		50ms		50ms	50ms	30ms
BH		55ms		55ms		55ms		55ms		55ms	55ms	33ms
CH		60ms		60ms		60ms		60ms		60ms	60ms	36ms
DH		65ms		65ms		65ms		65ms		65ms	65ms	39ms
EH		70ms		70ms		70ms		70ms		70ms	70ms	42ms
FH		75ms		75ms		75ms		75ms		75ms	75ms	45ms

	Option 1						
	RESET Sync Option	VIN Detection	PAVDD Discharge Function	NAVDD Discharge Function	VGH Discharge Function	VGL Discharge Function	VCOM Discharge Function
Data Address	12h						
Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Min	-	-	-	-	-	-	-
Max	-	-	-	-	-	-	-
Default	00h	00h	00h	00h	01h	01h	00h
Resolution	-	-	-	-	-	-	-
0H	Power off Delay	UVLO Falling	On	On	On	On	On
1H	VGH Sync	2.1V	Off	Off	Off	Off	Off
2H		2.4V					
3H		2.7V					

	Option 2				Option 3				
	PAVDD Slew Rate	NAVDD Slew Rate	VGL Slew Rate	VGH Slew Rate	VGL Internal/External Option	Freq. Spread Option(EMI)	OTP	UVP	SCP
Data Address	13h				14h				
Bits	[7:6]	[5:4]	[3:2]	[1:0]	[5]	[4:3]	[2]	[1]	[0]
Min	Slowest	Slowest	Slowest	Slowest	-	Off	-	-	-
Max	Fast	Fast	Fast	Fast	-	6%	-	-	-
Default	01h	01h	01h	01h	00h	00h	00h	00h	00h
Resolution	-	-	-	-	-	3%	-	-	-
0H	Fast	Fast	Fast	Fast	Internal	Off	On	On	On
1H	Normal	Normal	Normal	Normal	External	3%	Off	Off	Off
2H	Slow	Slow	Slow	Slow		6%			
3H	Slowest	Slowest	Slowest	Slowest					

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
Data Address	X	16h						17h		
Bits	[7:0]	[5]	[4]	[3]	[2]	[1]	[0]	[3]	[2:1]	[0]
Min	VCOM_C-1.27V	-	-	-	-	-	-	-	-	-
Max	VCOM_C+1.28V	-	-	-	-	-	-	-	-	-
Default	08h	01h	01h	01h	01h	01h	01h	00h	01h	00h
Resolution	10mV	-	-	-	-	-	-	-	-	-
0H	VCOM_C-1.27V	Off	Off	Off	Off	Off	Off	FAULT not pull low	0.25s	Off
1H	VCOM_C-1.26V	On	On	On	On	On	On	FAULT pull low	0.50s	On
2H	VCOM_C-1.25V								1.00s	
3H	VCOM_C-1.24V								2.00s	
4H	VCOM_C-1.23V									
5H	VCOM_C-1.22V									
6H	VCOM_C-1.21V									
7H	VCOM_C-1.20V									
8H	VCOM_C-1.19V									
9H	VCOM_C-1.18V									
AH	VCOM_C-1.17V									
BH	VCOM_C-1.16V									
CH	VCOM_C-1.15V									
DH	VCOM_C-1.14V									
EH	VCOM_C-1.13V									
FH	VCOM_C-1.12V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
10H	VCOM_C-1.11V									
11H	VCOM_C-1.10V									
12H	VCOM_C-1.09V									
13H	VCOM_C-1.08V									
14H	VCOM_C-1.07V									
15H	VCOM_C-1.06V									
16H	VCOM_C-1.05V									
17H	VCOM_C-1.04V									
18H	VCOM_C-1.03V									
19H	VCOM_C-1.02V									
1AH	VCOM_C-1.01V									
1BH	VCOM_C-1.00V									
1CH	VCOM_C-0.99V									
1DH	VCOM_C-0.98V									
1EH	VCOM_C-0.97V									
1FH	VCOM_C-0.96V									
20H	VCOM_C-0.95V									
21H	VCOM_C-0.94V									
22H	VCOM_C-0.93V									
23H	VCOM_C-0.92V									
24H	VCOM_C-0.91V									
25H	VCOM_C-0.90V									
26H	VCOM_C-0.89V									
27H	VCOM_C-0.88V									
28H	VCOM_C-0.87V									
29H	VCOM_C-0.86V									
2AH	VCOM_C-0.85V									
2BH	VCOM_C-0.84V									
2CH	VCOM_C-0.83V									
2DH	VCOM_C-0.82V									
2EH	VCOM_C-0.81V									
2FH	VCOM_C-0.80V									
30H	VCOM_C-0.79V									
31H	VCOM_C-0.78V									
32H	VCOM_C-0.77V									
33H	VCOM_C-0.76V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
34H	VCOM_C-0.75V									
35H	VCOM_C-0.74V									
36H	VCOM_C-0.73V									
37H	VCOM_C-0.72V									
38H	VCOM_C-0.71V									
39H	VCOM_C-0.70V									
3AH	VCOM_C-0.69V									
3BH	VCOM_C-0.68V									
3CH	VCOM_C-0.67V									
3DH	VCOM_C-0.66V									
3EH	VCOM_C-0.65V									
3FH	VCOM_C-0.64V									
40H	VCOM_C-0.63V									
41H	VCOM_C-0.62V									
42H	VCOM_C-0.61V									
43H	VCOM_C-0.60V									
44H	VCOM_C-0.59V									
45H	VCOM_C-0.58V									
46H	VCOM_C-0.57V									
47H	VCOM_C-0.56V									
48H	VCOM_C-0.55V									
49H	VCOM_C-0.54V									
4AH	VCOM_C-0.53V									
4BH	VCOM_C-0.52V									
4CH	VCOM_C-0.51V									
4DH	VCOM_C-0.50V									
4EH	VCOM_C-0.49V									
4FH	VCOM_C-0.48V									
50H	VCOM_C-0.47V									
51H	VCOM_C-0.46V									
52H	VCOM_C-0.45V									
53H	VCOM_C-0.44V									
54H	VCOM_C-0.43V									
55H	VCOM_C-0.42V									
56H	VCOM_C-0.41V									
57H	VCOM_C-0.40V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
58H	VCOM_C-0.39V									
59H	VCOM_C-0.38V									
5AH	VCOM_C-0.37V									
5BH	VCOM_C-0.36V									
5CH	VCOM_C-0.35V									
5DH	VCOM_C-0.34V									
5EH	VCOM_C-0.33V									
5FH	VCOM_C-0.32V									
60H	VCOM_C-0.31V									
61H	VCOM_C-0.30V									
62H	VCOM_C-0.29V									
63H	VCOM_C-0.28V									
64H	VCOM_C-0.27V									
65H	VCOM_C-0.26V									
66H	VCOM_C-0.25V									
67H	VCOM_C-0.24V									
68H	VCOM_C-0.23V									
69H	VCOM_C-0.22V									
6AH	VCOM_C-0.21V									
6BH	VCOM_C-0.20V									
6CH	VCOM_C-0.19V									
6DH	VCOM_C-0.18V									
6EH	VCOM_C-0.17V									
6FH	VCOM_C-0.16V									
70H	VCOM_C-0.15V									
71H	VCOM_C-0.14V									
72H	VCOM_C-0.13V									
73H	VCOM_C-0.12V									
74H	VCOM_C-0.11V									
75H	VCOM_C-0.10V									
76H	VCOM_C-0.09V									
77H	VCOM_C-0.08V									
78H	VCOM_C-0.07V									
79H	VCOM_C-0.06V									
7AH	VCOM_C-0.05V									
7BH	VCOM_C-0.04V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
7CH	VCOM_C-0.03V									
7DH	VCOM_C-0.02V									
7EH	VCOM_C-0.01V									
7FH	VCOM_C									
80H	VCOM_C+0.01V									
81H	VCOM_C+0.02V									
82H	VCOM_C+0.03V									
83H	VCOM_C+0.04V									
84H	VCOM_C+0.05V									
85H	VCOM_C+0.06V									
86H	VCOM_C+0.07V									
87H	VCOM_C+0.08V									
88H	VCOM_C+0.09V									
89H	VCOM_C+0.10V									
8AH	VCOM_C+0.11V									
8BH	VCOM_C+0.12V									
8CH	VCOM_C+0.13V									
8DH	VCOM_C+0.14V									
8EH	VCOM_C+0.15V									
8FH	VCOM_C+0.16V									
90H	VCOM_C+0.17V									
91H	VCOM_C+0.18V									
92H	VCOM_C+0.19V									
93H	VCOM_C+0.20V									
94H	VCOM_C+0.21V									
95H	VCOM_C+0.22V									
96H	VCOM_C+0.23V									
97H	VCOM_C+0.24V									
98H	VCOM_C+0.25V									
99H	VCOM_C+0.26V									
9AH	VCOM_C+0.27V									
9BH	VCOM_C+0.28V									
9CH	VCOM_C+0.29V									
9DH	VCOM_C+0.30V									
9EH	VCOM_C+0.31V									
9FH	VCOM_C+0.32V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
A0H	VCOM_C+0.33V									
A1H	VCOM_C+0.34V									
A2H	VCOM_C+0.35V									
A3H	VCOM_C+0.36V									
A4H	VCOM_C+0.37V									
A5H	VCOM_C+0.38V									
A6H	VCOM_C+0.39V									
A7H	VCOM_C+0.40V									
A8H	VCOM_C+0.41V									
A9H	VCOM_C+0.42V									
AAH	VCOM_C+0.43V									
ABH	VCOM_C+0.44V									
ACH	VCOM_C+0.45V									
ADH	VCOM_C+0.46V									
AEH	VCOM_C+0.47V									
AFH	VCOM_C+0.48V									
B0H	VCOM_C+0.49V									
B1H	VCOM_C+0.50V									
B2H	VCOM_C+0.51V									
B3H	VCOM_C+0.52V									
B4H	VCOM_C+0.53V									
B5H	VCOM_C+0.54V									
B6H	VCOM_C+0.55V									
B7H	VCOM_C+0.56V									
B8H	VCOM_C+0.57V									
B9H	VCOM_C+0.58V									
BAH	VCOM_C+0.59V									
BBH	VCOM_C+0.60V									
BCH	VCOM_C+0.61V									
BDH	VCOM_C+0.62V									
BEH	VCOM_C+0.63V									
BFH	VCOM_C+0.64V									
C0H	VCOM_C+0.65V									
C1H	VCOM_C+0.66V									
C2H	VCOM_C+0.67V									
C3H	VCOM_C+0.68V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
C4H	VCOM_C+0.69V									
C5H	VCOM_C+0.70V									
C6H	VCOM_C+0.71V									
C7H	VCOM_C+0.72V									
C8H	VCOM_C+0.73V									
C9H	VCOM_C+0.74V									
CAH	VCOM_C+0.75V									
CBH	VCOM_C+0.76V									
CCH	VCOM_C+0.77V									
CDH	VCOM_C+0.78V									
CEH	VCOM_C+0.79V									
CFH	VCOM_C+0.80V									
D0H	VCOM_C+0.81V									
D1H	VCOM_C+0.82V									
D2H	VCOM_C+0.83V									
D3H	VCOM_C+0.84V									
D4H	VCOM_C+0.85V									
D5H	VCOM_C+0.86V									
D6H	VCOM_C+0.87V									
D7H	VCOM_C+0.88V									
D8H	VCOM_C+0.89V									
D9H	VCOM_C+0.90V									
DAH	VCOM_C+0.91V									
DBH	VCOM_C+0.92V									
DCH	VCOM_C+0.93V									
DDH	VCOM_C+0.94V									
DEH	VCOM_C+0.95V									
DFH	VCOM_C+0.96V									
E0H	VCOM_C+0.97V									
E1H	VCOM_C+0.98V									
E2H	VCOM_C+0.99V									
E3H	VCOM_C+1.00V									
E4H	VCOM_C+1.01V									
E5H	VCOM_C+1.02V									
E6H	VCOM_C+1.03V									
E7H	VCOM_C+1.04V									

		Channel ON/OFF Option						Auto Refresh Option		
	VCOM_F	RESET EN	VCOM EN	NAVDD EN	VGH EN	VGL EN	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
E8H	VCOM_C+1.05V									
E9H	VCOM_C+1.06V									
EAH	VCOM_C+1.07V									
EBH	VCOM_C+1.08V									
ECH	VCOM_C+1.09V									
EDH	VCOM_C+1.10V									
EEH	VCOM_C+1.11V									
EFH	VCOM_C+1.12V									
F0H	VCOM_C+1.13V									
F1H	VCOM_C+1.14V									
F2H	VCOM_C+1.15V									
F3H	VCOM_C+1.16V									
F4H	VCOM_C+1.17V									
F5H	VCOM_C+1.18V									
F6H	VCOM_C+1.19V									
F7H	VCOM_C+1.20V									
F8H	VCOM_C+1.21V									
F9H	VCOM_C+1.22V									
FAH	VCOM_C+1.23V									
FBH	VCOM_C+1.24V									
FCH	VCOM_C+1.25V									
FDH	VCOM_C+1.26V									
FEH	VCOM_C+1.27V									
FFH	VCOM_C+1.28V									

	Power Off Sequence					
	PAVDD Off Delay Time	NAVDD Off Delay Time	VGH Off Delay Time	VGL Off Delay Time	FAULT Analysis Clear Option	VCOM Off Delay Time
Data Address	18h	19h	1Ah	1Bh	1Ch	
Bits	[2:0]	[2:0]	[2:0]	[2:0]	[3]	[2:0]
Min	0ms	0ms	0ms	0ms	-	0ms
Max	14ms	14ms	14ms	14ms	-	14ms
Default	00h	00h	00h	00h	00h	00h
Resolution	2ms	2ms	2ms	2ms	-	2ms
0H	0ms	0ms	0ms	0ms	Not Clear	0ms
1H	2ms	2ms	2ms	2ms	Clear	2ms
2H	4ms	4ms	4ms	4ms		4ms
3H	6ms	6ms	6ms	6ms		6ms
4H	8ms	8ms	8ms	8ms		8ms
5H	10ms	10ms	10ms	10ms		10ms
6H	12ms	12ms	12ms	12ms		12ms
7H	14ms	14ms	14ms	14ms		14ms

	FAULT Analysis(DAC)			
	PAVDD FAULT	VGL FAULT	VGH FAULT	NAVDD FAULT
Data Address	1Dh			
Bits	[3]	[2]	[1]	[0]
Min	-	-	-	-
Max	-	-	-	-
Default	00h	00h	00h	00h
Resolution	-	-	-	-
0H	No Fault	No Fault	No Fault	No Fault
1H	Happen	Happen	Happen	Happen

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-32L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / 27.5°C/W) = 3.63W for a WQFN-32L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 19 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

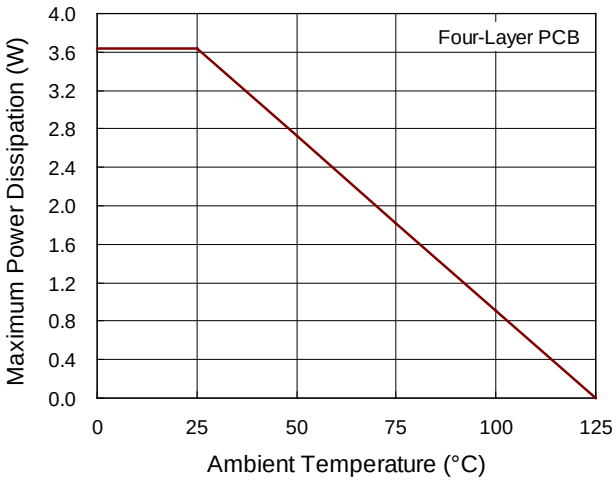


Figure 19. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RTQ6749-QT. The following descriptions are the guidelines for better PCB layout :

- The power components such as inductor (L1, L2, L3), fly cap (C14), input cap(C1, C2, C3, C6) and output cap(C4, C5, C7, C8, C9, C11, C12) must be placed as close as possible to reduce power loop. The PCB trace between power components must be as short and wide as possible.
- Minimize the size of the LX, LXP, LXN node and keep it wide and short. Keep the LX, LXP and LXN node away from those sensing pins (COMP, VCOM, NTC) and analog ground.
- The power ground (PGND1, PGND) consists of input and output capacitor grounds.
- The compensation circuit (R1, C18) should be kept away from the power loops and should be shielded with a ground trace to prevent any noise coupling. Place the compensation components as close as possible to COMP pin.
- The exposed pad of the chip should be connected to a large negative voltage plane for thermal consideration.

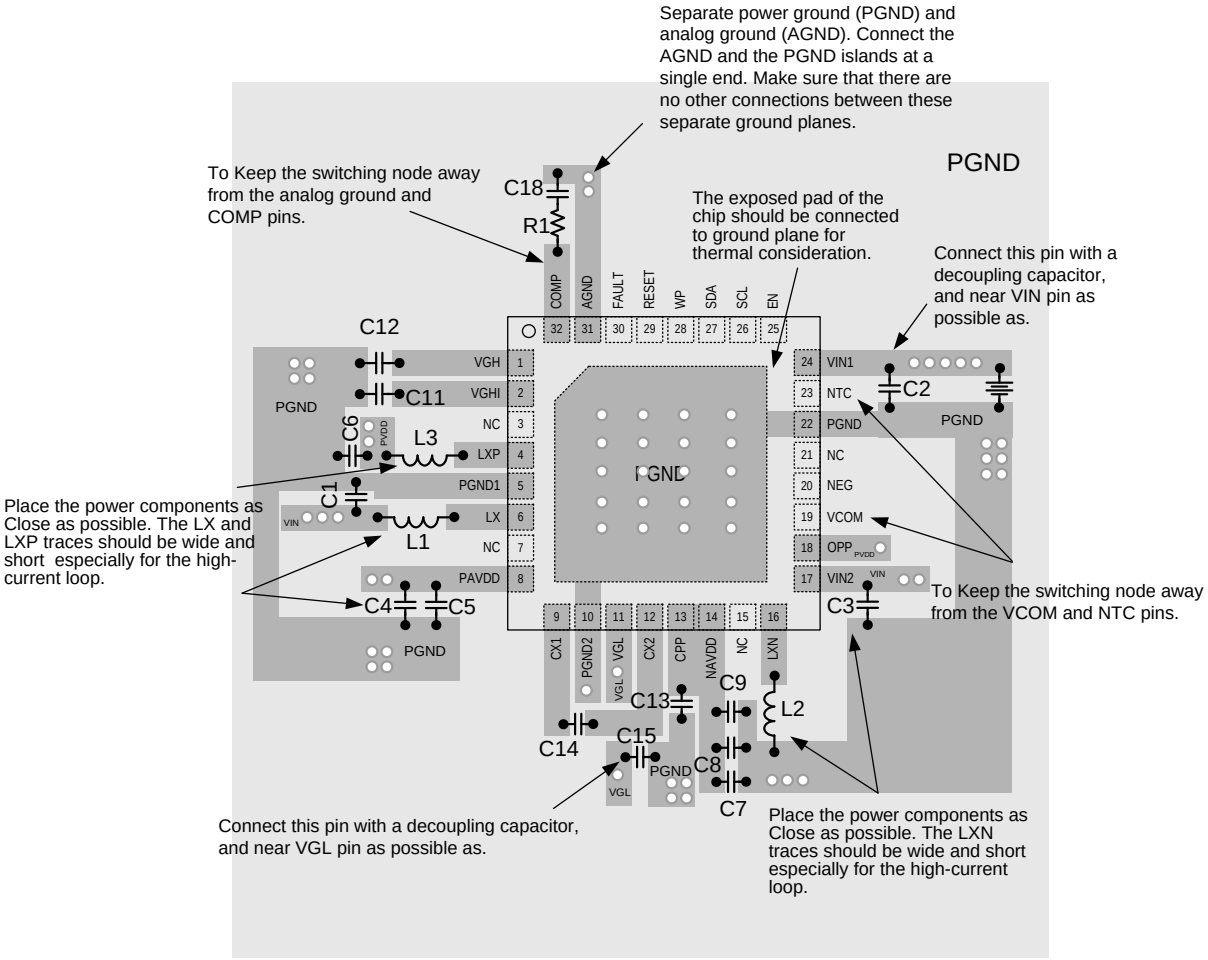
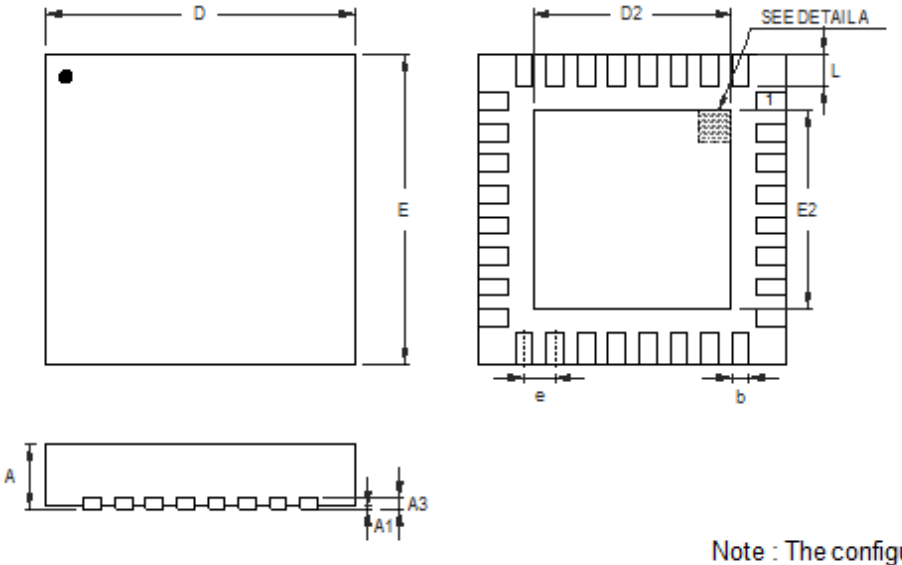


Figure 20. PCB Layout Guide

Outline Dimension

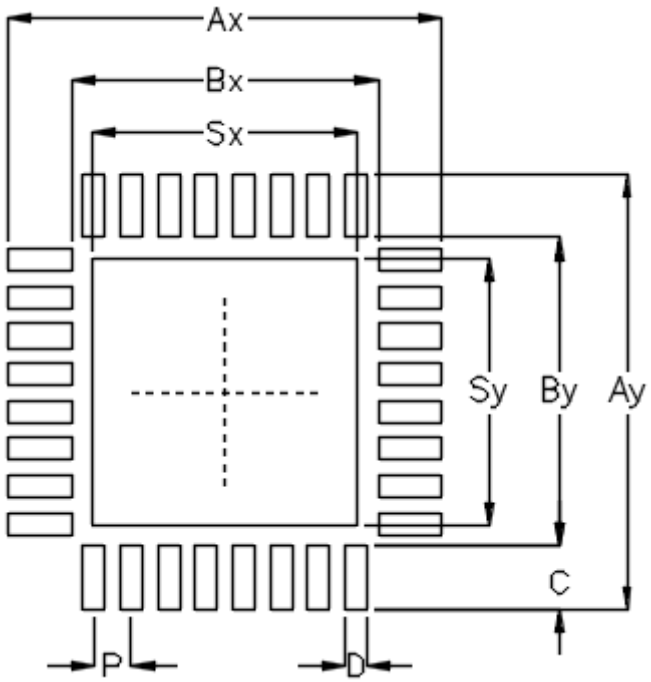


Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 32L QFN 5x5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-32	32	0.50	5.80	5.80	4.10	4.10	0.85	0.30	3.55	3.55	±0.05

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单击下面可查看定价，库存，交付和生命周期等信息

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