Micro-Power Voltage Detector with Manual Reset

General Description

The RT9807 is a micro-power voltage detector with deglitched manual reset input which supervises the power supply voltage level for microprocessors (μP) or digital systems. It provides internally fixed threshold levels ranging from 1.2V to 3.3V with 0.1V per step, which covers most digital applications. It features low supply current of 3μA.

The RT9807 performs supervisory function by sending out a reset signal whenever the VDD voltage falls below a preset threshold level. The timeout period of this reset signal can be adjusted via an external capacitor. Once VDD recovers above the threshold level, the reset signal will be released after a certain delay time. To manually pull reset signal low, just pull the manual reset input (MR) below the specified logic-low level.

The RT9807 is available in an SOT-23-5 package.

Ordering Information

RT9807-□□□

- Package Type
  B : SOT-23-5
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Output Voltage
  12 : 1.2V
  13 : 1.3V
  :
  32 : 3.2V
  33 : 3.3V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

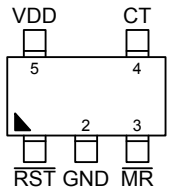
- **Monitor System Voltages from 0.9V to 5.5V**
- **Capacitor-Adjustable Reset Timeout Period**
- **Manual Reset Input**
- **Low Quiescent Current**
- **High Accuracy ±1.5%**
- **Low Functional Supply Voltage 0.9V**
- **N-Channel Open-Drain Output**
- **Small SOT-23-5 Package**
- **RoHS Compliant and Halogen Free**

Applications

- Computers
- Controllers
- Intelligent Instruments
- Critical uP and uC Power Monitoring
- Portable/Battery-Powered Equipment

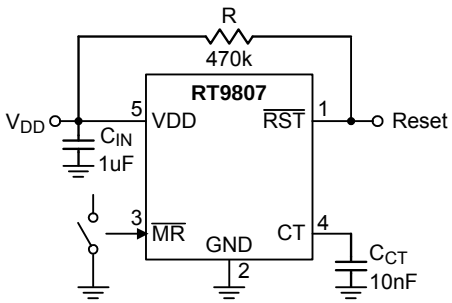
Pin Configurations

(TOP VIEW)



SOT-23-5

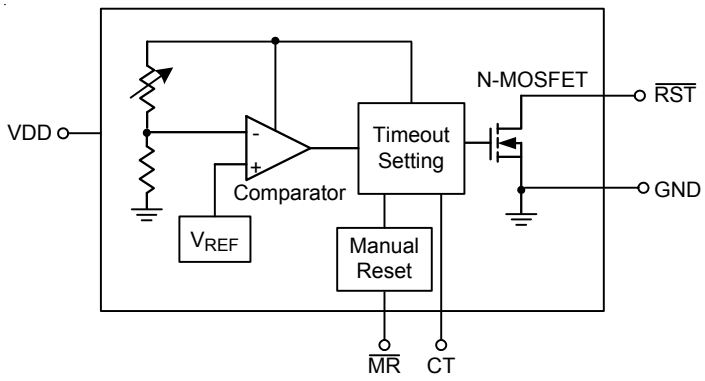
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	$\overline{RST}$	Reset Output Pin. (Open drain)
2	GND	Ground Pin.
3	$\overline{MR}$	Manual Reset Pin.
4	CT	Connect an external capacitor for setting reset timeout period.
5	VDD	Supply Voltage Input Pin.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{DD} ---------- –0.3V to 6V
- Reset Output Voltage, $\overline{RST}$ ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-5 ---------- 0.4W
- Package Thermal Resistance (Note 2)
  SOT-23-5, θ_{JA} ---------- 250°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 0 to 70°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating VDD Range		V_{DD}	Temp = 25°C	0.9	--	5.5	V
			Temp = 0 to 70°C	1	--	5.5	
Supply Current		I_{DD}	V_{TH} = 3V, V_{DD} = 4.5V	--	3	5	μA
Reset Threshold		V_{TH}		1.2	--	3.3	V
Threshold Voltage Accuracy		ΔV_{TH}	Temp = 25°C	–1.5	--	1.5	%
			Temp = 0 to 70°C	–2	--	2	
Threshold Voltage Hysteresis		V_{HYS}		--	50 x V_{TH}	--	mV
Reset Threshold Tempco				--	100	--	ppm/°C
VDD Drop to Reset Delay		t_{RP}	Drop = V_{TH} – 250mV	--	100	--	μs
$\overline{RST}$ Output Voltage Low (Note 5)		V_{OL}	V_{DD} < $V_{TH(min.)}$, I_{SINK} = 3.5mA	--	--	0.4	V
$\overline{MR}$ Input Threshold voltage	Logic-High	V_{IH}		0.7V_{DD}	--	--	V
	Logic-Low	V_{IL}		--	--	0.25V_{DD}	
$\overline{MR}$ Glitch Rejection				--	80	--	ns
$\overline{MR}$ to Reset Propagation Delay		$t_{\overline{MR}}$		--	4	--	μs
$\overline{MR}$ Pull-up Resistance		$R_{\overline{MR}}$		--	20	--	kΩ
Reset Timeout Period		t_{RP}	C_{CT} = 1500pF	2	5	7	ms
			C_{CT} = 0pF	0.15	0.275	0.4	
CT Source Current		I_{RAMP}		--	240	--	nA
CT Source Threshold Voltage		$V_{TH-RAMP}$		--	0.65	--	V
CT Threshold Hysteresis				--	33	--	mV

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

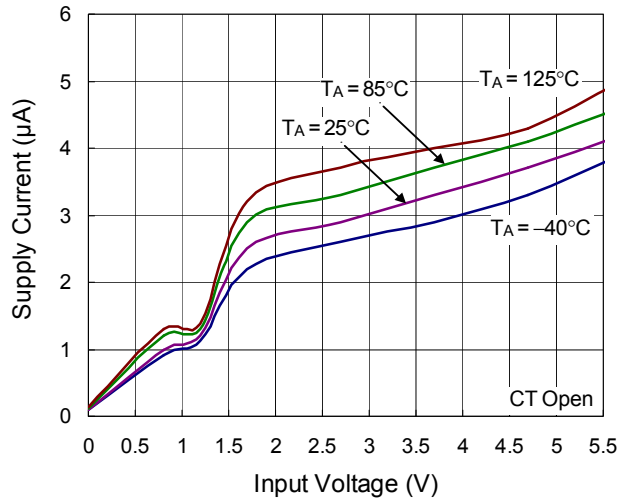
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

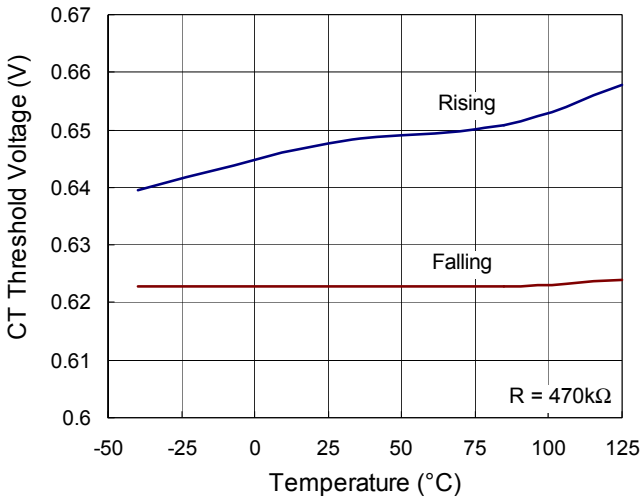
Note 5. The voltage V_{OL} can be calculated by V_{OL} = V_{DD} - I_r x R. Where R is the pull-up resistor and I_r is the current flowing through the pull-up resistor. For typical application R = 100kΩ, VOL is less than 0.2V.

Typical Operating Characteristics

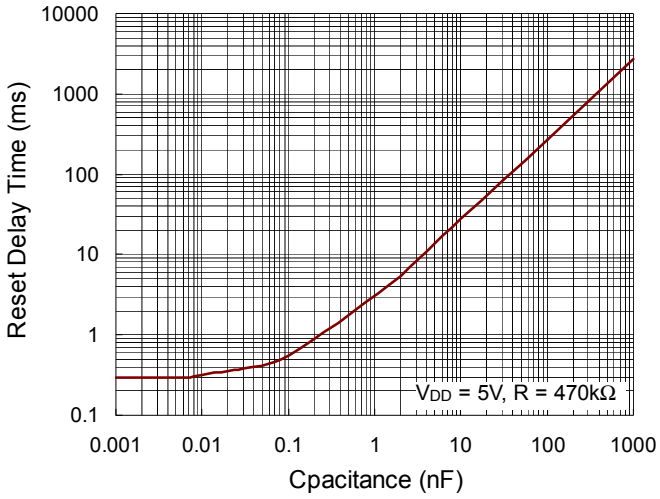
Supply Current vs. Input Voltage



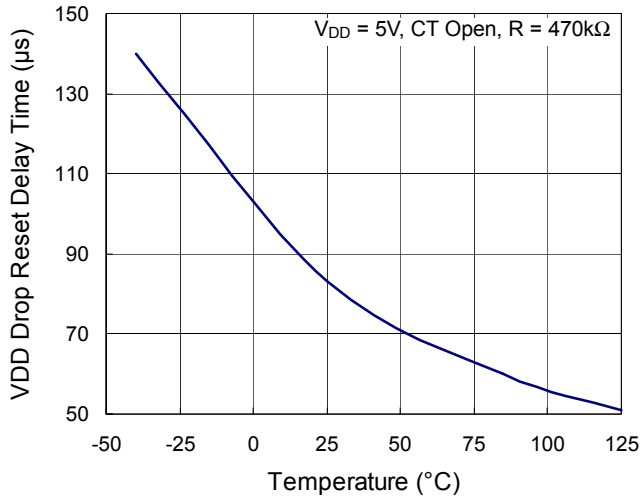
CT Threshold Voltage vs. Temperature



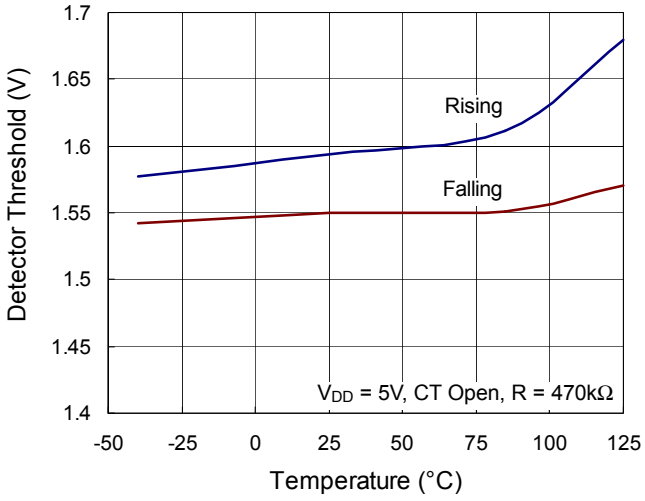
Reset Delay Time vs Capacitance



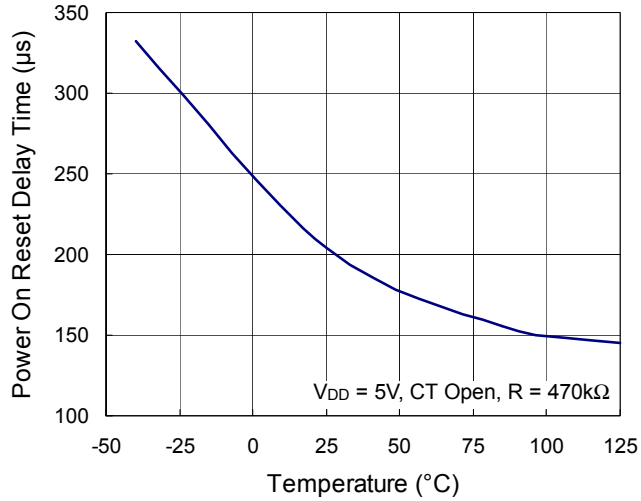
VDD Drop Reset Delay Time vs. Temperature



Detector Threshold vs. Temperature



Power On Reset Delay Time vs. Temperature



Application Information

The RT9807 provides adjustable reset delay time to fit the need of a variety of μP applications. The reset delay time of the RT9807 can be adjusted by connecting a capacitor between the CT pin and GND. The CT capacitor must fit the need of low-leakage (<10nA), and it is recommended to use a ceramic capacitor such as X7R or NPO type.

Reset Delay Time Setting

When the VDD voltage exceeds the VDD threshold voltage, a current source will start to charge the CT capacitor and the CT voltage will rise. When the CT voltage exceeds 0.65V, the $\overline{RST}$ voltage will change from low to high. Therefore, there is a delay time between the point of VDD reaching its threshold voltage and the $\overline{RST}$ active-high point. The delay time can be calculated according to the following equation.

$$t_{DELAY}(\mu s) = 2.71 \times 10^6 \times C_{CT}(\mu F) + 275(\mu s)$$

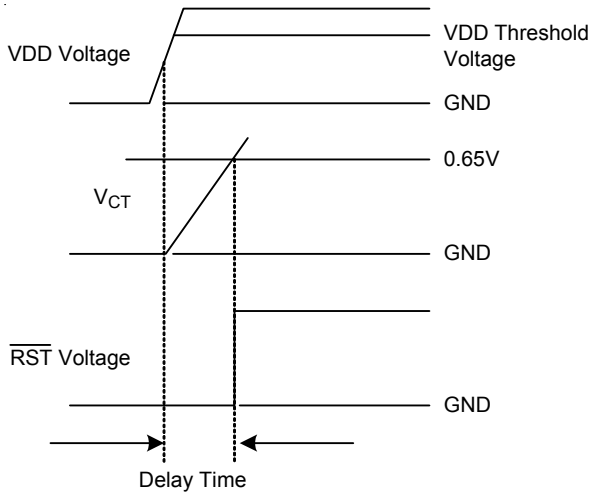


Figure 1. Delay Time

Operating with a Voltage Divider

The voltage detector monitors the V_{CC} voltage to generate a reset signal when V_{CC} is higher than the detecting level. The detecting level is determined by an external resistive voltage divider.

$$V_{CC\_TH} = V_{TH} \times \left(1 + \frac{R1}{R2}\right),\ V_{TH}: \text{Threshold Voltage.}$$

$$V_{CC\_HYS} = V_{HYS} \times \left(1 + \frac{R1}{R2}\right)$$

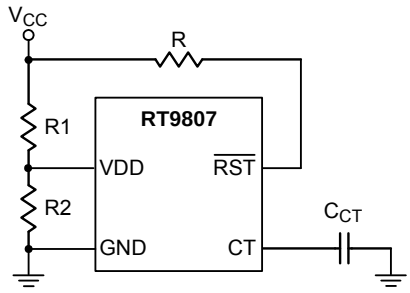


Figure 2. Voltage Divider

The rising and falling of the VCC and $\overline{RST}$ voltage can be explained in five steps as shown in the following diagram.

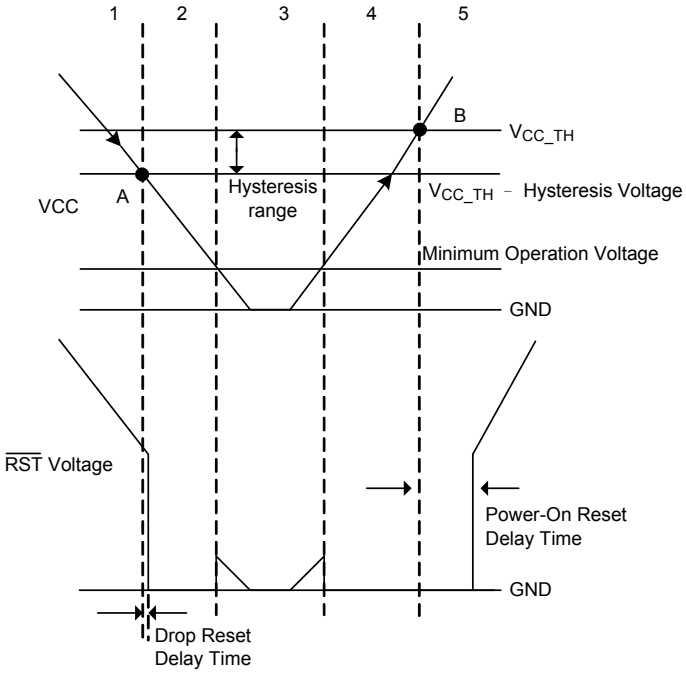


Figure 3. Operation Diagram

1. $\overline{RST}$ voltage is pulled up to VCC voltage.
2. When the VCC voltage is down to the detector threshold voltage (Point A), $\overline{RST}$ voltage becomes low level.
3. When the VCC voltage is lower than minimum operating voltage, the $\overline{RST}$ voltage is indefinite. In the case of open drain type, $\overline{RST}$ voltage is equal to pull-up voltage.
4. $\overline{RST}$ voltage becomes low level.
5. When the VCC voltage exceeds the threshold voltage (Point B), the internal source current will start to charge CT capacitor. The $\overline{RST}$ voltage will go high after a delay time when the CT capacitor voltage reaches 0.65V.

Interfacing to Other Voltages

The RT9807 is an open-drain voltage detector that can provide different voltage level of reset signals for processor application. As shown in Figure 4, the open-drain output can be connected to another voltage level less than 5.5V. This allows for easy logic compatibility to various microprocessors.

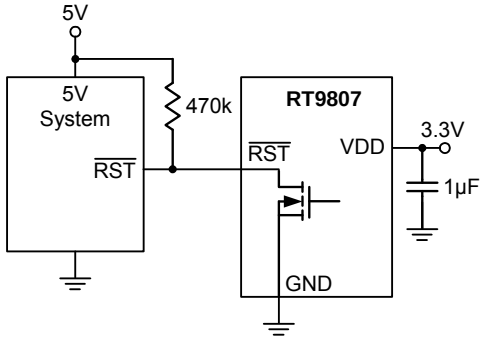


Figure 4

Manual Reset Input

Many processor based products require manual reset capability, allowing the user or external logic circuitry to initiate a reset. A logic low on MR asserts reset. Reset remains asserted while MR is low and for the reset timeout period after MR returns high. Connect a normally open momentary switch from MR to ground to create a manual reset function.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of the RT9807, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOT-23-5 package, the thermal resistance θ_{JA} is 250°C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (250°C/W) = 0.4W for SOT-23-5 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9807 package, the derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

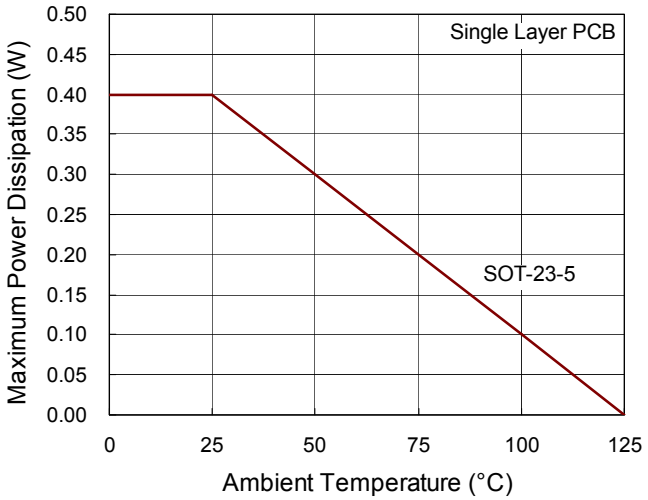


Figure 5. Derating Curve for RT9807 Package

Layout Considerations

CT is a precise current source. When developing the layout for the application, be careful to minimize board capacitance and leakage currents around this pin.

Traces connected to CT should be kept as short as possible. Traces carrying high-speed digital signals and traces with large voltage potentials should be routed as far from CT as possible. Leakage current and stray capacitance (e.g., a scope probe) at this pin can cause errors in the reset delay time.

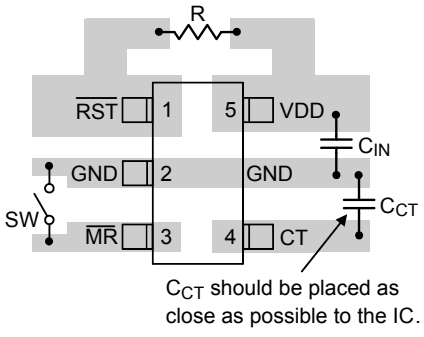
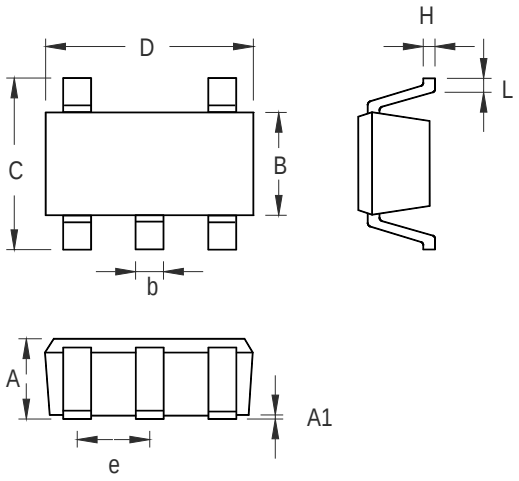


Figure 6. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package

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