

RT4805A 2.5MHz, Synchronous Boost Regulator with Bypass Mode

Purpose

The RT4805A is a Boost converter with the input voltage range from 1.8V to 5V and provides 2A output current. This document explains the function and use of the RT4805A evaluation board (EVB), and provides information to enable operation, output voltage setting of the evaluation board.

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Introduction

General Product Information

The RT4805A allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li-lon battery chemistries.

The RT4805A is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed to a maximum load current of 2A. Quiescent current in Shutdown Mode is less than 1µA, which maximizes battery life. The regulator transitions smoothly between Bypass and normal Boost Mode. The device can be forced into Bypass Mode to reduce quiescent current. The RT4805A is available in the WL-CSP-16B 1.67x1.67 (BSC) package.

Product Feature

- 4 Few External Components : 0.47µH Inductor and 0603 Case Size Input and Output Capacitors
- Input Voltage Range : 1.8V to 5V
- Output Range from 2.85V to 4.4V
 - VSEL = L 3.6V

VSEL = H 3.7V

- + Maximum Continuous Load Current : 2A at V_{IN} > 2.65V Boosting V_{OUT} to 3.35V
- Up to 96% Efficient
- + True Bypass Operation when V_{IN} > Target V_{OUT}
- Internal Synchronous Rectifier
- True Load Disconnectwhen Shut Down
- Forced Bypass Mode
- VSEL Control to Optimize Target VOUT
- Short-Circuit Protection
- I²C Controlled Interface
- Ultra low Operating Quiescent Current
- Small WL-CSP 16B Package

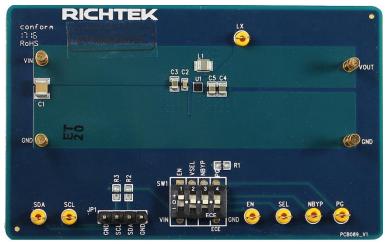
Key Performance Summary Table

Key Features	Evaluation Board Number : PCB089_V1
Default Input Voltage	3.0V
Max Output Current	2A
Default Output Voltage	Vout_H = 3.7V, Vout_L = 3.6V
Default Marking & Package Type	WL-CSP-16B 1.67x1.67 (BSC)



Bench Test Setup Conditions

Headers Description and Placement



Carefully inspect all the components used in the EVB according to the following Bill of Materials table, and then make sure all the components are undamaged and correctly installed. If there is any missing or damaged component, which may occur during transportation, please contact our distributors or e-mail us at <u>evb_service@richtek.com</u>.

Test Points

The EVB is provided with the test points and pin names listed in the table below.

Test point/ Pin name	Signal	Comment (expected waveforms or voltage levels on test points)		
VIN	Input voltage	Input voltage with range 1.8V to 5V.		
EN	V _{OUT} Enable	Enable control pin for VOUT.		
LX	Switching Node	Switching Node.		
PGND/AGND	Ground	Ground.		
SDA/SCL	I2C Control	Pins to set functions such as VOUT, ILIM.		
VOUT	Output Voltage	Default voltage : 5V \pm 2%.		
PGOOD	Power Good	Power Good. It is a open-drain output. PGOOD pin pulls low automatically if the overload or OTP event occurs.		
VSEL	VOUT Select GPIO	Output Voltage Select. When boost is running, this pin can be used to select output voltage.		
nBYP Inverse Bypass Signal		Bypass. This pin can be used to activate Forced Bypass Mode. When this pin is LOW, the bypass switches are turned on and the IC is otherwise inactive.		

Power-up & Measurement Procedure

- 1. Connect input voltage ($1.8V < V_{IN} < 5.0V$).
- 2. To use a switch at "H" option to tie EN pin to input voltage VIN via SW1 or external voltage for enabling the device. Inversely, to use a jumper at "L" option to tie EN pin to ground GND for disabling the device.
- 3. To verify the output voltage V_{OUT} via the I2C interface.
- 4. To connect an external load up to 1A and verify the output voltage and current.

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I2C Register Setting

The register as the table shown can be programmed by a MCU through the dedicated I2C interface. The device slave address is 0x39.

Name CONFIG		Function	Addr	
		MODE control & Spread modulation control	0x01	
Bit	Mode	name	Reset	Description
7	R/W	RESET	0	0 : Disable ID detection function 1 : Enable ID detection function
[6 : 5] R/W ENABLE[1 : 0]		ENABLE[1:0]	0	 00 : Device operation follows hardware control signal (refer to table 1) 01 : Device operation in auto transition mode (boost/bypass) regardless of the nBYP control signal (EN = 1) 10 : Device is forced in pass-through mode regardless of the nBYP control signal (EN = 1) 11 : Device is in shutdown mode. The output voltage is reduced to a minimum value (V_{IN} - V_{OUT} ≤ 3.6V) regardless of the nBYP control signal (EN = 1)
4 R/W		Reserved	0	
3 R/W PG Confi		PG Config.	1	 0 : PG pin = H, it is not allowed. PG pin = L, it is shut down. 1 : PG pin is for power good indication.
2 R/W		SSFM	0	0 : Spread spectrum modulation is disabled. 1 : Spread spectrum modulation is enabled in PWM mode.
[1:0] R/W		MODE_CTRL[1:0]	01	 00 : Device operation follows hardware control signal. 01 : PFM with automatic transition into PWM operation. 10 : Forced PWM operation. 11 : PFM with automatic transition into PWM operation (VSEL = L), forced PWM operation (VSEL = H).
Name		Function	Addr	
VOUTFLOOR		Output Voltage Selection	0x02	
Rit Mode		namo	Posot	Description

voon	LOOK	Selection	0702		
Bit	Mode	name	Reset	Description	
[7 : 5]	R/W	Reserved	000		
[4 : 0]	R/W	VOUT[4 : 0]	01111	$\begin{array}{l} 00000 : V_{OUT} = 2.85V\\ 00001 : V_{OUT} = 2.9V\\ 00010 : V_{OUT} = 2.95V\\ 00011 : V_{OUT} = 3V\\ 00100 : V_{OUT} = 3.05V\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ $	



Name		Function	Addr			
VOUTROOF		Output Voltage Selection	0x03			
Bit Mode		name	Reset	Description		
[7 : 5]	R/W	Reserved	000			
[4 : 0] R/W		VOUT[4 : 0]	10001	00000 : V _{OUT} = 2.85V 00001 : V _{OUT} = 2.9V 00010 : V _{OUT} = 2.95V 00011 : V _{OUT} = 3V 00100 : V _{OUT} = 3.05V 10001 : V _{OUT} = 3.7V (default) 11111 : V _{OUT} = 4.4V		
Na	me	Function	Addr			
ILIN	ISET	Set current limit & Softstart current limit	0x04			
Bit	Mode	name	Reset	Description		
[7:6]	R/W	Reserved	00			
5	R/W	ILIM_OFF	0	0 : Current Limit Enabled 1 : Current Limit Disabled		
4	R/W	Soft-Start	1	 0 : Boost soft-start current is limited per ILIM bit settings 1 : Boost soft-start current is limited to ca. 1250mA inductor valley current 		
[3 : 0]	R/W	ILIM[3 : 0]	1101	1000 : 1500mA 1001 : 2000mA 1010 : 2500mA 1011 : 3000mA 1100 : 3500mA 1101 : 4000mA (default) 1110 : 4500mA 1111 : 5000mA		

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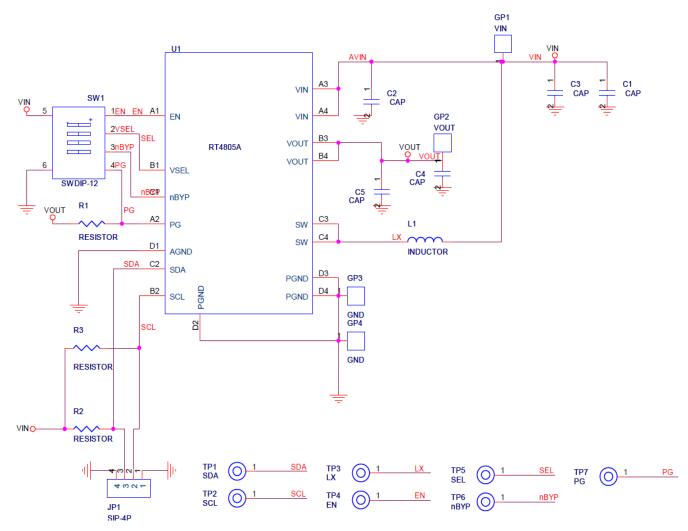
RT4805AWSC Evaluation Board

Name		Function	Addr		
STATUS		Read IC status 0x0			
Bit	Mode	name	Reset	Description	
7	R	TSD	0	0 : Normal operation. 1 : Thermal shutdown tripped. The flag is reset after readout.	
6	R	HOTDIE	0	0 : TJ < 115°C. 1 : TJ > 115°C.	
5	R	DCDCMODE	0	0 : Device operates in PFM mode. 1 : Device operates in PWM mode.	
4	R	OPMODE	0	0 : Device operates in pass-through mode. 1 : Device operates in dc/dc mode.	
3	R	ILIMPT	0	 0 : Normal operation. 1 : Indicates that the bypass FET current limit has triggered. Th flag is reset after readout. 	
2	R	ILIMBST	0	 0 : Normal operation. 1 : Indicates that the average input current limit has triggered for 1.5ms in dc/dc boost mode. This flag is reset after readout. 	
1	R	FAULT	0	 0 : Normal operation. 1 : Indicates that a fault condition has occurred. This flag is rese after readout. 	
0	0 R PGOOD		0	 0 : Indicates the output voltage is out of regulation. 1 : Indicates the output voltage is within its nominal range. This bit is set if the converter is forced in pass-through mode. 	



Schematic, Bill of Materials & Board Layout

EVB Schematic Diagram

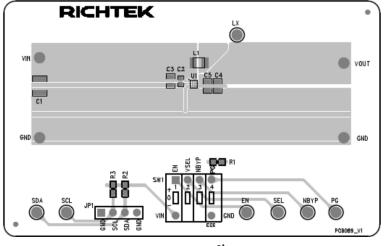


Bill of Materials

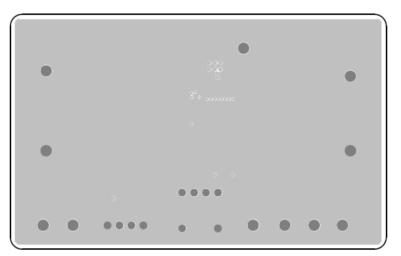
Reference	Qty	Part number	Description	Package	Manufacture
U1	1	RT4805AWSC	Boost Converter	WL-CSP-16B 1.67x1.67	Richtek
C1	1	GRM32ER61A107ME20L	100µF/10V/X5R/1210	C-1210	Murata
C2	1	GRM188R61H105KAAL	1.0µF/50V/X7R/0603	C-0603	Murata
C3	1	EMK212ABJ106KG	10µF/16V/X7R/0805	C-0805	Taiyo
C4, C5	2 LMK212BBJ226MG		22µF/6.3V/X7R/0805	C-0805	Taiyo
L1	1	DFE2520F-R47M	0.47µH	L-2520	ТОКО
R1	1	PFR05105FNH	1MΩ/0402/1%	R-0402	乾坤
R2, R3 2 PFR05102FNH		1kΩ/0402/1%	R-0402	乾坤	



PCB Layout

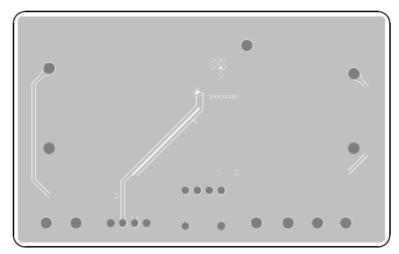


Top View (1st layer)

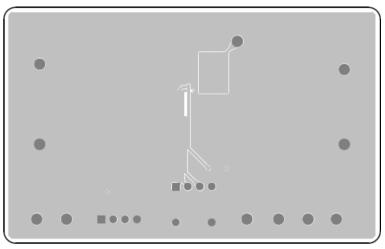


PCB Layout—Inner Side (2nd Layer)





PCB Layout—Inner Side (3rd Layer)



Bottom View (4th Layer)



More Information

For more information, please find the related datasheet or application notes from Richtek website <u>http://www.richtek.com</u>.

Important Notice for Richtek Evaluation Board

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