ROHM SEMICONDUCTOR

Datasheet

Single-chip Type with Built-in FET Switching Regulators

Flexible Step-down Switching Regulators with Built-in Power MOSFET

BD9876AEFJ

●General Description

Output 3.0A and below High Efficiency Rate Step-down Switching Regulator Power MOSFET Internal Type BD9876AEFJ mainly used as secondary side Power supply, for example from fixed Power supply of 12V, 24V etc, Step-down Output of 1.2V/1.8V/3.3V/5V, etc, can be produced. This IC has external Coil/Capacitor down-sizing through 300kHz Frequency operation, inside Nch-FET SW for 45V "withstand-pressure" commutation and also, high speed load response through Current Mode Control is a simple external setting phase compensation system, through a wide range external constant, a compact Power supply can be produced easily.

●Features

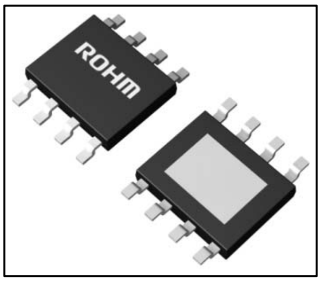
- Internal 200 mΩ Nch MOSFET
- Output Current 3A
- Oscillation Frequency 300kHz
- Synchronizes to External Clock (200kHz～500kHz)
- Feedback Voltage 1.0V±1.0%
- Internal Soft Start Function
- Internal Over Current Protect Circuit, Low Input Error Prevention Circuit, Heat Protect Circuit
- ON/OFF Control through EN Pin (Standby Current 0 A Typ.)
- Package: HTSOP-J8 Package

●Key Specifications

Input Voltage	7V to 42V
Ref. Precision (Ta=25℃)	±1.0%
Max Output Current	3A (Max.)
Operating Temperature	-40℃ to 105℃
Max Junction Temperature	-55℃ to 150℃

●Packages

HTSOP-J8 4.90mm x 6.00mm x 1.00mm



HTSOP-J8

●Applications

- For Household machines in general that have 12V/24V Lines, etc.

●Typical Application Circuits

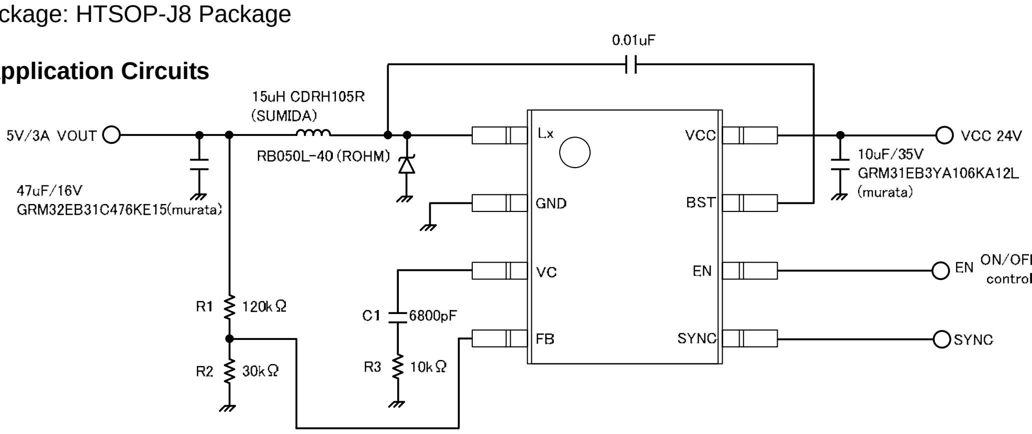


Figure 1. Typical Application Circuit

○Structure : Silicon Monolithic Integrated Circuit ○This product is not designed for normal operation with in a radioactive.

●Pin Configuration

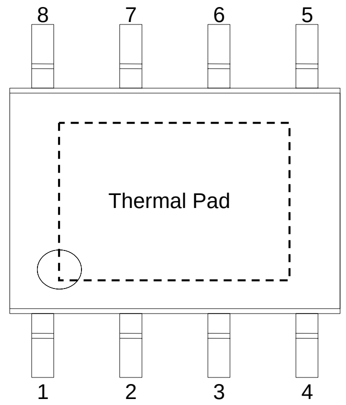


Figure 2. Pin Configuration (TOP VIEW)

●Pin Description

Pin No.	Pin Name	Description
1	Lx	Terminal for inductor
2	GND	Ground pin
3	VC	Error amplifier output
4	FB	Inverting node of the trans conductance error amplifier
5	SYNC	Input pin of an external signal for the device synchronized by external signal
6	EN	Stand-by ON/OFF pin
7	BST	Voltage Supply pin for High Side FET Driver
8	VCC	Voltage input pin
-	Thermal Pad	PAD for enhance the radiation of heat. Connect to GND absolutely.

●Block Diagram

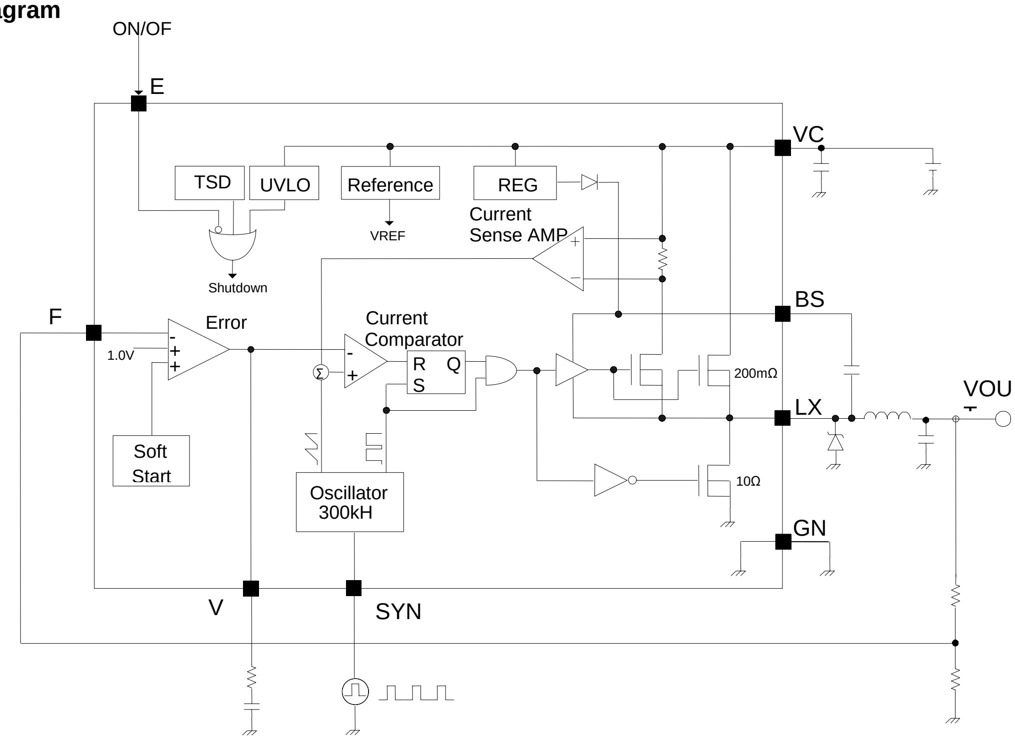


Figure 3. Block Diagram

●Description of Blocks

1. Reference
   This Block generates Error Amp Standard Voltage.
   Standard Voltage is 1.0V.

2. REG
   This is a Gate Drive Voltage Generator and 5V Low Saturation regulator for internal Circuit Power supply.

3. OSC
   This is a precise wave Oscillation Circuit with Operation Frequency fixed to 300 kHz fixed (self-running mode).
   To implement the synchronization feature connect a square wave (Hi Level: higher than 2V Low Level: lower than 0.8V) to the SYNC pin. The synchronization frequency range is 200 kHz to 500 kHz.
   After connecting the rising edge of LX will be synchronized to the falling edge of SYNC pin signal after 3 count.
   At the synchronization remove the external clock, the device transitions self-running mode after 7 microseconds.

4. Soft Start
   A Circuit that does Soft Start to the Output Voltage of DC/DC Comparator, and prevents Rush Current during Start-up. Soft Start Time is set at IC internal, after 10ms from starting-up EN Pin, Standard Voltage comes to 1.0V, and Output Voltage becomes set Voltage.

5. ERROR AMP
   This is an Error amplifier what detects Output Signal, and outputs PWM Control Signal.
   Internal Standard Voltage is set to 1.0V. Also, C and R are connected between the Output (VC) Pin GND of Error Amp as Phase compensation elements. (See P.11)

6. ICOMP
   This is a Voltage-Pulse Width Converter that controls Output Voltage in response to Input Voltage.
   This compares the Voltage added to the internal SLOPE waveform in response to the FET WS Current with Error amplifier Output Voltage, controls the width of Output Pulse and outputs to Driver.

7. Nch FET SW
   This is an internal commutation SW that converts Coil Current of DC/DC Comparator.
   It contains 45V" with stand pressure" 200mΩ SW.
   Because the Current Rating of this FET is 3.5A included ripple current, please use at within 3.5A.
   The device has the circuit of over current protection for protecting the FET from over current.
   To detect OCP 2 times sequentially, the device will stop and after 13 msec restart.

8. UVLO
   This is a Low Voltage Error Prevention Circuit.
   This prevents internal circuit error during increase of Power supply Voltage and during decline of Power supply Voltage.
   It monitors VCC Pin Voltage and internal REG Voltage, And when VCC Voltage becomes 6.4V and below, it turns OFF all Output FET and turns OFF DC/DC Comparator Output, and Soft Start Circuit resets.
   Now this Threshold has Hysteresis of 200mV.

9. TSD
   This is a Heat Protect (Temperature Protect) Circuit.
   When it detects an abnormal temperature exceeding Maximum Junction Temperature (Tj=150℃), it turns OFF all Output FET, and turns OFF DC/DC Comparator Output. When Temperature falls, it has/with Hysteresis and automatically returns.

10. EN
   With the Voltage applied to EN Pin(6pin), IC ON/OFF can be controlled.
   When a Voltage of 2.0V or more is applied, it turns ON, at Open or 0V application, it turns OFF.
   About 550kΩ Pull-down Resistance is contained within the Pin.

●Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
VCC-GND Supply Voltage	VCC	45	V
BST-GND Voltage	VBST	50	V
BST-Lx Voltage	⊿VBST	7	V
EN-GND Voltage	VEN	45	V
Lx-GND Voltage	VLX	45	V
FB-GND Voltage	VFB	7	V
VC-GND Voltage	VC	7	V
SYNC-GND Voltage	SYNC	7	V
High-side FET Drain Current	IDH	3.5	A
Power Dissipation	Pd	3.76(*1)	W
Operating Temperature	Topr	-40～+105	℃
Storage Temperature	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

(*1)During mounting of 70×70×1.6t mm 4layer board (Copper area: 70mm×70mm).Reduce by 30.08mW for every 1℃ increase. (Above 25℃)

●Electrical Characteristics (Unless otherwise specified Ta=25℃, VCC=24V, Vo=5V,EN=3V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
【Circuit Current】						
Stand-by current of VCC	Ist	―	0	10	μA	VEN=0V
Circuit current of VCC	Icc	―	1	2	mA	FB=1.2V
【Under Voltage Lock Out (UVLO)】						
Detect Voltage	Vuv	6.1	6.4	6.7	V	
Hysteresis width	Vuvhy	―	200	300	mV	
【Oscillator】						
Oscillating frequency	fosc	270	300	330	kHz	
Max Duty Cycle	Dmax	85	91	97	%	
【Error Amp】						
FB threshold voltage	VFB	0.990	1.000	1.010	V	
Input bias current	IFB	-1.0	0	1.0	μA	VFB=0V
Error amplifier DC gain	A_{VEA}	700	7000	70000	V/V	
Trans Conductance	G_{EA}	110	220	440	μA/V	IVC=±10μA, VC=1.5V
Soft Start Time	Tsoft	7	10	13	ms	
【Current Sense Amp】						
VC to switch current transconductance	G_{CS}	5	10	20	A/V	
【Output】						
Lx NMOS ON resistance	RonH	―	200	340	mΩ	
Lx pre-charge NMOS ON resistance	RonL	―	10	17	Ω	

Over Current Detect Current		Iocp	3.5	6	—	A	
【CTL】							
EN Pin Control voltage	ON	VENON	2	—	VCC	V	
	OFF	VENOFF	-0.3	—	0.8	V	
EN Pin input current		REN	2.7	5.5	11	µA	VEN=3V
【SYNC】							
SYNC Pin Control voltage	High	VSYNCH	2.0	—	5.5	V	
	Low	VSYNCL	-0.3	—	0.8	V	
SYNC Pin input current		REN	6	12	24	µA	VSYNC=3V
SYNC falling edge to LX rising edge delay		tdelay	200	400	600	ns	

◎Not designed to withstand radiation.

●Operating Ratings(Ta=25℃)

Item	Symbol	Ratings			Unit
		Min	Typ	Max	
Power Supply Voltage	VCC	7	—	42	V
Output Voltage	VOUT	1.0(*2)	—	VCC×0.7	V

(*2)Restricted by minimum on pulse typ. 200ns

●Detailed Description

◇Synchronizes to External Clock

The SYNC pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to SYNC pin. The square wave amplitude must transition lower than 0.8V and higher than 2.0V on the SYNC pin and have an on time greater than 100ns and an off time greater than 100ns. The synchronization frequency range is 200 kHz to 500 kHz. The rising edge of the LX will be synchronized to the falling edge of SYNC pin signal after SYNC input pulse 3 count. At the synchronization, the external clock is removed, the device transitions self-running mode after 7 microseconds.

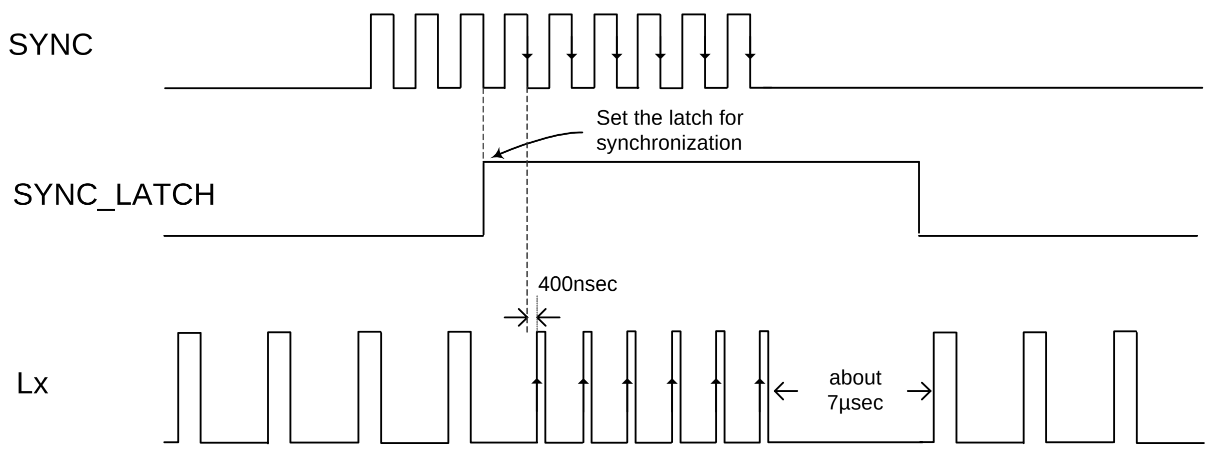


Figure 4. Timing chart at Synchronization

◇The case of not using the function of synchronization

Although the SYNC pin is pulled down by resistor in this device, if the function of the synchronization is not used, it is recommended to connect SYNC pin to ground.

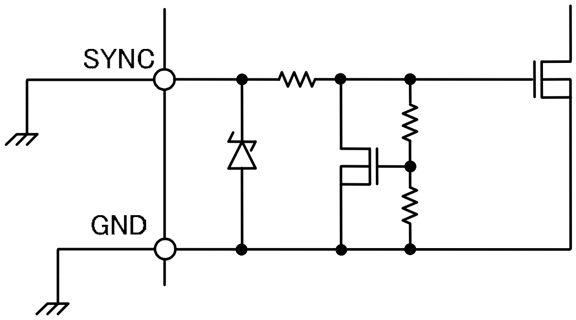


Figure 5. the method to disposal the SYNC pin without synchronization

◇SOFT START

The soft start time of BD9876AEFJ is determined by the DCDC operating frequency (self-run mode 300 kHz ⇒10ms). If synchronization is used at the time of EN=ON, The soft start time is restricted by SYNC pin input pulse frequency. SYNC pin input pulse frequency is fosc_ex kHz, the soft start time is expressed by below equation.

$$Tss = \frac{300}{fosc\_ex} \times 10 \text{ [ms]}$$

◇OCP operation

The device has the circuit of over current protection for protecting the FET from over current. To detect OCP 2 times sequentially, the device will stop and after 13 msec restart.

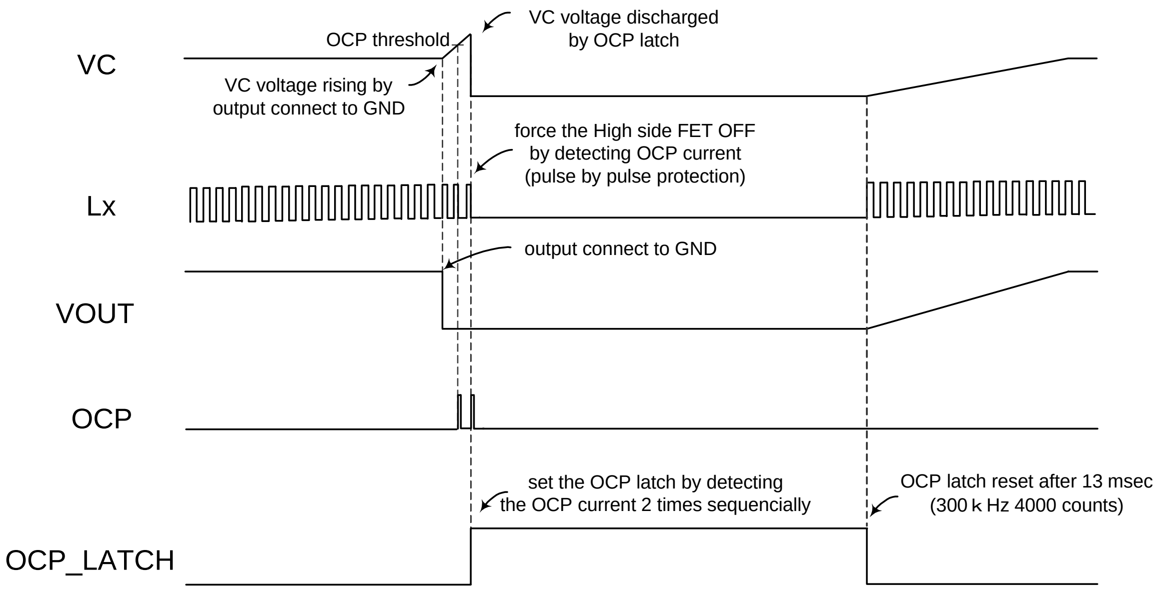


Figure 6. Timing chart at OCP operation

◇OCP operation at soft start

BD9876AEFJ have the function to change the OCP reference voltage according to slope for soft start to prevent IC from abnormal current at higher input voltage. This function restricts the OCP threshold a half of the specification value (typ.3A).

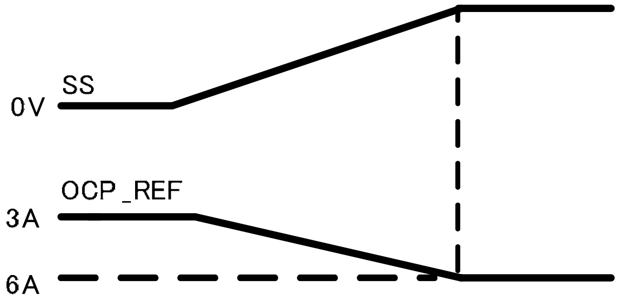


Figure 7. the relation SS node voltage and OCP reference voltage.

●**Reference Data** (Unless otherwise specified, Ta=25℃, VCC=24V, Vo=5V, EN=3V)

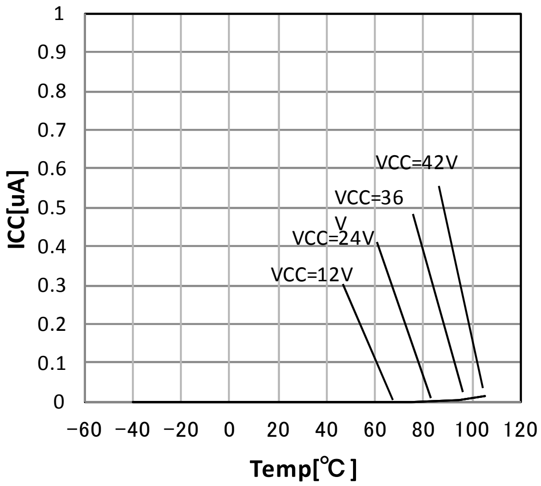


Figure 8. Standby Current
Temperature Characteristics

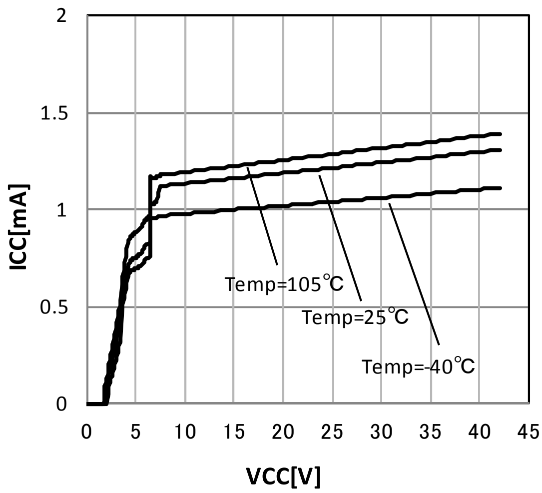


Figure 9. Circuit Current
Power supply Voltage Characteristics

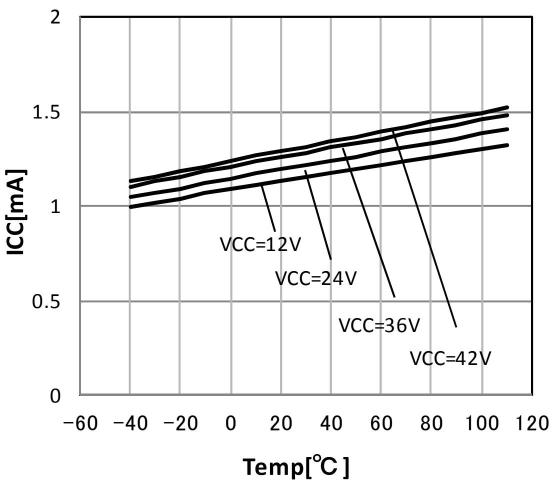


Figure 10. Circuit Current
Temperature Characteristics

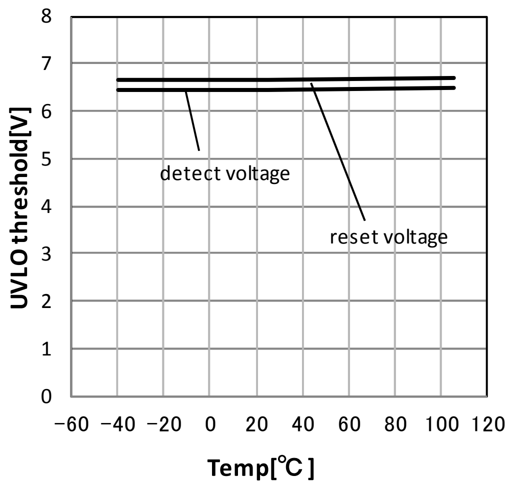


Figure 11. UVLO Threshold
Temperature Characteristics

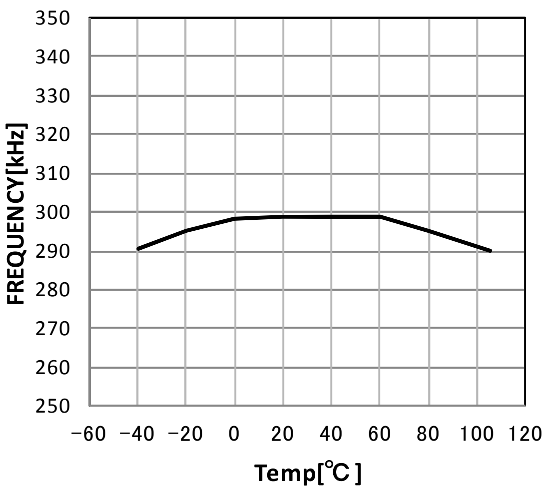


Figure 12. Oscillation Frequency
Temperature Characteristics

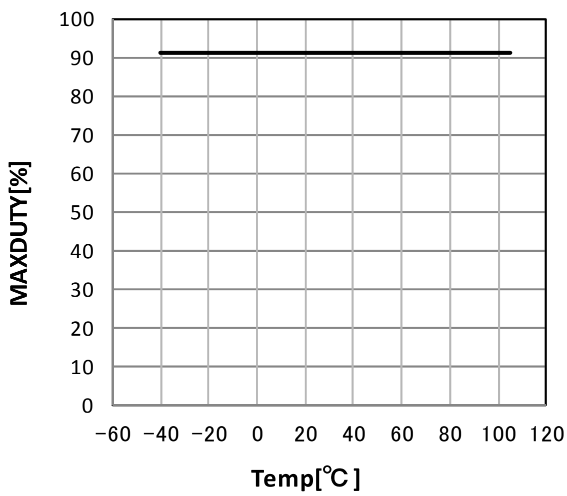


Figure 13. Max Duty
Temperature Characteristics

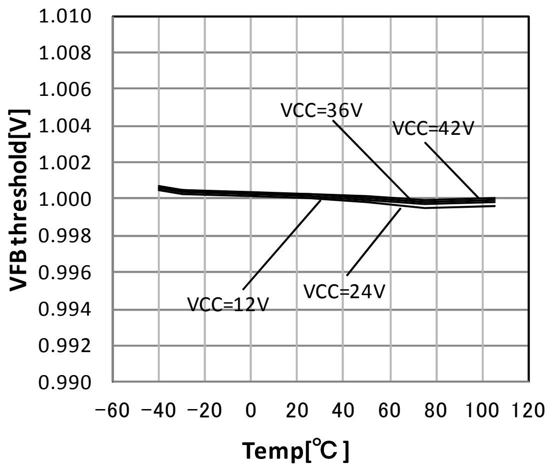


Figure 14. FB Threshold Voltage
Temperature Characteristics

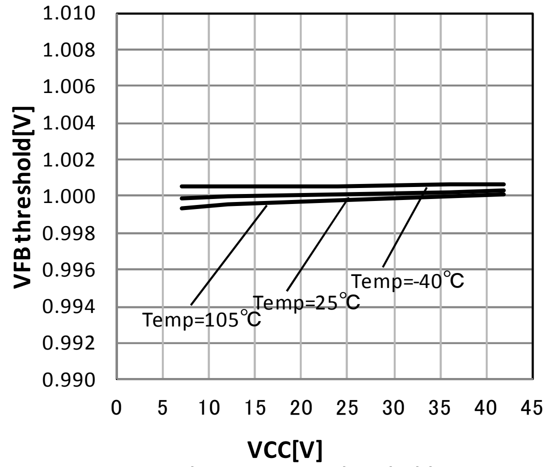


Figure 15. FB Threshold
Power supply Characteristics

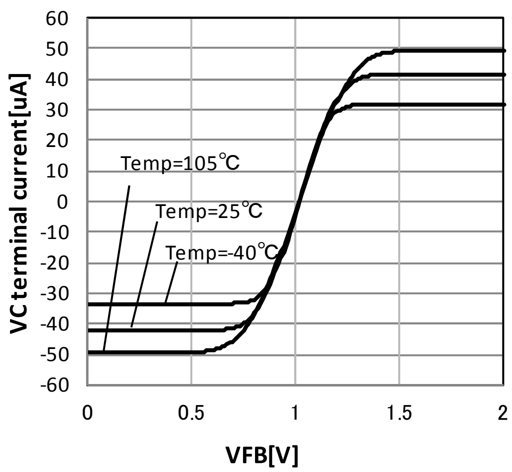


Figure 16. FB Voltage - IVC
Current Characteristics

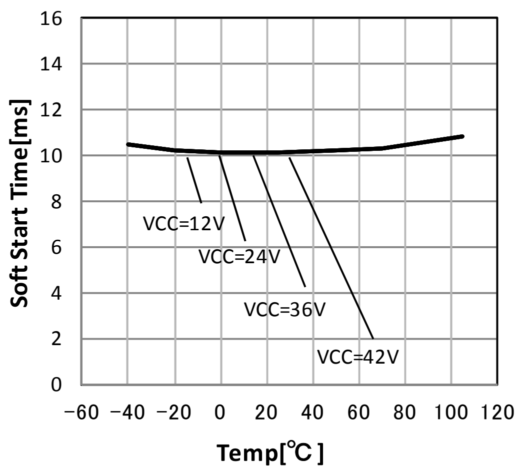


Figure 17. Soft Start Time
Temperature Characteristics

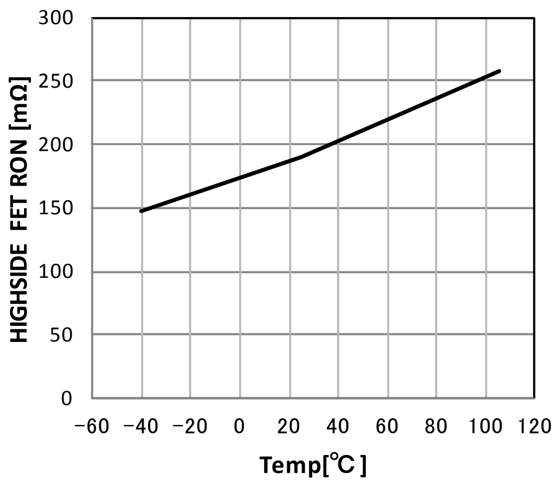


Figure 18. Nch FET ON Resistance
Temperature Characteristics

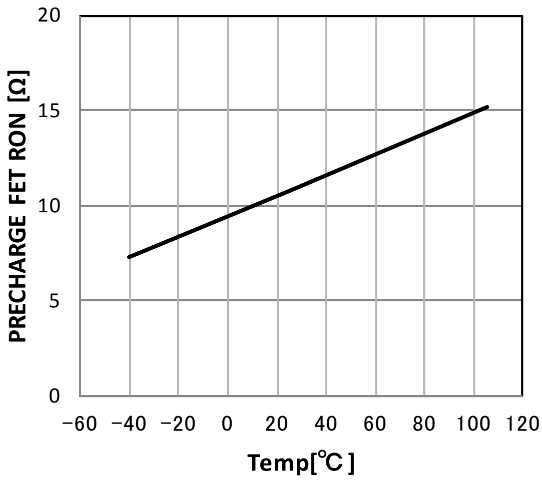


Figure 19. Pre-charge FET ON
Resistance Temperature Characteristics

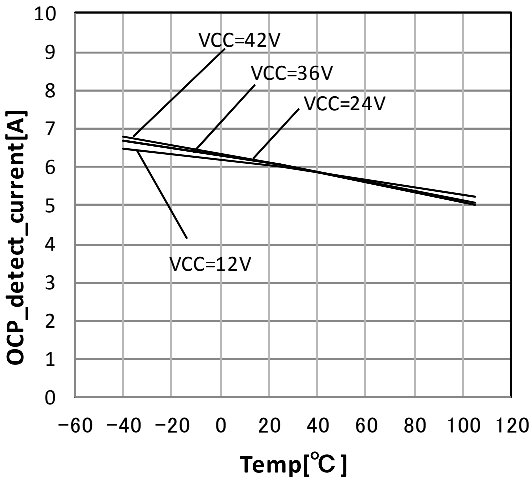


Figure 20. OCP Detect Current
Temperature Characteristics

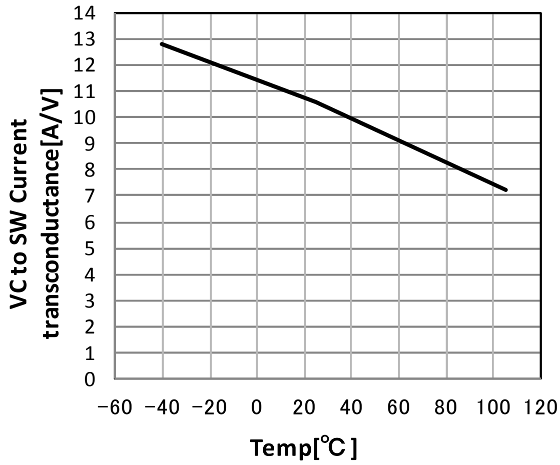


Figure21. VC to SW current transconductance
Temperature characteristics

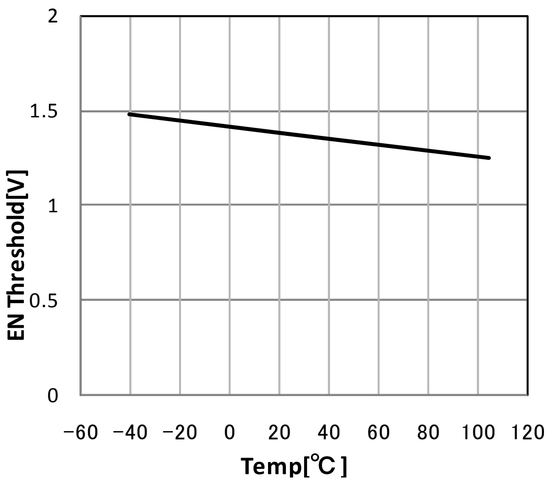


Figure 22.. EN Threshold
Temperature Characteristics

●**Example of Reference Application Circuit** (Input 24V, Output 5.0V)

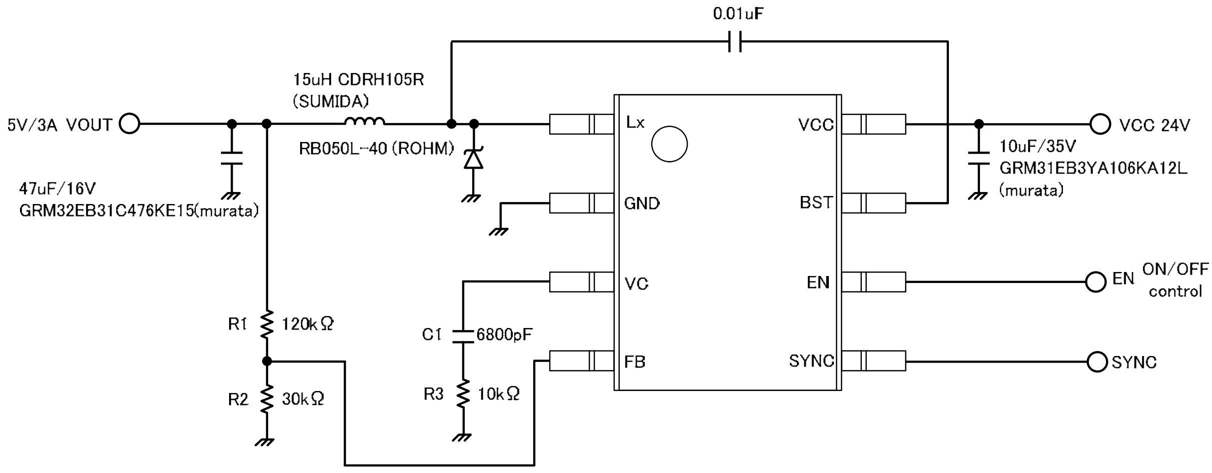


Figure 23. Reference Application Circuit

●**Reference Application Data** (Example of Reference Application Circuit)

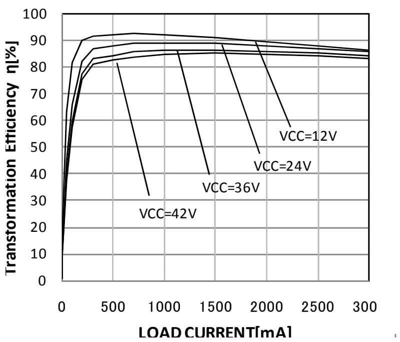


Figure 24. Electric Power Conversion Rate

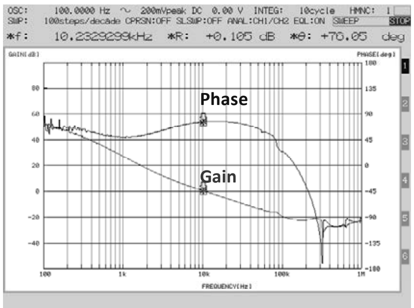


Figure 25. Frequency Response Characteristics (Io=0.5A)

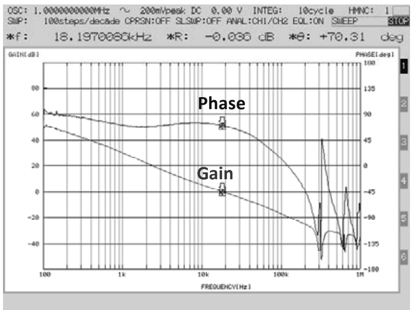


Figure 26. Frequency Response Characteristics (Io=3.0A)

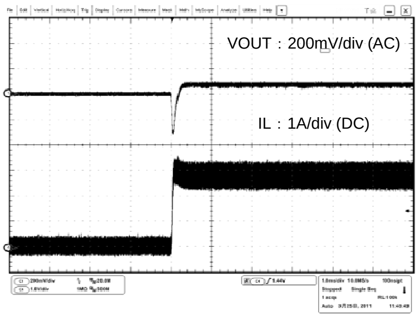


Figure 27. Load Response Characteristics (Io=0A→3.0A)

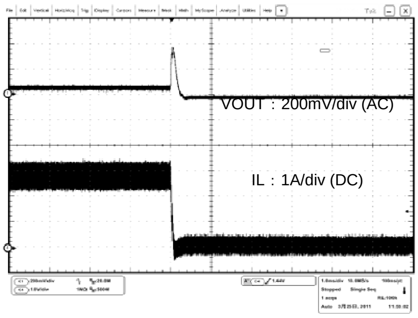


Figure 28. Load Response Characteristics (Io=3.0A→0A)

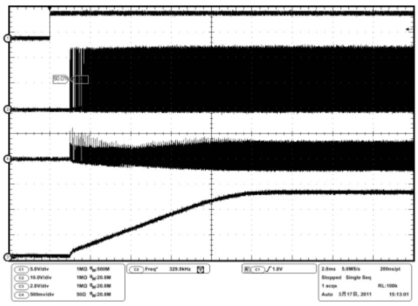


Figure 29. startup Waveform

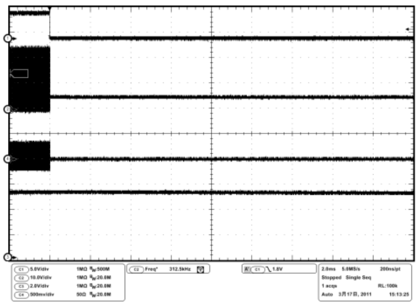


Figure 30. Stop Waveform

●**Example of Reference Application Circuit** (Input 24V, Output 12V)

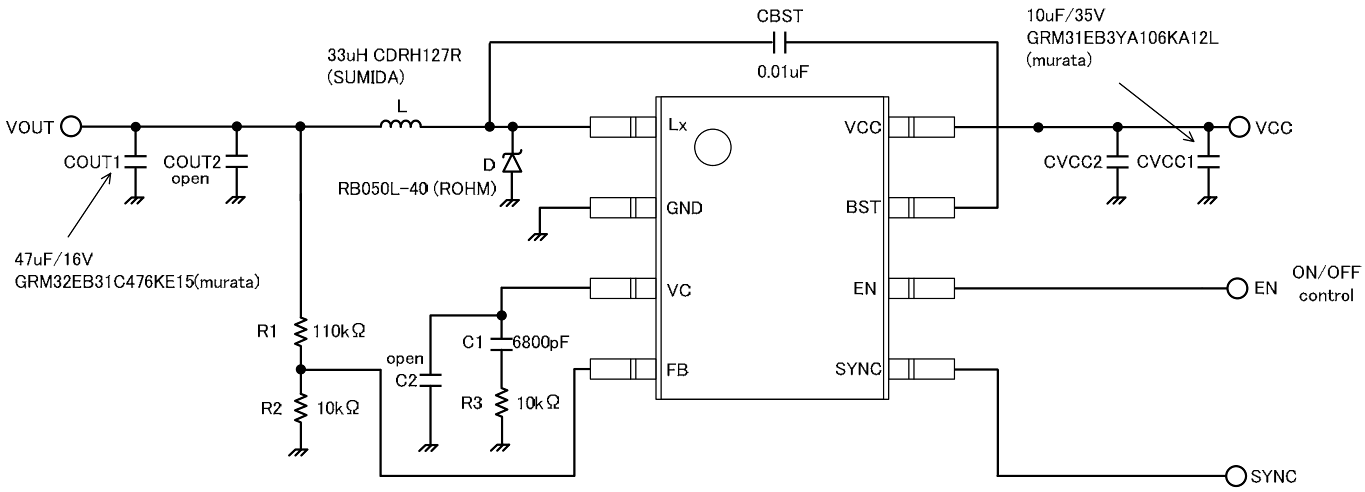


Figure 31. Reference Application Circuit

●**Reference Application Data** (Example of Reference Application Circuit)

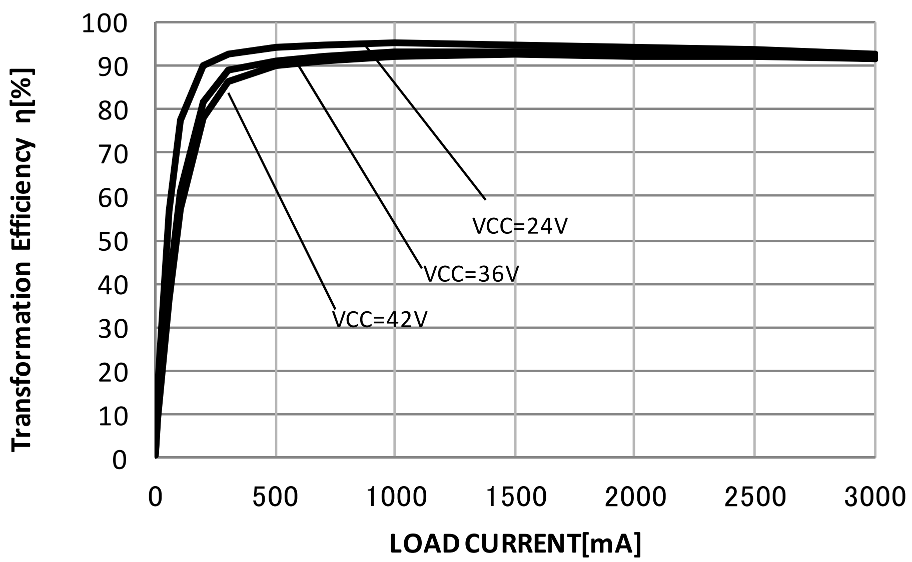


Figure 32. Electric Power Conversion Rate

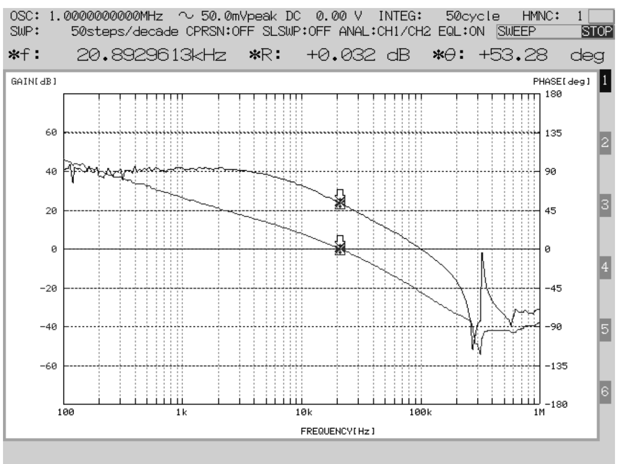


Figure 33. Frequency Response Characteristics (Io=0.5A)

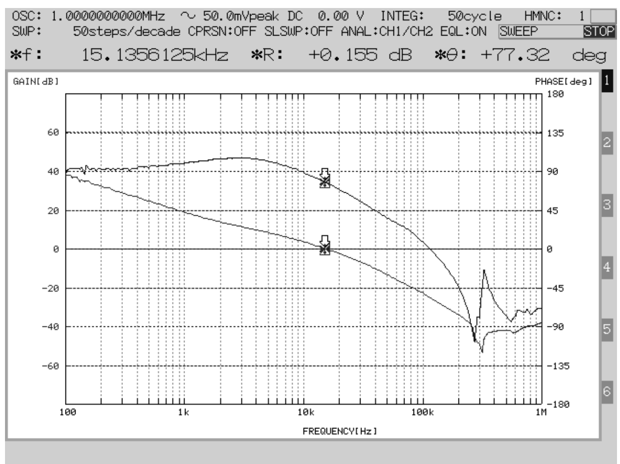


Figure 34. Frequency Response Characteristics (Io=3.0A)

●**Example of Reference Application Circuit** (Input 24V, Output 3.3V)

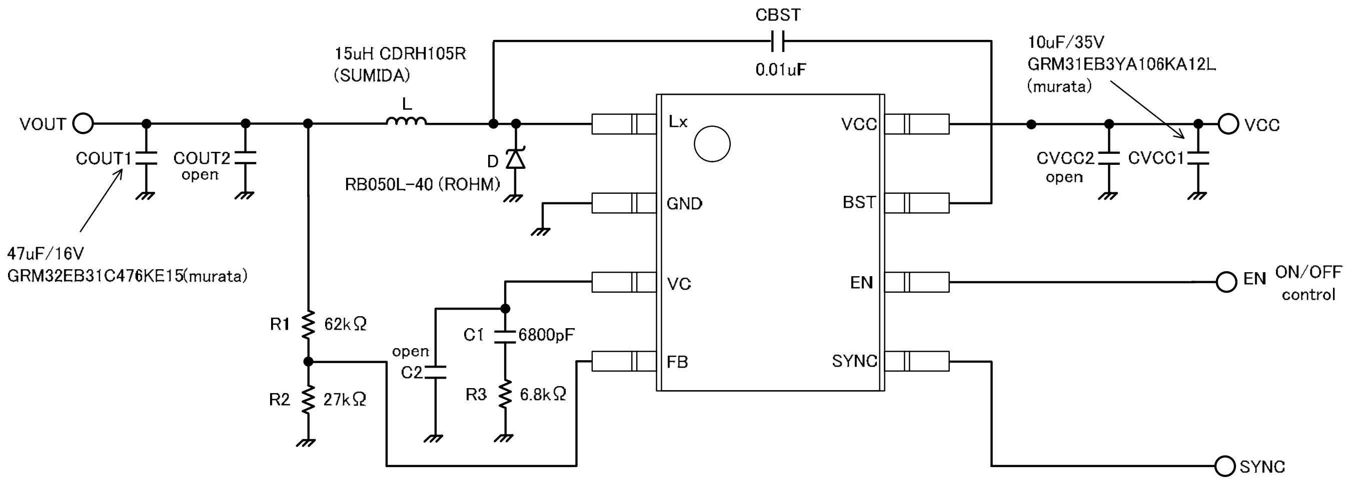


Figure 35. Reference Application Circuit

●**Reference Application Data** (Example of Reference Application Circuit)

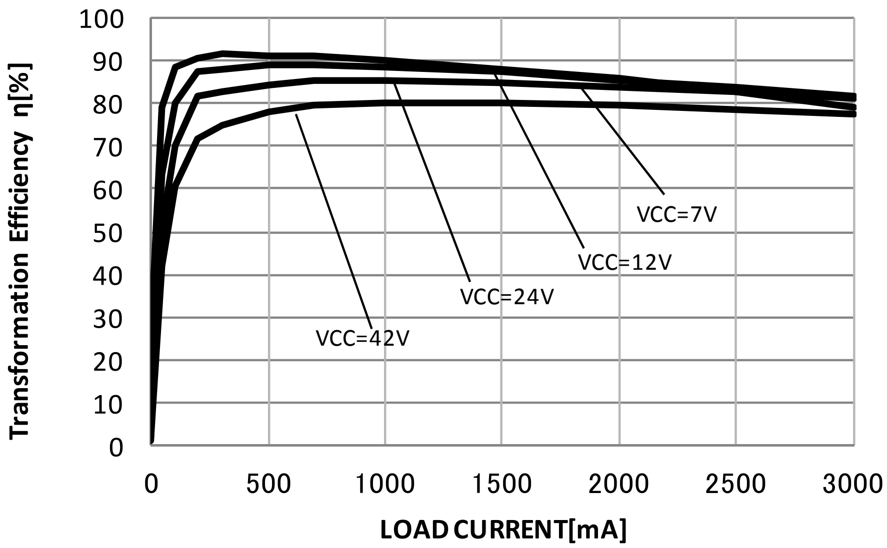


Figure 36. Electric Power
Conversion Rate

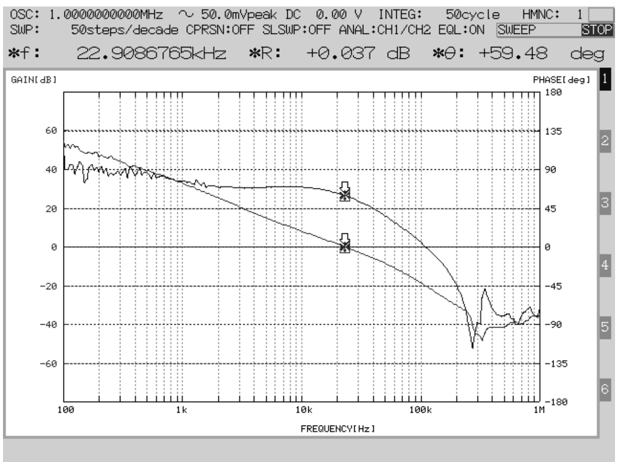


Figure 37. Frequency Response
Characteristics (Io=0.5A)

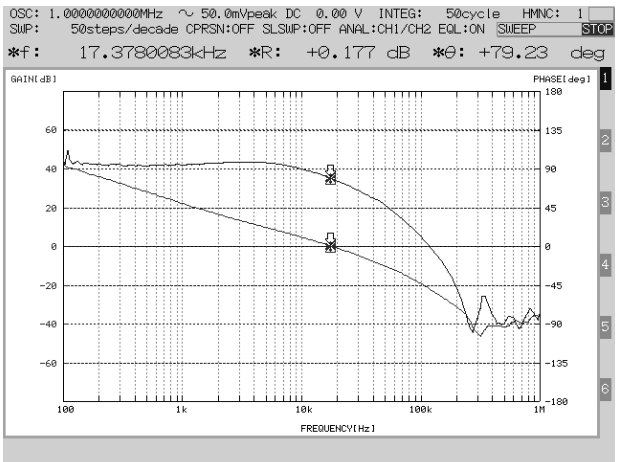


Figure 38. Frequency Response
Characteristics (Io=3.0A)

●**Example of Reference Application Circuit** (Input 24V, Output -12V)

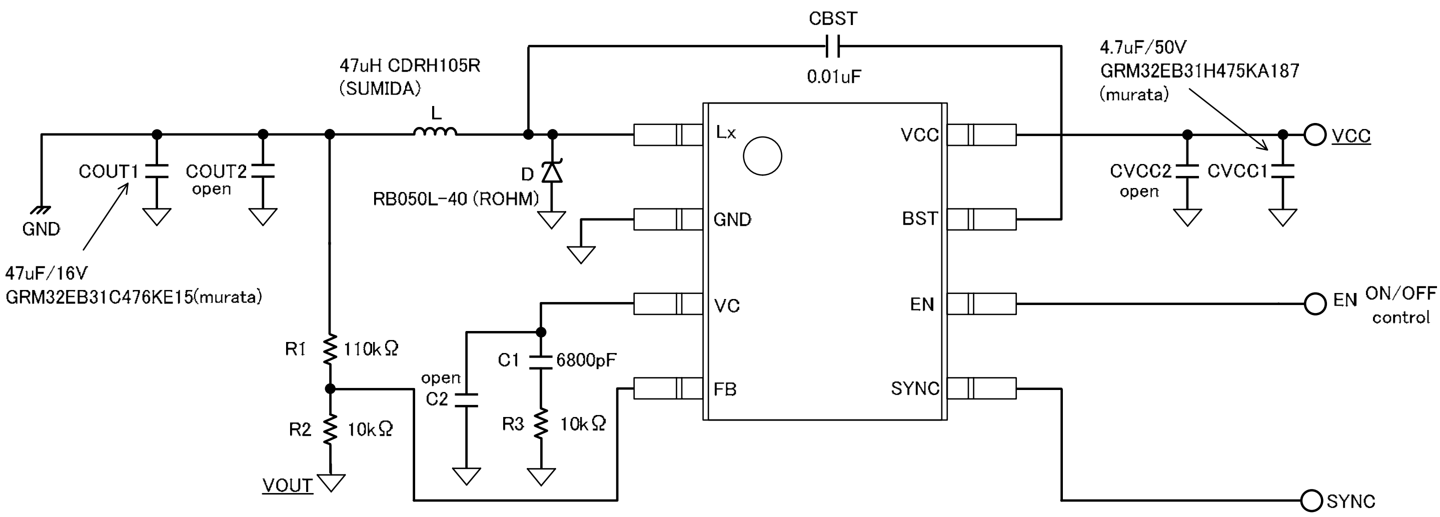


Figure 39. Reference Application Circuit

●**Reference Application Data** (Example of Reference Application Circuit)

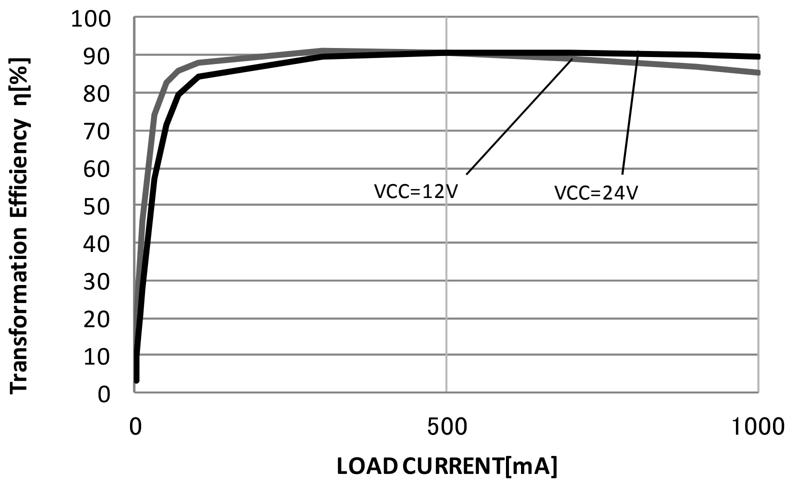
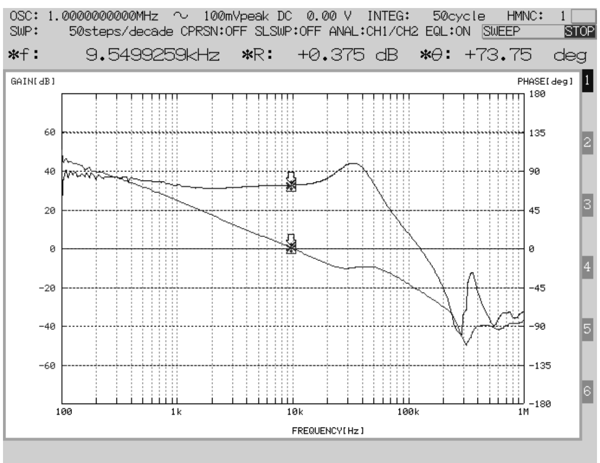


Figure 40. Electric Power
Conversion Rate



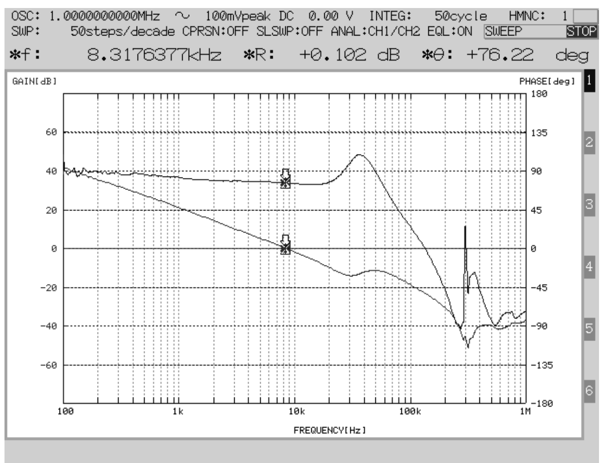


Figure 41. Frequency Response
Characteristics (Io=0.5A)

Figure 42. Frequency Response
Characteristics (Io=3.0A)

●Evaluation Board Pattern (Reference)

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VCC pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VCC pin, and the anode of the catch diode. See Fig.28 for a PCB layout example. The GND pin should be tied directly to the thermal pad under the IC and the thermal pad.

The thermal pad should be connected to any internal PCB ground planes using multiple VIAs directly under the IC. The LX pin should be routed to the cathode of the catch diode and to the output inductor. Since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

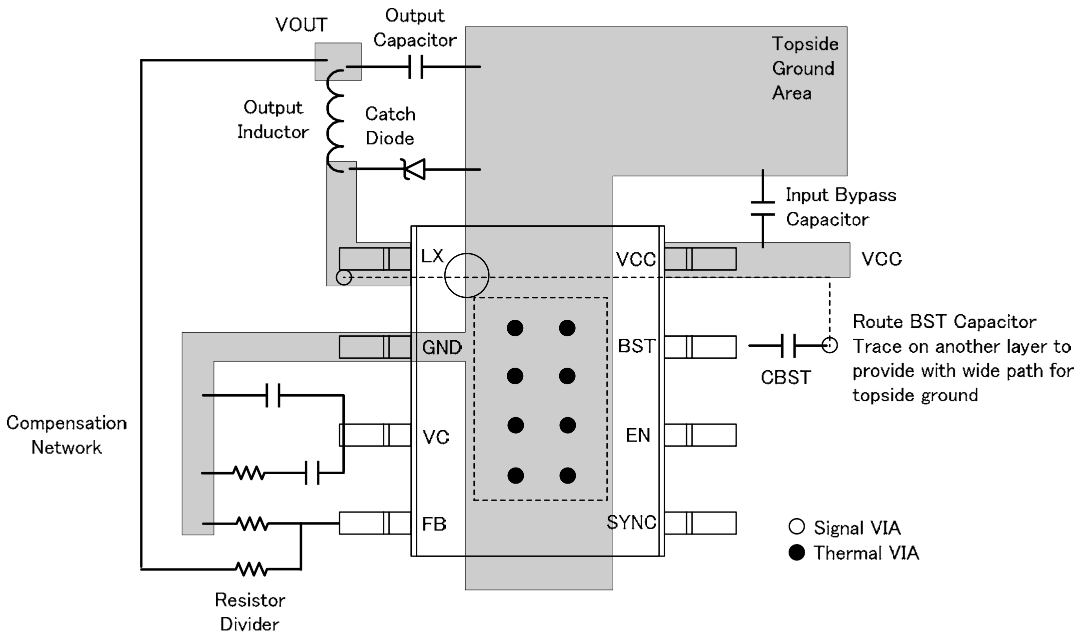


Figure 43. Evaluation Board Pattern

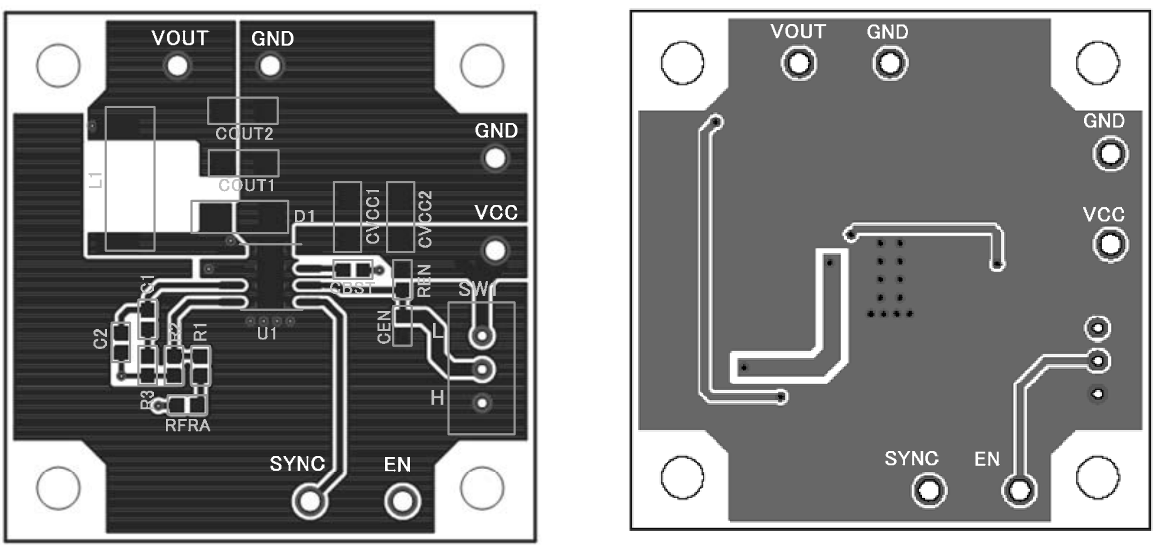


Figure 44. Reference Board Pattern

●Power Dissipation

It is shown below reducing characteristics of power dissipation to mount 70mm×70mm×1.6mm^t PCB
Junction temperature must be designed not to exceed 150℃.

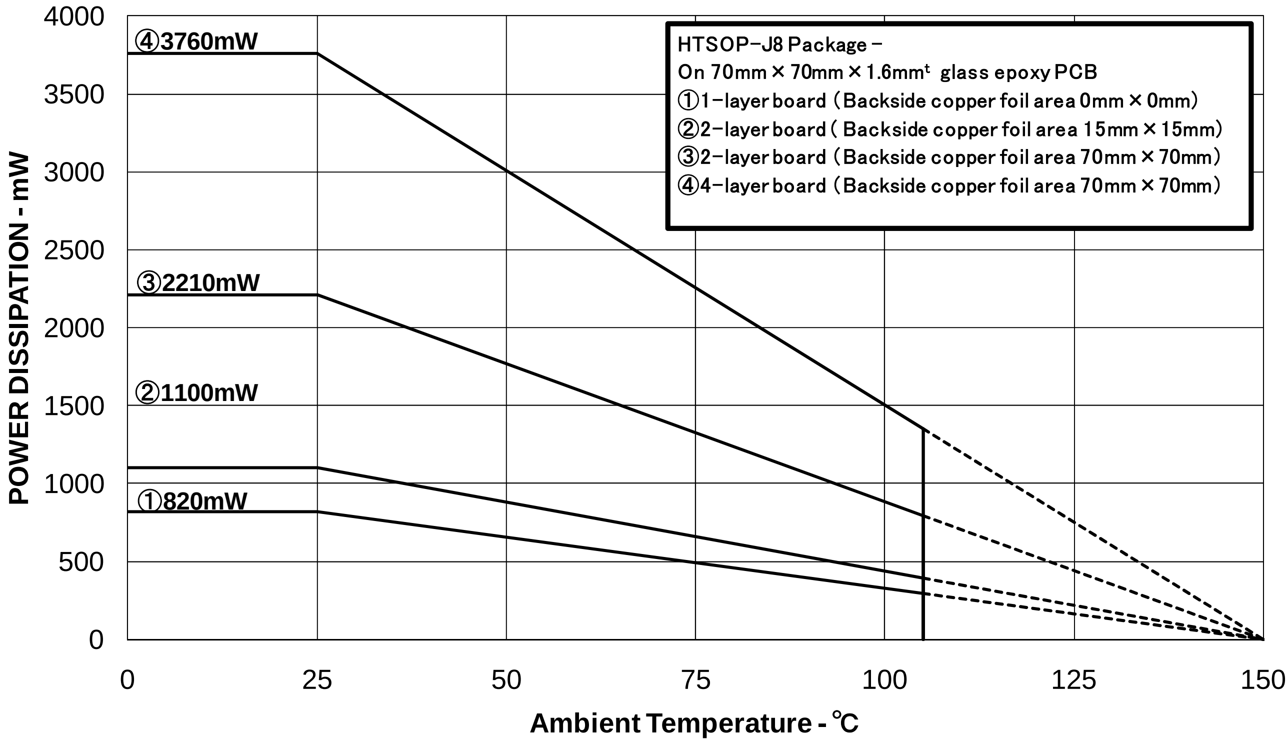


Figure 45. Power Dissipation (70mm × 70mm × 1.6mm^t 1layer PCB)

●Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous mode operations. They should not be used if the device is working in the discontinuous conduction mode.
The device power dissipation includes:
1) Conduction loss： Pcon = $IOUT^2$ × RonH × VOUT/VCC
2) Switching loss: Psw = 1.25 × 10^{-9} × VCC^2 × IOUT × fsw
3) Gate charge loss： Pgc = 22.8 × 10^{-9} × fsw
4) Quiescent current loss： Pq = 1.0 × 10^{-3} × VCC
Where:
IOUT is the output current (A), RonH is the on-resistance of the high-side MOSFET（Ω）, VOUT is the output voltage (V).
VCC is the input voltage (V), fsw is the switching frequency (Hz).
Therefore
Power dissipation of IC is the sum of above dissipation.
Pd = Pcon + Psw + Pgc + Pq
For given Tj, Tj =Ta + θja × Pd
Where:
Pd is the total device power dissipation (W), Ta is the ambient temperature (℃)
Tj is the junction temperature (℃), θja is the thermal resistance of the package (℃)

●Application Components Selection Method

(1) Inductor
Something of the shield Type that Fulfills the Current Rating (Current value Ipecac below), with low DCR (Direct Current Resistance element) is recommended.
Value of Inductor influences Inductor Ripple Current and becomes the cause of Output Ripple.
In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

$$I_{peak} = I_{out} + \Delta I_L/2 \ [A] \quad (1)$$

$$\Delta I_L = \frac{V_{in} - V_{out}}{L} \times \frac{V_{out}}{V_{in}} \times \frac{1}{f} \ [A] \quad (2)$$

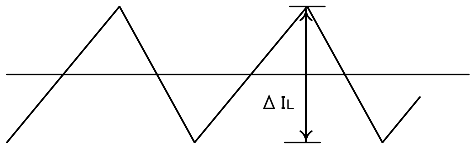


Figure 46. Inductor Current

(η: Efficiency, ⊿IL: Output Ripple Current, f: Switching Frequency)

For design value of Inductor Ripple Current, please carry out design tentatively with about 20%～50% of Maximum Input Current.

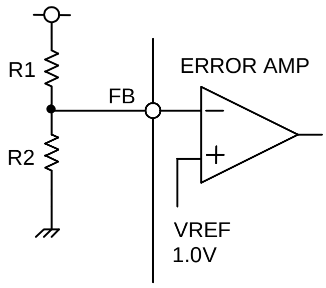
※When current that exceeds Coil rating flows to the coil, the Coil causes a Magnetic Saturation, and there are cases wherein a decline in efficiency, oscillation of output happens. Please have sufficient margin and select so that Peak Current does not exceed Rating Current of Coil.

(2) Output Capacitor
In order for Capacitor to be used in Output to reduce Output Ripple, Low Ceramic Capacitor of ESR is recommended.
Also, for Capacitor Rating, on top of putting into consideration DC Bias Characteristics, please use something whose Maximum Rating has sufficient margin with respect to the Output Voltage.
Output Ripple Voltage is looked for using the following formula.

$$V_{pp} = \Delta I_L \times \frac{1}{2\pi \times f \times C_o} + \Delta I_L \times R_{ESR} \quad [V] \quad \cdots \quad (3)$$

Please design in a way that it is held within Capacity Ripple Voltage.

(3) Output Voltage Setting
ERROR AMP internal Standard Voltage is 1.0V. Output Voltage is determined as seen in (4) formula.



$$V_o = \frac{(R1+R2)}{R2} \times 1.0 \ [V] \quad \cdots \quad (4)$$

Figure 47.Voltage Return Resistance Setting Method

(4) Bootstrap Capacitor
Please connect from 0.01µF (Laminate Ceramic Capacitor) between BST Pin and Lx Pins.

(5) Schottky diode

Recommend selecting a diode which is satisfied with maximum input voltage of the application, and which is larger than maximum current rating. If Vf of Schottky diode is large, there is a possibility that Vf of internal parasitic diode and Vf of Schottky diode reverse and might cause IC error operation when increasing a difference in temperature with IC. Recommend using a diode with smaller Vf as possible, and location is recommended to be nearest to the pin.
BD9876AEFJ use below diode is recommended.

品番	V_{RM}[V]	I_O[A]	V_F[V]	I_R[mA]
RB050L-40	40	3	0.55	1
RB055L-30	30	3	0.55	3

(6) About Adjustment of DC/DC Comparator Frequency Characteristics

Role of Phase compensation element C1, C2, R3 (See P.7. Example of Reference Application Circuit)

Stability and Responsiveness of Loop are controlled through VC Pin which is the output of Error Amp.
The combination of zero and pole that determines Stability and Responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC Pin.

DC Gain of Voltage Return Loop can be calculated for using the following formula.

$$Adc = Rl \times Gcs \times A_{EA} \times \frac{V_{FB}}{Vout}$$

Here, VFB is Feedback Voltage (1.0V).A_{EA} is Voltage Gain of Error amplifier (typ: 77dB),
Gcs is the Trans-conductance of Current Detect (typ: 10A/V), and Rl is the Output Load Resistance value.

There are 2 important poles in the Control Loop of this DC/DC.
The first occurs with/ through the output resistance of Phase compensation Capacitor (C1) and Error amplifier.
The other one occurs with/through the Output Capacitor and Load Resistor.
These poles appear in the frequency written below.

$$fp1 = \frac{G_{EA}}{2\pi \times C1 \times A_{EA}}$$

$$fp2 = \frac{1}{2\pi \times COUT \times Rl}$$

Here, G_{EA} is the trans-conductance of Error amplifier (typ: 220 µA/V).

Here, in this Control Loop, one zero becomes important. With the zero which occurs because of Phase compensation Capacitor C1 and Phase compensation Resistor R3, the Frequency below appears.

$$fz1 = \frac{1}{2\pi \times C1 \times R3}$$

Also, if Output Capacitor is big, and that ESR (RESR) is big, in this Control Loop, there are cases when it has an important, separate zero (ESR zero).
This ESR zero occurs due to ESR of Output Capacitor and Capacitance, and exists in the Frequency below.

$$fz_{ESR} = \frac{1}{2\pi \times COUT \times RESR} \quad \text{(ESR zero)}$$

In this case, the 3rd pole determined with the 2nd Phase compensation Capacitor (C2) and Phase Correction Resistor (R3) is used in order to correct the ESR zero results in Loop Gain.
This pole exists in the frequency shown below.

$$fp3 = \frac{1}{2\pi \times C2 \times R3} \quad \text{(Pole that corrects ESR zero)}$$

The target of Phase compensation design is to create a communication function in order to acquire necessary band and Phase margin.

Cross-over Frequency (band) at which Loop gain of Return Loop becomes “0” is important.
When Cross-over Frequency becomes low, Power supply Fluctuation Response, Load Response, etc worsens.
On the other hand, when Cross-over Frequency is too high, instability of the Loop can occur.
Tentatively, Cross-over Frequency is targeted to be made 1/20 or below of Switching Frequency.
Selection method of Phase Compensation constant is shown below.

1. Phase Compensation Resistor (R3) is selected in order to set to the desired Cross-over Frequency.
   Calculation of RC is done using the formula below.

$$R3 = \frac{2\pi \times COUT \times fc}{GEA \times GCS} \times \frac{Vout}{VFB}$$

   Here, fc is the desired Cross-over Frequency. It is made about 1/20 and below of the Normal Switching Frequency (fs).

2. Phase compensation Capacitor (C1) is selected in order to achieve the desired phase margin.
   In an application that has a representative Inductance value (about several µH∼20µH), by matching zero of compensation to 1/4 and below of the Cross-over Frequency, sufficient Phase margin can be acquired. C1 can be calculated using the following formula.

$$C1 > \frac{4}{2\pi \times R3 \times fc}$$

   RC is Phase compensation Resistor.

3. Examination whether the second Phase compensation Capacitor C2 is necessary or not is done.
   If the ESR zero of Output Capacitor exists in a place that is smaller than half of the Switching Frequency, a second Phase compensation Capacitor is necessary. In other words, it is the case wherein the formula below happens.

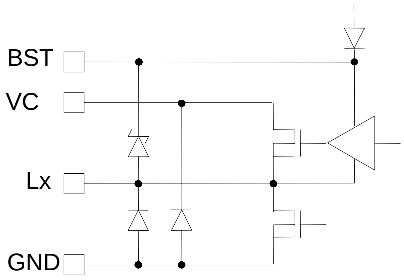
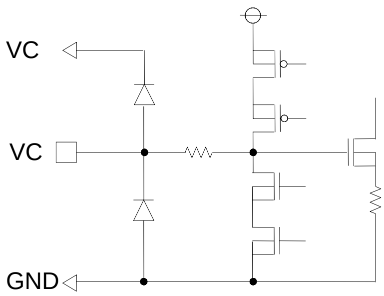
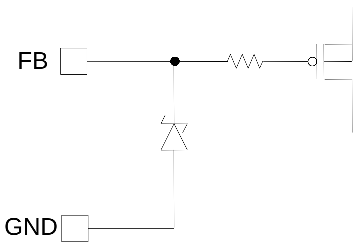
$$\frac{1}{2\pi \times COUT \times RESR} < \frac{fs}{2}$$

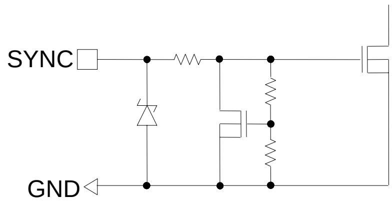
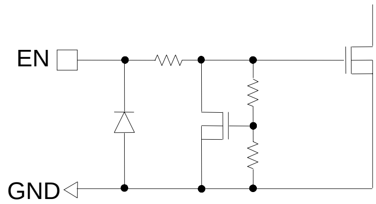
   In this case, add the second Phase compensation Capacitor C2, and match the frequency of the third pole to the Frequency fp3 of ESR zero.

   C2 is looked for using the following formula.

$$C2 = \frac{COUT \times RESR}{R3}$$

●I/O Equivalent Schematic

Pin. No	Pin. Name	Pin Equivalent Schematic
1 2 7 8	Lx GND BST VCC	
3	VC	
4	FB	

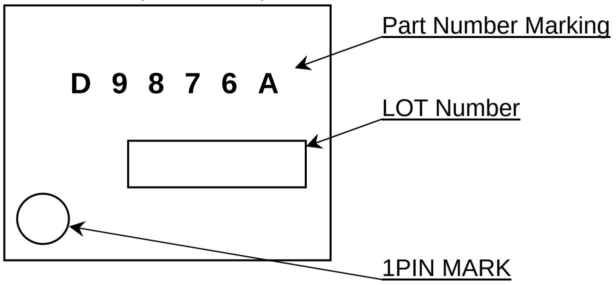
Pin. No	Pin. Name	Pin Equivalent Schematic
5	SYNC	
6	EN	

●Ordering part number

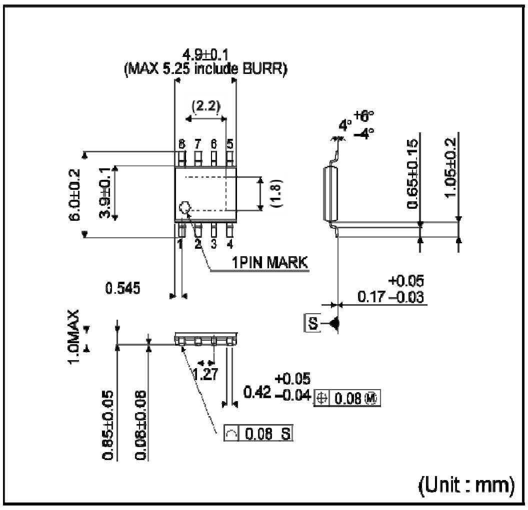
B	D	9	8	7	6	A	E	F	J	-	E 2

- Part Number
- package
  EFJ : HTSOP-J8
- Packaging and forming specification
  E2: Embossed tape and reel

●External information

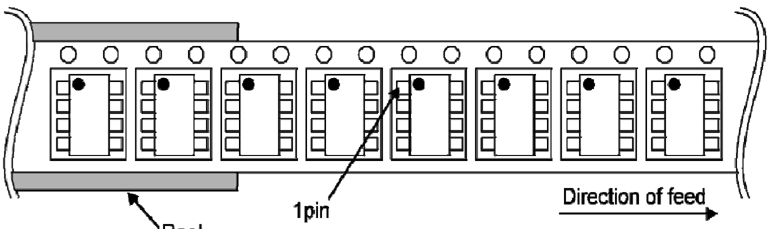


HTSOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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