

Omnipolar Detection Hall IC

(Dual Outputs for both S and N Pole Polarity Detection)

BU52777GWZ

General Description

The omnipolar detection Hall IC incorporating a polarity determination circuit enables separate operation (output) of both the South and North poles. Using a magnet and the device, detection of open and close of the cover are possible in smart phones and tablets, and detection of putting wireless earphones in a case, and detection of front/back side or rotational direction are possible in digital cameras and other applications involving display panels.

Features

- Omnipolar Detection (OUT1 = S-pole Detection; OUT2 = N-pole Detection)
- Micro Power Operation (Small Current Using Intermittent Operation Method)
- Ultra-compact Package

Applications

- Smart Phones, Tablets, Wireless Earphones, Notebook Computers, Digital Cameras, etc.

Key Specifications

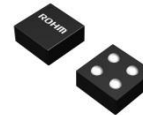
- VDD Voltage Range: 2.5 V to 4.5 V
- Operate Point: ± 15 mT (Typ)
- Hysteresis: 2 mT (Typ)
- Period: 50 ms (Typ)
- Supply Current (AVG): 1.7 μ A (Typ)
- Output Type: CMOS
- Operating Temperature Range: -40 °C to +85 °C

Package

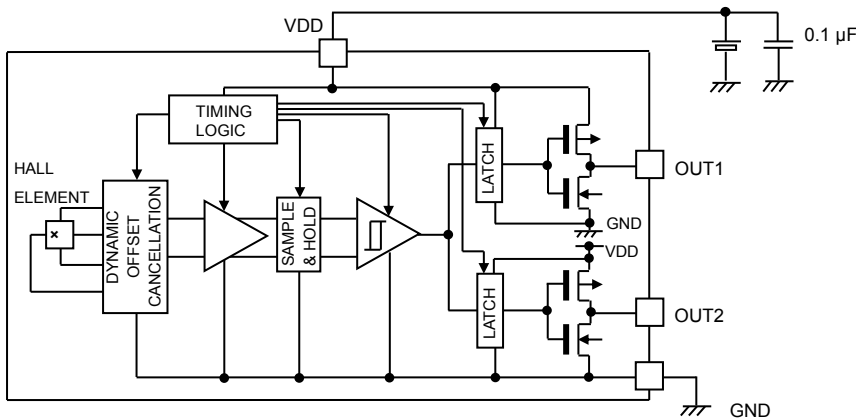
UCSP35L1

W(Typ) x D(Typ) x H(Max)

0.80 mm x 0.80 mm x 0.40 mm



Typical Application Circuit and Block Diagram



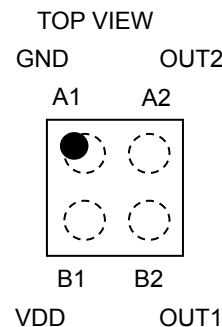
Adjust the bypass capacitor value as necessary, according to power supply noise conditions, etc.

Pin Descriptions

Pin No.	Pin Name	Function
A1	GND	Ground
A2	OUT2	Output (Detect to the north pole)
B1	VDD	Power supply ^(Note 1)
B2	OUT1	Output (Detect to the south pole)

(Note 1) Dispose a bypass capacitor between VDD and GND.

Pin Configurations



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

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Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V _{DD}	7.0	V
Output Current	I _{OUT}	±0.5	mA
Power Dissipation	P _d	0.10	W
Storage Temperature Range	T _{stg}	-40 to +125	°C
Maximum Junction Temperature	T _{Jmax}	125	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V _{DD}	2.5	3.0	4.5	V
Operating Temperature	T _{opr}	-40	+25	+85	°C

Magnetic and Electrical Characteristics (Unless otherwise specified V_{DD} = 3.0 V Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operate Point	B _{OPS}	-	15	17	mT	Output: OUT1 (Detect to the south pole)
	B _{OPN}	-17	-15	-		Output: OUT2 (Detect to the north pole)
Release Point	B _{RPS}	11	13	-	mT	Output: OUT1 (Detect to the south pole)
	B _{RPN}	-	-13	-11		Output: OUT2 (Detect to the north pole)
Hysteresis	B _{HYSS}	-	2	-	mT	-
	B _{HYSN}	-	2	-		-
Period	t _P	-	50	100	ms	-
Output High Voltage	V _{OH}	V _{DD} -0.2	-	-	V	I _{OUT} = -0.5 mA
Output Low Voltage	V _{OL}	-	-	0.2	V	I _{OUT} = +0.5 mA
Supply Current	I _{DD}	-	1.7	3.5	μA	Average

(Note) Polarity of Magnetic flux density is defined as positive when south pole side of magnet approaches top surface of the device.

Measurement Circuit

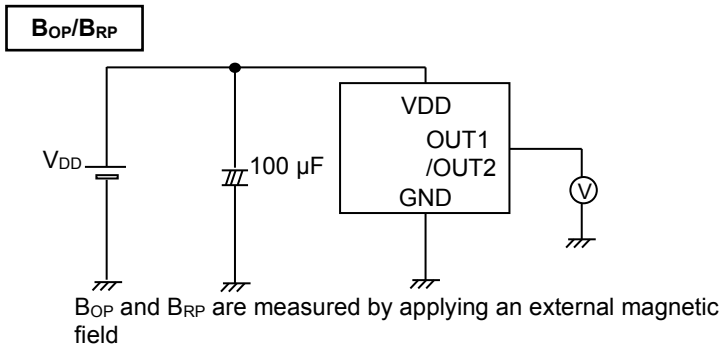


Figure 1. B_{OP}, B_{RP} Measurement Circuit

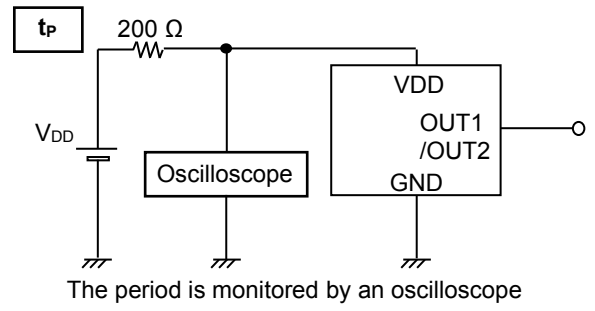


Figure 2. t_p Measurement Circuit

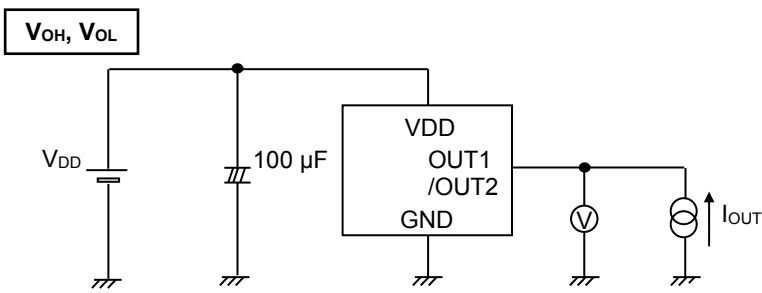


Figure 3. V_{OH}, V_{OL} Measurement Circuit

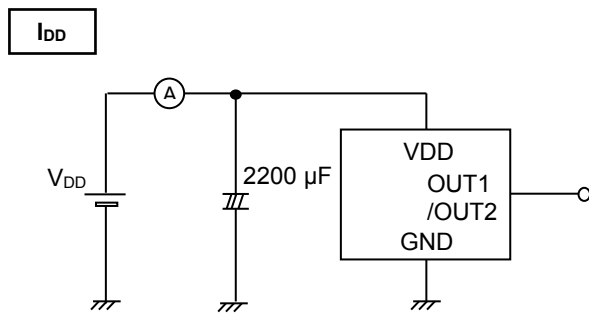


Figure 4. I_{DD} Measurement Circuit

Typical Performance Curves

(Reference data)

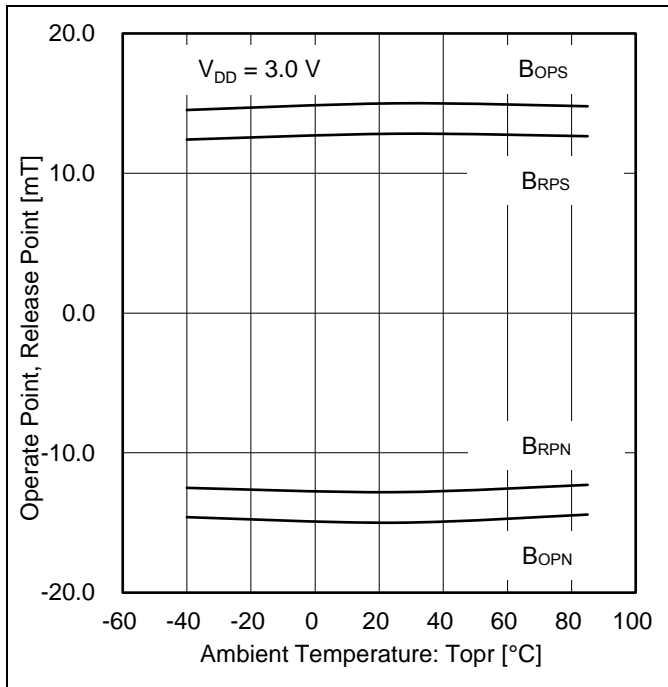


Figure 5. Operate Point, Release Point vs Ambient Temperature

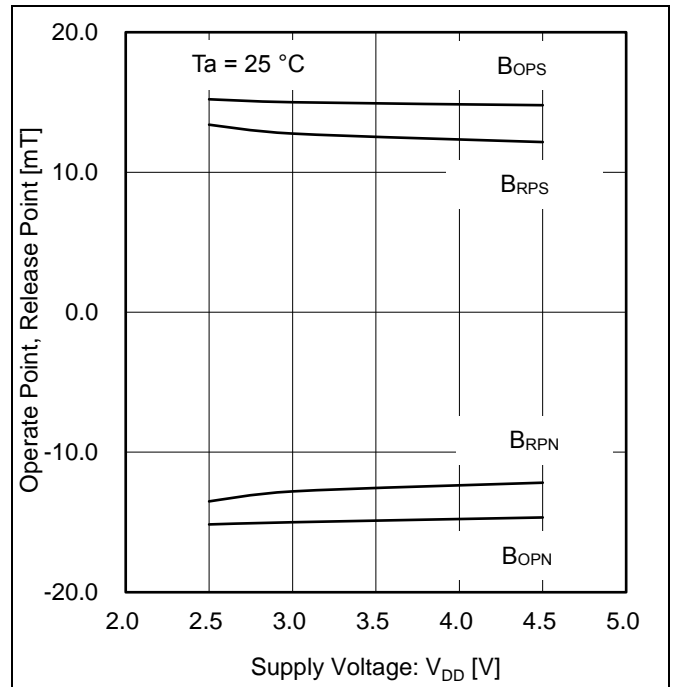


Figure 6. Operate Point, Release Point vs Supply Voltage

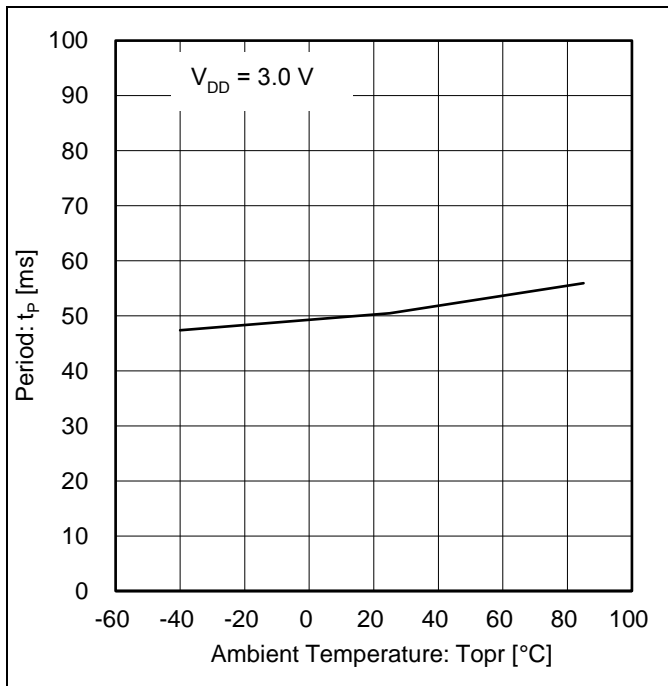


Figure 7. Period vs Ambient Temperature

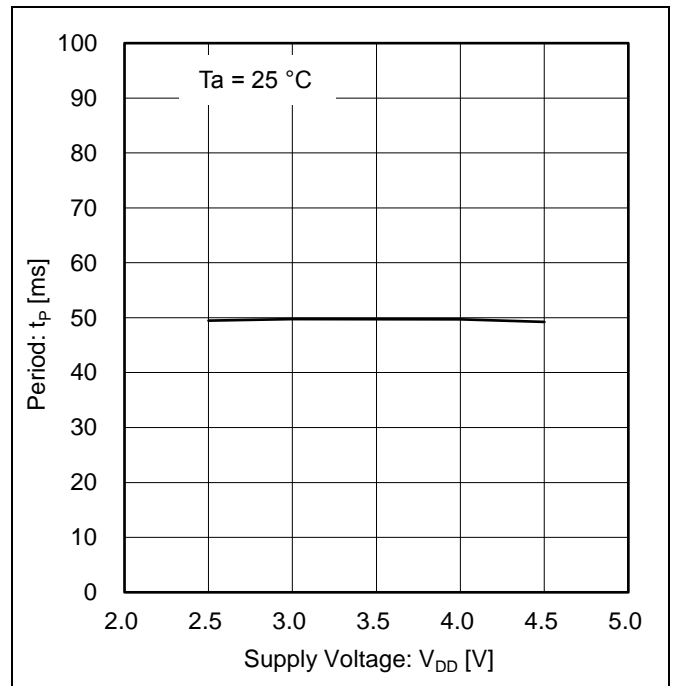


Figure 8. Period vs Supply Voltage

Typical Performance Curves - continued
(Reference data)

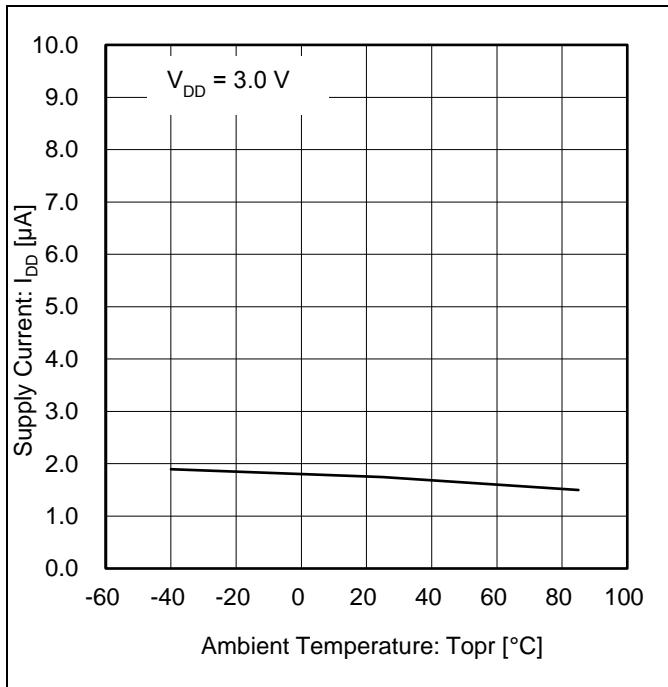


Figure 9. Supply Current vs Ambient Temperature

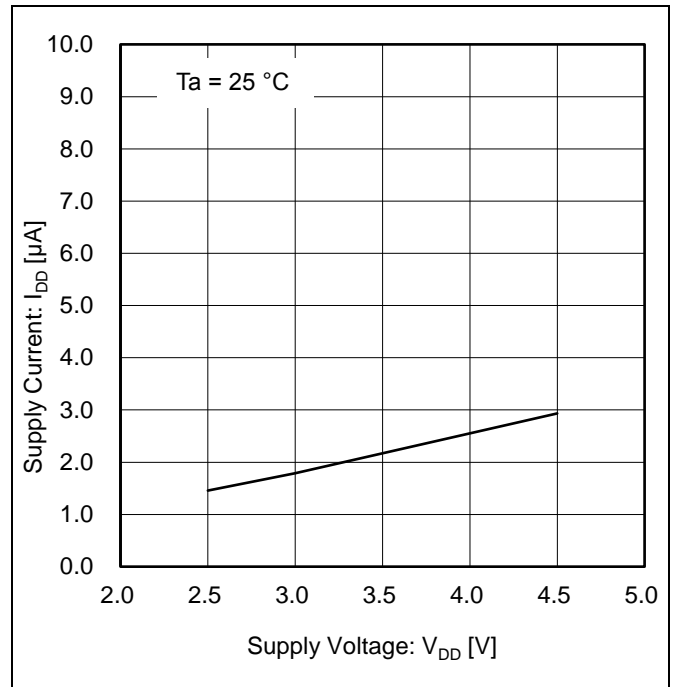


Figure 10. Supply Current vs Supply Voltage

Description of Operations

Micropower Operation (Small Current Consumption Using Intermittent Sensing)

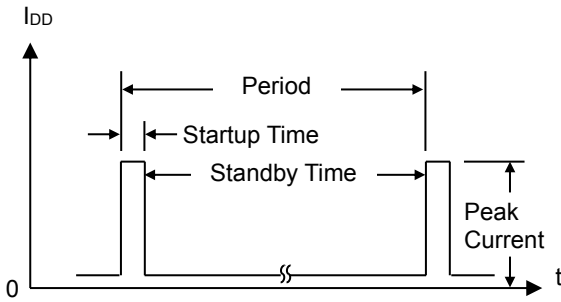


Figure 11. Timing Chart of Micropower Operation

The omnipolar detection Hall IC uses intermittent sensing save energy. At startup, the Hall elements, amplifier, comparator, and other detection circuits powered on and magnetic detection begins. During standby, the detection circuits powered off, thereby reducing current consumption. The detection results are held and output during standby time.

$$Period: t_p \text{ [ms]}$$

$$Startup \text{ Time: } \frac{t_p}{8192} \times 2 \text{ [ms]}$$

$$Peak \text{ Current: } 12 \text{ [mA]}$$

(Peak Current is reference data. This is not 100 % tested.)

(Offset Cancellation)

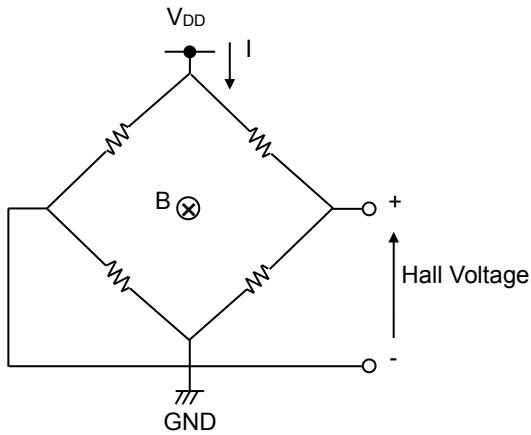


Figure 12. Equivalent Circuit of Hall Elements

The Hall elements are shown with an equivalent Wheatstone (resistor) bridge circuit. Offset voltage may be generated by a differential in this bridge resistance, or can arise from changes of resistance due to package or bonding stress. A dynamic offset cancellation circuit is employed to cancel this offset voltage.

When the Hall elements are connected as shown in Figure 12 and a magnetic field is applied perpendicular to the Hall elements, a voltage is generated at the mid-points of the bridge. This is known as Hall voltage.

Dynamic offset cancellation switches the wiring (shown in the figure 12) to redirect the current flow to a 90 ° angle from its original path, and thereby cancels the offset voltage of Hall. Only the magnetic signal is maintained in the sample/hold circuit process and then released.

Description of Operations - continued

(Magnetic Field Detection Mechanism)

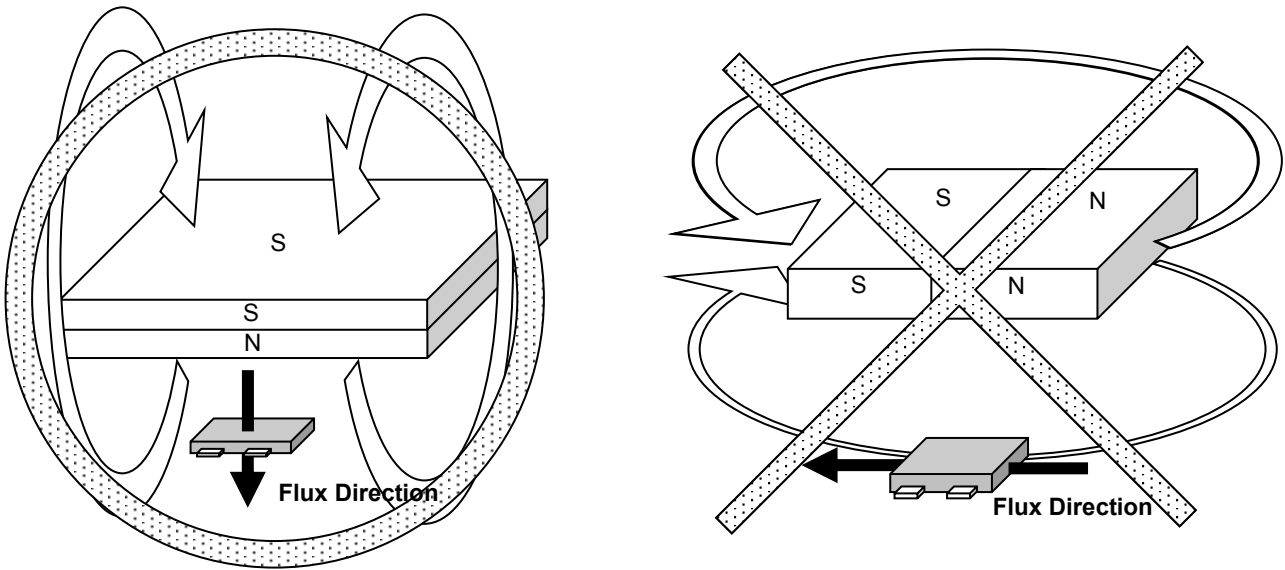


Figure 13. Direction of the Detectable Magnetic Field

The Hall IC cannot detect magnetic fields that run horizontal to the package top layer. Be certain to configure the Hall IC so that the magnetic field is perpendicular to the top layer.

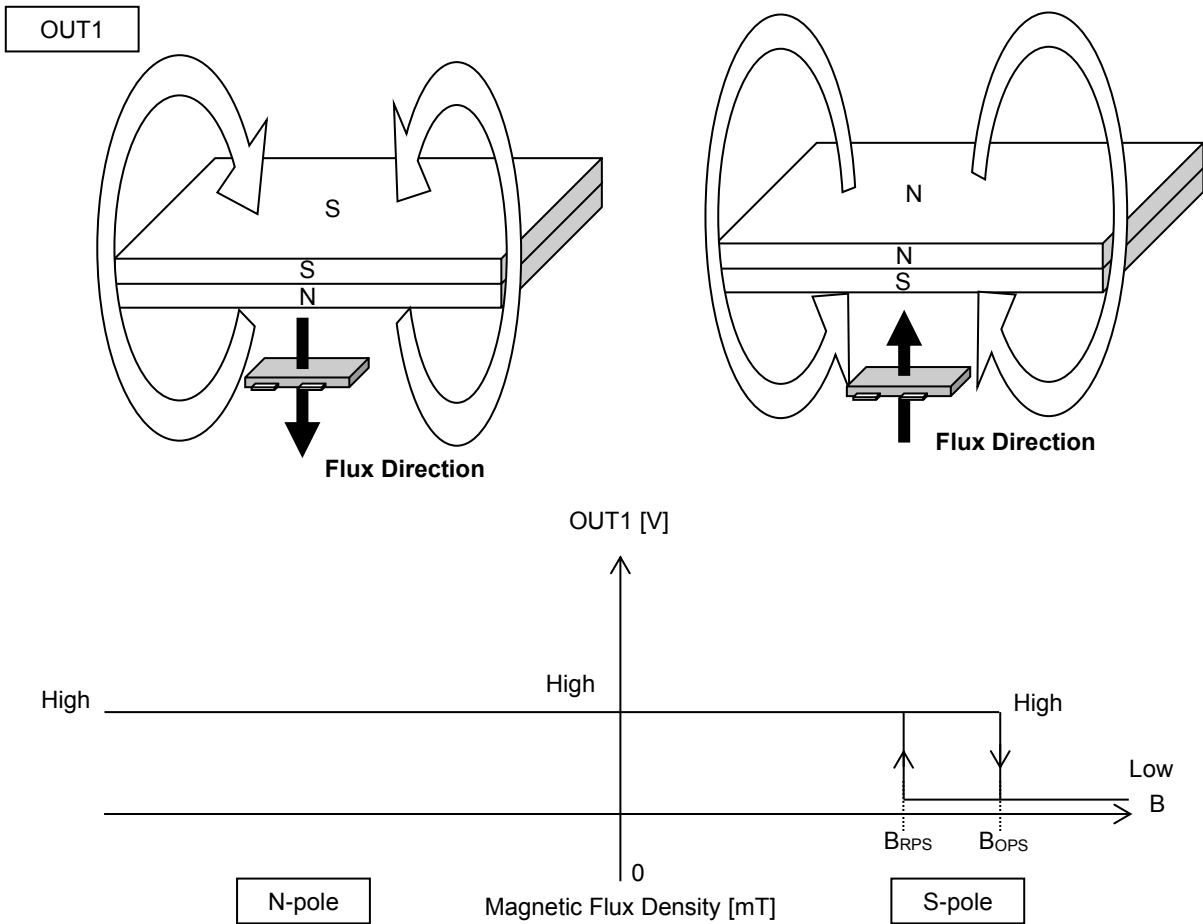


Figure 14. S-pole Detection

OUT1 detects only S pole magnetic field. (OUT1 doesn't detect N pole.)

Description of Operations - continued

OUT2

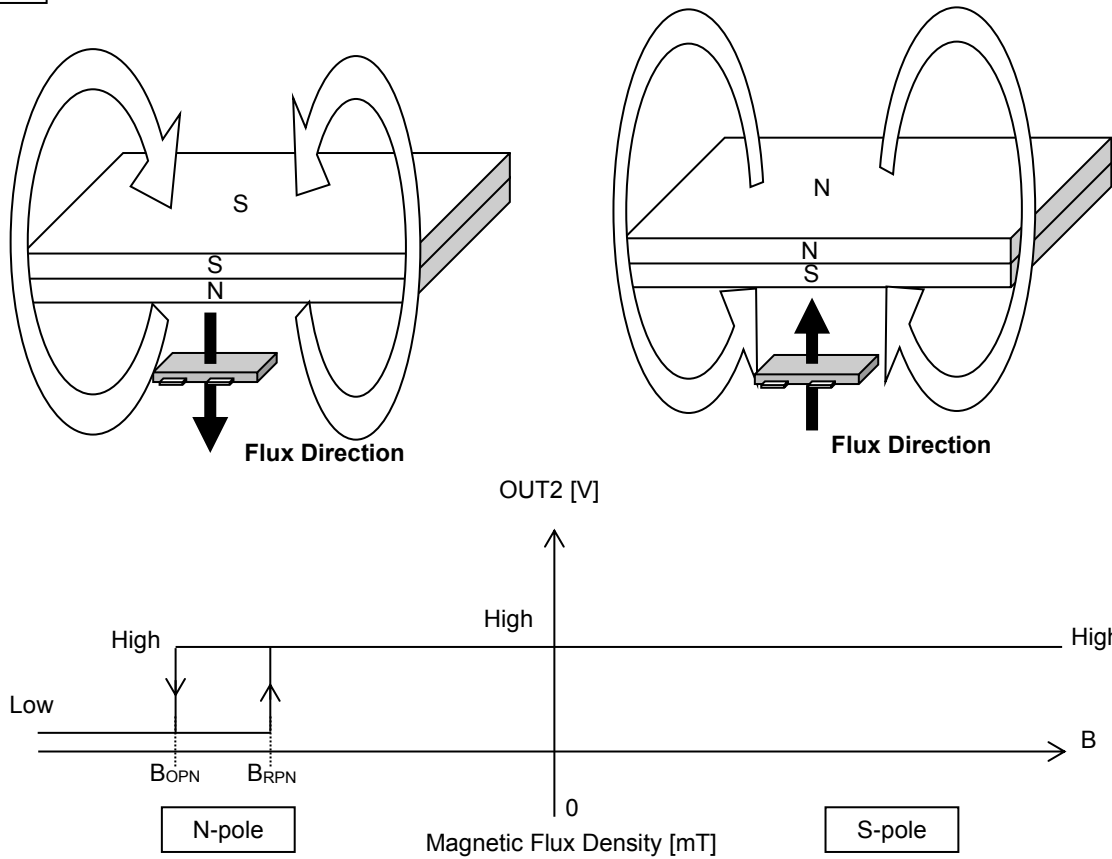


Figure 15. N-pole Detection

OUT2 detects only N pole magnetic field. (OUT2 doesn't detect S pole.)

The dual output omnipolar detection Hall IC detects magnetic fields running perpendicular to the top surface of the package. When the distance between magnet and Hall IC is far and magnetic flux density is smaller than the operate point (B_{OP}), output goes HIGH. When the magnet gets closer to the IC and magnetic density rises to the operate point, the output switches LOW. In LOW output mode, the distance from the magnet to the IC increases again until the magnetic density falls to a point just below B_{OP} , and output returns HIGH. The point where magnetic flux density restores a HIGH output is known as the release point, B_{RP} . This detection and adjustment mechanism is designed to prevent noise and other erratic system operation.

Intermittent Operation at Power ON

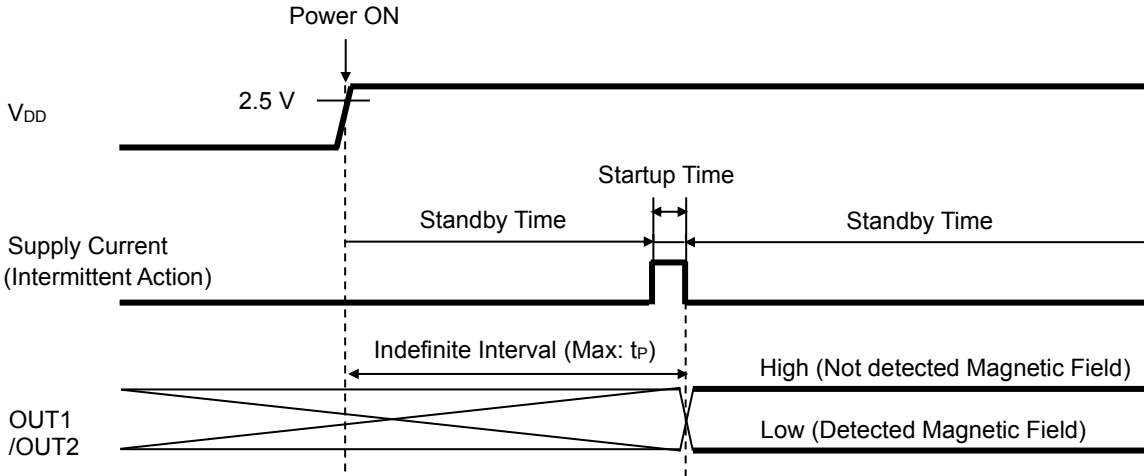


Figure 16. Timing Chart of Intermittent Operation at Power ON

The omnipolar detection Hall IC adopts an intermittent operation method in detecting the magnetic field during startup, as shown in Figure 16. The IC outputs the detection result and maintains the output condition during the standby period. The output is an indefinite interval from power ON to the first end of startup (Max: t_P).

Magnet Selection

Neodymium and ferrite are major permanent magnets. Neodymium generally offers greater magnetic power per volume than ferrite, thereby enabling miniaturization of magnet. The larger neodymium magnet is, the stronger magnetic flux density is. And the farther detection distance is, the weaker it is. Therefore, the proper size and detection distance of the magnet should be determined according to the operate point of Hall IC. To increase the magnet's detection distance, the magnet which is thicker or larger sectional area is used.

Position of the Hall Element
(Reference)

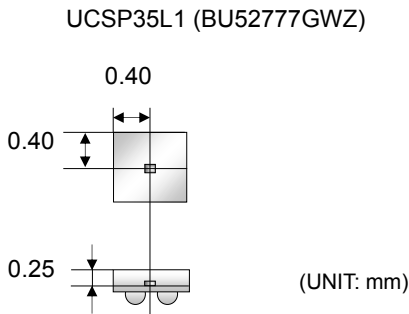


Figure 17. Position of the Hall Element

Output Equivalence Circuit

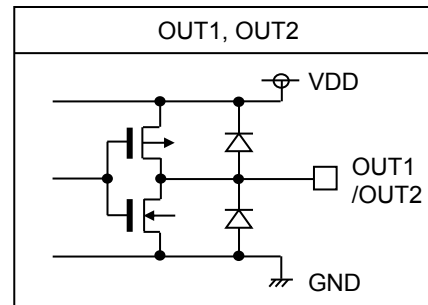


Figure 18. Output Equivalence Circuit

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

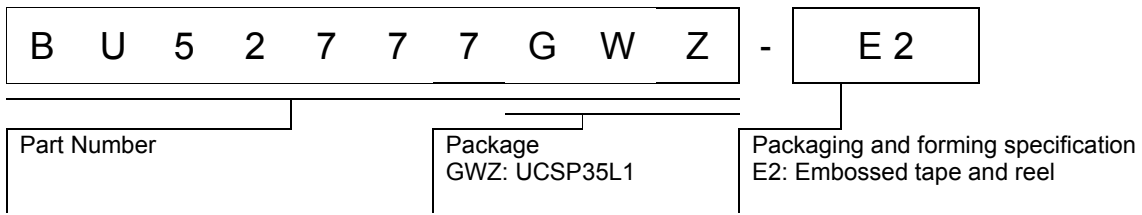
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

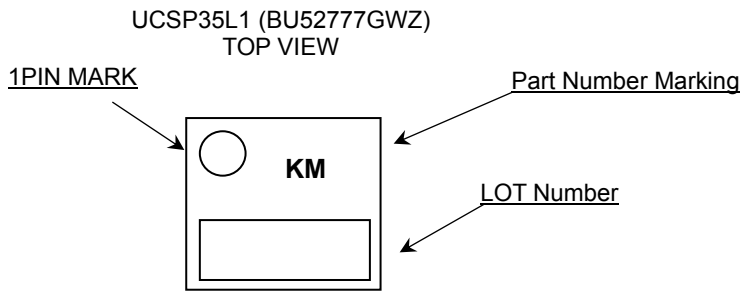
12. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information



Marking Diagrams



Revision History

Date	Revision	Changes
11.Mar.2021	001	New Release

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 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
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- Confirm that operation temperature is within the specified range described in the product specification.
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