Structure : Silicon Monolithic Integrated Circuit
Product Name : Power Driver For CD Players

Device Name : **BA5968FP**

Features :

- 5-ch driver comprising of 4 channels for BTL drivers and 1 channel for reversible drivers
- Use of the HSOP-28PIN power package allows downsizing of the set.
- A built-in thermal shutdown circuit installed.
- A wide dynamic range (6.0V (Typ.) when VCC=8V, RL=8Ω)

<BTL Driver>

- For 2 of 4 channels, the input terminal is connected to the general OP-AMP, which allows a differential input and the addition of signals.

<Loading Driver>

- A built-in brake function installed
- A built-in diode for protecting against over-voltage caused by a counter electromotive force
- The output voltage control terminal (LDCTL) is used to control the output voltage. (Applicable only to the voltage on the 'H' side)

○ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	Vcc	13.5	V
Power Dissipation	Pd	1.7 *1	W
Operating Temperature Range	Topr	-40 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

*1 When mounted on the glass/epoxy board with the size: 70 mm×70 mm, the thickness: 1.6 mm, and the rate of copper foil occupancy area: 3% or less.
Over Ta=25°C, derating at the rate of 13.6mV/°C.

○ RECOMMENDED OPERATING CONDITIONS
(To determine a power supply voltage, the power dissipation must be taken into consideration.)

VCC	4.3 to 9V

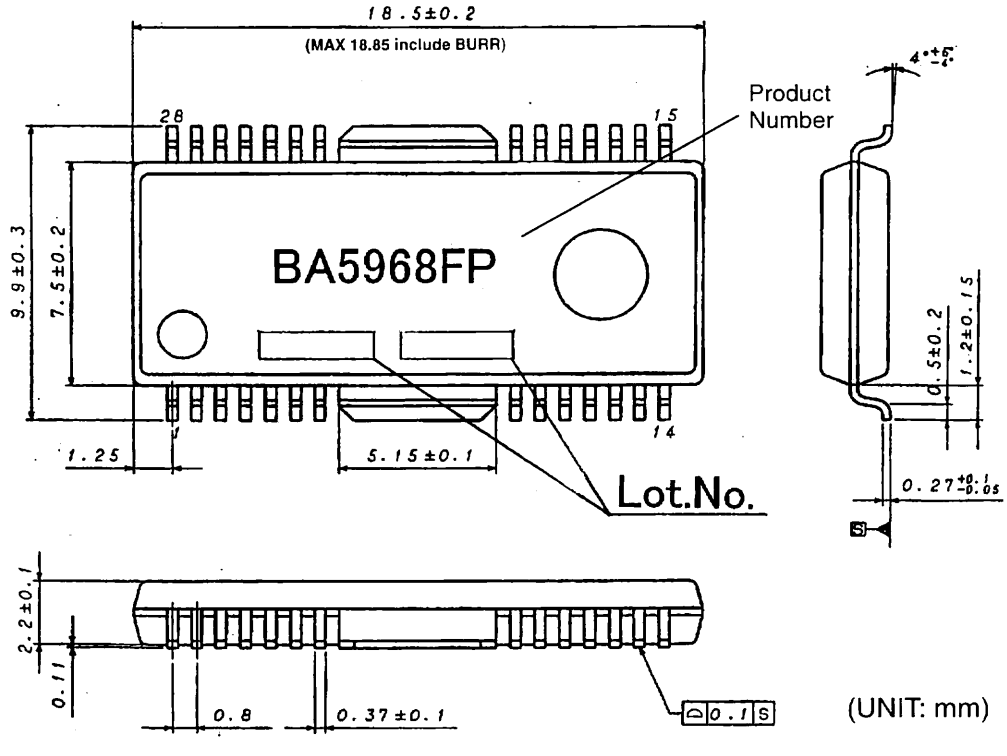
This product has not been checked for the strategic materials (or service) defined in the Foreign Exchange and Foreign Trade Control Low of Japan so that a verification work is required before exporting it.
Not designed for radiation resistance.

O ELECTRIC CHARACTERISTICS

(Ta=25°C, Vcc=8V, BIAS=2.5V, RL=8Ω, unless otherwise noted.)

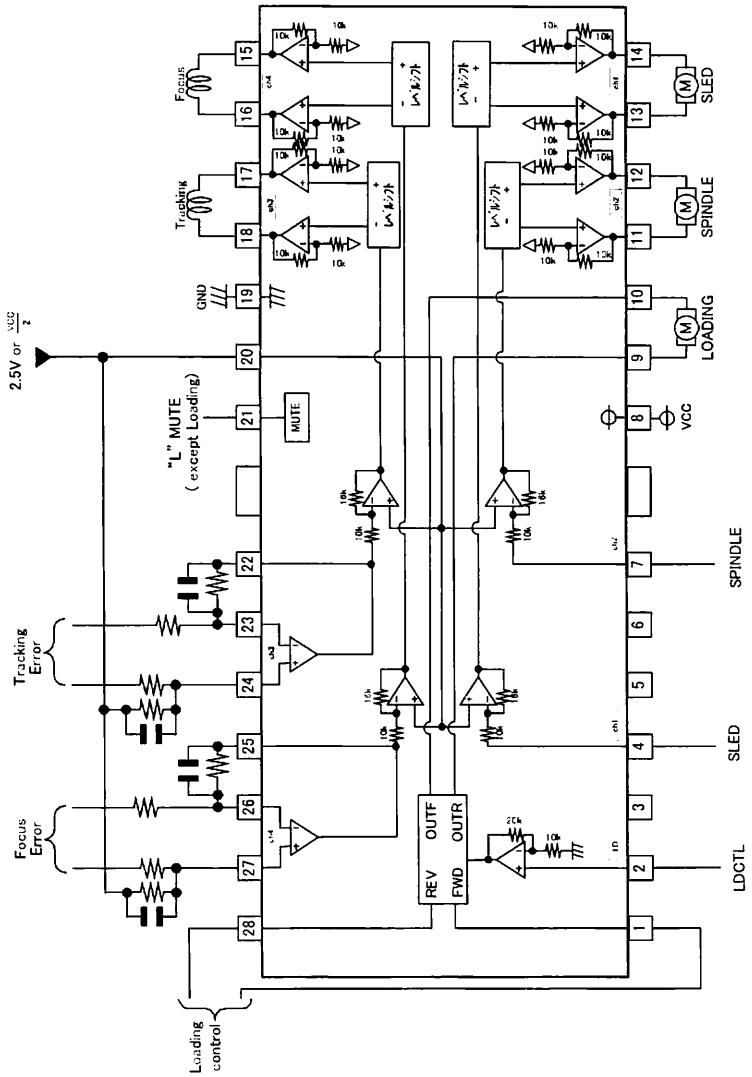
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Quiescent Circuit Current	ICC	-	24	34	mA	No load applied
<BTL Driver>						
Output Offset Voltage	VOO	-50	0	50	mV	
Maximum Output Amplitude	VOM	5.4	6.0	-	V	
Voltage Gain	GVC	14.0	16.1	18.0	Db	
Mute ON Voltage	VMTON	-	-	0.5	V	
Mute OFF Voltage	VMTOFF	1.5	-	-	V	
Mute Terminal Input Current	IMUTE	-	180	270	µA	VMUTE=5V
Bias Drop Mute ON Voltage	VBMUTE ON	-	-	0.5	V	
Bias Drop Mute OFF Voltage	VBMUTE OFF	1.1	-	-	V	
Bias Terminal Input Current	IBIAS	-	75	120	µA	VBIAS=2.5V
<Pre-stage Operational Amplifier>						
Common Mode Input Range	VICM	0.5	-	6.8	V	
Input Offset Voltage	VOFOP	-6	0	6	mV	
Input Bias Current	UBOP	-	-	300	nA	
High-level Output Voltage	VOHOP	7.5	-	-	V	
Low-level Output Voltage	VOLOP	-	-	0.5	V	
Output Driving Current Sink	ISIN	1	-	-	mA	VCC with 50Ω
Output Driving Current Source	ISOU	1	-	-	MA	GND with 50Ω
Slew Rate	SROP	-	1	-	V/us	100kHz square wave, 2Vpp output
<Loading Driver>						
Output Saturation Voltage 1	VSAT1	0.6	0.9	1.4	V	Sum of upper side + lower side, IL=200mA
Output Saturation Voltage 1 F/R Difference	ΔVSAT1	-	-	0.1	V	F/R difference of Output Saturation Voltage 1
Output Saturation Voltage 2	VSAT2	0.7	1.2	2.0	V	Sum of upper side + lower side, IL=500mA
Voltage Gain	LGVC	6.6	8.6	10.6	dB	VOLD over VLDCTL (VLDCTL=2V)
<Loading Logic Input>						
Input High-level Voltage	VIHLD	1.5	-	VCC	V	
Input Low-level Voltage	VILLD	-0.3	-	0.5	V	
Input High-level Current	IIHLD	-	180	270	µA	VFWD=VREV=5V

O OUTLINE DIMENSIONS, SYMBOLS



Rev. A

O APPLICATION CIRCUIT DIAGRAM



Resistance unit: [Ω]

O PIN NUMBERS, PIN NAMES

No.	Pin name	Description	No.	Pin name	Description
1	FWD	Loading driver FWD input terminal	15	VO4(+)	Driver CH4 positive output
2	LDCTL	Loading driver output voltage control terminal	16	VO4(-)	Driver CH4 negative output
3	TEST	TEST	17	VO3(+)	Driver CH3 positive output
4	IN1	CH1 input terminal	18	VO3(-)	Driver CH3 negative output
5	TEST	TEST	19	GND	Ground terminal
6	TEST	TEST	20	BIAS	Bias input terminal
7	IN2	CH2 input terminal	21	MUTE	Mute control terminal
8	VCC	Power supply terminal	22	OPOT3	CH3 pre-stage amp output terminal
9	VOL(-)	Loading driver negative output	23	OPIN3(-)	CH3 pre-stage amp inverted input terminal
10	VOL(+)	Loading driver positive output	24	OPIN3(+)	CH3 pre-stage amp non-inverted input terminal
11	VO2(-)	Driver CH2 negative output	25	OPOUT4	CH4 pre-stage amp output terminal
12	VO2(+)	Driver CH2 positive output	26	OPIN4(-)	CH4 pre-stage amp inverted input terminal
13	VO1(-)	Driver CH1 negative output	27	OPIN4(+)	CH4 pre-stage amp non-inverted input terminal
14	VO1(+)	Driver CH1 positive output	28	REV	Loading driver REV input terminal

Note: The positive or negative polarity of driver outputs is determined by the input polarity. (For example, when the voltage on the pin 4 is HIGH, the output voltage on the pin 14 becomes HIGH.)

O CAUTIONS ON USE

(1) Setting the voltage on the Mute terminal to open or 0.5V or less will activate a mute function for the output current. Under condition of normal use, the Mute terminal should be pull-up to 1.5V or above.
(2) When the voltage applied on the Bias terminal (pin 20) has dropped to 0.5V (Typ.) or less, the mute function will be activated. Under conditions of normal use, it should be set to 1.1V or above.
(3) When the power supply voltage drops to 3.8V (Typ.) or less, the internal circuit will turn OFF and, when recovering to 4.0V (Typ.) or above, the circuit will startup again.
(4) Thermal shutdown (TSD) or power supply voltage drop will activate the mute functions on all drivers, while mute ON or bias terminal voltage drop will on the BTL drivers except loading drivers. The pre-stage OP-amps cannot be muted in any cases described above.
While muting, the output terminals of the BTL driver are set to the value of the internal bias voltage ((VCC-0.7)/2V).
(5) Loading Driver - Logic Input Truth Table

FWD (1pin)	REV (28pin)	VOL (+) (10pin)	VOL (-) (9pin)	Function
L	L	OPEN	OPEN	Open mode
L	H	L	H	Reverse mode
H	L	H	L	Forward mode
H	H	L	L	Brake mode

The input circuitry for PIN 1 and PIN 28 is designed to avoid the driver output upper/lower transistors from turning ON synchronously, but, for better reliability, the motor positive/negative inversion input must stay once in the open mode. It is recommendable to set the open mode period to 10msec or above.
The potential between the outputs can be controlled by the LDCTL terminal (PIN 2). It outputs the voltage of 2.7 times (8.6dB Typ.) of the input at PIN 2.
(6) Even though a radiating fin is connected to the GND inside of the package, it must be connected to the external GND.
(7) Basically, applying a voltage below the IC sub-potential to any terminals must be avoided. Due to a counter electromotive force of the load, if the output on each driver has dropped to the IC sub-potential (GND) or less, an operation margin must be considered and examined.
(8) The TEST terminal must be set to open.
(9) About absolute maximum ratings
Exceeding the absolute maximum ratings, such as the applied voltage or the operating temperature range, may cause permanent device damage. As these cases cannot be limited to the broken short mode or the open mode, if a special mode where the absolute maximum ratings may be exceeded is assumed, it is recommended to take mechanical safety measures such as attaching fuses.
(10) About power supply lines
As a measure against the back current regenerated by a counter electromotive force of the motor, a capacitor to be used as a regenerated-current path can be installed between the power supply and GND and its capacitance value should be determined after careful check that any problems, for example, a leak capacitance of the electrolytic capacitor at low temperature, are not found in various characteristics.
(11) About GND potential
The electric potential of the GND terminal must be kept lowest in the circuitry at any operation states.
(12) About thermal design
With consideration of the power dissipation (Pd) under conditions of actual use, a thermal design provided with an enough margin should be done.
(13) About operations in a strong electric field
When used in a strong electric field, note that a malfunction may occur.
(14) ASO
When using this IC, the output Tr must be set not to exceed the values specified in the absolute maximum ratings and ASO.
(15) Thermal shutdown circuit
This IC incorporates a thermal shutdown circuit (TSD circuit). When the chip temperature reaches the value shown below, the coil output to the motor will be set to open.

The thermal shutdown circuit is designed only to shut off the IC from a thermal runaway and not intended to protect or guarantee the entire IC functions.
Therefore, users cannot assume that the TSD circuit once activated can be used continuously in the subsequent operations.

TSD ON Temperature [°C] (typ.)	Hysteresis Temperature [°C] (typ.)
175	25

(16) About earth wiring patterns
When a small signal GND and a large current GND are provided, it is recommended that the large current GND pattern and the small signal GND pattern should be separated and grounded at a single point of the reference point of the set in order to prevent the voltage of the small signal GND from being affected by a voltage change caused by the resistance of the pattern wiring and the large current.
Make sure that the GND wiring patterns of the external components will not change, too.

(17) This IC is a monolithic IC which has a P^+ isolations and P substrate to isolate elements each other.
This P layer and an N layer in each element form a PN junction to construct various parasitic elements.
Due to the IC structure, the parasitic elements are inevitably created by the potential relationship.
Activation of the parasitic elements can cause interference between circuits and may result in a malfunction or, consequently, a fatal damage. Therefore, make sure that the IC must not be used under conditions that may activate the parasitic elements, for example, applying the lower voltage than the ground level (GND, P substrate) to the input terminals.
In addition, do not apply the voltage to input terminals without applying the power supply voltage to the IC. Also while applying the power supply voltage, the voltage of each input terminal must not be over the power supply voltage, or within the guaranteed values in the electric characteristics.

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