Datasheet

Motor / Actuator Drivers for DC Brush Motor Series

Automotive 8ch Half Bridge Driver with SPI Control

BD16938EFV-C

General Description

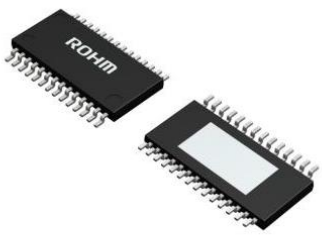
The BD16938EFV-C is 8ch half bridge driver for automotive applications. It can drive compact DC brush motors directly and each output can be controlled in three modes (High, Low and High Impedance).
MCU can control the driver via 16bit Serial Peripheral Interface (SPI). The absolute voltage is 40V rated with low ON resistance packaged in compact package, which contributes to realize high reliability, low energy consumption and low cost.

Key Specifications

■ Supply Voltage	6.3V to 32V
■ Operating Temperature Range	-40°C to +125°C
■ Output Current	1.0A(Max)
■ Output ON Resistance (High Side)	0.8Ω(Typ)
■ Output ON Resistance (Low Side)	0.6Ω(Typ)

Package

Package	W(Typ) x D(Typ) x H(Max)
HTSSOP-B28	9.70mm x 6.40mm x 1.00mm



Features

- AEC-Q100 Qualified(Note 1)
- 1.0A DMOS Half Bridge 8 Circuits
- Three Mode Output Control (High, Low & High Impedance)
- Low Standby Current
- Built-in Protection Diode Against Output Reverse Voltage
- Over Current Protection at VS Supply Stage (OCP)
- Under Load Detection at VS Supply Stage (ULD)
- Over Voltage Protection with OVDSEL Mode at VS Supply Stage (OVP)
- Under Voltage Lock Out at Supply Stage (UVLO)
- Thermal Shutdown (TSD), Thermal Warning (TW)

(Note 1) Grade 1

Applications(Note 2)

Automotive Body Electronics, HVAC, Door Mirrors, etc.

Typical Application Circuit

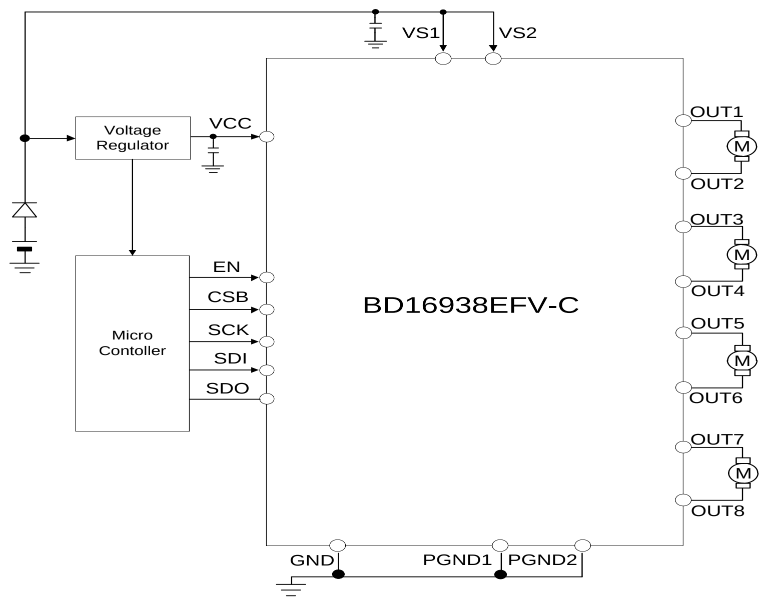


Figure 1. Typical Application Circuit

(Note 2) Please make sure you consult our company sales representative before mass production, if it is used except Door Mirror and HVAC.

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

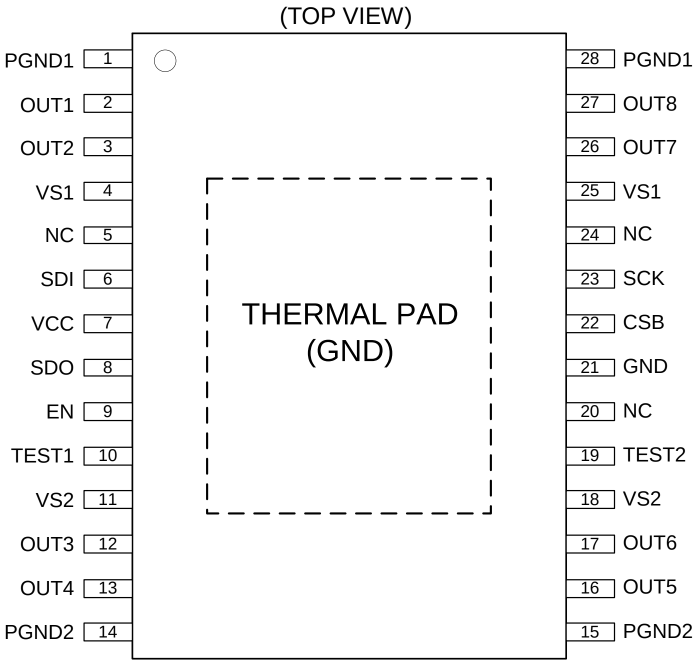


Figure 2. Pin Configuration

Pin Description

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	PGND1	GND for output stages	28	PGND1	GND for output stages
2	OUT1	Half bridge output 1	27	OUT8	Half bridge output 8
3	OUT2	Half bridge output 2	26	OUT7	Half bridge output 7
4	VS1	Power supply for output stages	25	VS1	Power supply for output stages
5	NC	No Connection	24	NC	No Connection
6	SDI	SPI data input	23	SCK	SPI clock input
7	VCC	Logic supply	22	CSB	SPI chip select input
8	SDO	SPI data output	21	GND	Small signal GND(Note 1)
9	EN	Enable input	20	NC	No Connection
10	TEST1	Test mode input1(Note 2)	19	TEST2	Test mode input2(Note 2)
11	VS2	Power supply for output stages	18	VS2	Power supply for output stages
12	OUT3	Half bridge output 3	17	OUT6	Half bridge output 6
13	OUT4	Half bridge output 4	16	OUT5	Half bridge output 5
14	PGND2	GND for output stages	15	PGND2	GND for output stages

(Note 1) Connect to GND for power dissipation.
(Note 2) Connect TEST1, TEST2 to GND

Block Diagram

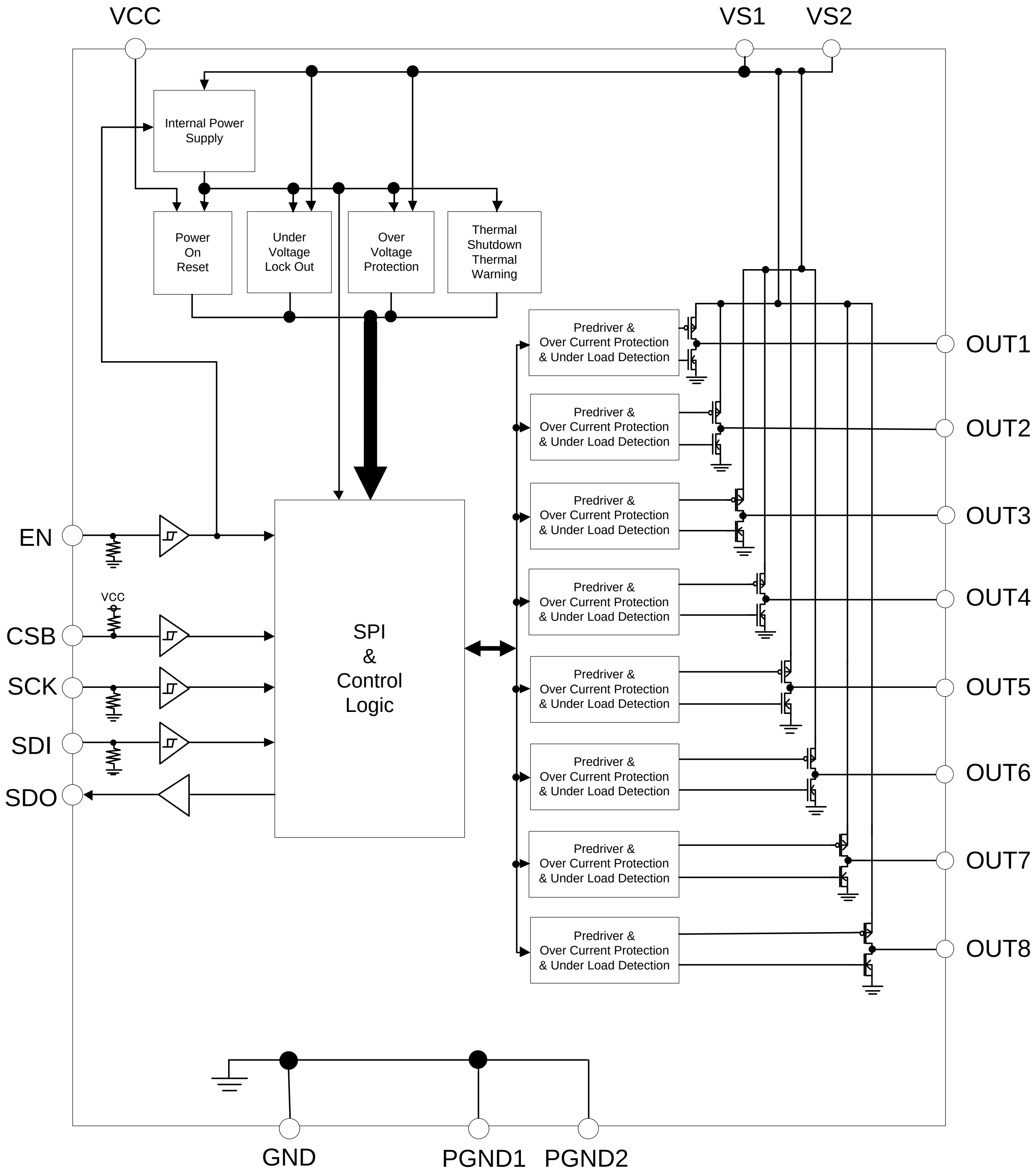


Figure 3. Block Diagram

Absolute Maximum Ratings (Tj = 25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{VS}(Note 1)	-0.3 to +40	V
Logic Supply Voltage	V_{CC}	-0.3 to +7.0	V
Output Voltage	V_{OUT1} to V_{OUT8}	-0.3 to +40	V
Output Current	I_O	1.0	A
Logic Input Voltage	V_{SDI}, V_{SCK}, V_{CSB}, V_{EN}	-0.3 to V_{CC}+0.3	V
Test Input Voltage	V_{TEST1}, V_{TEST2}	-0.3 to +40	V
Logic Output Voltage	V_{SDO}	-0.3 to V_{CC}+0.3	V
SDO Output Current	I_{SDO}	5.0	mA
Operating Temperature Range	Topr	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature Range	Tj	-40 to +150	°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

(Note 1) V_{VS} = V_{VS1}, V_{VS2}

Thermal Resistance (Note 2)

Parameter	Symbol	Thermal Resistance(Typ)		Unit
		1s(Note 4)	2s2p(Note 5)	
HTSSOP-B28				
Junction to Ambient	θ_{JA}	107.0	25.1	°C/W
Junction to Top Characterization Parameter(Note 3)	Ψ_{JT}	6	3	°C/W

(Note 2) Based on JESD51-2A(Still-Air)

(Note 3) This thermal characterization parameter reports the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 6) This thermal via connects with the copper pattern of all layers

Recommended Operating Conditions (Ta = -40°C to +125°C)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage(Note 7)	V_{VS}	6.3	12	32	V
Logic Supply Voltage(Note 7)	V_{CC}	3.0	5	5.5	V
Logic Input Voltage(Note 7)	V_{EN}, V_{CSB}, V_{SCK}, V_{SDI}	0	-	V_{CC}	V

(Note 7) In order to start operation, apply the voltage to VCC(Logic supply voltage) after VS(Power supply voltage) exceeds the minimum operating voltage range (6.3V). After VCC(Logic supply voltage) exceeds the minimum operating voltage range(3.0V) then apply the voltage to the Logic input pins.

Electrical Characteristics

(Unless otherwise specified, V_{VS} = 6.3V to 32V, V_{CC} = 3.0V to 5.5V, -40°C ≤ Tj ≤ +150°C)

Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
Circuit Current						
VS Circuit Current1	I_{VS1}	-	0	10	µA	EN = 0V
VS Circuit Current 2	I_{VS2}	-	7	15	mA	
VCC Circuit Current 1	I_{VCC1}	-	0	10	µA	EN = 0V
VCC Circuit Current 2	I_{VCC2}	-	0.1	0.5	mA	
Output						
Output ON Resistance High Side 1	R_{ONH1}	-	0.8	1.5	Ω	I_{Load} = 0.1A to 0.8A, -40°C ≤ Tj < +25°C
Output ON Resistance High Side 2	R_{ONH2}	-	1.2	1.85	Ω	I_{Load} = 0.1A to 0.8A, 25°C ≤ Tj ≤ 150°C
Output ON Resistance Low Side 1	R_{ONL1}	-	0.6	1.4	Ω	I_{Load} = 0.1A to 0.8A, -40°C ≤ Tj < +25°C
Output ON Resistance Low Side 2	R_{ONL2}	-	1.1	1.65	Ω	I_{Load} = 0.1A to 0.8A, 25°C ≤ Tj ≤ 150°C
Output Leakage High Side	I_{LH}	-	0	10	µA	OUT1 to OUT8 = 0V
Output Leakage Low Side	I_{LL}	-	0	10	µA	OUT1 to OUT8 = V_{VS}
Output Diode Voltage High Side	V_{FH}	0.2	0.8	1.4	V	I_{Load} = 0.6A
Output Diode Voltage Low Side	V_{FL}	0.2	0.8	1.4	V	I_{Load} = -0.6A
Serial Input						
Input High Voltage	V_{IH}	V_{CC} x 0.6	-	-	V	
Input Low Voltage	V_{IL}	-	-	V_{CC} x 0.2	V	
Input High Current 1	I_{IH1}	-	50	100	µA	(SDI, SCK, EN) = VCC = 5V
Input High Current 2	I_{IH2}	-	0	10	µA	CSB = VCC = 5V
Input Low Current 1	I_{IL1}	-	0	10	µA	(SDI, SCK, EN) = 0V
Input Low Current 2	I_{IL2}	-	50	100	µA	CSB = 0V, VCC = 5V
Serial Output						
Output High Voltage	V_{OH}	V_{CC} - 0.6	-	-	V	I_{Load} = -1.0mA
Output Low Voltage	V_{OL}	-	-	0.6	V	I_{Load} = 1.0mA
Protections						
VS Under Voltage Lock Out (ON to OFF)	V_{UVDH}	5.3	5.8	6.3	V	
VS Under Voltage Lock Out (OFF to ON)	V_{UVDL}	5.0	5.5	6.0	V	
VS Over Voltage Protection1 (OFF to ON)	V_{OVPH1}	32.5	36	39.5	V	OVPSEL = 0
VS Over Voltage Protection 1 (ON to OFF)	V_{OVPL1}	30	33.5	37	V	OVPSEL = 0
VS Over Voltage Protection 2 (OFF to ON)	V_{OVPH2}	18	20	22	V	OVPSEL = 1
VS Over Voltage Protection 2 (ON to OFF)	V_{OVPL2}	16.2	18	19.8	V	OVPSEL = 1
VCC Power On Reset(ON to OFF)	V_{PORH}	2.6	2.8	3.0	V	
VCC Power On Reset(OFF to ON)	V_{PORL}	2.4	2.6	2.8	V	
Over Current Protection	I_{OCP}	1.05	1.55	2.05	A	
Over Current Protection Delay Time	t_{DOC}	10	25	50	µs	
Under Load Detection(Note 1)	I_{UD}	2	11	20	mA	
Under Load Detection Delay Time	t_{DUD}	200	370	600	µs	

(Note 1) Measured when there is no load in other channels.

Electrical Characteristics – continued
(Unless otherwise specified, V_{VS} = 6.3V to 32V, V_{CC} = 3.0V to 5.5V, -40°C ≤ Tj ≤ +150°C)

Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
Protections						
Thermal Warning(Note 1)	T_{TW}	100	125	150	°C	
Thermal Warning Hysteresis(Note 1)	T_{TWHYS}	-	10	-	°C	
Thermal Shutdown(Note 1)	T_{TSD}	150	175	200	°C	
Thermal Shutdown Hysteresis(Note 1)	T_{TSDHYS}	-	25	-	°C	
Driver Output Timing						
High Side Turn On Time	t_{ONH}	-	-	38.0	µs	V_{VS} = 12V, No Load
Low Side Turn On Time	t_{ONL}	-	-	38.0	µs	V_{VS} = 12V, No Load
OUT Rise Time	t_{LHR}	-	1.0	8.0	µs	V_{VS} = 12V, No Load
OUT Fall Time	t_{HLF}	-	1.0	8.0	µs	V_{VS} = 12V, No Load

(Note 1) Design guaranteed. No shipping inspection.

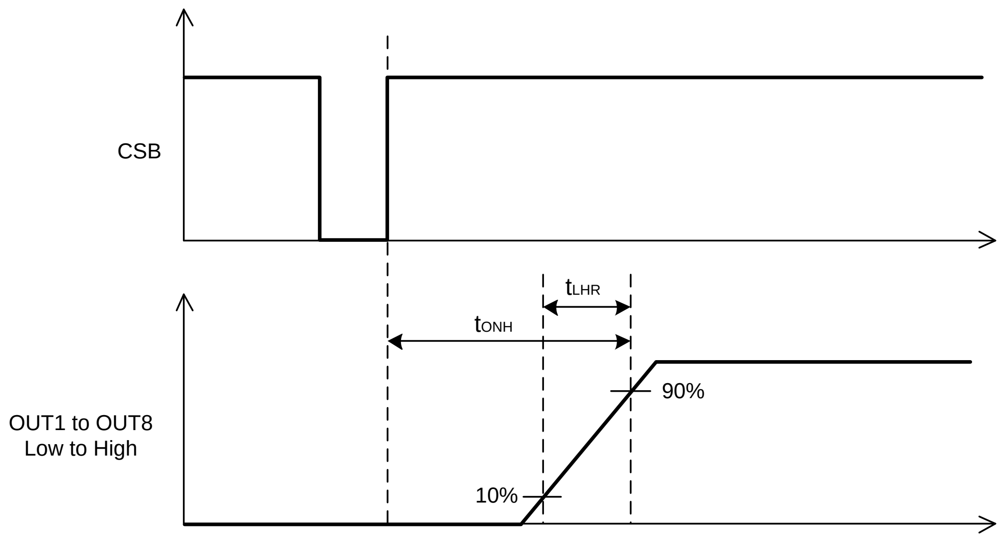


Figure 4. Driver Output Timing (Low to High)

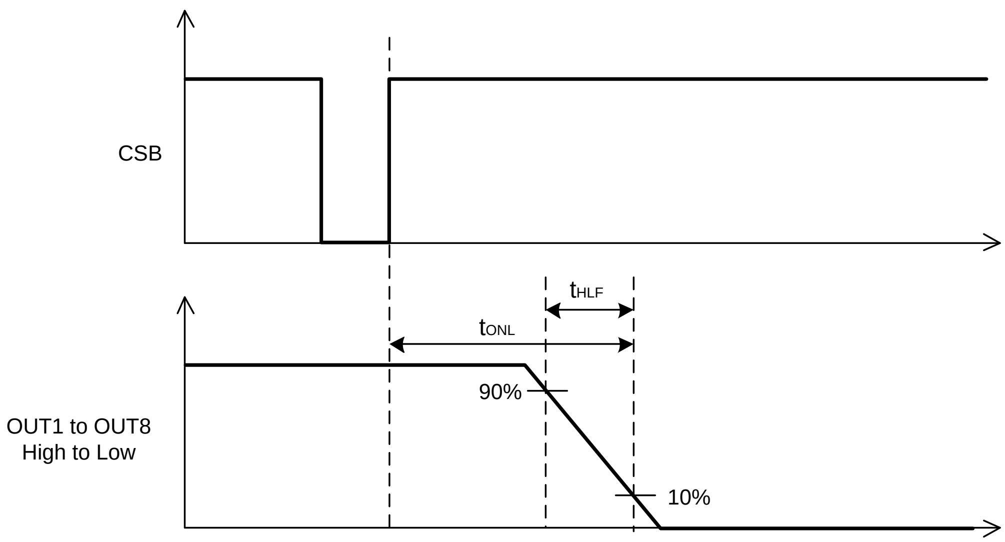


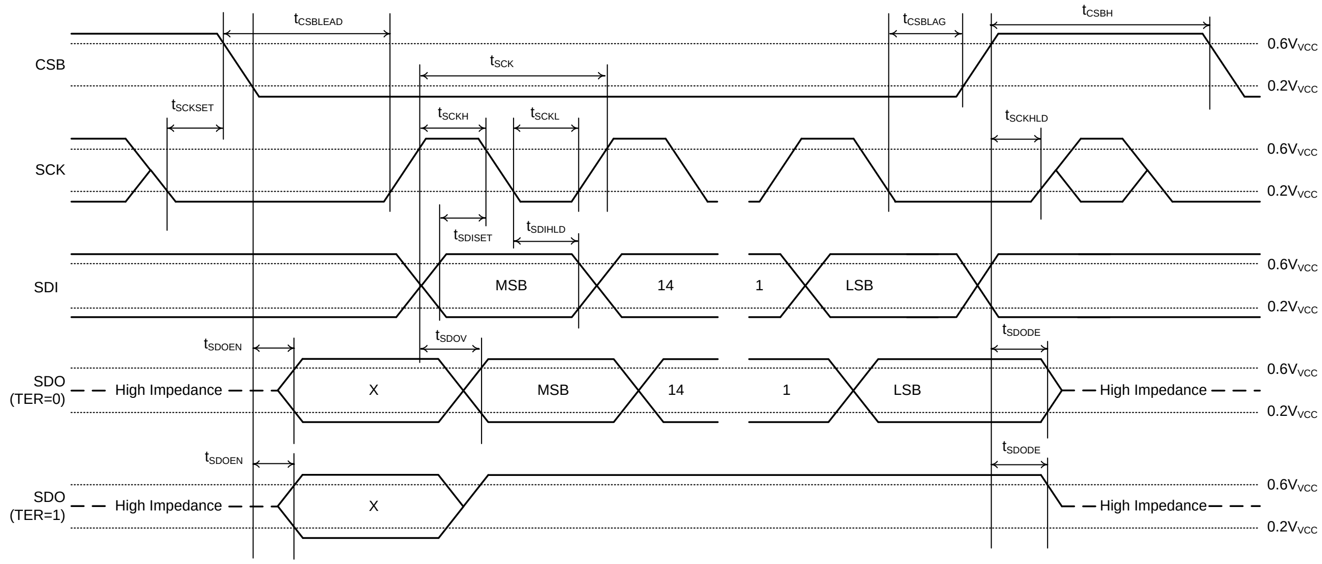
Figure 5. Driver Output Timing (High to Low)

Electrical Characteristics – continued

(Unless otherwise specified, V_{VS} = 6.3V to 32V, V_{CC} = 3.0V to 5.5V, -40°C ≤ Tj ≤ +150°C)

Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
Serial Peripheral Interface						
SCK Frequency	f_{SCK}	-	-	4.1	MHz	
SCK Period	t_{SCK}	243	-	-	ns	
SCK High Time	t_{SCKH}	87.5	-	-	ns	
SCK Low Time	t_{SCKL}	87.5	-	-	ns	
SCK Setup Time	t_{SCKSET}	125	-	-	ns	
SCK Hold Time	t_{SCKHLD}	125			ns	
CSB Lead Time	$t_{CSBLEAD}$	125	-	-	ns	
CSB Lag Time	t_{CSBLAG}	125	-	-	ns	
CSB High Time	t_{CSBH}	20	-	-	μs	
SDI Setup Time	t_{SDISET}	50	-	-	ns	
SDI Hold Time	t_{SDIHLD}	50	-	-	ns	
SDO Valid Time	t_{SDOV}	-	-	100	ns	No Load
SDO Enable After CSB Falling Edge	t_{SDOEN}	-	-	125	ns	(Note 1)
SDO Disable After CSB Rising Edge	t_{SDODE}	-	-	500	ns	(Note 1)

(Note 1) The timing is prescribed in 0% and 100% of VCC to GND amplitude.



X: Unstable state
TER(Internal signal): “0” in normal operation / “1” in detecting erroneous SPI transmission

Figure 6. Serial Interface Timing

Typical Performance Curves

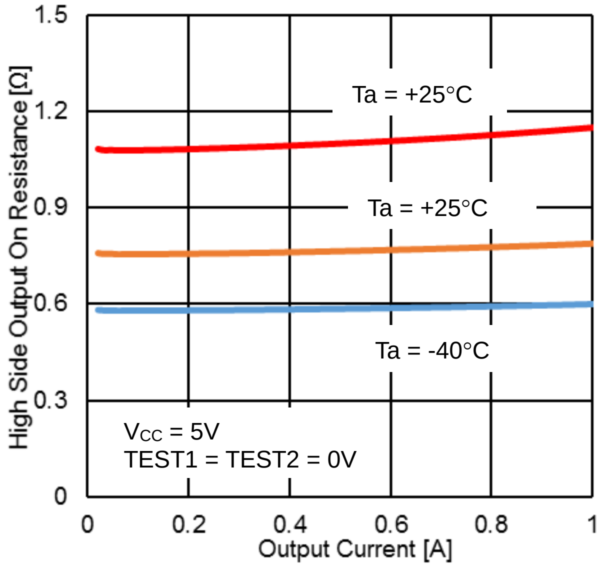


Figure 7. Output ON Resistance vs Output Current
(Output ON Resistance High Side, V_{VS} = 12V)

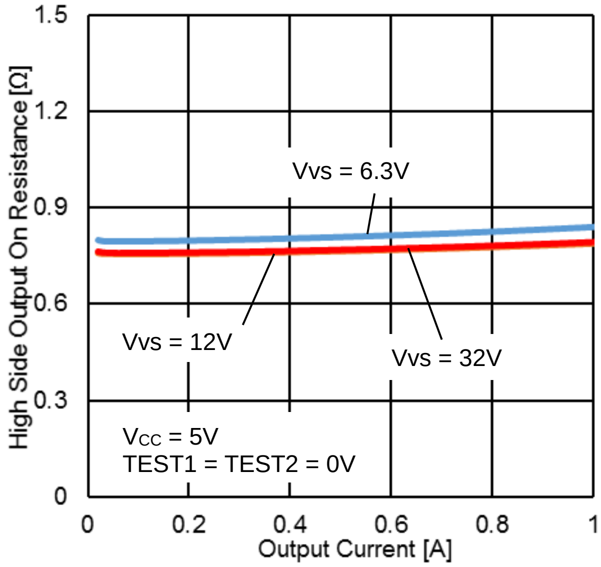


Figure 8. Output ON Resistance vs Output Current
(Output ON Resistance High Side, Ta=25°C)

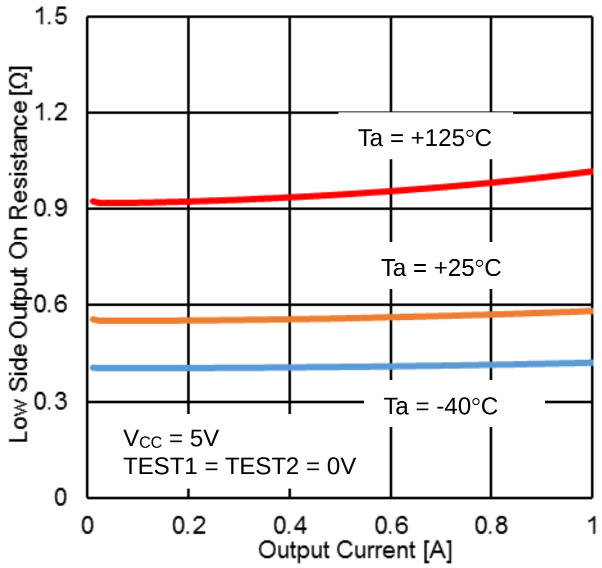


Figure 9. Output ON Resistance vs Output Current
(Output ON Resistance Low Side, Vvs = 12V)

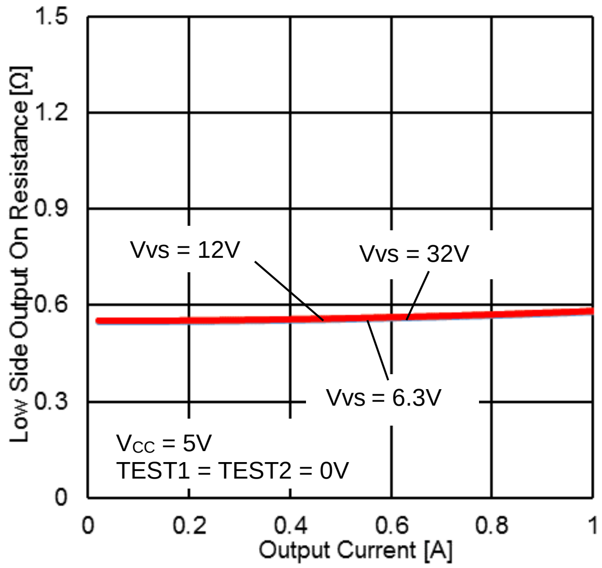
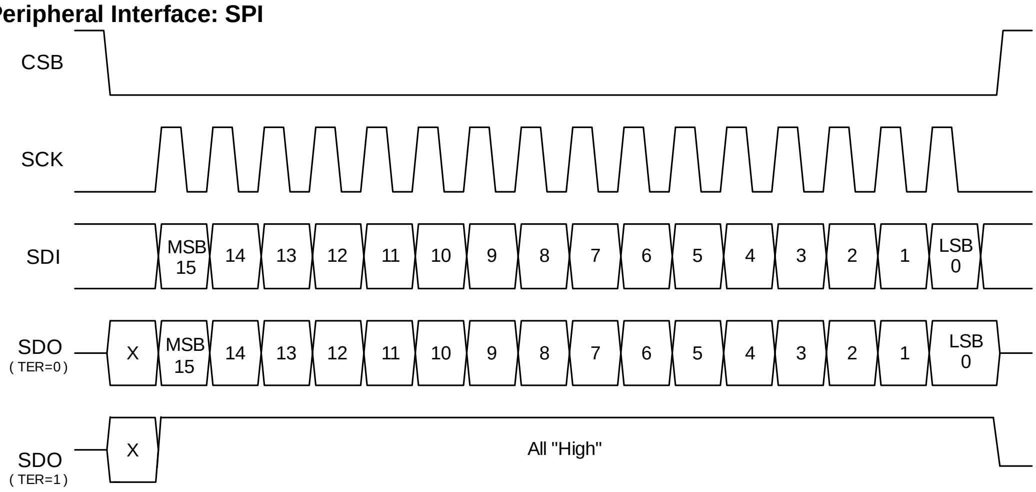


Figure 10. Output ON Resistance vs Output Current
(Output ON Resistance Low Side, Ta = 25°C)

Description of Blocks

1. Serial Peripheral Interface: SPI



X: Unstable state
TER(Internal signal): "0" in normal operation / "1" in detecting erroneous SPI transmission

Figure 11. SPI Communication Format

16bit serial interface is equipped to control on / off of driver and various protections as well as to read out the state of protections. Input / Output register and the functions are described below.

(1) Input Data Register1- Input Pattern Bit15 = 1, Bit14 = 0

Bit Number	Name	Description	Bit Status	Initial Value
15	WE	Write Enable	0 : Read 1 : Write & Read	-
14	WR_AD	Write Address	0 : Address A 1 : Address B	-
13	RD_AD	Read Address	0 : Address A 1 : Address B	-
12	SRR	Status Reset Register (This bit will self-clear)	0 : Normal 1 : Reset	0
11	HSC4	Control High Side 4 (OUT4)	0 : High Side Off 1 : High Side On	0
10	LSC4	Control Low Side 4 (OUT4)	0 : Low Side Off 1 : Low Side On	0
9	HSC3	Control High Side 3 (OUT3)	0 : High Side Off 1 : High Side On	0
8	LSC3	Control Low Side 3 (OUT3)	0 : Low Side Off 1 : Low Side On	0
7	HSC2	Control High Side 2 (OUT2)	0 : High Side Off 1 : High Side On	0
6	LSC2	Control Low Side 2 (OUT2)	0 : Low Side Off 1 : Low Side On	0
5	HSC1	Control High Side 1 (OUT1)	0 : High Side Off 1 : High Side On	0
4	LSC1	Control Low Side 1 (OUT1)	0 : Low Side Off 1 : Low Side On	0
3	UNDERLOAD	Under Loads Register Mode (OUT1 to OUT8)	0 : On 1 : Off	0
2	TSDSTH	TSDS Register Mode	0 : Latch 1 : Through	0
1	PSSTH	OVPS / UVLOS Register Mode	0 : Latch 1 : Through	0
0	RESERVE	Reserve	0 : Normal 1 : Prohibit	0

Description of Blocks – continued

(2) Input Data Register2- Input Pattern Bit15 = 1, Bit14 = 1

Bit Number	Name	Description	Bit Status	Initial Value
15	WE	Write Enable	0 : Read 1 : Write & Read	-
14	WR_AD	Write Address	0 : Address A 1 : Address B	-
13	RD_AD	Read Address	0 : Address A 1 : Address B	-
12	SRR	Status Reset Register (This bit will self-clear)	0 : Normal 1 : Reset	0
11	HSC8	Control High Side 8 (OUT8)	0 : High Side Off 1 : High Side On	0
10	LSC8	Control Low Side 8 (OUT8)	0 : Low Side Off 1 : Low Side On	0
9	HSC7	Control High Side 7 (OUT7)	0 : High Side Off 1 : High Side On	0
8	LSC7	Control Low Side 7 (OUT7)	0 : Low Side Off 1 : Low Side On	0
7	HSC6	Control High Side 6 (OUT6)	0 : High Side Off 1 : High Side On	0
6	LSC6	Control Low Side 6 (OUT6)	0 : Low Side Off 1 : Low Side On	0
5	HSC5	Control High Side 5 (OUT5)	0 : High Side Off 1 : High Side On	0
4	LSC5	Control Low Side 5 (OUT5)	0 : Low Side Off 1 : Low Side On	0
3	OVPSEL	OVP Threshold Select	0 : V_{OVPH1}, V_{OVPL1} 1 : V_{OVPH2}, V_{OVPL2}	0
2	RESERVE	Reserve	-	-
1	RESERVE	Reserve	-	-
0	RESERVE	Reserve	0 : Normal 1 : Prohibit	0

Input of High Side On and Low Side On is prohibited. The input of High Side On and Low Side On results in High Side Off and Low Side Off state.

If WE(Bit15: Write Enable) is set to ‘1’, then Input Data Registers will be written and output will be Read Data as well depending on the previous SPI command.

It can select the Write Registers by setting WR_AD(Bit14: Write Address) bit.
Read Data can be selected from the table of Read register by setting WR_AD(Bit14: Write Address) and RD_AD(Bit13: Read Address). For Read Data information, please refer below from Output Data Register1 to Output Data Register4.

If WE(Bit15: Write Enable) is set to ‘0’, then Input Data Registers will not be written (the transferred write data Bits 12 to 0 in this case will be ignored) and output will be only Read Data depending on the previous SPI command setting of WR_AD(Bit14: Write Address) and RD_AD(Bit13: Read Address).

Daisy Chain input is not supported.

Description of Blocks – continued

(3) Output Data Register1- Input Pattern Bit15 = 0, Bit14 = 0, Bit13 = 0

Bit Number	Name	Description	Bit Status	Initial Value
15	-	-	-	0
14	TSDS	Thermal Shutdown Status	0 : Normal 1 : Fault	1 (Note 1)
13	TWS	Thermal Warning Status	0 : Normal 1 : Fault	1 (Note 1)
12	-	-	-	0
11	HSS4	Status High Side 4 (OUT4)	0 : High Side Off 1 : High Side On	0
10	LSS4	Status Low Side 4 (OUT4)	0 : Low Side Off 1 : Low Side On	0
9	HSS3	Status High Side 3 (OUT3)	0 : High Side Off 1 : High Side On	0
8	LSS3	Status Low Side 3 (OUT3)	0 : Low Side Off 1 : Low Side On	0
7	HSS2	Status High Side 2 (OUT2)	0 : High Side Off 1 : High Side On	0
6	LSS2	Status Low Side 2 (OUT2)	0 : Low Side Off 1 : Low Side On	0
5	HSS1	Status High Side 1 (OUT1)	0 : High Side Off 1 : High Side On	0
4	LSS1	Status Low Side 1 (OUT1)	0 : Low Side Off 1 : Low Side On	0
3	OCPS	Over Current Protection Status (OUT1 to OUT4)	0 : Normal 1 : Fault	1 (Note 1)
2	UNDERLOADS	Under Loads Status (OUT1 to OUT4)	0 : Normal 1 : Fault	1 (Note 1)
1	OVPS	Over Voltage Protection Status	0 : Normal 1 : Fault	1 (Note 1)
0	UVLOS	UVLO(VS) Status	0 : Normal 1 : Fault	1 (Note 1)

(Note 1) Default state is “1(Fault)”. Set SRR register to “1” at the start which will reset this values.

Description of Blocks – continued

(4) Output Data Register2- Input Pattern Bit15 = 0, Bit14 = 0, Bit13 = 1

Bit Number	Name	Description	Bit Status	Initial Value
15	-	-	-	0
14	TSDS	Thermal Shutdown Status	0 : Normal 1 : Fault	1(Note 1)
13	TWS	Thermal Warning Status	0 : Normal 1 : Fault	1(Note 1)
12	-	-	-	0
11	UNDERLOAD4	Under Load Status OUT4	0 : Normal 1 : Fault	1(Note 1)
10	UNDERLOAD3	Under Load Status OUT3	0 : Normal 1 : Fault	1(Note 1)
9	UNDERLOAD2	Under Load Status OUT2	0 : Normal 1 : Fault	1(Note 1)
8	UNDERLOAD1	Under Load Status OUT1	0 : Normal 1 : Fault	1(Note 1)
7	OCPH4	Over Current Protection High Side Status OUT4	0 : Normal 1 : Fault	1(Note 1)
6	OCPL4	Over Current Protection Low Side Status OUT4	0 : Normal 1 : Fault	1(Note 1)
5	OCPH3	Over Current Protection High Side Status OUT3	0 : Normal 1 : Fault	1(Note 1)
4	OCPL3	Over Current Protection Low Side Status OUT3	0 : Normal 1 : Fault	1(Note 1)
3	OCPH2	Over Current Protection High Side Status OUT2	0 : Normal 1 : Fault	1(Note 1)
2	OCPL2	Over Current Protection Low Side Status OUT2	0 : Normal 1 : Fault	1(Note 1)
1	OCPH1	Over Current Protection High Side Status OUT1	0 : Normal 1 : Fault	1(Note 1)
0	OCPL1	Over Current Protection Low Side Status OUT1	0 : Normal 1 : Fault	1(Note 1)

(Note 1) Default state is "1(Fault)". Set SRR register to "1" at the start which will reset this values.

Description of Blocks – continued

(5) Output Data Register3- Input Pattern Bit15 = 0, Bit14 = 1, Bit13 = 0

Bit Number	Name	Description	Bit Status	Initial Value
15	-	-	-	0
14	TSDS	Thermal Shutdown Status	0 : Normal 1 : Fault	1 (Note 1)
13	TWS	Thermal Warning Status	0 : Normal 1 : Fault	1 (Note 1)
12	-	-	-	0
11	HSS8	Status High Side 8 (OUT8)	0 : High Side Off 1 : High Side On	0
10	LSS8	Status Low Side 8 (OUT8)	0 : Low Side Off 1 : Low Side On	0
9	HSS7	Status High Side 7 (OUT7)	0 : High Side Off 1 : High Side On	0
8	LSS7	Status Low Side 7 (OUT7)	0 : Low Side Off 1 : Low Side On	0
7	HSS6	Status High Side 6 (OUT6)	0 : High Side Off 1 : High Side On	0
6	LSS6	Status Low Side 6 (OUT6)	0 : Low Side Off 1 : Low Side On	0
5	HSS5	Status High Side 5 (OUT5)	0 : High Side Off 1 : High Side On	0
4	LSS5	Status Low Side 5 (OUT5)	0 : Low Side Off 1 : Low Side On	0
3	OCPS	Over Current Protection Status (OUT5 to OUT8)	0 : Normal 1 : Fault	1 (Note 1)
2	UNDERLOADS	Under Loads Status (OUT5 to OUT8)	0 : Normal 1 : Fault	1 (Note 1)
1	OVPS	Over Voltage Protection Status	0 : Normal 1 : Fault	1 (Note 1)
0	UVLOS	UVLO(VS) Status	0 : Normal 1 : Fault	1 (Note 1)

(Note 1) Default state is “1(Fault)”. Set SRR register to “1” at the start which will reset this values.

Description of Blocks – continued

(6) Output Data Register4- Input Pattern Bit15 = 0, Bit14 = 1, Bit13 = 1

Bit Number	Name	Description	Bit Status	Initial Value
15	-	-	-	0
14	TSDS	Thermal Shutdown Status	0 : Normal 1 : Fault	1(Note 1)
13	TWS	Thermal Warning Status	0 : Normal 1 : Fault	1(Note 1)
12	-	-	-	0
11	UNDERLOAD8	Under Load Status OUT8	0 : Normal 1 : Fault	1(Note 1)
10	UNDERLOAD7	Under Load Status OUT7	0 : Normal 1 : Fault	1(Note 1)
9	UNDERLOAD6	Under Load Status OUT6	0 : Normal 1 : Fault	1(Note 1)
8	UNDERLOAD5	Under Load Status OUT5	0 : Normal 1 : Fault	1(Note 1)
7	OCPH8	Over Current Protection High Side Status OUT8	0 : Normal 1 : Fault	1(Note 1)
6	OCPL8	Over Current Protection Low Side Status OUT8	0 : Normal 1 : Fault	1(Note 1)
5	OCPH7	Over Current Protection High Side Status OUT7	0 : Normal 1 : Fault	1(Note 1)
4	OCPL7	Over Current Protection Low Side Status OUT7	0 : Normal 1 : Fault	1(Note 1)
3	OCPH6	Over Current Protection High Side Status OUT6	0 : Normal 1 : Fault	1(Note 1)
2	OCPL6	Over Current Protection Low Side Status OUT6	0 : Normal 1 : Fault	1(Note 1)
1	OCPH5	Over Current Protection High Side Status OUT5	0 : Normal 1 : Fault	1(Note 1)
0	OCPL5	Over Current Protection Low Side Status OUT5	0 : Normal 1 : Fault	1(Note 1)

(Note 1) Default state is “1(Fault)”. Set SRR register to “1” at the start which will reset this values.

Description of Blocks – continued

(7) Settings of Error Output Registers

< PSSTH , TSDSTH >	Under Voltage Lock Out UVLOS	Over Voltage Protection OVPS	Thermal Shutdown TSDS	Over Current Protection OCPS
< 0 , 0 >	Latch	Latch	Latch	Latch
< 0 , 1 >	Latch	Latch	Self Recovery	Latch
< 1 , 0 >	Self Recovery	Self Recovery	Latch	Latch
< 1 , 1 >	Self Recovery	Self Recovery	Self Recovery	Latch

PSSTH, TSDSTH has to be set initially, and it shouldn't be changed in the middle of operation.

Either Latch or Self Recovery are selectable on UVLOS, OVPS and TSDS error output registers. Only Latch is available on OCPS error output register.
(The registers control only the operation mode of error output registers. It cannot change the operation of OUT1 to OUT8 terminals.)
Refer to the explanations of Protection Functions as far as OUT1 to OUT8 operations are concerned.

(8) Erroneous SPI Transmission (Transmission Error: TER)

When CSB signal becomes Low to High it will be assumed that SPI has completed the transfer, and the internal registers will be updated. When SCK inputs high pulse of 16, 24, 32, … (8+8xN values) except while CSB is low, erroneous SPI transmission is detected. If the error is detected, OUT1 to OUT8 outputs High Impedance and each error output register (OCPS, UNDERLOADS, TSDS, TWS, OVPS, and UVLOS) maintains the prior status accordingly. But SDO signal become high in the next transferring of SPI by TER.
At the same time, if the CSB High period (t_{CSBH}) goes below the specified 20μs, an erroneous SPI transmission can be detected. The transmission error status is refreshed every time CSB rises.

TER(Internal signal) : "0" in normal operation / "1" in detecting erroneous SPI transmission

Description of Blocks – continued

2. Over Voltage Protection (OVP)

All outputs become High impedance if VS terminal voltage goes up to V_{OVPH} [When OVPSEL = 0, V_{OVPH1} = 36V(Typ) and When OVPSEL = 1, V_{OVPH2} = 20V(Typ)] or above. And OVPS register is set ‘1’. Then, the outputs return to the normal operation when VS terminal voltage goes down to V_{OVPL} [When OVPSEL = 0, V_{OVPL1} = 33.5V(Typ) and When OVPSEL = 1, V_{OVPL2} = 18V(Typ)] or below.
It can select either Latch mode or Self-Recovery mode for OVPS output register by PSSTH input register.
In case PSSTH input register is set ‘0’, OVPS output register become Latch mode.
In case PSSTH input register is set ‘1’, OVPS output register become Self-Recovery mode.
In case of Self-Recovery mode, OVPS output register return to ‘0’ automatically, when VS terminal voltage goes down to V_{OVPL} or below. But, in case Latch mode, OPVS output register keeps ‘1’, if VS terminal voltage goes down to V_{OVPL} or below. It can reset for the latch of OVPS by SRR register.
OVP doesn’t operate when EN terminal is set to Low level. Please don’t to exceed the absolute maximum power supply voltage to avoid the IC being destroyed.

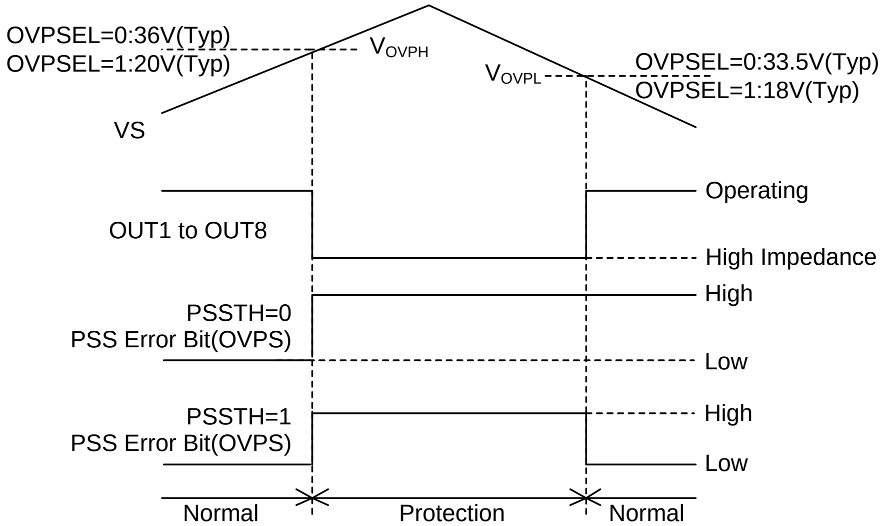


Figure 12. OVP Timing Chart

3. Under Voltage Lock Out (UVLO)

All outputs become High impedance if VS terminal voltage goes down to 5.5V(Typ) or below. And UVLOS output register is set ‘1’. Then, when VS terminal voltage goes up to 5.8V(Typ) or above, the outputs return to the normal operation mode.
It can select either Latch mode or Self-Recovery mode for UVLOS output register by PSSTH input register.
In case PSSTH input register is set ‘0’, UVLOS output register become Latch mode.
In case PSSTH input register is set ‘1’, UVLOS output register become Self-Recovery mode.
In case of Self-Recovery mode, UVLOS output register return to ‘0’ automatically, when VS terminal voltage goes up to 5.8V(Typ) or above. It can reset for the latch of UVLOS by SRR register.

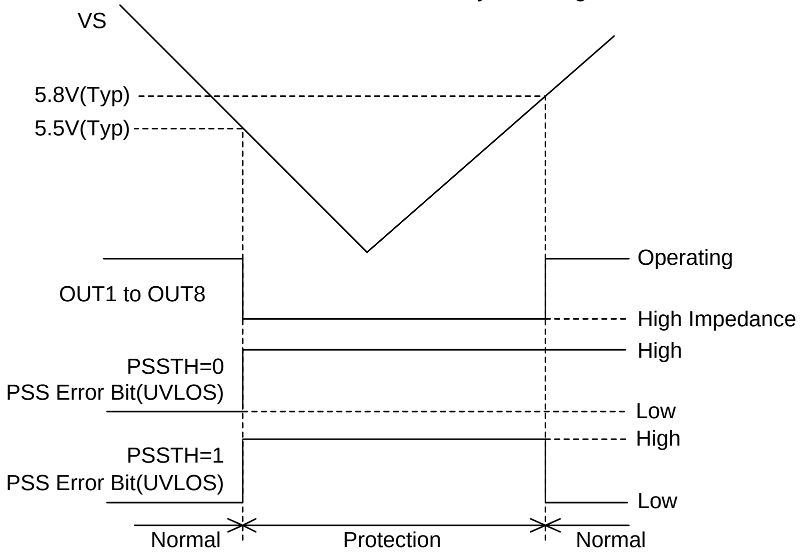


Figure 13. UVLO Timing Chart

Description of Blocks – continued

4. Over Current Protection (OCP)

If the current flows 1.55A(Typ) or above at the output terminal and pass 25µs(Typ), over current is protected. And OCPS register is set “1”. Only the Over Current Protected output terminal is latched at High impedance. In order to release the latch, it has to be reset by SRR register or EN terminal. This 25µs delay time is implemented to avoid the malfunction caused by noise.
OCP function protects the IC from destruction caused by output short. However, the continuous overcurrent condition causes the IC heating up or degraded, thus please take the appropriate measure such as making this IC into stand-by mode by application program when over current condition continues. Register OCPH1 to OCPH8, OCPL1 to OCPL8 will be set to specify OCP condition for the respective channels. (Please refer the output data register tables.)

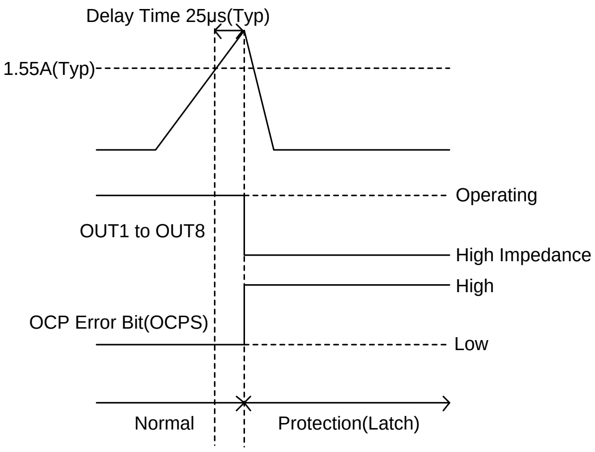


Figure 14. OCP Timing Chart

5. Thermal Shutdown (TSD) / Thermal Warning (TW)

If the junction temperature goes up to 175°C(Typ) or above, all outputs become High impedance. And TSDS output register is set ‘1’. Then, when the junction temperature goes down to 150°C(Typ) or below, the outputs return to the normal operation.
It can select either Latch mode or Self-Recovery mode for TSDS output register by TSDSTH input register.
In case TSDSTH input register is set ‘0’, TSDS output register become Latch mode.
In case TSDSTH input register is set ‘1’, TSDS output register become Self-Recovery mode.
In case of Self-Recovery mode, TSDS output register return to ‘0’ automatically, when the junction temperature goes down to 150°C(Typ) or below. It can reset for the latch of TSDS by SRR register.
When the junction temperature goes up to 125°C(Typ) or above, TWS output register is set to ‘1’.
It can also select either Latch mode or Self-Recovery mode for TWS output register by TSDSTH input register.
In case TSDSTH input register is set ‘0’, TWS output register become Latch mode.
In case TSDSTH input register is set ‘1’, TWS output register become Self-Recovery mode.
In case of Self-Recovery mode, TWS output register return to ‘0’ automatically, when the junction temperature goes down to 115°C(Typ) or below. It can reset for the latch of TWS by SRR register.
TW don’t affect the output condition.

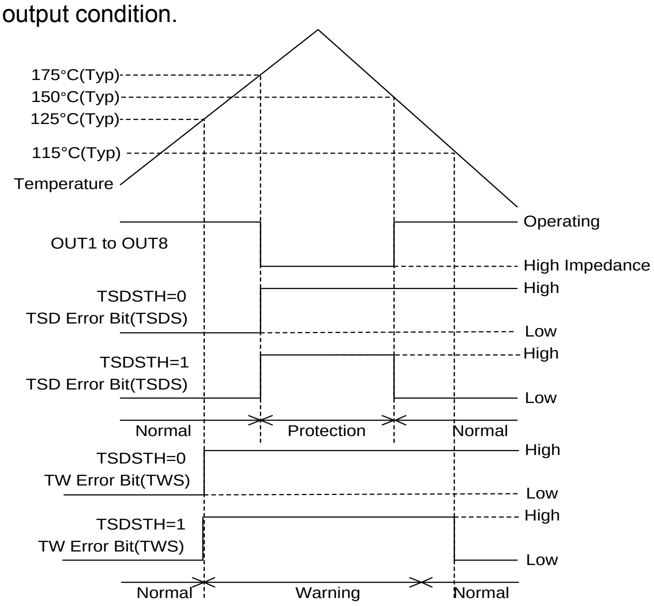


Figure 15. TSD / TW Timing Chart

Description of Blocks – continued

6. Under Load Detection (ULD)

When the current flows 11mA(Typ) or below at the output terminal and pass 370µs(Typ), Under Load is detected. And UNDERLOADS register is set '1'. The output is not turned off if Under Load is detected, but the fault is latched by the UNDERLOADS register. In order to release the latch, it has to be reset by SRR register. This 370µs delay time is implemented to avoid the malfunction caused by noise. Register UNDERLOAD1 to UNDERLOAD8 can be set to specify ULD condition for the respective channels. (Please refer the output data register tables.)

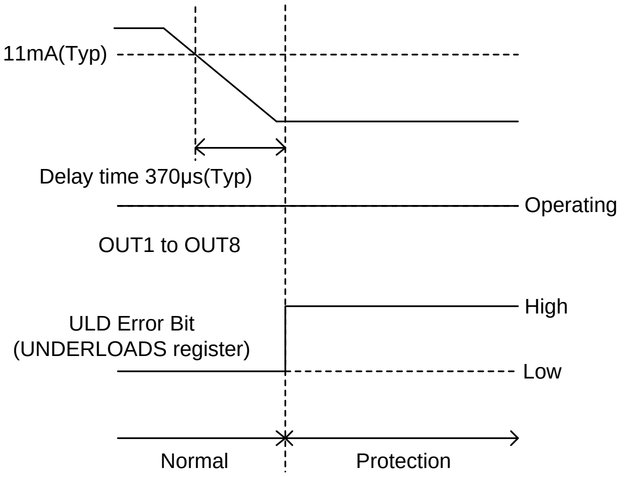


Figure 16. Under Load Timing Chart 1

(Note)
When use the motor that the detection time need more than 370µs(Typ) such as Figure 17, please set UNDERLOAD register to '1' at once, and then reset UNDERLOAD register to '0' after the load current becomes stable.

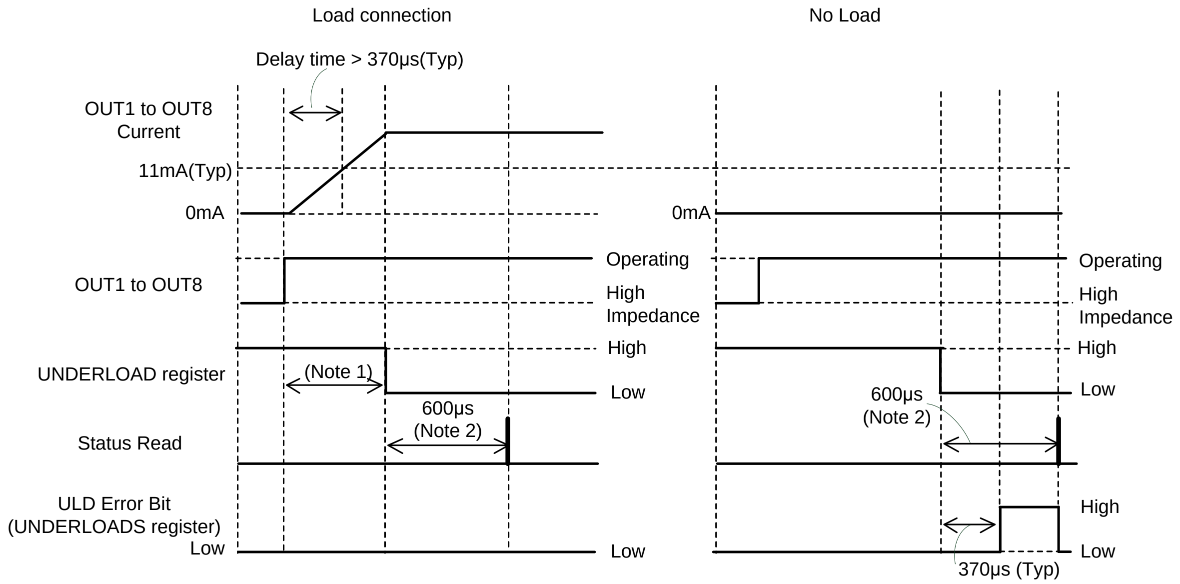
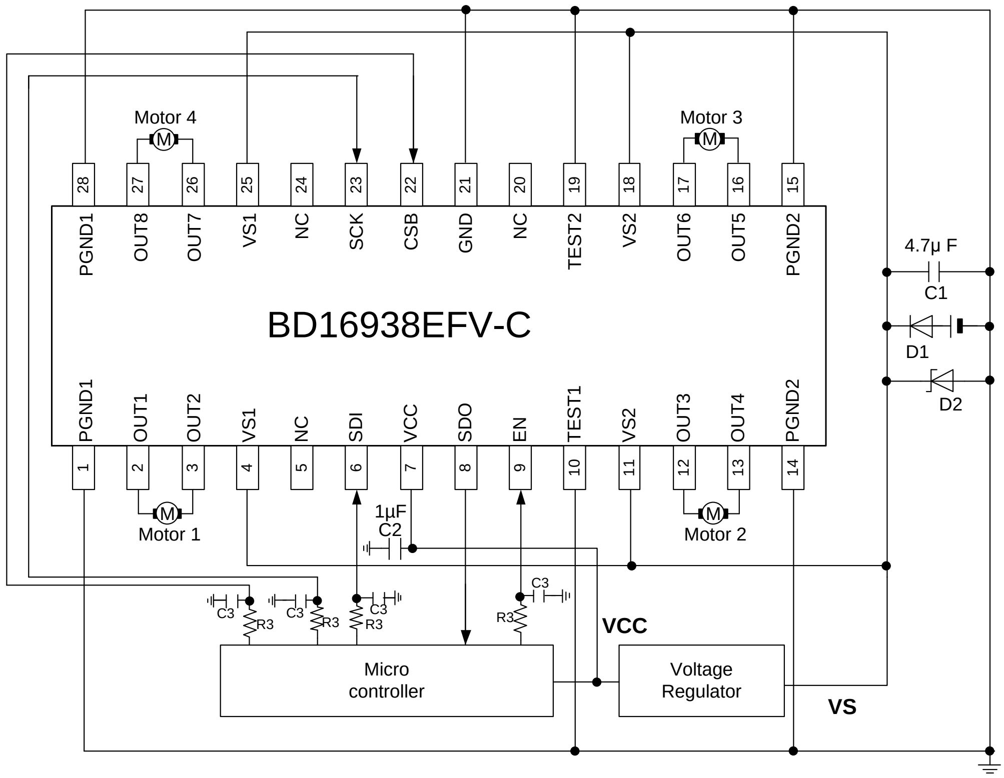


Figure 17. Under Load Timing Chart 2

(Note 1) This time should be determined based on response of the load connected.
(Note 2) OPEN detection time requires minimum 600µs, so please use it by an interval of at least 600µs.

Recommended Application Example



The external circuit constants shown in the diagram above represent a recommended value, respectively.
(NC terminal: OPEN)

Figure 18. Recommended Application Example

Cautions on Designing of Application Circuits

1. Applicable Motors

Be noted that The BD16938EFV-C motor driver can only drive DC motors and cannot drive stepping motors.

2. VS and VCC

Be sure to mount a power supply capacitor in the vicinity of the IC pins between the VS and PGND and between the VCC and GND. Determine the capacitance of the capacitor after fully ensuring that it presents no problems in characteristics. (The recommended value of between VS and GND is 4.7µF or more. The recommended value of between VCC and GND is 1.0µF or more.)
Cause a short circuit between VS (set them to the same potential) before using the IC.

3. Counter-Electromotive Force

The counter-electromotive force may vary with operating conditions and environment, and individual motor characteristics. Fully ensure that the counter-electromotive force presents no problems in the operation or the IC.

4. Fluctuations in Output Pin Voltage

If any output pin makes a significant fluctuation in the voltage to fall below GND potential due to heat generation conditions, power supply, motor to be used, and other conditions, this may result in malfunctions or other failures. In such cases, take appropriate measures, including the addition of a Schottky diode between the output pin and ground.

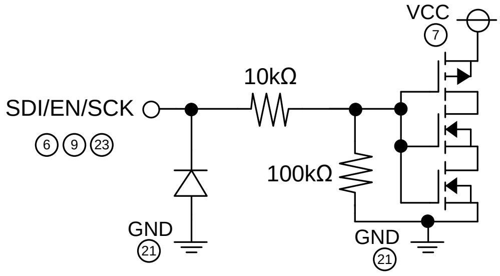
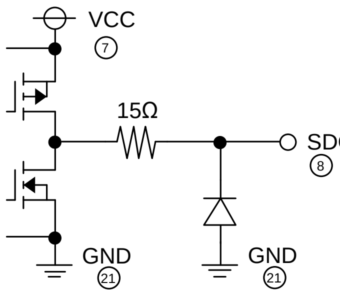
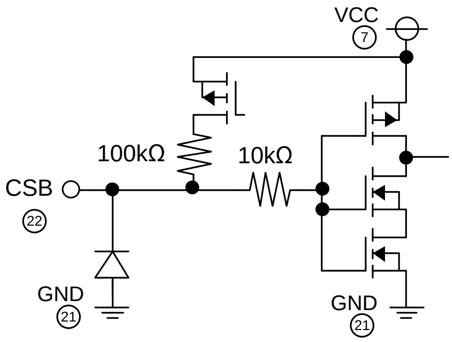
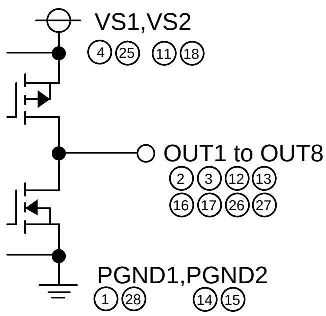
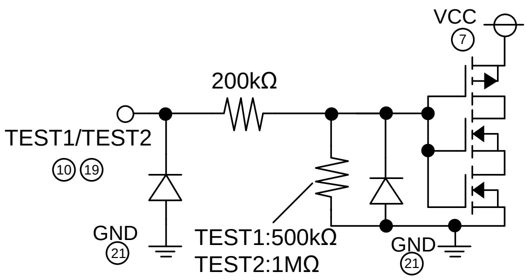
5. Rush Current

This IC has no built-in circuit that limits rush currents caused by applying current to the power supply or switching operation mode. To avoid the rush currents, take physical measures such as adding a current-limiting resistor between VS pins and the power supply.

6. Thermal Pad

Since a thermal pad is connected to the sub side of this IC, connect it to the ground potential. Do not use the thermal pad as ground interconnect.

I/O Equivalence Circuits

Pin No.	Pin Name	I/O Equivalence Circuit
6 9 23	SDI EN SCK	
8	SDO	
22	CSB	
2, 3 12, 13 16, 17 26, 27	OUT1 to OUT8	
10 19	TEST1 TEST2	

The resistance values shown in the above diagram are typical values.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

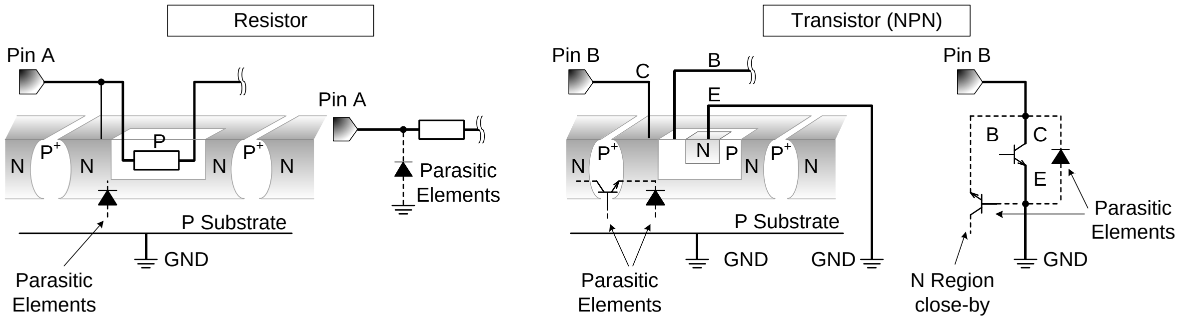


Figure 19. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC’s maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

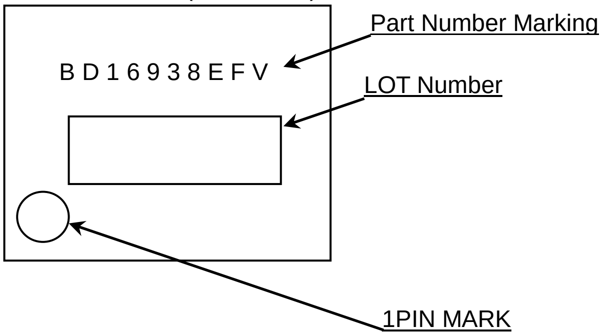
Ordering Information

B D 1 6 9 3 8 E F V - CE 2

- Part Number
- Package
  EFV: HTSSOP-B28
- Product Rank
  C: for Automotive
  Packing and Forming Specification
  E2: Embossed Tape and Reel

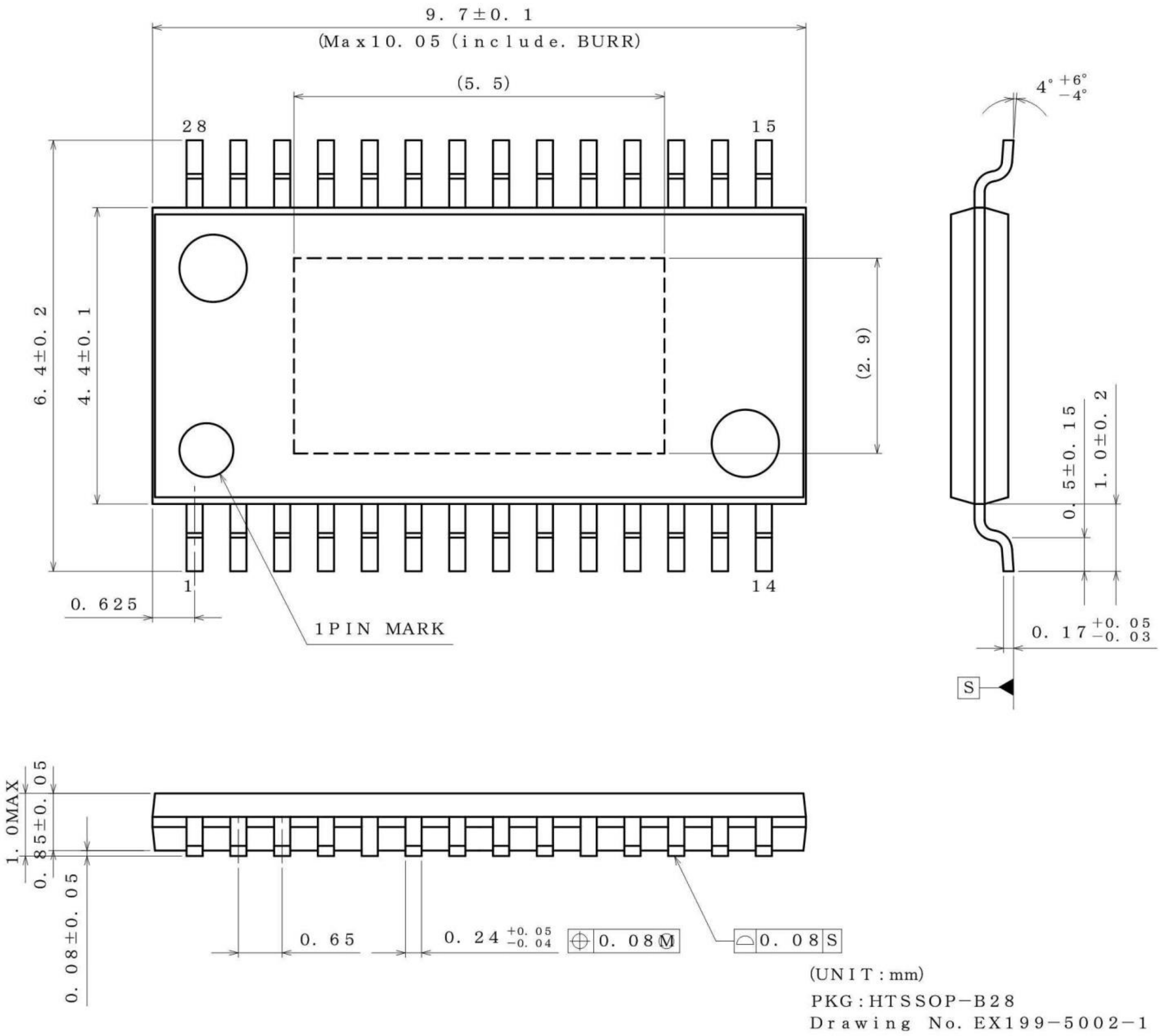
Marking Diagram

HTSSOP-B28 (TOP VIEW)



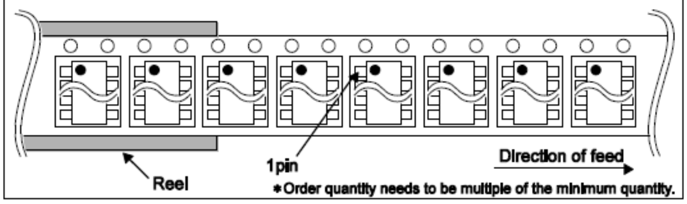
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
28.Feb.2017	001	New Release

Notice

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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