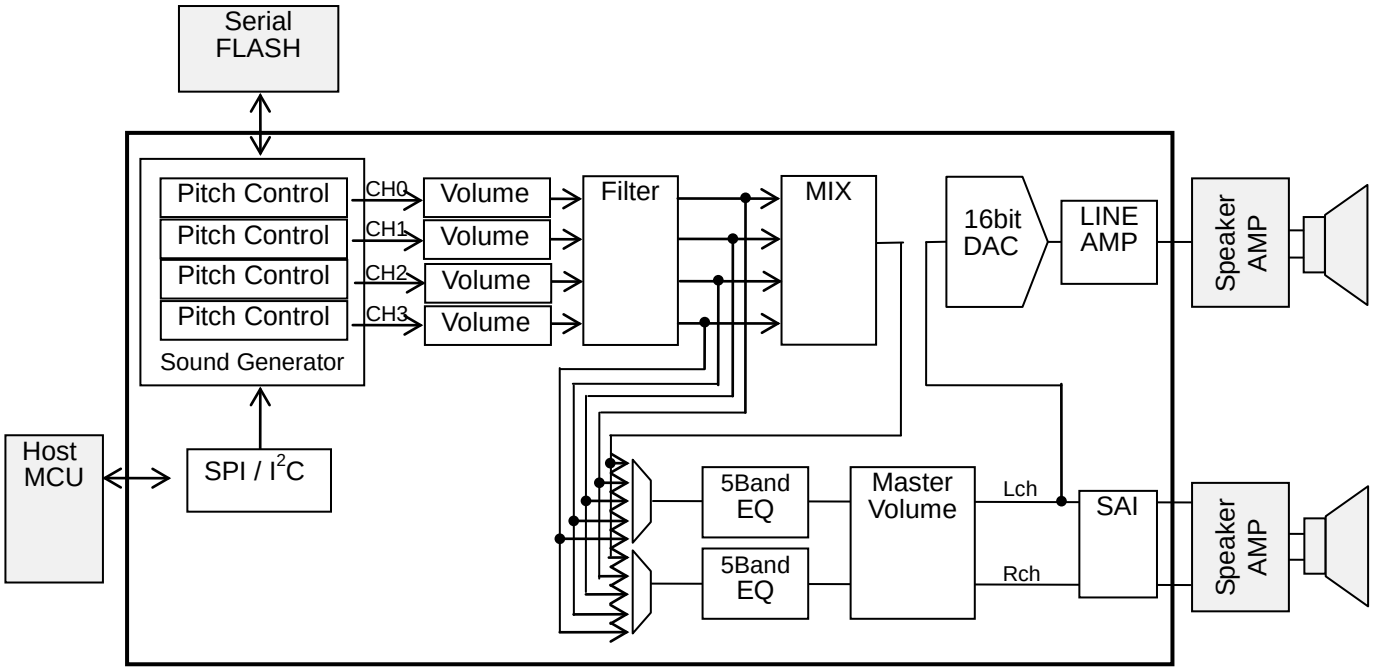
ML22120

Speech Synthesis LSI with pitch control function for Automotive

■ Overview

ML22120 is a speech synthesis LSI with a serial flash memory interface for sound data and compatible with the sound data playback function (Sound Generator).
It has a Clock Synchronous Serial Interface and I^2C interface (slave).
The pitch and volume can be changed dynamically by controlling the setting register.
It adopts a 16-bit D/A converter and low-pass filter which realize high-quality sound.
It has the 5Band equalizer as a sound quality effect processing.
The functions necessary for sound output are integrated into a single chip, so that sound functions can be realized simply by adding this LSI and an external speaker amplifier.

In this data sheet, the sound data playback function is referred to as Sound Generator.



Application Circuit

■ Feature

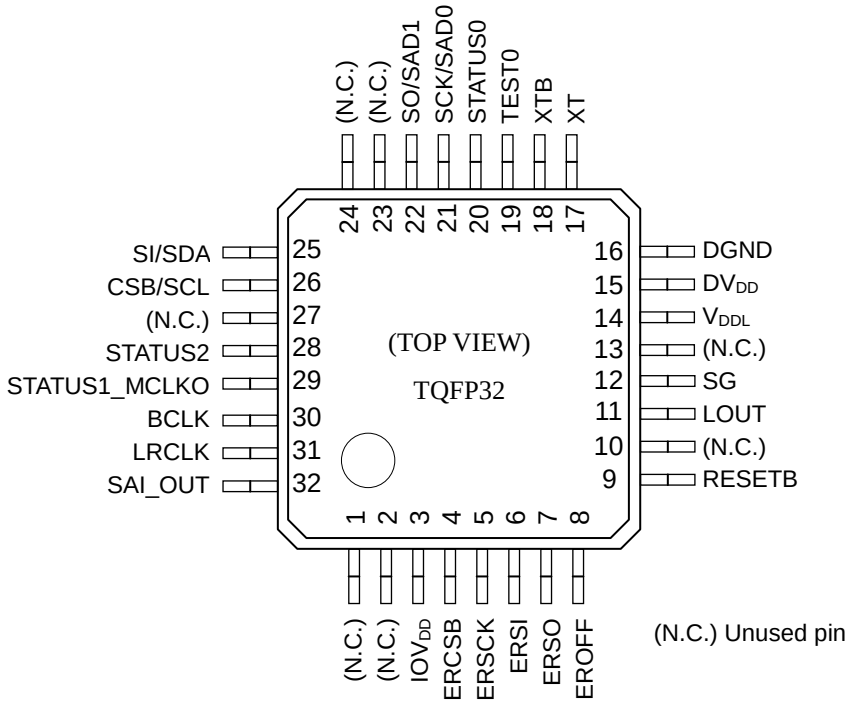
- Sound Generator
  - Speech synthesis algorithm: 16bit Straight PCM
  - Maximum number of phrases: 64 Phrases
  - Flash memory capacity: Maximum 128Mbits

Sampling frequency (kHz)	48.0	24.0	12.0	32.0	16.0	8.0
Maximum sound production time (sec)	174	349	698	262	524	1048

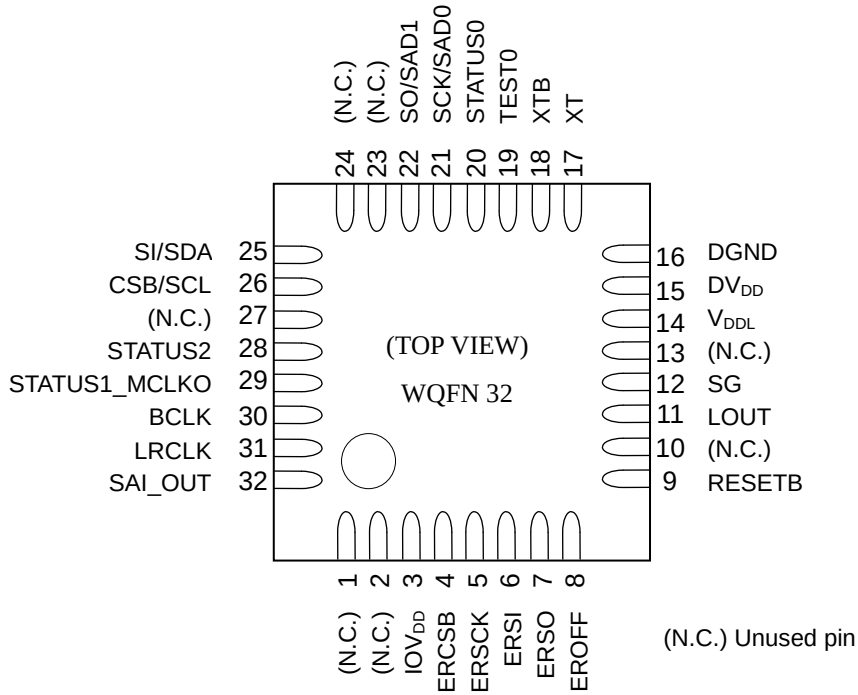
- Sampling frequency: 48.0kHz/24.0kHz/12.0kHz, 32.0kHz/16.0kHz/8.0kHz
- Playback function
  - Repeat function
  - Mixing-function: 4-channels
  - Volume adjustment function:
    - Volume setting for each channel -76.7dB to +25.5dB/0.1dB step (including MUTE)
    - Master volume setting for Lch/Rch -76.7dB to +25.5dB/0.1dB step (including MUTE)
    - With fade function
  - Pitch adjustment function: 4-channels
    - CH0/CH1:0.0625 times to 4 times (0.00390625 times step)
    - CH2/CH3:0.0625 times to 1 times (0.00390625 times step)
    - With fade function
- Serial audio interface (master)
  - PCM format: 16bit Straight PCM
  - Sampling frequency at transfer(gfs): 48.0/32.0kHz (not depend on the sampling frequency of the Sound Generator)
  - Data length: 16bit
  - MCLK frequency: 128/256/512gfs selectable
  - BCLK frequency: 32gfs to 64gfs
  - LRCLK transfer mode/ frame synchronous transfer mode selectable
  - LRCLK forward/reverse selectable
  - 1-bit delay ON/OFF selectable
  - MSB first/LSB first selectable
- 5Band equalizer — Band center frequency, Band width, and Gain can be set.
- Low-pass filter
- 16-bit D/A converter
- Line amplifier output: 10kΩ driving
- MCU interface: Clock Synchronous Serial Interface/I^2C Interface (Slave)
- Master clock frequency: 4.096MHz, 4.000MHz
- Power-supply voltage: 2.7V to 3.6V
- Power-supply voltage for a serial flash memory interface: 2.7V to 3.6V
- Operating temperature range: -40 ^{O}C to +105 ^{O}C（ +125 ^{O}C^{*1}） *1 Key interlocking application
- Package: 32-pin TQFP (7mm x 7mm, 0.8mm pitch)
  32-pin WQFN (5mm x 5mm, 0.5mm pitch)
  24-pin WQFN (4mm x 4mm, 0.5mm pitch)
- Ordered Part Name: ML22120TB (32-pin TQFP)
  ML22120GD (32-pin WQFN) Under Development
  ML22120GP (24-pin WQFN)

■ Pin Configuration (TOP VIEW)

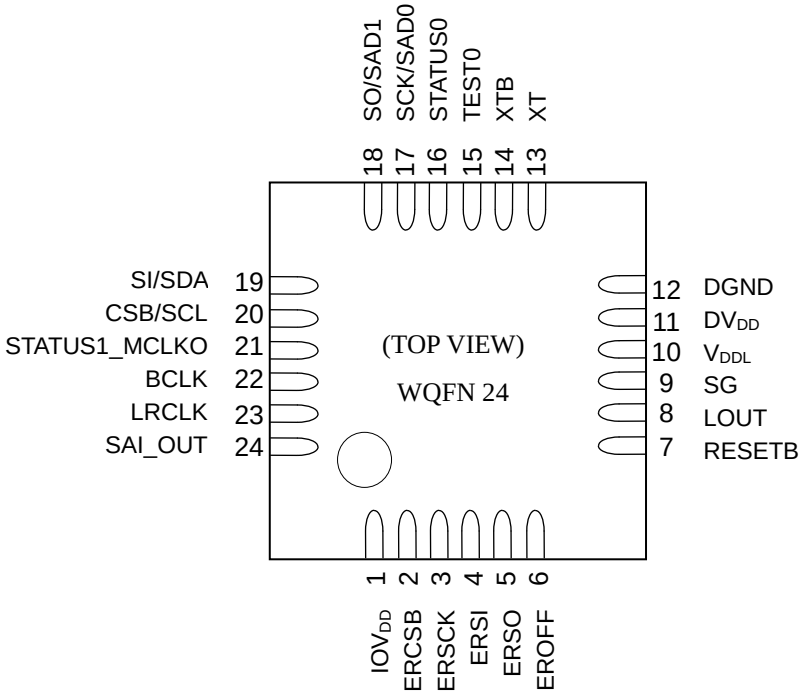
● ML22120TB



● ML22120GD



● ML22120GP



■ Pin Description

Pin 32 pin	Pin 24 pin	Symbol	I/O	Attribute	Description	Initial value *1
3	1	IOV_{DD}	P	-	Serial flash memory interface power supply pin. Connect a bypass capacitor between this pin and the DGND pin.	—
4	2	ERCSB	O	Negative	Serial flash memory interface chip select output pin. Output the "H" level during non-access and the "L" level during access. Setting the EROFF pin to "L" enables output.	H
5	3	ERSCK	O	-	Serial flash memory interface serial clock output pin. Setting the EROFF pin to "L" enables output.	L
6	4	ERSI	I	-	Serial flash memory interface serial data input pin. Setting the EROFF pin to "L" enables input. A pull-down resistor is internally connected.	L
7	5	ERSO	O	-	Serial flash memory interface serial data output pin. Setting the EROFF pin to "L" enables output.	L
8	6	EROFF	I	Positive	Pin to disable the serial flash memory interface. When this bit is set to "L", the serial flash memory interface pin is enabled. A pull-down resistor is internally connected. Set this pin to "L" during playback operation using serial flash memory. When this pin set to "H", the serial flash memory interface is in a condition of high-impedance. Set to "H" when rewriting by connecting the FLASH writer to ERCSB / ERSCK / ERSI / ERSO.	L
9	7	RESETB	I	Negative	Reset-input pin. The LSI is initialized by the "L" level input. After a reset is input, all the circuits stop operating and enter the standby state. At power-on, input an "L" level to this pin. After the power supply voltage stabilizes, set this pin to an "H" level.	—
11	8	LOUT	O	-	Used exclusively for line amplifier output.	L
12	9	SG	O	-	Reference voltage output pin for line amplifier. Connect a capacitor between this pin and DGND pin.	L
14	10	V_{DDL}	O	-	1.5V regulator output pin. Used as internal power supply. Connect a capacitor between this pin and DGND pin as close as possible.	L
15	11	D_{VDD}	P	-	Digital power supply pin. Connect a bypass capacitor between this pin and the DGND pin.	—
16	12	DGND	G	-	Digital ground pin.	—
1, 2, 10, 13, 23, 24, 27	-	N.C.	-	-	Unused pin. Leave open.	Hi-Z

*1 Initial value at reset input and standby. The pin whose IO is "I" indicates a fixed level from outside.

Pin 32 pin	Pin 24 pin	Symbol	I/O	Attribute	Description	Initial value *1
17	13	XT	I	Negative	Crystal or ceramic resonator connection pin. A feedback resistor of about 1MΩ is built in between the XT pin and the XTB pin. To use an external clock, input from this pin. Delete the capacitor when a crystal or ceramic resonator is connected. When using a resonator, connect it as close as possible. Leave it open when not in use.	L
18	14	XTB	O	Positive	Crystal or ceramic resonator connection pin. When an external clock is used, leave it open and capacitor is not required when a crystal or ceramic resonator is connected. When using a resonator, connect it as close as possible. Leave it open when not in use.	H
19	15	TEST0	I	Positive	Input pin for testing. A pull-down resistor is internally connected. Fix to the DGND.	L
20	16	STATUS0	O	-	Status output pin 0. Set the OUTSTAT0_0 to 5 registers to select the output of various statuses, playback status of each channel, and internal error status.	L
21	17	SCK/SAD0	I	-	SCK: Synchronous serial interface clock input pin.	L
			I	-	SAD0: I^2C slave address select pin. Set the slave address by fixing it to DV_{DD} or DGND.	—
22	18	SO/SAD1	O	-	SO: Synchronous serial interface data output pin. When the status is read, the data is output in synchronization with SCK. when the status is not read, this pin enters a high-impedance state.	Hi-Z
			I	-	SAD1: I^2C slave address select pin. Set the slave address by fixing it to DV_{DD} or DGND.	—
25	19	SI/SDA	I	-	SI: Synchronous serial interface data input pin. Data is fetched in synchronization with SCK.	L
			IO	-	SDA: I^2C slave serial data input/output pin. An input / output pin used for setting the write mode / read mode, writing the slave address, and writing / reading data. When using an I^2C, be sure to insert a pull-up resistor between DV_{DD} pin. Output: Nch MOS OPEN DRAIN output Input: High-impedance input	Hi-Z
26	20	CSB/SCL	I	Negative	CSB: Synchronous serial interface chip select pin. The SCK and SI inputs are accepted only when this pin is at the "L" level.	H
			I	-	SCL: I^2C slave serial clock pin. When using an I^2C, be sure to insert a pull-up resistor between DV_{DD} pin.	Hi-Z
28	-	STATUS2	O	-	Status output pin 2. Set the OUTSTAT2 register to select internal error status.	L
29	21	STATUS1_ MCLKO	O	-	Status output pin 1 or SAI master clock output pin. When the MCLKSEL bit of the IFSEL register is set to "0", set the OUTSTAT1_0 to 5 registers to select the output of various statuses, playback status of each channel, and internal error status. When the MCLKSEL bit of the IFSEL register is set to "1", SAI master clock is output.	L
30	22	BCLK	O	-	SAI bit clock output pin.	L
31	23	LRCLK	O	-	SAI word clock output pin.	L
32	24	SAI_OUT	O	-	SAI bit data output pin. Output data at the falling edge of BCLK.	L

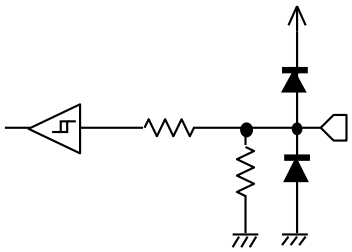
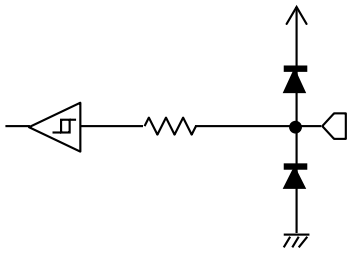
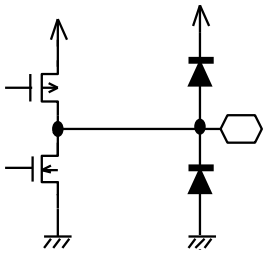
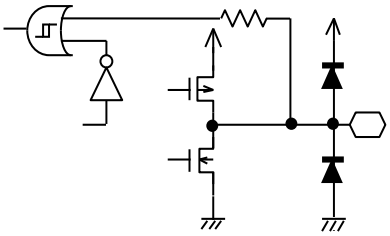
*1 Initial value at reset input and standby. The pin whose IO is "I" indicates a fixed level from outside.

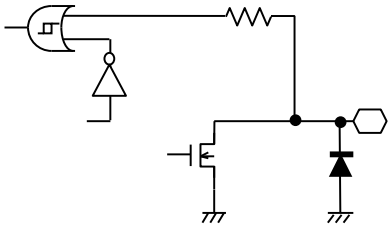
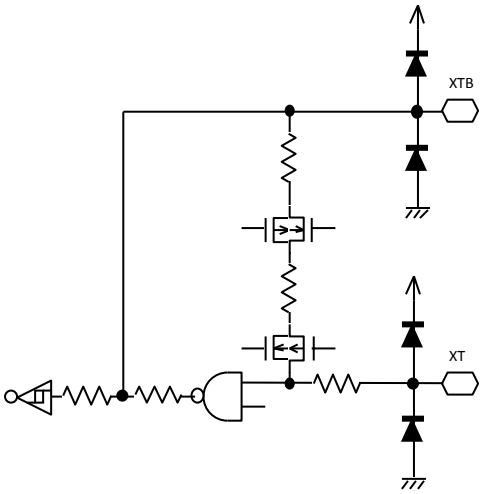
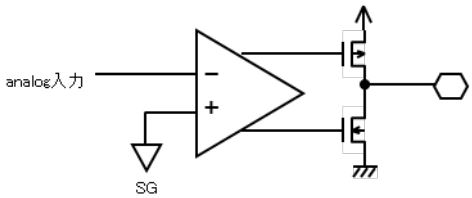
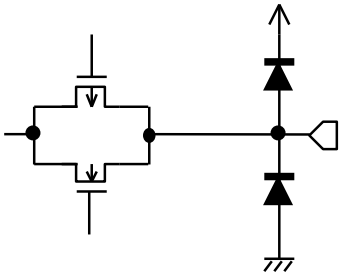
■ Termination of Unused Pins

This section explains how to terminate unused pins.

Symbol	Recommended pin termination
EROFF	Connect to the DGND.
TEST0	
XT	Leave open.
XTB	
LOUT	
STATUS0	
STATUS1_ MCLKO	
STATUS2	
BCLK	
LRCLK	
SAI_OUT	
N.C.	

■ I/O Equivalent Circuit

Classification	Circuit	Overview
A		Attribute: Input Power: DV_{DD} Function: CMOS inputs with pull-down Applicable pin: TEST0
		Attribute: Input Power: IOV_{DD} Function: CMOS inputs with pull-down Applicable pin: EROFF, ERSI
B		Attribute: Input Power: DV_{DD} Function: CMOS inputs Applicable pin: SCK/SAD0, RESETB
C		Attribute: Output Power: DV_{DD} Function: CMOS outputs Applicable pin: STATUS0, STATUS1_MCLKO, STATUS2, LRCLK, BCLK, SAI_OUT
		Attribute: Output Power: IOV_{DD} Function: CMOS outputs Applicable pin: ERCSB, ERSCK, ERSO
D		Attribute: Input/output Power: DV_{DD} Function: CMOS inputs / outputs Applicable pins: SO/SAD1

Classification	Circuit	Overview
E		Attribute: input/output Power: DV_{DD} Function: CMOS inputs / Nch Open Drain outputs Applicable pins: CSB/SCL, SI/SDA
F		Attribute: Oscillator circuit Power: DV_{DD} Function: 4.096M, 4.000M oscillation Applicable pins: XT, XTB
G		Attribute: Analog Power: DV_{DD} Function: Sound output Applicable pin: LOUT
H		Attribute: Analog Power: DV_{DD} Function: Line amplifier reference voltage output Applicable pins: SG

■ Electrical characteristics

● Absolute maximum rating

DGND=0V, Ta=25°C

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	DV_{DD} IOV_{DD}	—	-0.3 to +4.6	V
Input voltage 1	V_{IN1}	—	-0.3 to DV_{DD}+0.3	V
Input voltage 2	V_{IN2}	—	-0.3 to IOV_{DD}+0.3	V
Allowable loss	P_D	When the LSI is mounted on JEDEC 2-layer board.	1000	mW
Output short-circuit current	I_{OS}	Applies to pins other than V_{DDL} pin.	10	mA
		Applies to the V_{DDL} pin.	50	mA
Storage temperature	T_{STG}	—	-55 to +150	°C

● Recommended operating conditions

DGND=0V

Parameter	Symbol	Condition	Range			Unit
DV_{DD}, IOV_{DD}, Power-supply voltage	DV_{DD} IOV_{DD}	—	2.7 to 3.6			V
Operating temperature	Top	—	-40 to +105 (+125[*1])			°C
			Min.	Typ.	Max.	
Master clock frequency	f_{OSC}	—	Typ -5%	4.096 4.000	Typ +5%	MHz

*1 Key interlocking application

● DC characteristics

DV_{DD}=IOV_{DD}=2.7 to 3.6V, DGND=0V, Ta=-40 to +125°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.*1	Max.	Unit
"H" input voltage 1	V_{IH1}	—	CSB/SCL SCK/SAD0 SI/SDA (SO)/SAD1 XT RESETB TEST0	0.8×DV_{DD}	—	DV_{DD}	V
"H" input voltage 2	V_{IH2}	—	EROFF ERSI	0.8×IOV_{DD}	—	IOV_{DD}	V
"L" input voltage 1	V_{IL1}	—	CSB/SCL SCK/SAD0 SI/SDA (SO)/SAD1 XT RESETB TEST0	0	—	0.2×DV_{DD}	V
"L" input voltage 2	V_{IL2}	—	EROFF ERSI	0	—	0.2×IOV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = -50µA	XTB	DV_{DD}-0.4	—	—	V
"H" output voltage 2	V_{OH2}	I_{OH} = -1mA	LRCLK BCLK SAI_OUT SO/(SAD1) STATUS0 STATUS1_MCLKO STATUS2	DV_{DD}-0.4	—	—	V
"H" output voltage 3	V_{OH3}	I_{OH} = -1mA	ERCSB ERSCK ERSO	IOV_{DD}-0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 50µA	XTB	—	—	0.4	V
"L" output voltage 2	V_{OL2}	I_{OL} = 2mA	LRCLK BCLK SAI_OUT SO/(SAD1) STATUS0 STATUS1_MCLKO STATUS2	—	—	0.4	V
"L" output voltage 3	V_{OL3}	I_{OL} = 2mA	ERCSB ERSCK ERSO	—	—	0.4	V
"L" output voltage 4	V_{OL4}	I_{OL} = 3mA	(SI)/SDA (CSB)/SCL	—	—	0.4	V
Output leakage current 1	I_{OOH1}	VOH=DV_{DD} (in high-impedance state)	(SI)/SDA (CSB)/SCL SO/(SAD1)	—	—	10	µA
	I_{OOL1}	VOL=DGND (in high-impedance state)		–10	—	—	µA
Output leakage current 2	I_{OOH2}	VOH=IOV_{DD} (in high-impedance state)	ERCSB ERSCK ERSO	—	—	10	µA
	I_{OOL2}	VOL=DGND (in high-impedance state)		–10	—	—	µA

DV_{DD}=IOV_{DD}=2.7 to 3.6V, DGND=0V, Ta=-40 to +125°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.*1	Max.	Unit
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	XT	0.8	5.0	20	µA
"H" input current 2	I_{IH2}	V_{IH} = DV_{DD}	CSB/SCL SCK/SAD0 SI/SDA (SO)/SAD1 RESETB	—	—	10	µA
"H" input current 3	I_{IH3}	V_{IH} = DV_{DD}	TEST0	20	300	700	µA
"H" input current 4	I_{IH4}	V_{IH} = IOV_{DD}	EROFF	20	300	700	µA
"H" input current 5	I_{IH5}	V_{IH} = IOV_{DD}	ERSI	2	40	300	µA
"L" input current 1	I_{IL1}	V_{IL} = DGND	XT	–20	–5.0	–0.8	µA
"L" input current 2	I_{IL2}	V_{IL} = DGND	CSB/SCL SCK/SAD0 SI/SDA (SO)/SAD1 RESETB EROFF TEST0	–10	—	—	µA
During playback Current consumption	I_{DDO}	f_{OSC}=4.096MHz fs=48kHz, f=1kHz, (4ch simultaneous) operating the line amplifier output	—	—	6*2	15*2	mA
Standby Current consumption*3	I_{DDS}	Ta=-40 to +55°C	—	—	1*2	10.0*2	µA
		Ta=-40 to +125°C	—	—	1*2	30.0*2	µA

*1 Typ. : DV_{DD}=IOV_{DD}=3.0V,DGND=0 V,Ta=25°C

*2 Total values of the DV_{DD} pin and IOV_{DD} pin

*3 RESETB pin is at the “L” level.

● Analog Part Characteristics

DV_{DD}=IOV_{DD}=2.7 to 3.6V, DGND=0V, Ta=-40 to +125°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RC4MHz	Frc	—	3.68	4.096	4.51	MHz
Line amplifier output resistance	R_{LA1}	When 1/2DV_{DD} ± 1 mA is applied	—	—	300	Ω
Line amplifier output-load-resistance	R_{LA2}	For DGND	10	—	—	kΩ
Line amplifier Out put Voltage Range	V_{AO}	No output load	DV_{DD} /6	—	DV_{DD}×5/6	V
SG pin output voltage	V_{SG}	—	0.95x DV_{DD} /2	DV_{DD} /2	1.05x DV_{DD} /2	V
SG pin output resistance	R_{SG}	—	57	96	135	kΩ

● AC characteristic

DV_{DD}=IOV_{DD}=2.7 to 3.6V, DGND=0V, Ta=-40 to +125°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle	f_{duty}	—	40	50	60	%
RESETB input pulse width	t_{RST}	—	10	—	—	µs
Reset noise rejection pulse width	t_{NRST}	RESETB pin	—	—	0.1	µs
Initialization time after reset release	t_{PRC}	—	—	—	5	ms
Line amplifier power up time (with Pop Noise Suppression)	t_{PUP1}	4.096MHz external clock input POP="H" OUT_EN="L"→"H"	—	73	77	ms
Line amplifier power up time (without Pop Noise Suppression)	t_{PUP0}	4.096MHz external clock input POP="L" OUT_EN="L"→"H"	—	33	37	ms
Line amplifier power down time (with Pop Noise Suppression)	t_{PD1}	4.096MHz external clock input POP="H" OUT_EN="H"→"L"	—	144	148	ms
Line amplifier power down time (without Pop Noise Suppression)	t_{PD0}	4.096MHz external clock input POP="L" OUT_EN="H"→"L"	—	104	108	ms
Playback start time	t_{PSTA}	f_{OSC} = 4.096MHz	—	—	400	µs
Fade start time	t_{FAD}	f_{OSC} = 4.096MHz	—	—	400	µs
Playback stop time	t_{PSTP}	f_{OSC} = 4.096MHz	—	—	5	ms

● AC Characteristics (Clock Synchronous Serial Interface)

DV_{DD}=IOV_{DD}=2.7 to 3.6V, DGND=0V, Ta=-40 to +125°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK setup time from CSB falling edge	t_{SCKS}	—	100	—	—	ns
SCK input enable time from CSB falling edge	t_{ESCK}	—	100	—	—	ns
SCK hold time from CSB rising edge	t_{CSH}	—	100	—	—	ns
Data floating time from CSB rising edge	t_{DOZ}	RL=3KΩ	—	—	100	ns
Data setup time from SCK	t_{DIS}	—	50	—	—	ns
Data hold time from SCK	t_{DIH}	—	50	—	—	ns
Data output delay time from SCK	t_{DOD}	—	—	—	90	ns
SCK "H" level pulse width	t_{SCKH}	—	100	—	—	ns
SCK "L" level pulse width	t_{SCKL}	—	100	—	—	ns

<When rewriting the flash memory using the clock synchronous serial interface>

DV_{DD}=IOV_{DD}=2.7 to 3.6V, DGND=0V, Ta=-40 to +125°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK setup time from CSB falling edge	t_{SCKS}	—	125	—	—	ns
SCK input enable time from CSB falling edge	t_{ESCK}	—	125	—	—	ns
SCK hold time from CSB rising edge	t_{CSH}	—	125	—	—	ns
Data floating time from CSB rising edge	t_{DOZ}	RL=3KΩ	—	—	125	ns
Data setup time from SCK	t_{DIS}	—	50	—	—	ns
Data hold time from SCK	t_{DIH}	—	50	—	—	ns
Data output delay time from SCK	t_{DOD}	—	—	—	110	ns
SCK "H" level pulse width	t_{SCKH}	—	125	—	—	ns
SCK "L" level pulse width	t_{SCKL}	—	125	—	—	ns

● AC Characteristics (I^2C Interface)

DV_{DD}=IOV_{DD}=2.7 to 3.6V, DGND=0V, Ta=-40 to +125°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Min	Max.	Unit
SCL clock frequency	t_{SCL}	0	400	kHz
SCL hold time (start/restart condition)	$t_{HD;STA}$	0.6	—	µs
SCL clock "L" level time	t_{LOW}	1.3	—	µs
SCL clock "H" level time	t_{HIGH}	0.6	—	µs
SCL setup time (restart condition)	$t_{SU;STA}$	0.6	—	µs
SDA hold time	$t_{HD;DAT}$	0	—	µs
SDA setup time	$t_{SU;DAT}$	0.1	—	µs
SDA setup time (stop condition)	$t_{SU;STO}$	0.6	—	µs
Bus free time	t_{BUF}	1.3	—	µs
Capacitive load on each bus line	Cb	—	400	pF

● AC Characteristics (SAI Interface (Master))

DV_{DD}=IOV_{DD}=2.7 to 3.6V, DGND=0V, Ta=-40 to +125°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SAI_BCLK period	tC_BCLK	—	32gfs	—	64gfs	Hz
SAI_BCLK "H" period	tHW_BCLK	—	146	—	—	ns
SAI_BCLK "L" period	tLW_BCLK	—	146	—	—	ns
SAI_LRCLK delay time	tD_LRCLK	—	—	—	20	ns
SAI_SAIOUT delay time	tD_SAIOUT	—	—	—	20	ns

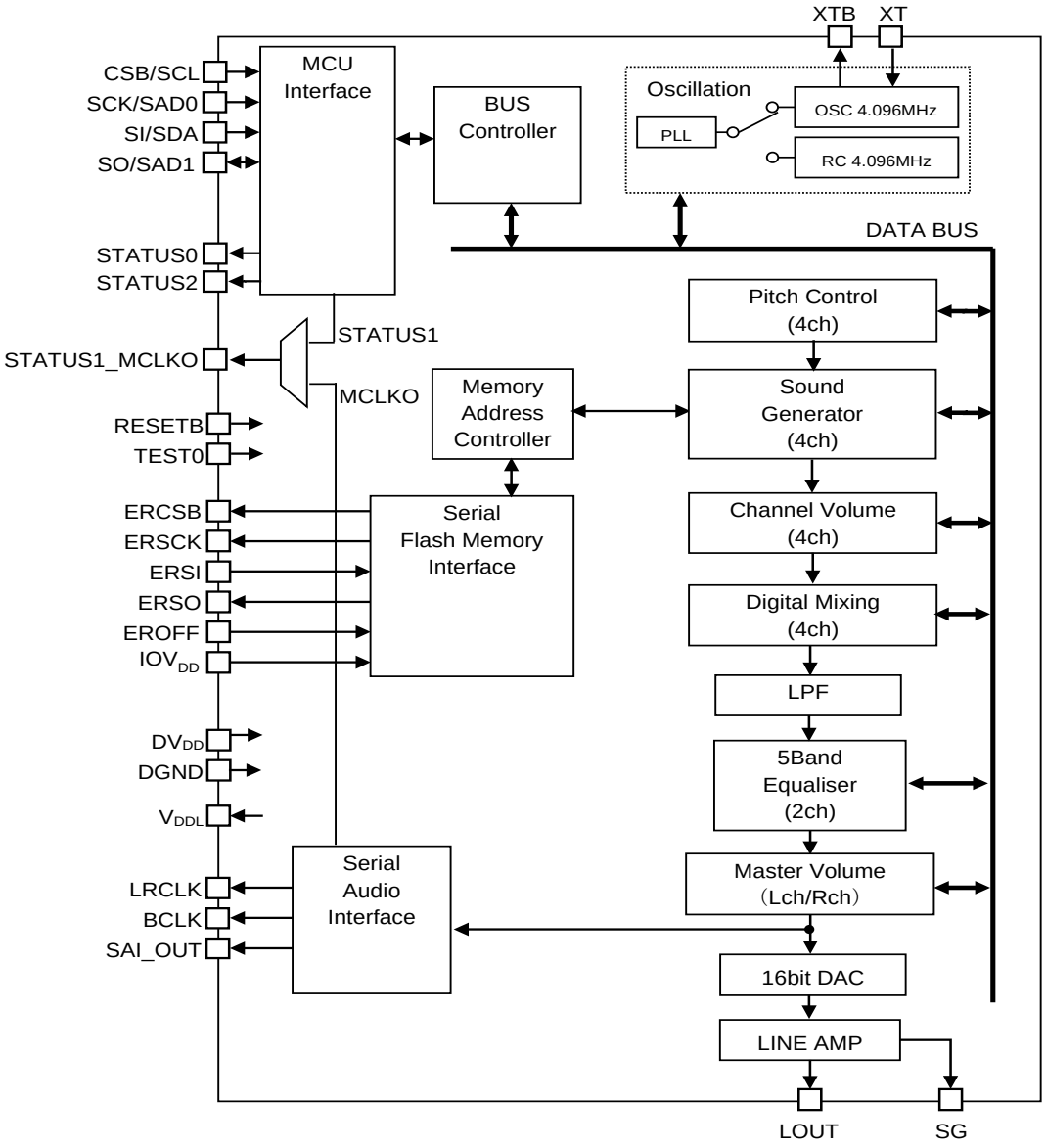
● AC Characteristics (Flash Memory Interface)

DV_{DD}=IOV_{DD}=2.7 to 3.6V, DGND=0V, Ta=-40 to +125°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
ERSCK enable time from ERCSB falling edge	t_{ECSS}	—	50	—	—	ns
ERSCK hold time from ERCSB rising edge	t_{ECSH}	—	50	—	—	ns
Data setup time from ERSCK rising edge	t_{EDIS}	—	10	—	—	ns
Data hold time from ERSCK rising edge	t_{EDIH}	—	10	—	—	ns
Data delay time from ERSCK falling edge	t_{EDOD}	—	—	—	5	ns
ERSCK frequency	t_{ESCKF}	—	1.228	16.384	17.20	MHz
ERSCK "H" level pulse width	t_{ESCKH}	—	26	—	—	ns
ERSCK "L" level pulse width	t_{ESCKL}	—	26	—	—	ns
ERCSB/ERSCK/ERSO delay time from EROFF rising edge	t_{EFLH}	—	—	—	1	ms
ERCSB/ERSCK/ERSO delay time from EROFF falling edge	t_{EFHL}	—	—	—	1	ms

■ Block diagram

The block diagram is shown below.

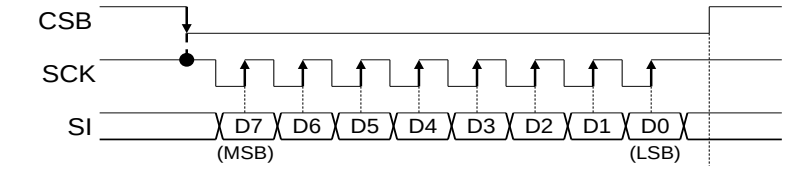


■ Function description

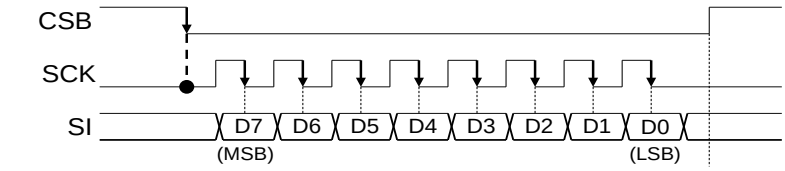
● Clock Synchronous Serial Interface

Various registers are written and read by the CSB, SCK, SI, SO pins.
For data inputting, after "L" level is input to the CSB pin, data is input to the SI pin in MSB first in synchronization with the input clock signal of the SCK pin. The SI pin data is loaded into the LSI in synchronization with the SCK pin clock, and the input data is determined by the SCK pin clock of the eighth pulse.
Write access and read access to the register can be selected according to the MSB data when each register address is set.
When the MSB of the address data is set to the “L” level, write access is performed, and the SI pin data is taken into the LSI as write data in synchronization with the SCK pin clock. If the MSB of the address data is set to “H” level, read access is performed and the data is output from the SO pin in synchronization with the SCK pin clock.
The address is automatically incremented while the CSB is at the "L" level, and data can be written and read continuously.
The selection of the rising or falling edge of the SCK pin clock depends on the state of the SCK pin at the falling edge of the CSB pin.
When the SCK pin is "H" at the falling edge of the CSB pin, the SI pin data is loaded into the LSI on the rising edge of the SCK pin clock, and the status signal is output from the SO pin on the falling edge of the SCK pin clock.
When the SCK pin is "L" at the falling edge of the CSB pin, the SI pin data is loaded into the LSI on the falling edge of the SCK pin clock, and the status signal is output from the SO pin on the rising edge of the SCK pin clock.
The serial interface can be returned to the initial state by setting the CSB pin to "H" level.
When the CSB pin is “H” level or when read data isn’t output, the SO pin is in a high impedance state.

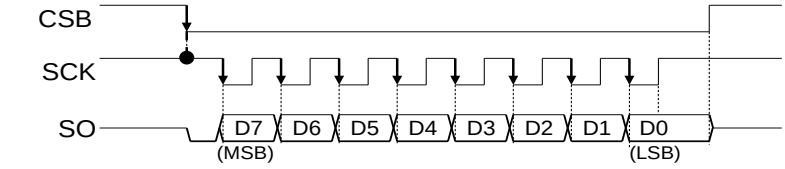
Data input timing: SCK rising edge operation
(When the SCK is "H" at the falling edge of the CSB)



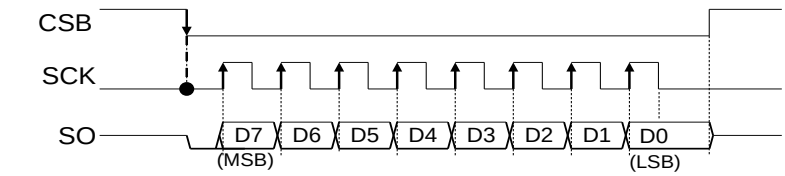
Data input timing: SCK falling edge operation
(When the SCK is "L" at the falling edge of the CSB)



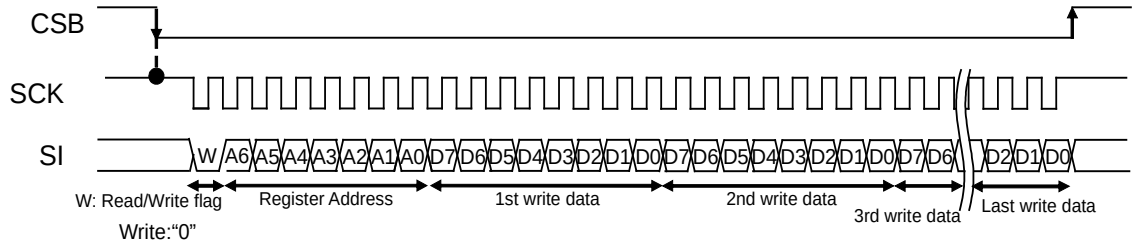
Data output timing: SCK falling edge operation
(When the SCK is "H" at the falling edge of the CSB)



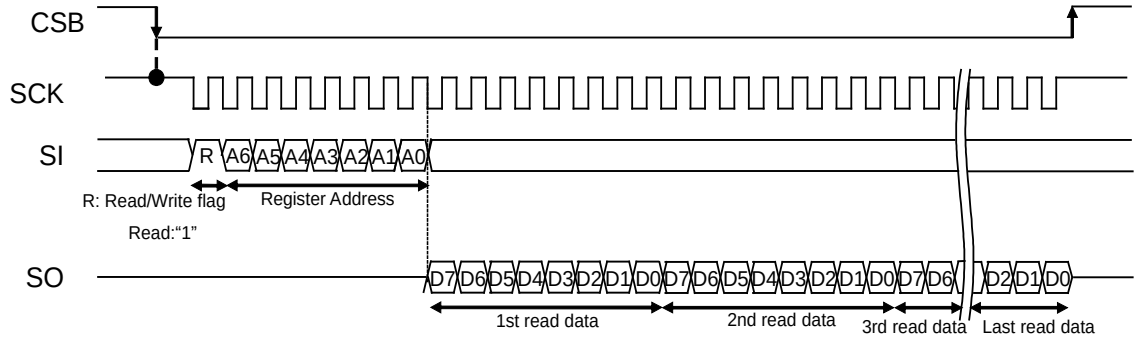
Data output timing: SCK rising edge operation
(When the SCK is "L" at the falling edge of the CSB)



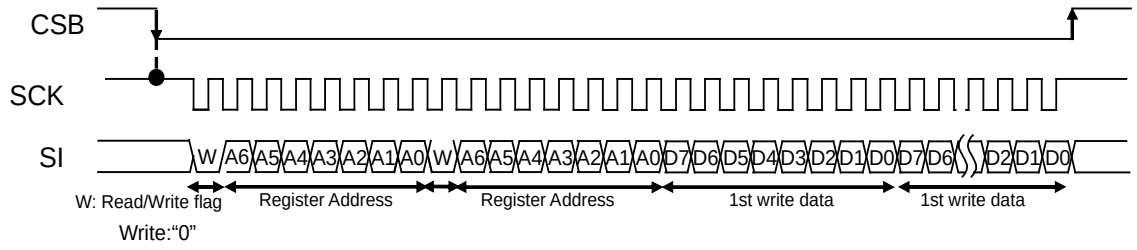
- One-time input mode
  - Timing chart when writing data



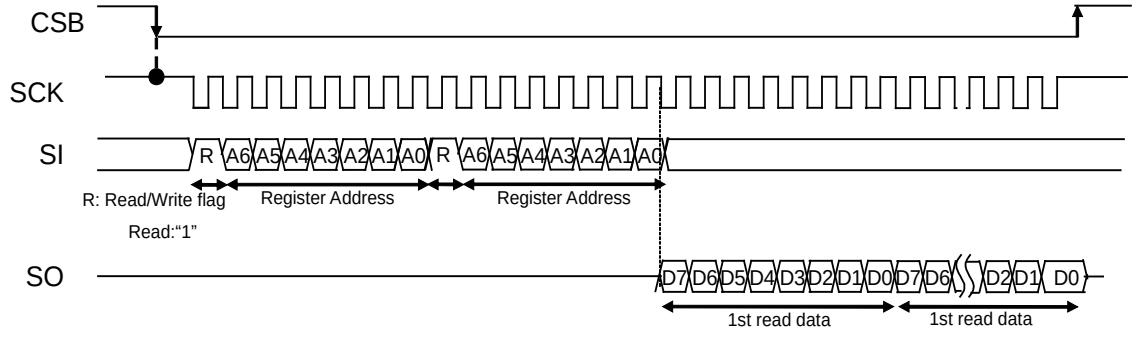
  - Timing chart when reading data



- Two-times input mode
  - Timing chart when writing data



  - Timing chart when reading data



In the two-times input mode, if two-times input error is detected when reading a register, read data "1" is output.

● I^2C Interface (Slave)

This serial interface conforms to the I^2C bus specifications. It supports Fast modes and can transmit and receive data at 400kbit/s. The SCL and SDA pins are used to write various register and to read the status. The slave addresses are set by the SAD 0 to 1 pins.
When I^2C is used, be sure to connect a pull-up resistor between SCL and SDA pins and DV_{DD} pin.
In the communication flow between the master and this device (slave) on the I^2C bus, after the start condition is set, the slave address (upper 3 bits of the slave address are set by the SAD0 to 1 pins) is entered in the first 7 bits, the data direction is determined in the 8th bit (when the 8th bit is "0", data is written from the master, and data is read from the master when "1") and communication is performed in byte units thereafter. At this time, acknowledgment is required for each byte.
The reception operation supports auto-increment transfer and random access transfer, and the transmission operation supports auto-increment operation. Use the I^2C access mode selection(I^2CSEL) register to set auto-increment transfer and random access transfer. The flow of write operation and read operation is shown below.

◆ One-time input mode

・Write operation (auto-increment transfer)

S	SA[6:0]	W	A	RA[7:0]	A	WD[7:0]	A	WD[7:0]	A	WD[7:0]	P

・Write operation (random access transfer)

S	SA[6:0]	W	A	RA[7:0]	A	WD[7:0]	A	RA[7:0]	A	WD[7:0]	P

・Read operation (auto-increment transfer)

S	SA[6:0]	W	A	RA[7:0]	A	Sr	SA[6:0]	R	A	RD1[7:0]	A	RD2[7:0]	~A	P

Dummy Write — Current address read

S: Start condition
SA[6:0]: Slave address
W: Read/Write flag Write="0"
A: Acknowledge
RA[7:0]: Register address in this LSI
WD[7:0]: Write data
P: Stop condition

Sr: Restart condition
R: Read/Write flag Read="1"
RD1,2[7:0]: Read data
~A: Not-Acknowledge
P: Stop condition

From master to slave

From slave to master

◆ Two-times input mode

・Write operation (random access transfer)

S	SA[6:0]	W	A	RA[7:0]	A	RA[7:0]	A	WD1[7:0]	A	WD1[7:0]	P

・Read operation (auto-increment transfer)

S	SA[6:0]	W	A	RA[7:0]	A	RA[7:0]	A	Sr	SA[6:0]	R	A	RD1[7:0]	A	RD1[7:0]	~A	P

Dummy Write　　Current address read

S: Start condition
SA[6:0]: Slave address
W: Read/Write flag　Write="0"
A: Acknowledge
RA[7:0]: Register address in this LSI
WD[7:0]: Write data
P: Stop condition

Sr: Restart condition
R: Read/Write flag　Read="1"
RD1[7:0]: Read data
~A: Not-Acknowledge
P: Stop condition

From master to slave

From slave to master

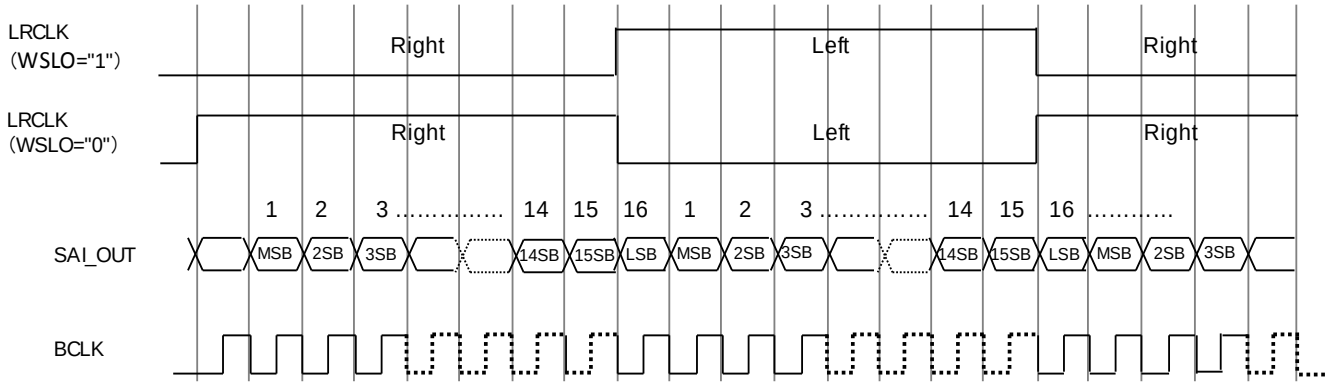
The slave address can be set as follows using the SAD1 to SAD0 pin.

Highest	SAD1	SAD0	Lower 4 bits	Slave address
1	0	0	0101	100_0101
1	0	1	0101	101_0101
1	1	0	0101	110_0101
1	1	1	0101	111_0101

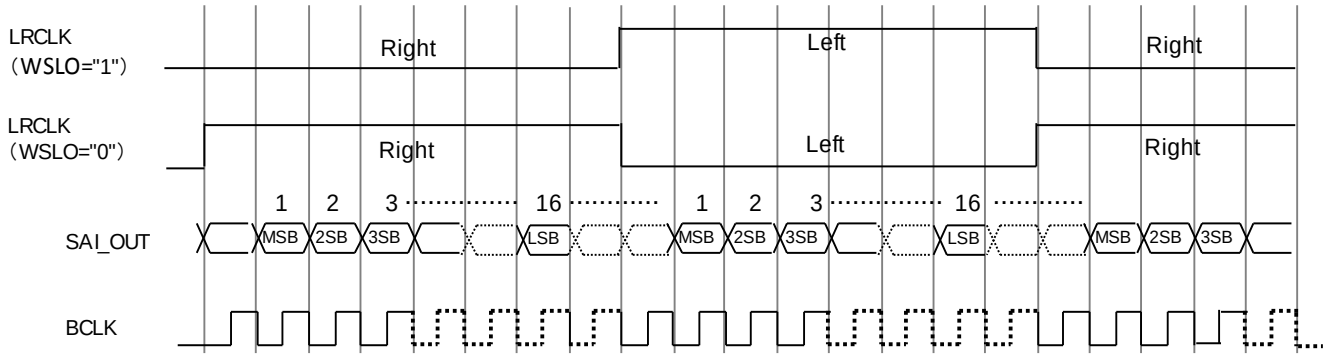
● SAI (Serial Audio Interface)

Various serial data formats are supported by a combination of register settings.
A WSLO, DLYO and FMTO are used to represent the supported formats.
For WSLO, DLYO and FMTO, refer to the " SAITCON register" in the "Registers" chapter.

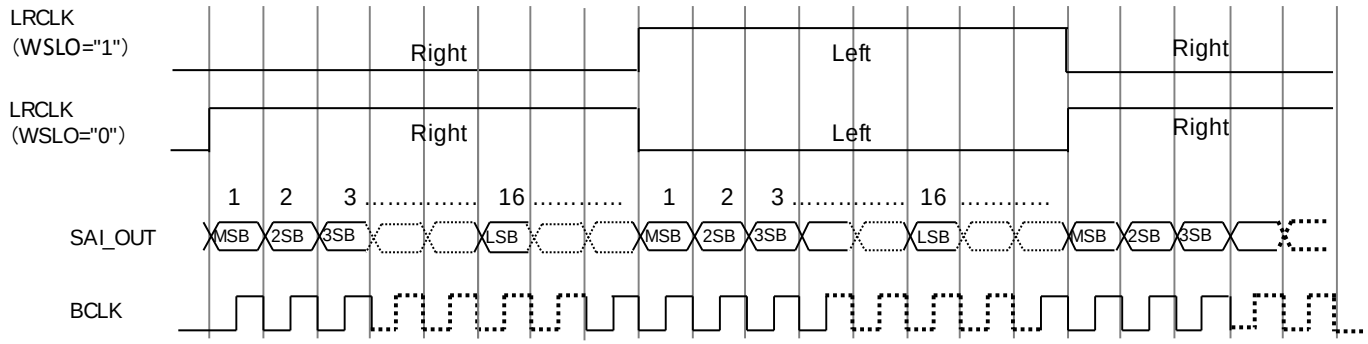
<DLYO="0", FMTO="0", ISSCKO="0">



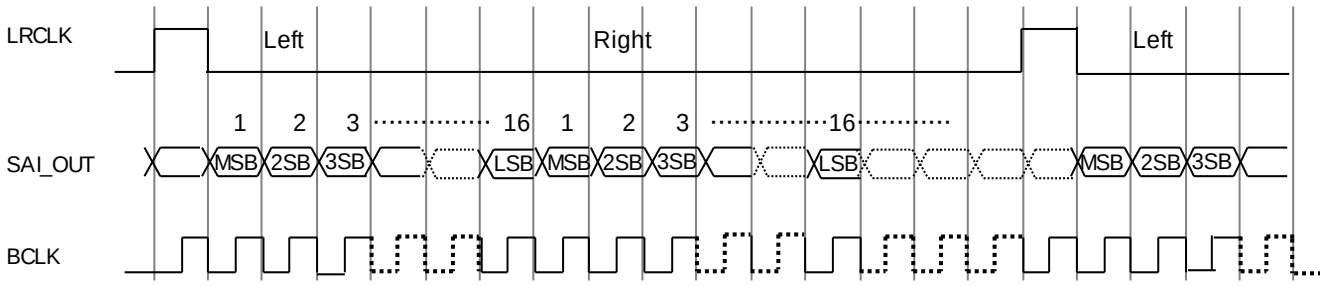
<DLYO="0", FMTO="0", ISSCKO="1">



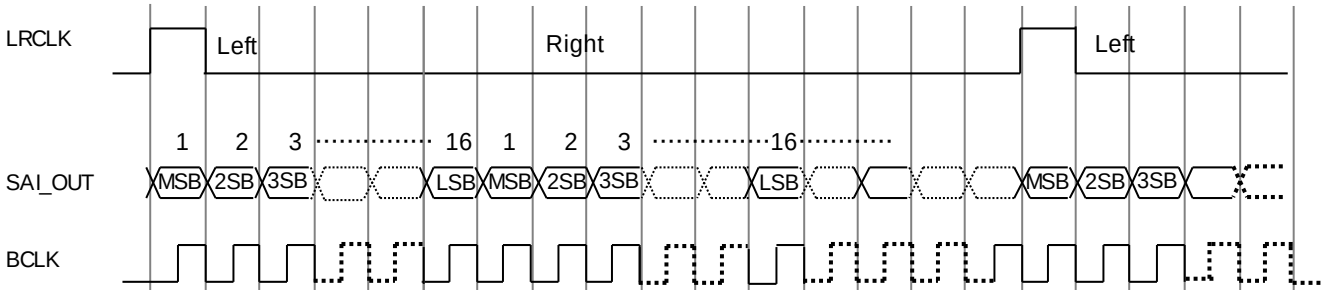
<DLYO="1", FMTO="0", ISSCKO="1">



<DLYO="0", FMTO="1", ISSCKO="1">
In frame synchronous transfer mode, Rch data follows immediately after Lch data.

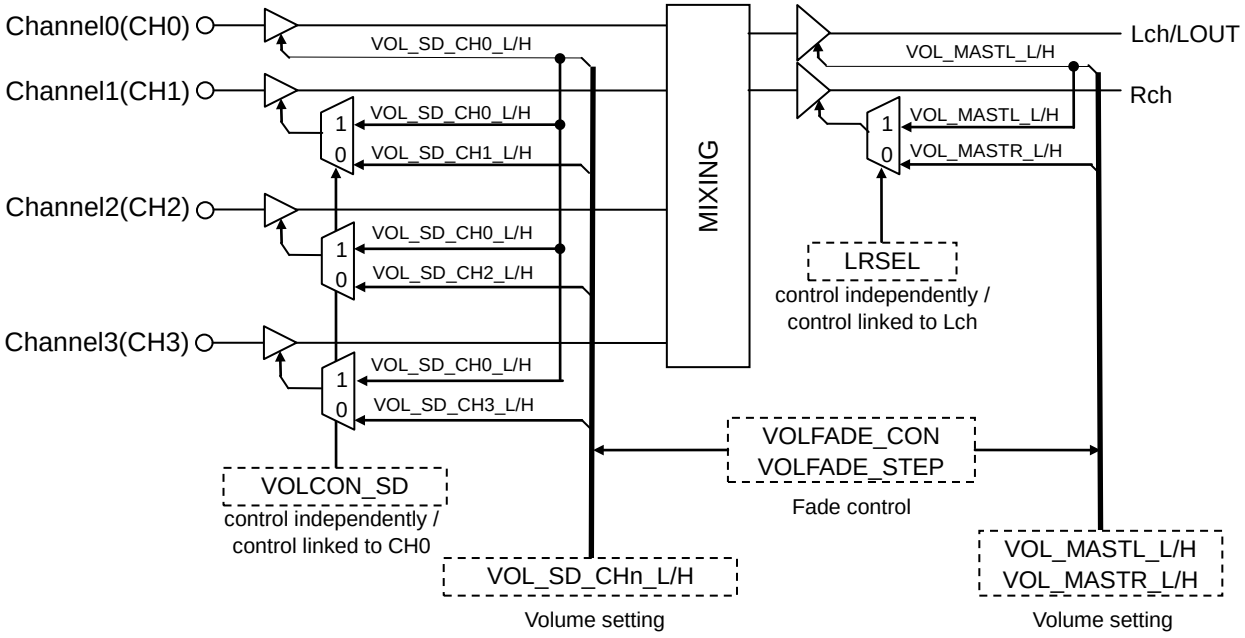


<DLYO="1", FMTO="1", ISSCKO="1">
In frame synchronous transfer mode, Rch data follows immediately after Lch data.



● Volume settings

For the SoundGenerator volume, set volume control independently / volume control linked to CH0 (initial value: volume control independently) of each channel by the VOLCON_SD register. Set the volume of each channel by the VOL_SD_CHn_L/H(n = 0 to 3) registers.
For the volume after mixing, set volume control independently / volume control linked to Lch (initial value: volume control independently) by the LRSEL register. The volume after mixing can be set by the VOL_MASTL_L/H register and VOL_MASTR_L/H register.



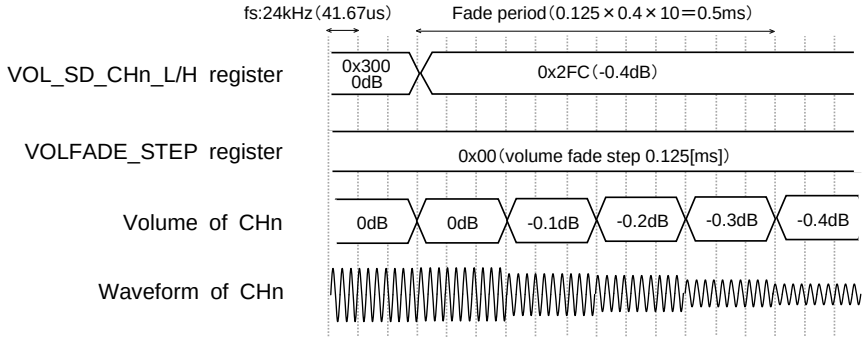
The combination of volume control for each channel is as follows.
—: Apply VOL_SD_CHn_L / H (volume control independently)
レ: Apply VOL_SD_CH0_L / H (volume control linked to CH0)

VOLCON_SD register VOLEN_SD_ CHn bit(n=1 to 3)	Volume control		
	CH3	CH2	CH1
000(Initial value)	—	—	—
001	—	—	レ
010	—	レ	—
011	—	レ	レ
100	レ	—	—
101	レ	—	レ
110	レ	レ	—
111	レ	レ	レ

Furthermore, by enabling fade when changing the volume in the VOLFADE_CON register, the volume transition time can be adjusted in the fade step set in the VOLFADE_STEP register. The volume changes every 0.1 dB.
Volume fade is effective when changing the volume of each channel using the VOL_SD_CHn_L/H(n = 0 to 3) registers, or when changing the VOL_MASTL_L/H register and VOL_MASTR_L/H register.

＜When changing the volume of each channel in the VOL_SD_CHn_L/H(n = 0 to 3) registers＞

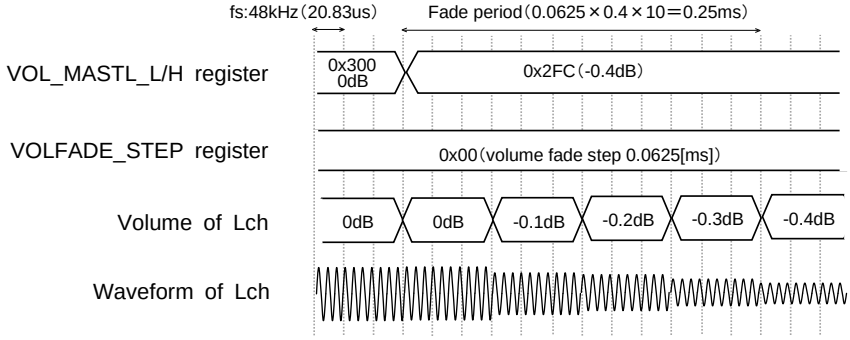
・When playing sound code data of fs = 24kHz



The volume transitions according to the sampling frequency (fs). If sound code data of different fs is being played at the same time, the volume transition time will be different. For the volume transition time, refer "VOLFADE_STEP register" in the "Registers" chapter.

＜When changing the volume by the VOL_MASTL_L/H register and VOL_MASTR_L/H register＞

・GFS bit = 0 (OUTMODE register).



The volume transitions at 48kHz or 32kHz depending on the GFS bit of the OUTMODE register. For the volume transition time, refer "VOLFADE_STEP register" in the "Registers" chapter.

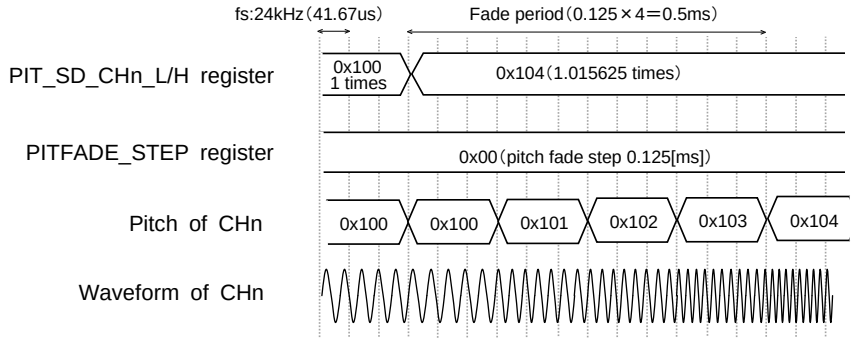
● Pitch settings

SoundGenerator can play while changing the pitch (playback speed).
The pitch magnification of CH 0 to 1 can be set from 0.0625 times to 3.9960938 times in 0.00390625 times steps.
The pitch magnification of CH 2 to 3 can be set from 0.0625 times to 1 time in 0.00390625 times steps.
For the pitch of the SoundGenerator, set pitch control independently / pitch control linked to CH0 (initial value:pitch control independently) by the PITCHCON_SD register.

The combinations of pitch for each channel are as follows.
—: Apply PIT_SD_CH1_L / H (pitch control independently)
レ: Apply PIT_SD_CH0_L / H (pitch control linked to CH0)

PITCHCON_SD register	Pitch control
PITCHEN_SD_CH1 bit	CH1
0	—
1	レ

Furthermore, by enabling fade when changing the pitch in the PITFADE_CON register, the pitch can be adjusted step by step in the pitch step set in the PITFADE_STEP register.

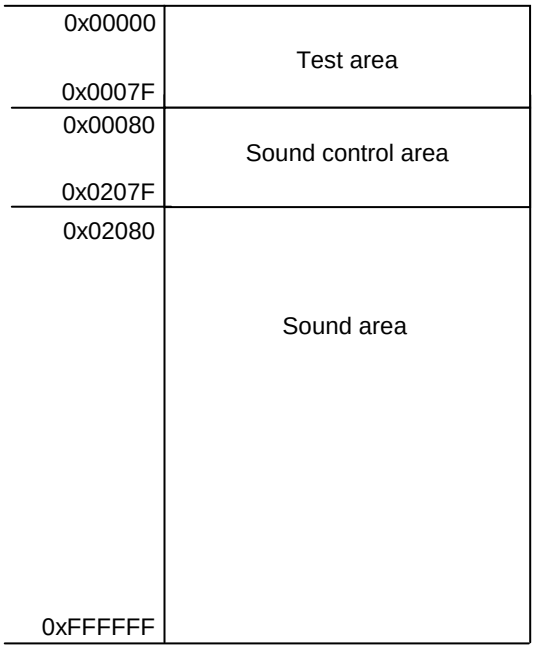


● Memory allocation and creating sound data

The sound code data stored in the serial flash memory consists of sound (i.e., phrase) control area, test area, and sound area. The sound control area manages the sound data in the Memory. It contains data for controlling sound data for 64 phrases. The sound area contains actual waveform data.

The Sound data is created using a dedicated tool (Speech LSI Utility).

Configuration of Serial Flash Memory Data (128Mbits)



● Playback time and memory capacity

The playback time depends on memory capacity and sampling frequency. The relationship is shown below.

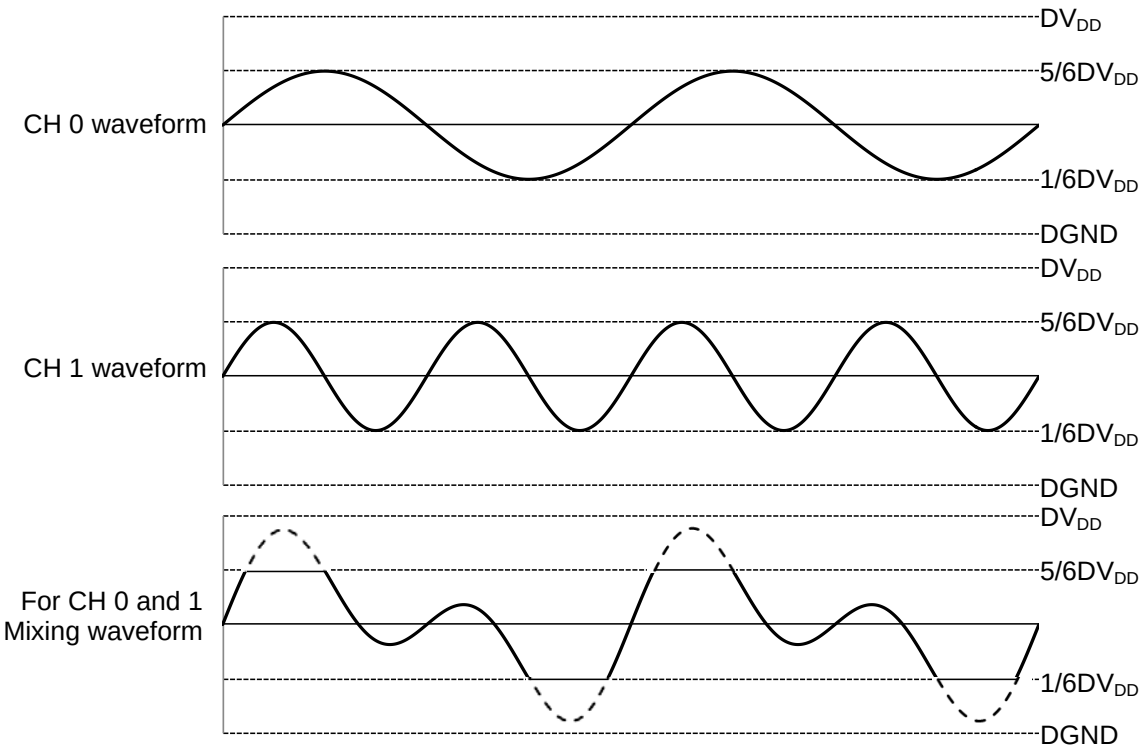
$$\text{Playback Time} = \frac{1.024 \times (\text{Memory Capacity (kbit)}-65)}{\text{Sampling frequency (kHz)} \times \text{bit length}} \quad \text{(sec)}$$

When sound data with a sampling frequency of 48 kHz is registered in the 4Mbit serial flash memory, the playback time will be approximately 5.37 seconds.

$$\text{Playback Time} = \frac{1.024 \times (4096(\text{kbit})- 65)}{48\ (\text{kHz}) \times 16\ (\text{bit})} \fallingdotseq 5.37(\text{sec})$$

● Waveform clamp precautions for mixing

When mixing, the clamp may be generated as shown in the figure below due to the calculation of the synthesis. If the clamp is known to be generated in advance, adjust the volume of each channel with the volume control register.
For details on volume control registers, refer the chapter "Registers".



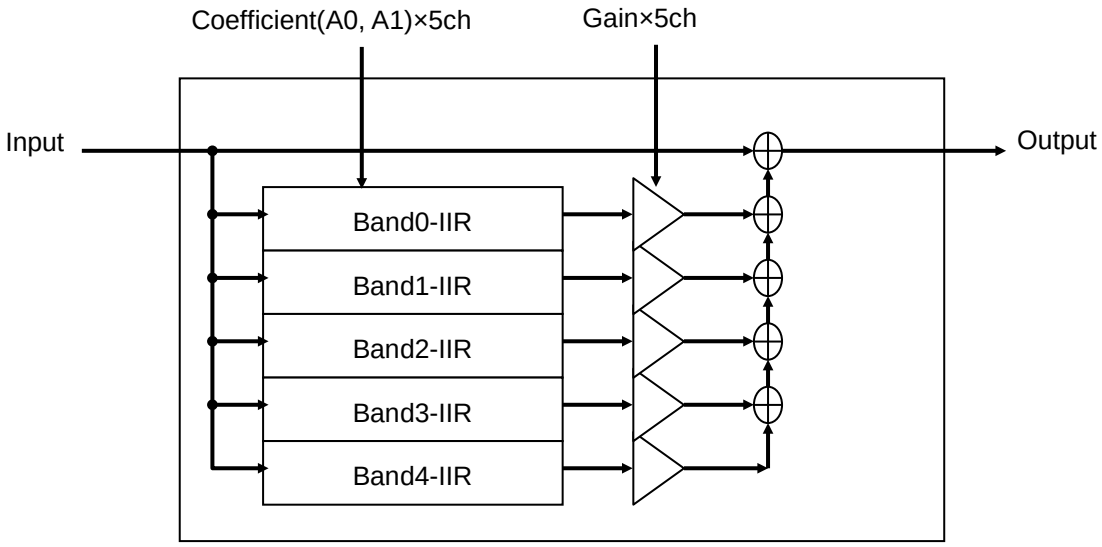
If the result of mixing CH 0 and 1 exceeds from the $1/6DV_{DD}$ to $5/6DV_{DD}$ level (as indicated by the broken line), the sound quality may be reduced by clamping.

● 5Band equalizer

The 5Band equalizer consists of a second-order IIR type Band Pass Filter. It is equipped with Lch (EQL) and Rch (EQR). The center frequency and band width of each band can be set arbitrarily. ON / OFF can be set by setting the EQLCON register and EQRCON register. The settings are as follows.

$A0 = (1-\tan\pi fb / fs) / (1 + \tan\pi fb / fs)$
$A1 = (-2\cos 2\pi f0 / fs) / (1 + \tan\pi fb / fs)$

f0: Center frequency of the band [Hz]
fb: -3dB bandwidth [Hz]
fs: sampling frequency [Hz]



For the actual register value, multiply the result of the above formula by 2^{14} and use the integer value rounded to the nearest whole number.
For details on Coefficient (A0, A1) and Gain, refer "Equalizer related registers" in the "Registers" chapter.
The equalizer can be adjusted using the dedicated tool (Speech LSI Utility). Set the value generated by the Speech LSI Utility in the "Equalizer related registers".

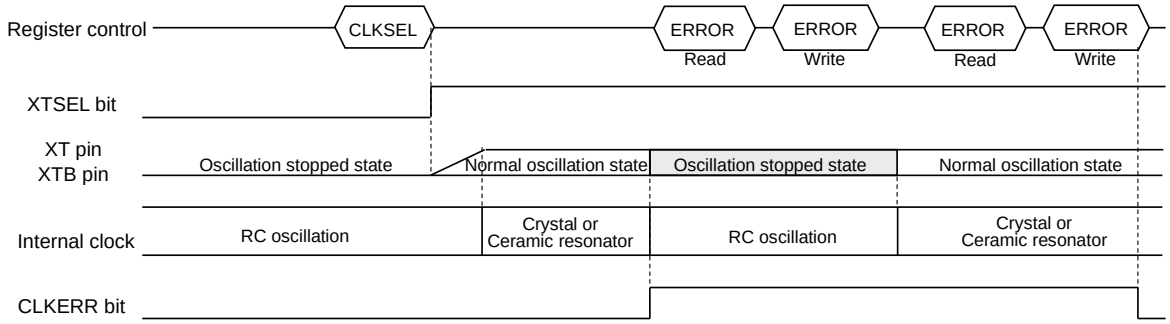
● Error detection function

It has a built-in error detection function, and the presence or absence of error detection can be read from the ERROR register. The presence or absence of error detection can be output to the STATUS0 pin (set by the OUTSTAT0_0 to 5 registers), the STATUS1_MCLKO pin (set by the OUTSTAT1_0 to 5 registers), and the STATUS2 pin (set by the OUTSTAT2 register). For details on the ERROR register, OUTSTAT0_0 to 5 registers, OUTSTAT1_0 to 5 registers, OUTSTAT2 register, refer the chapter "Registers".

The error detection is shown below.

◆ Detects the stop of clock input from a crystal resonator or ceramic resonator.

When oscillation stop is detected with the XTSEL bit of the CLKSEL register set to “1”, the CLKERR bit becomes “1”. At the same time, the clock backup function starts and automatically switches to the RC oscillation circuit (4.096MHz). The CLKERR bit can be read from the ERROR register. The CLKERR bit can be cleared by writing to the ERROR register. However, if the oscillation stop continues, the CLKERR bit continues to be “1”.

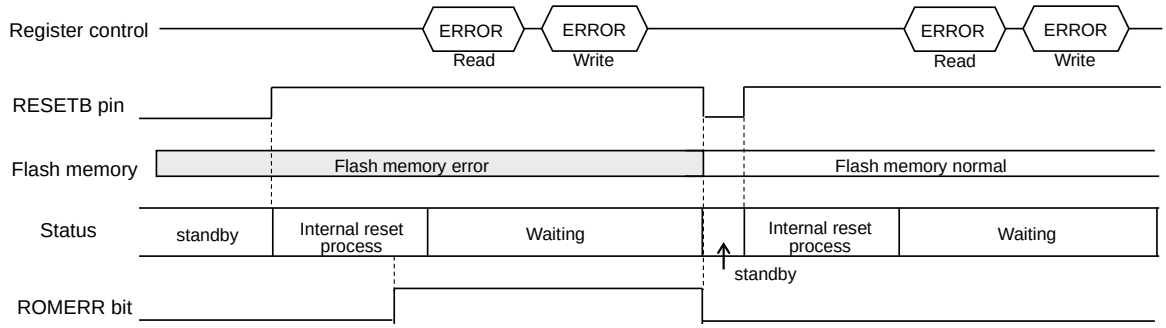


For details on the ERROR register and CLKSEL register, refer the chapter "Registers".

◆ Flash memory error detection

When the RESETB pin is set to the “L” → “H” level, the flash memory is read during the internal reset process. If an error is detected in the read data of the flash memory, the ROMERR bit becomes "1". In this case, initialize this LSI by resetting with the RESETB pin.

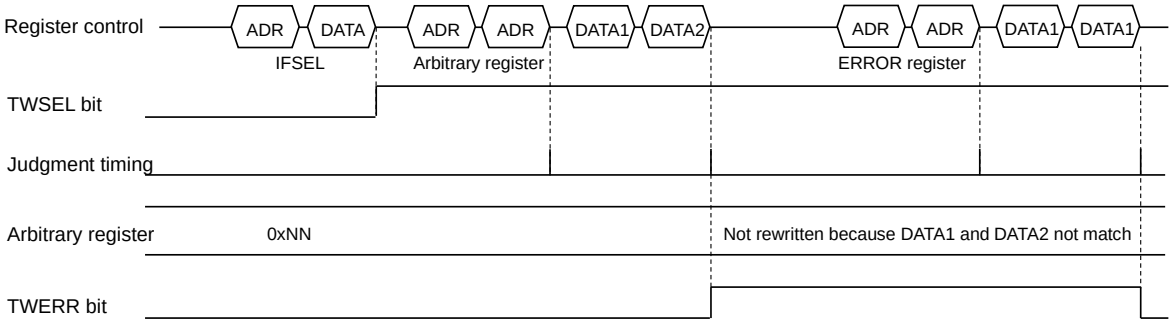
The ROMERR bit can be read from the ERROR register. The ROMERR bit is not cleared even if writing to the ERROR register.



For details on the ERROR register, refer the chapter "Registers".

◆ Two-times input error detection

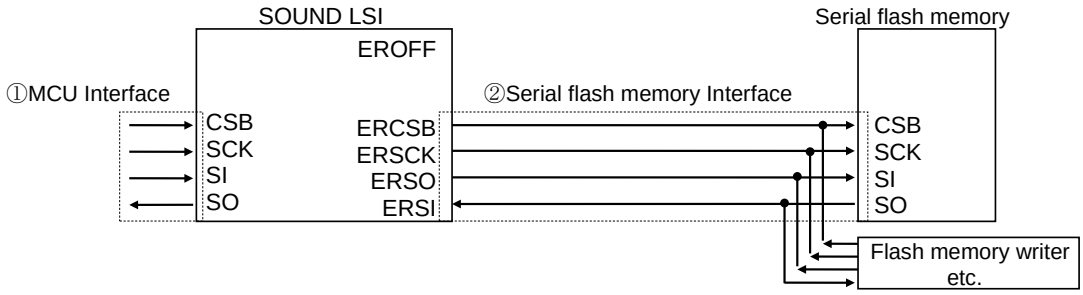
In order to prevent malfunction due to noise of the serial interface pin, it is equipped with a function to input address and data twice each. Setting the TWSEL bit of the IFSEL register to “1” shifts to the two-times input mode.
In the two-times input mode, the address and data is input two-times in succession, and it is valid only when the input data matches. If a mismatch occurs during the second data input after the first data input, the TWERR bit is set to "1", and the address or data entered is ignored.
The TWERR bit can be read from the ERROR register. The TWERR bit can be cleared by writing to the ERROR register.



For details on the ERROR register and IFSEL register, refer the chapter "Registers".

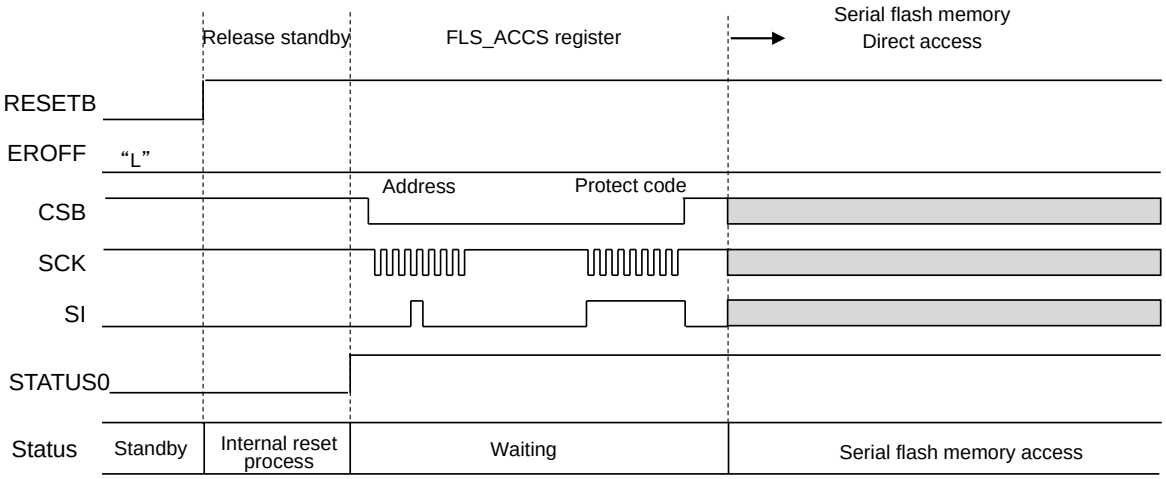
● Serial flash memory rewrite function

The serial flash memory can be rewritten in the following two ways.



① Rewrite using the clock synchronous serial interface of the MCU interface

By using the CSB, SCK, SI and SO pins, which are clock synchronous serial interfaces of the MCU interface the serial flash memory can be rewritten. When the protect code written in the FLS_ACCS register matches the information stored in the flash memory, direct access to the serial flash memory is enabled from the CSB, SCK, SI and SO pins.

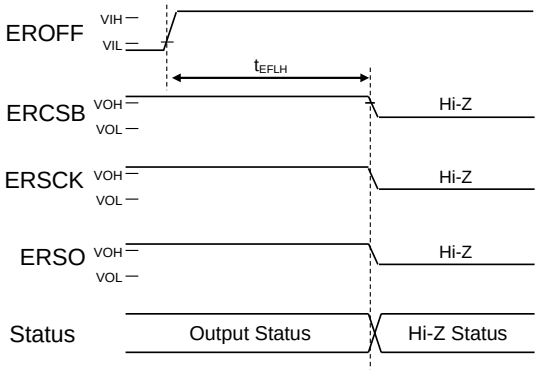


For details on the FLS_ACCS register, refer the chapter "Registers".

② Rewrite using serial flash memory interface without this LSI

The serial flash memory can be rewritten using the ERCSB, ERSCK, ERSI and ERSO pins that is the serial flash memory interface.

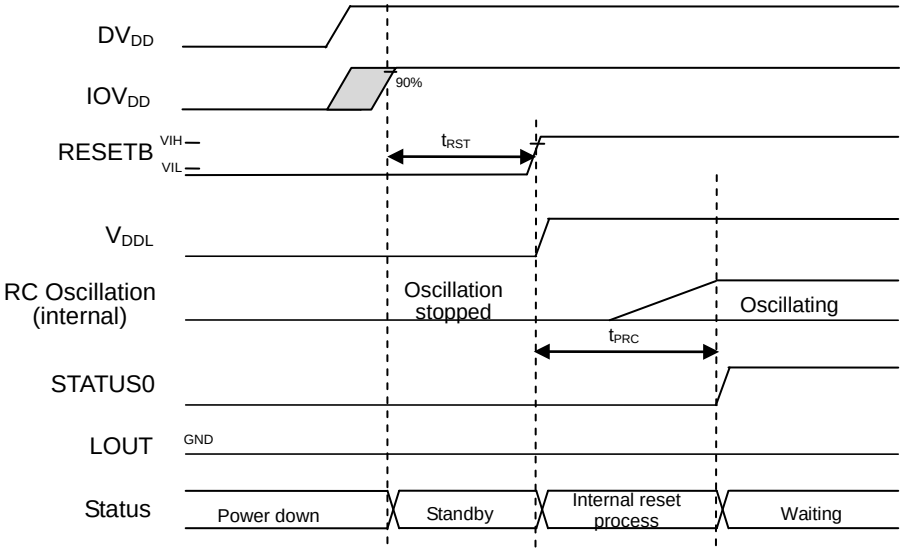
When the EROFF pin set to "H", the serial flash memory can be rewritten using the ERCSB, ERSCK, ERSI and ERSO pins without this LSI. (ERCSB, ERSCK and ERSO pins are in a condition of high-impedance.)



■ Timing chart

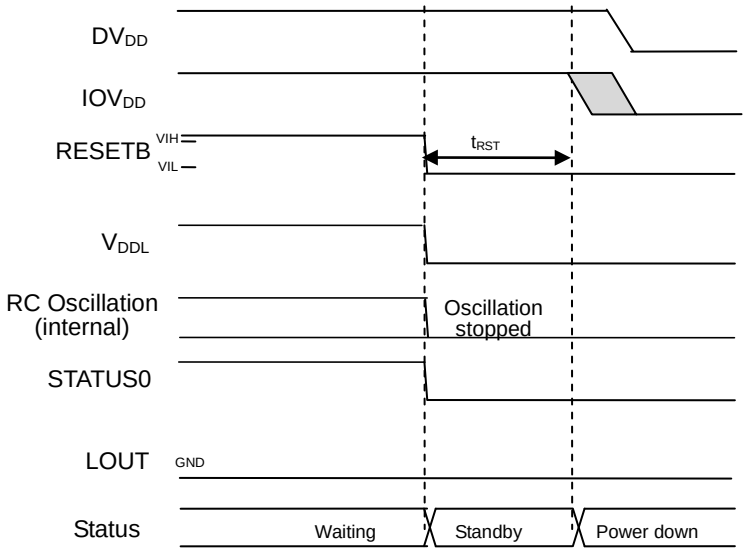
● Common

◆ Power-on timing



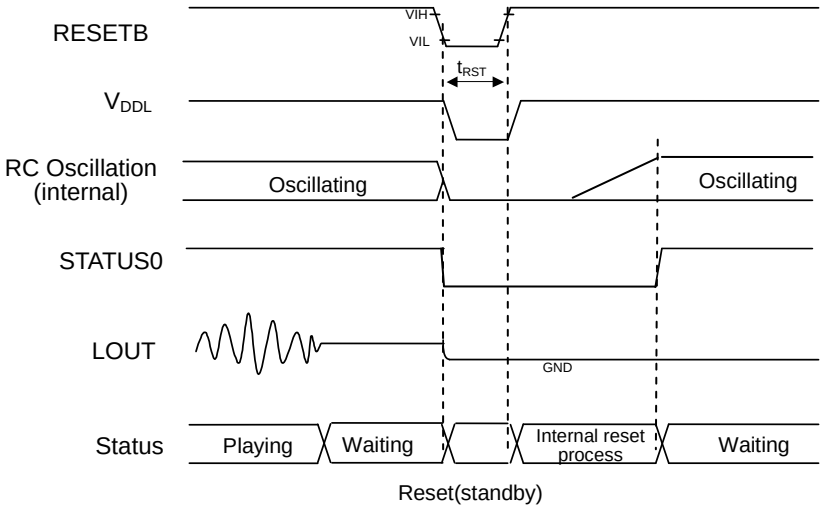
When turning on the power, enter "L" in the RESETB pin.
While the RESETB pin is at L level, it is in standby mode.
Start up in the order of DV_{DD} and IOV_{DD}.The DV_{DD} and IOV_{DD} can also start up at the same time.
After the reset is released (RESETB is at L → H level), it goes through internal reset processing and becomes waiting status (oscillating).
Access the register after t_{PRC} has elapsed or after the STATUS0 pin has become “H”.
Be sure to enter "L" at the RESETB pin when the DV_{DD} is below the (recommended) operating voltage range.

◆ Power-off timing

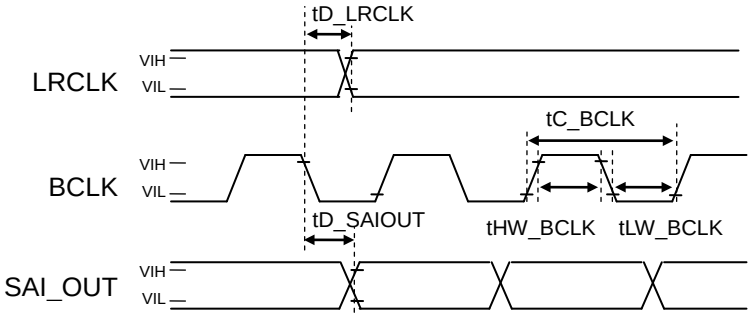


When turning off the power, enter "L" in the RESETB pin.
Shut down in the order of IOV_{DD} and DV_{DD}. The DV_{DD} and IOV_{DD} can also shut down at the same time.
Be sure to enter "L" at the RESETB pin when the DV_{DD} is below the (recommended) operating voltage range.

◆ Reset input timing

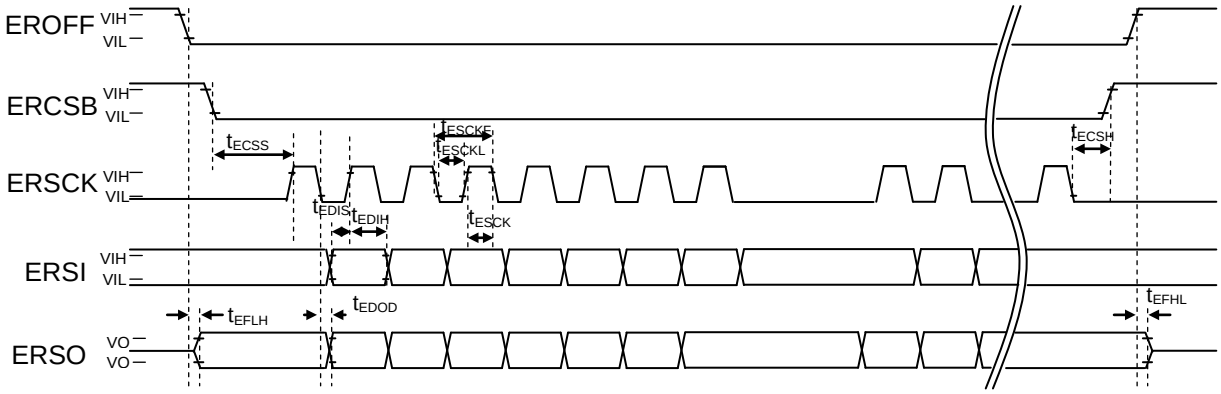


◆ SAI interface timing (master)



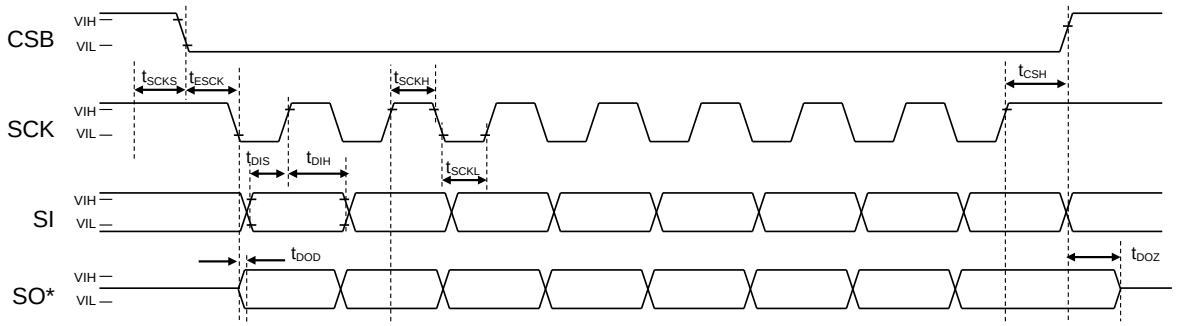
MCLKO is synchronized with BCLK.

◆ Serial flash memory interface timing

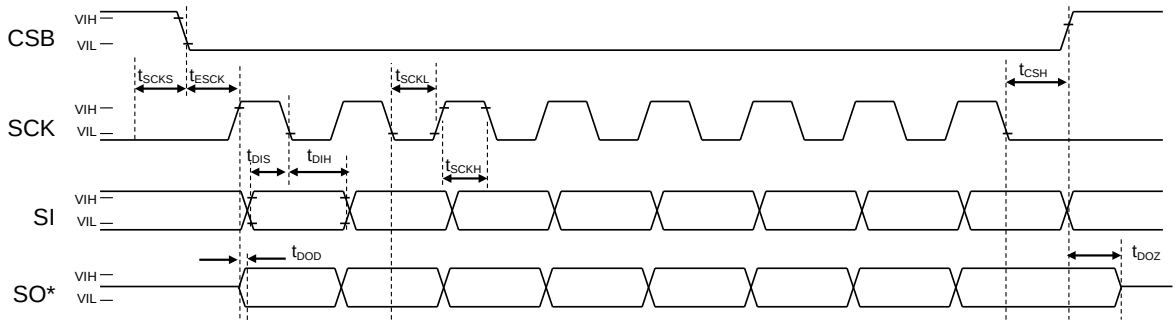


● Clock synchronous serial

◆ Clock Synchronous Serial Interface Timing (SCK Initial Value = "H" Level)

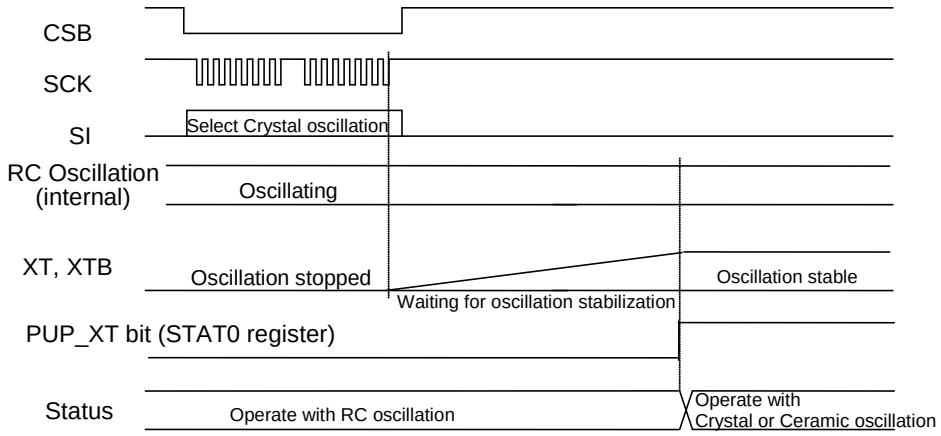


◆ Clock Synchronous Serial Interface Timing (SCK Initial Value = "L" Level)

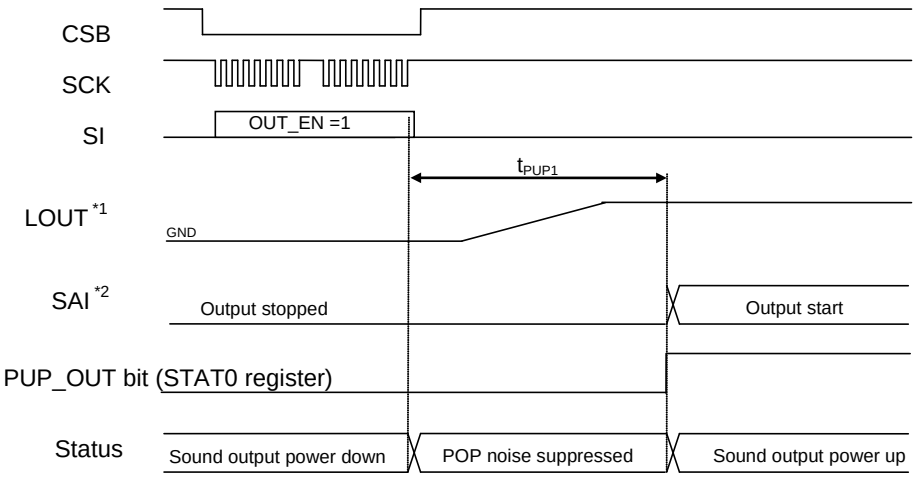


* Outputs "H" or "L" to the SO pin only when reading.
At the time of writing, the SO pin is in a high impedance state.

◆ Crystal oscillation switching timing

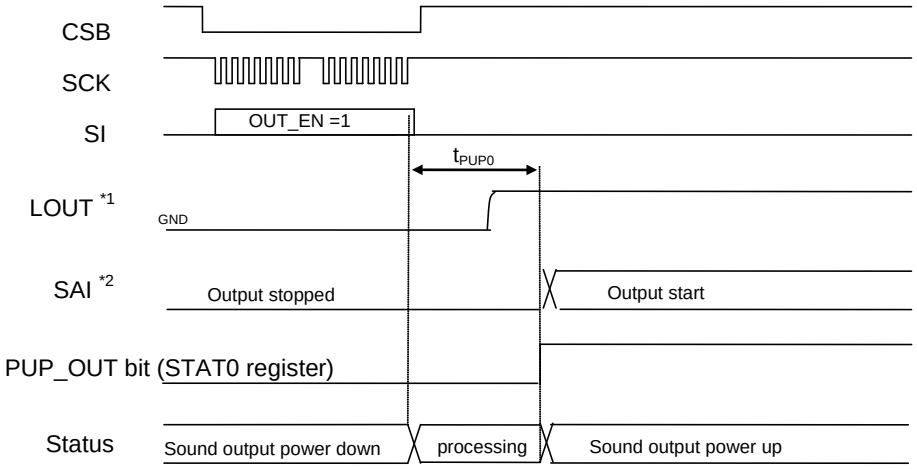


◆ Sound output power-up timing (pop noise countermeasure bit POP =“1”)



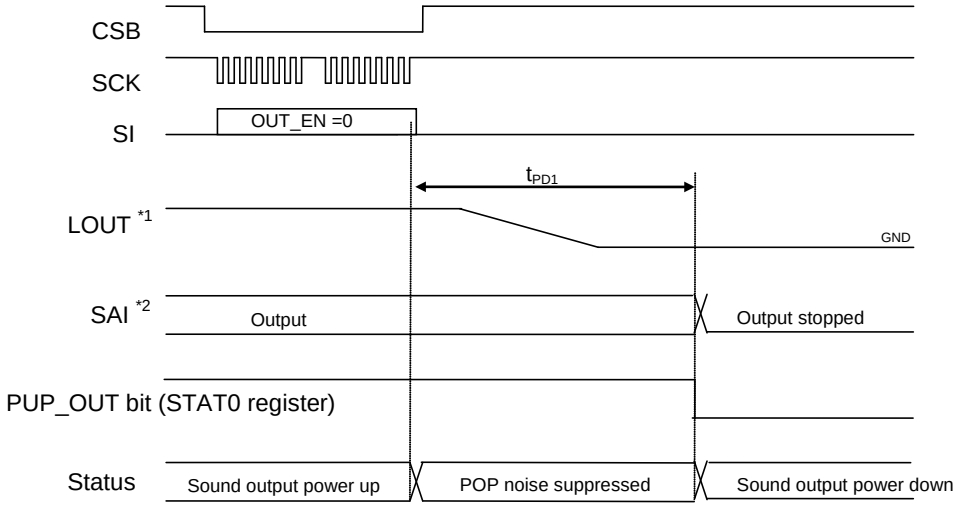
*1 If playback from the LINE amplifier is not selected in OUT_MD [1: 0] of the OUTMODE register, it is fixed to GND.
*2 If playback from the SAI pin is not selected in OUT_MD [1: 0] of the OUTMODE register, not output to the SAI pin (BCLK / LRCLK / SAI_OUT / STATUS1_MCLKO).

◆ Sound output power-up timing (pop noise countermeasure bit POP =“0”)



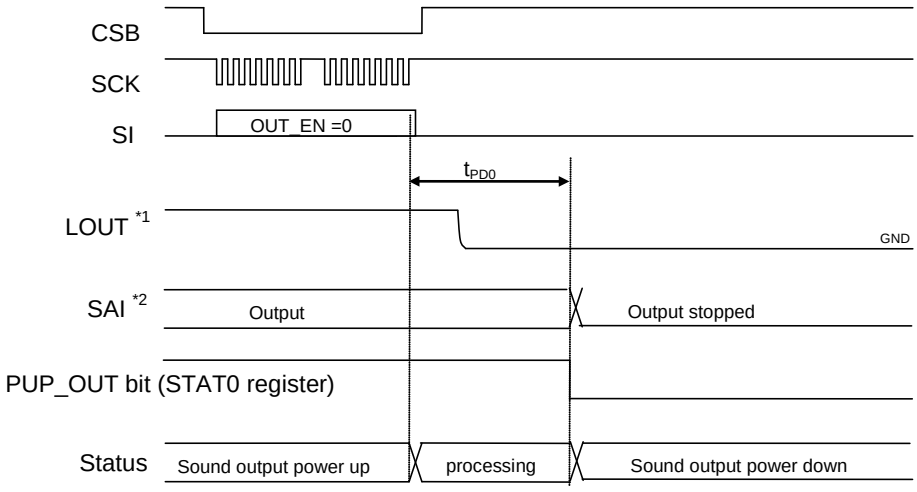
*1 If playback from the LINE amplifier is not selected in OUT_MD [1: 0] of the OUTMODE register, it is fixed to GND.
*2 If playback from the SAI pin is not selected in OUT_MD [1: 0] of the OUTMODE register, not output to the SAI pin (BCLK / LRCLK / SAI_OUT / STATUS1_MCLKO).

◆ Sound output power-down timing (pop noise countermeasure bit POP =“1”)



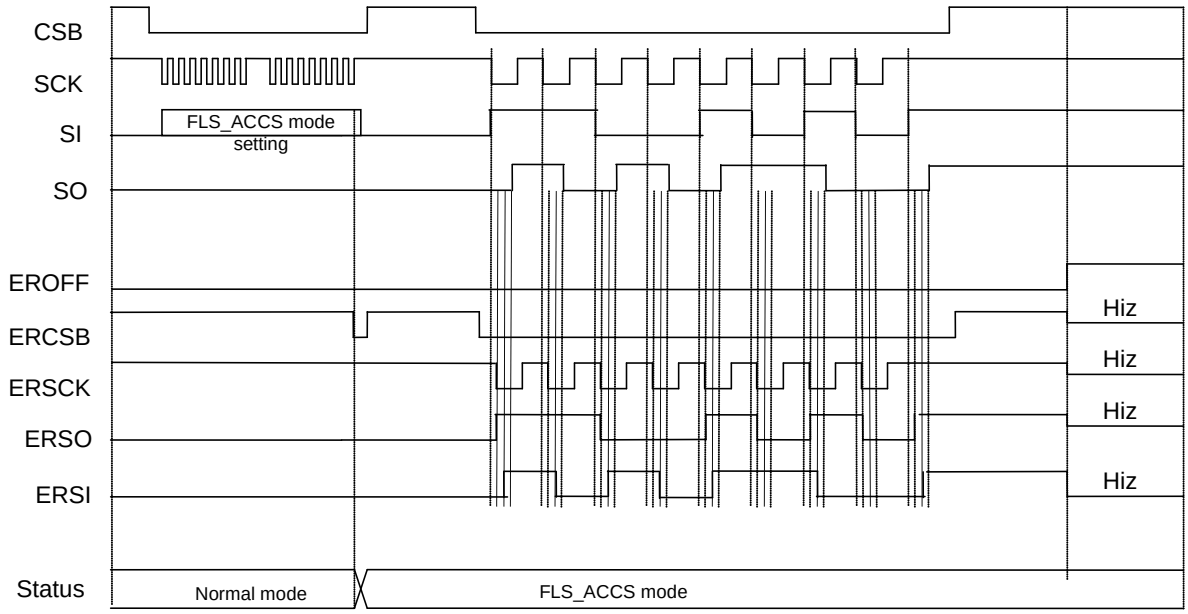
*1 If playback from the LINE amplifier is not selected in OUT_MD [1: 0] of the OUTMODE register, it is fixed to GND.
*2 If playback from the SAI pin is not selected in OUT_MD [1: 0] of the OUTMODE register, not output to the SAI pin (BCLK / LRCLK / SAI_OUT / STATUS1_MCLKO).

◆ Sound output power-down timing (pop noise countermeasure bit POP =“0”)



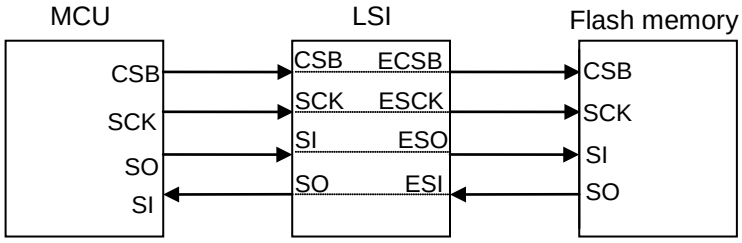
*1 If playback from the LINE amplifier is not selected in OUT_MD [1: 0] of the OUTMODE register, it is fixed to GND.
*2 If playback from the SAI pin is not selected in OUT_MD [1: 0] of the OUTMODE register, not output to the SAI pin (BCLK / LRCLK / SAI_OUT / STATUS1_MCLKO).

◆ Flash memory access flow

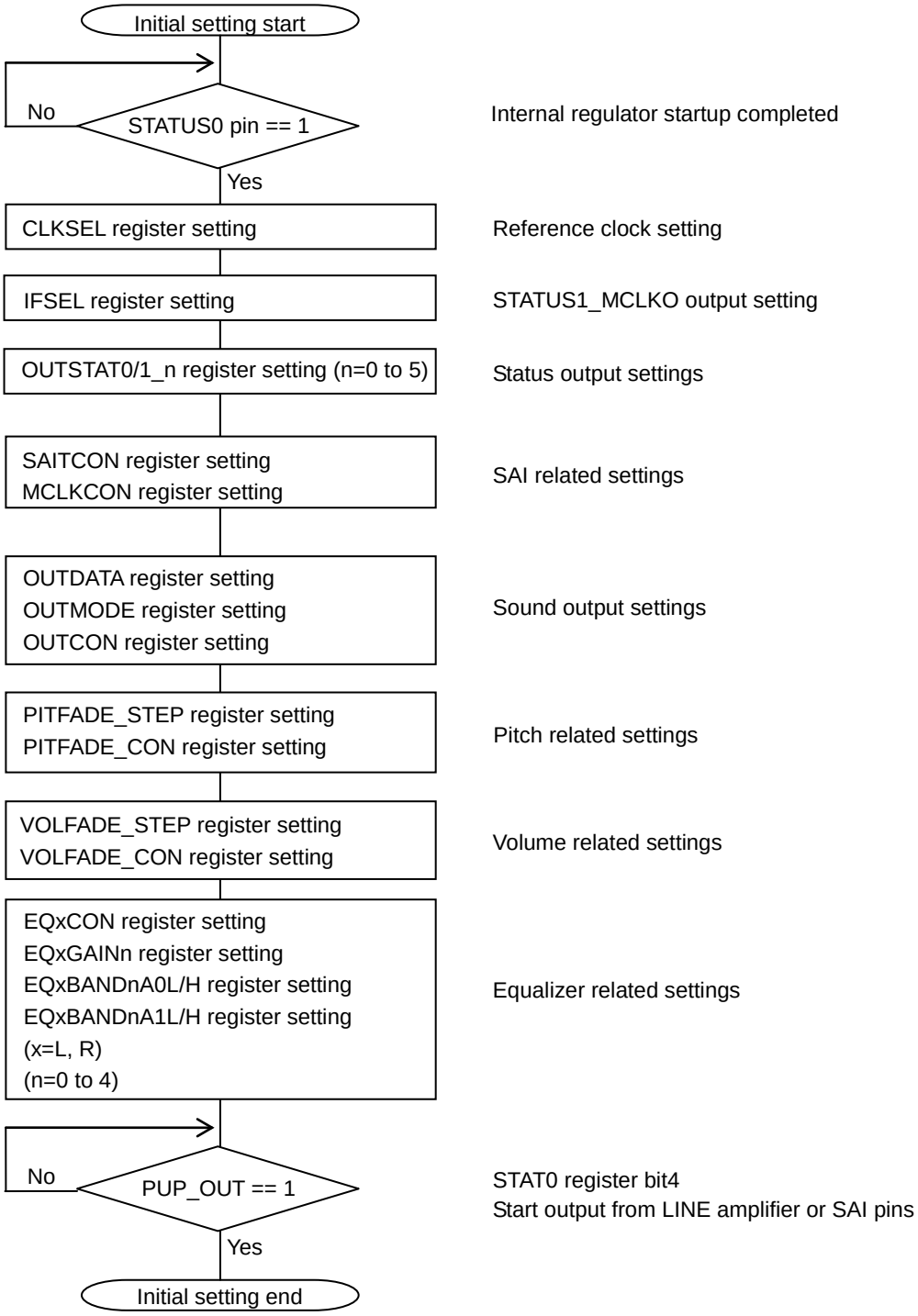


When FLS_ACCS mode is set, the pins are directly connected inside the LSI as shown below. When the EROFF pin is set to H level, the ERCSB, ERSCK, ERSO and ERSI pins are in the HiZ(high-impedance) state.

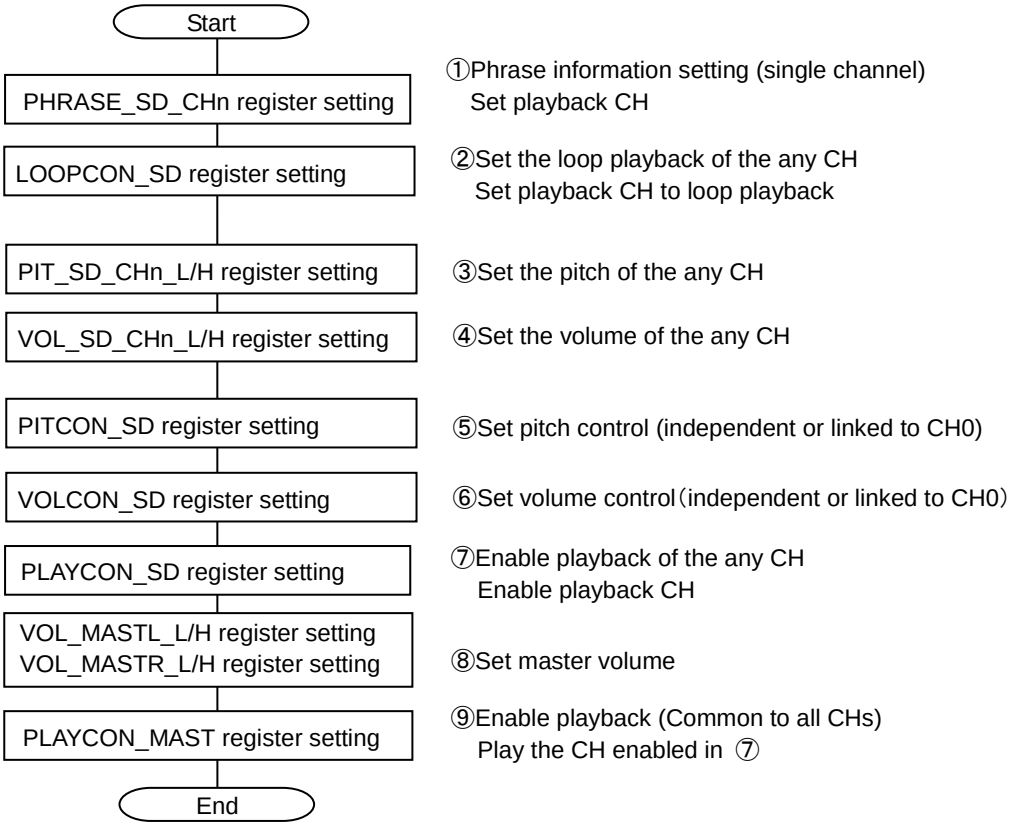
Symbol	I/O	Symbol to be connected	I/O	
			EROFF=L	EROFF=H
CSB	I	ERCSB	O	HiZ
SCK	I	ERSCK	O	HiZ
SI	I	ERSO	O	HiZ
SO	O	ERSI	I (Pull Down)	HiZ

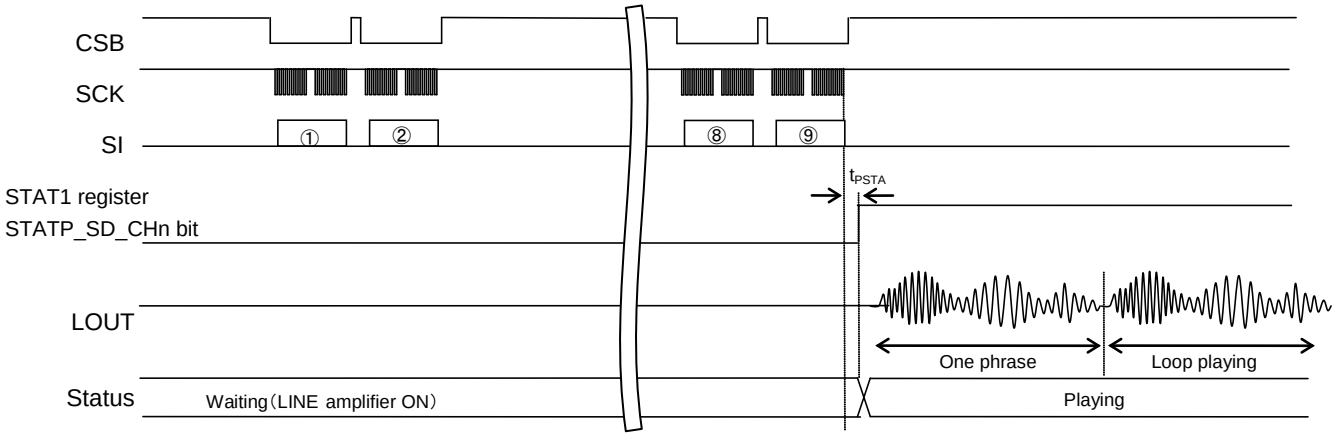


◆ SoundGenerator initial setting flow



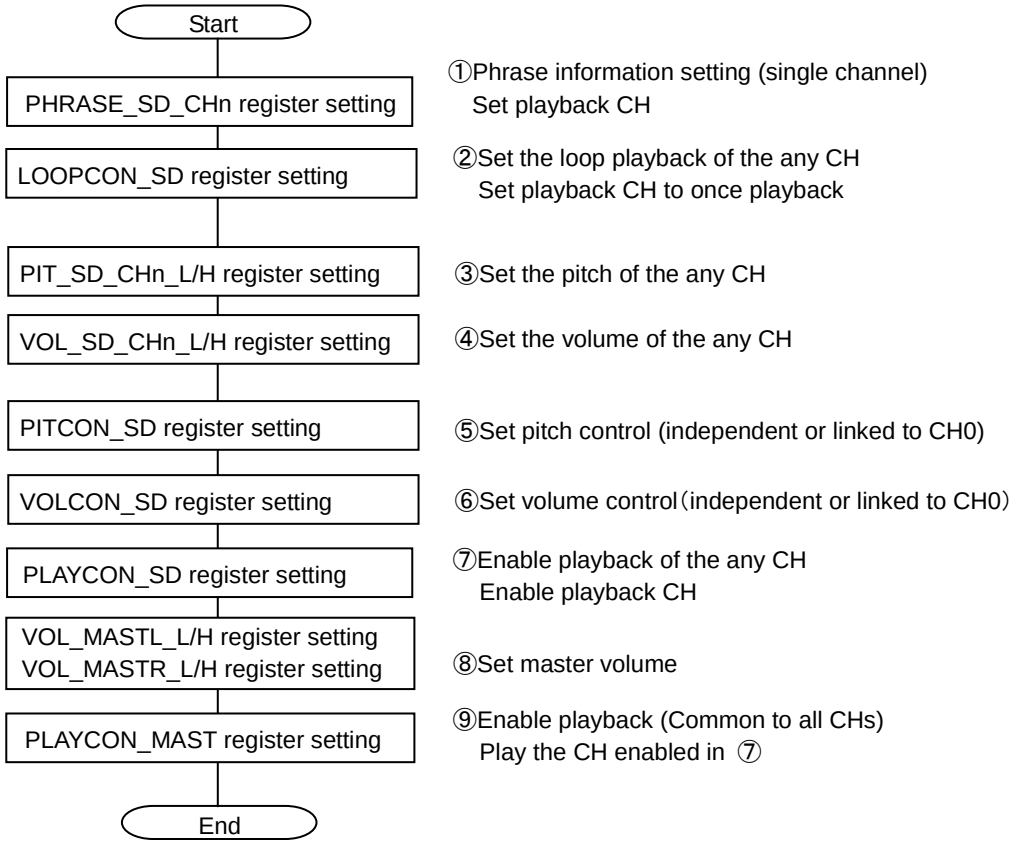
◆ SoundGenerator playback flow (Single channel / with loop)

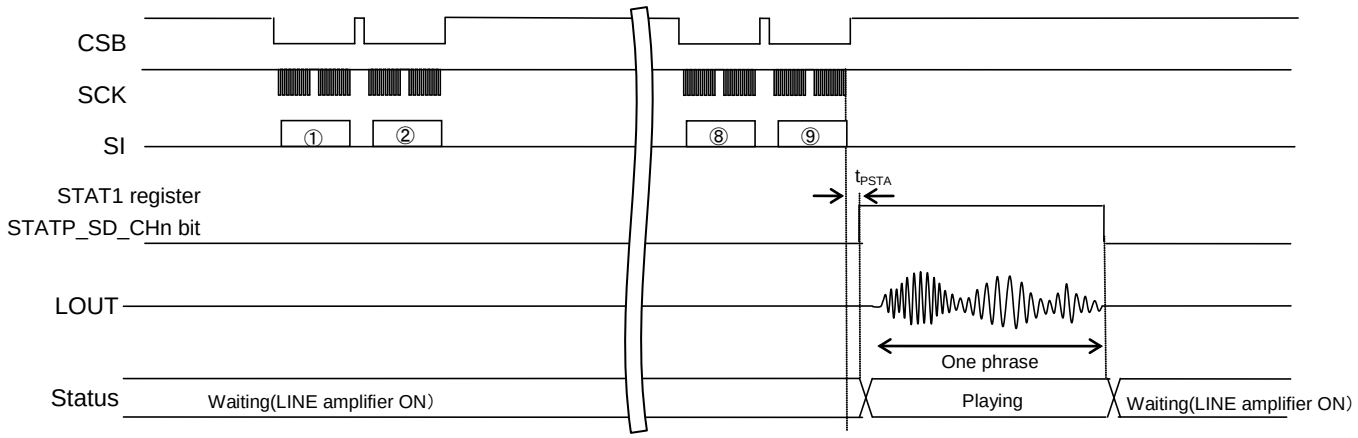




・SoundGenerator can select once playback or loop playback depending on the presence or absence of loop setting. To end loop playback, release the loop setting and wait for the phrase to end before ending playback. If want to end the playback immediately, disable the any CH.
・If phrases with different sampling frequencies are started playing on different channels at the same time, there may be a gap between the channels during a loop depending on the sound code data length.

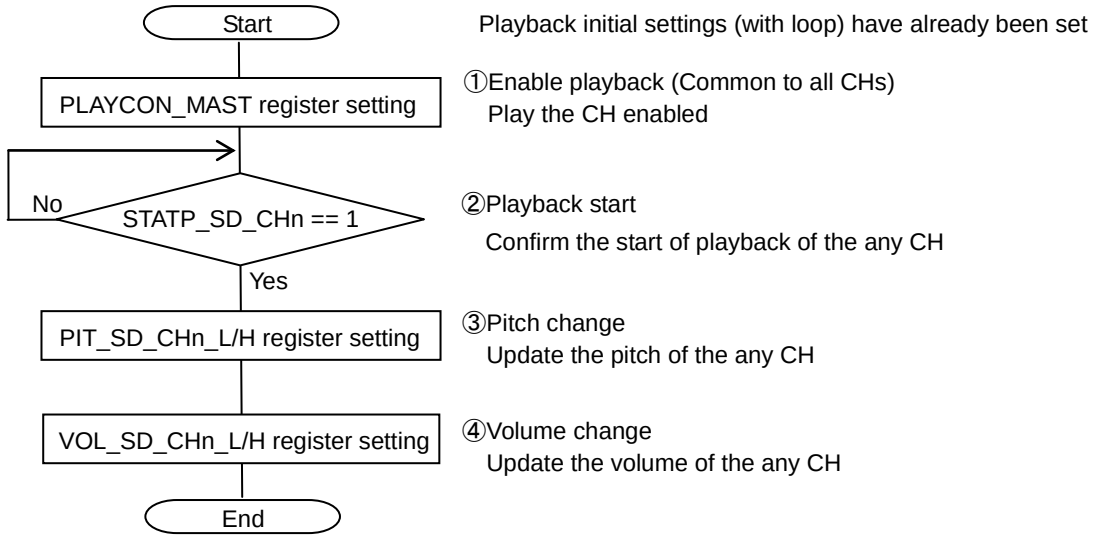
◆ SoundGenerator playback flow (Single channel / without loop)

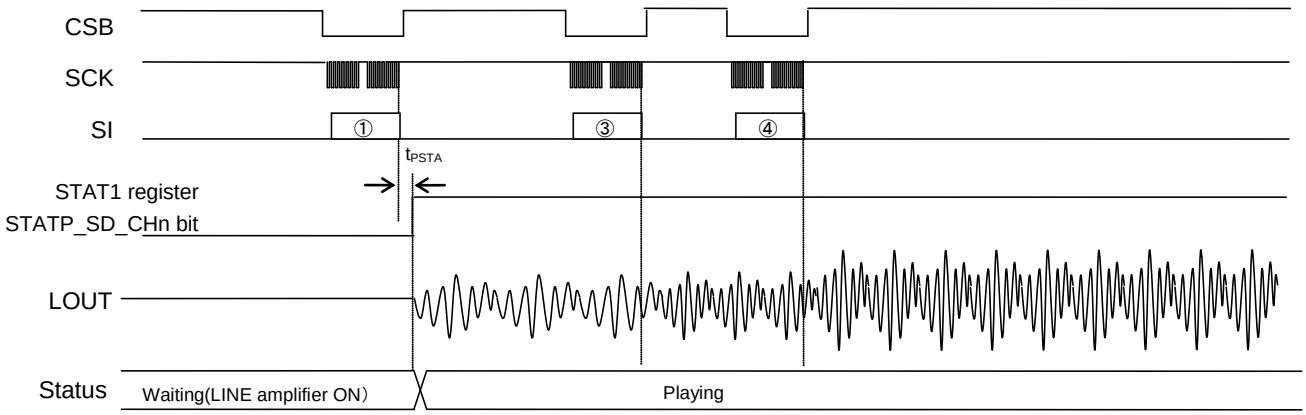




SoundGenerator can select once playback or loop playback depending on the presence or absence of loop setting. When playing once, the playback ends at the same time as the phrase ends.

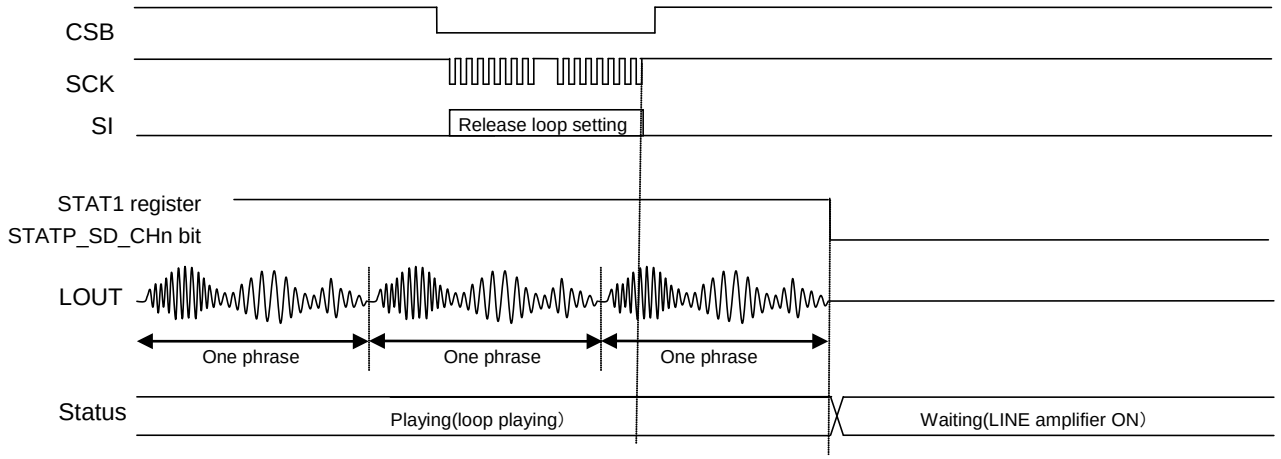
◆ SoundGenerator pitch / volume change flow during playback





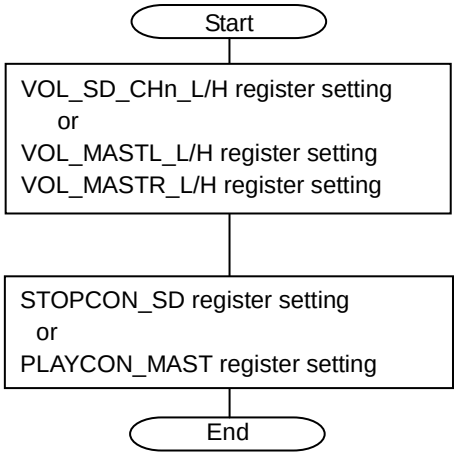
The pitch and volume can be changed during playback.

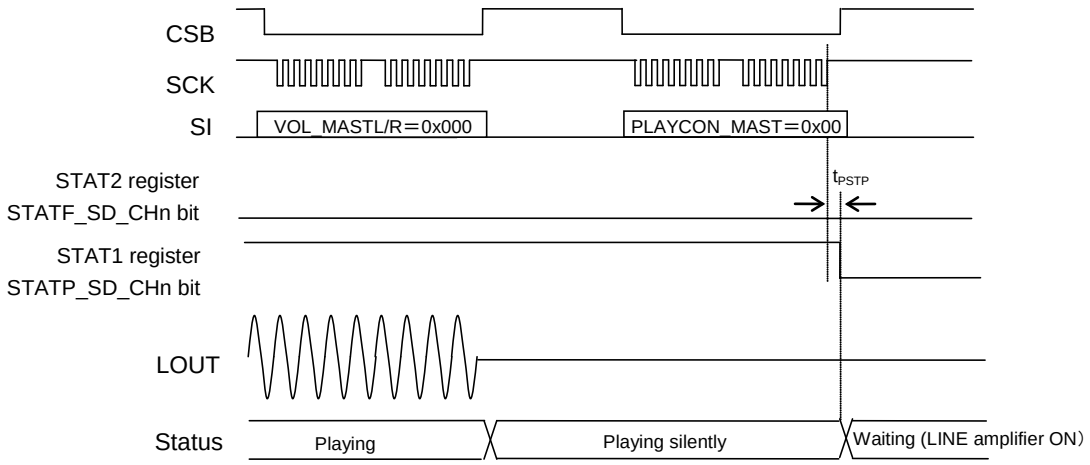
◆ SoundGenerator loop playback release timing



Loop playback is stopped at the end of the phrase.

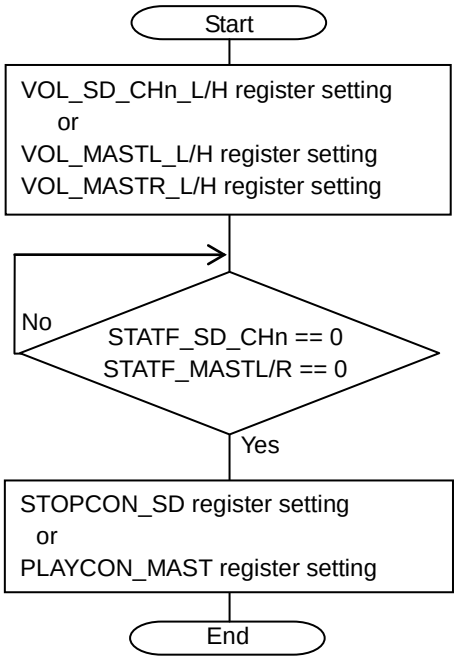
◆ Playback end timing (without fade)





・To stop the playback of multiple channels, set the volume (VOL_SD_CHn) of the any CH to MUTE.
To stop playback of all channels, set the master volume (VOL_MASTL L/H, VOL_MASTR L/H) to MUTE.
・To stop playback when playing a single channel, set the master volume (VOL_MASTL_L/H, VOL_MASTR_L/H) to MUTE.
・To restart playback after stopping playback in the PLAYCON_MAST register, refer to the SoundGenerator playback flow.

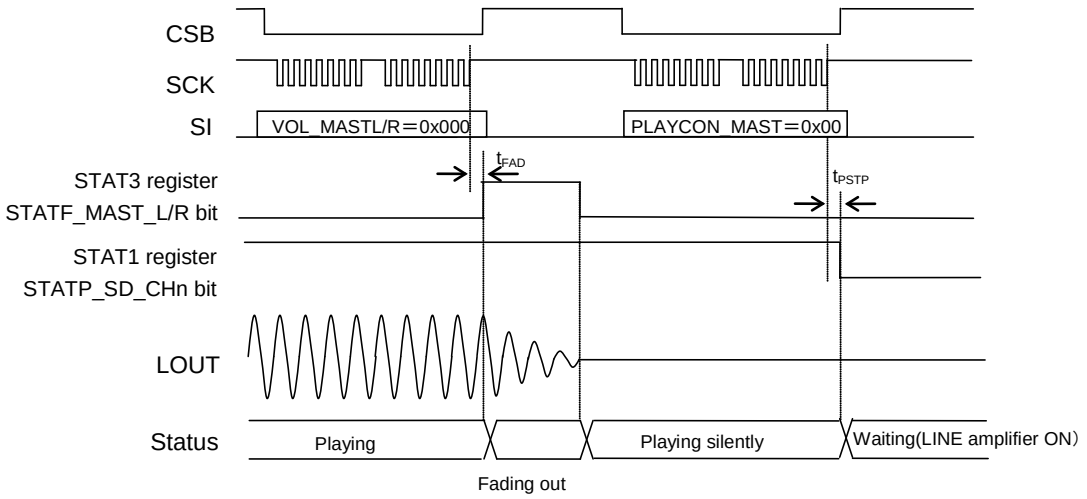
◆ Playback end timing (with fade)



①Set the volume of the any CH or master volume to MUTE.

②Confirm that the fade of the any CH or master volume is completed.

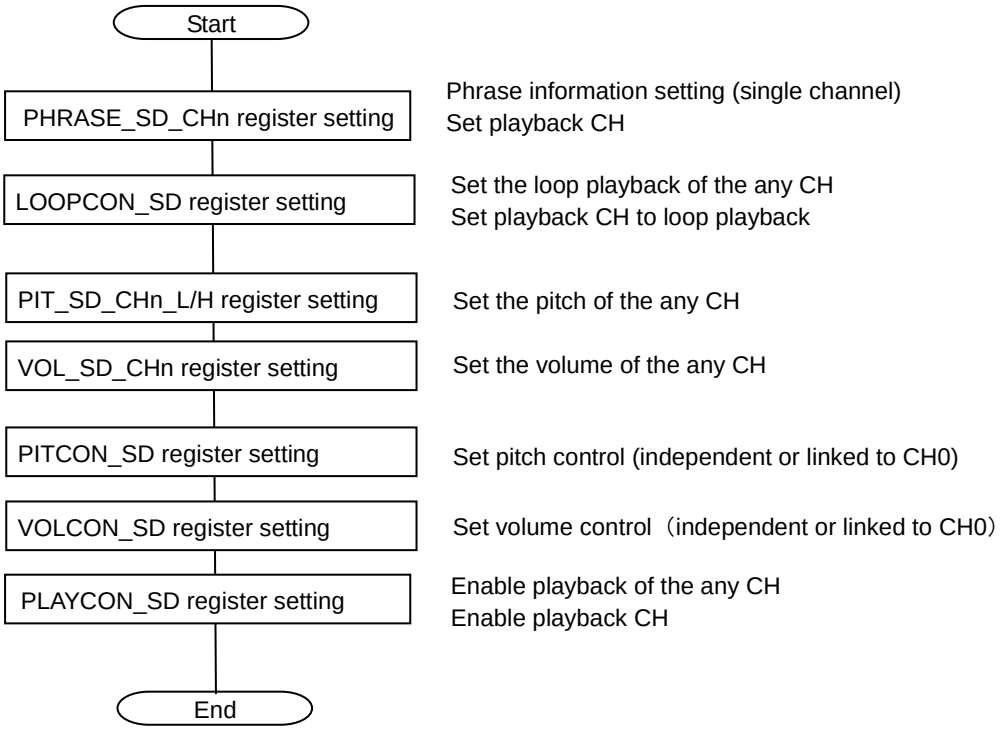
③Stops playback of the any CH or all CHs.



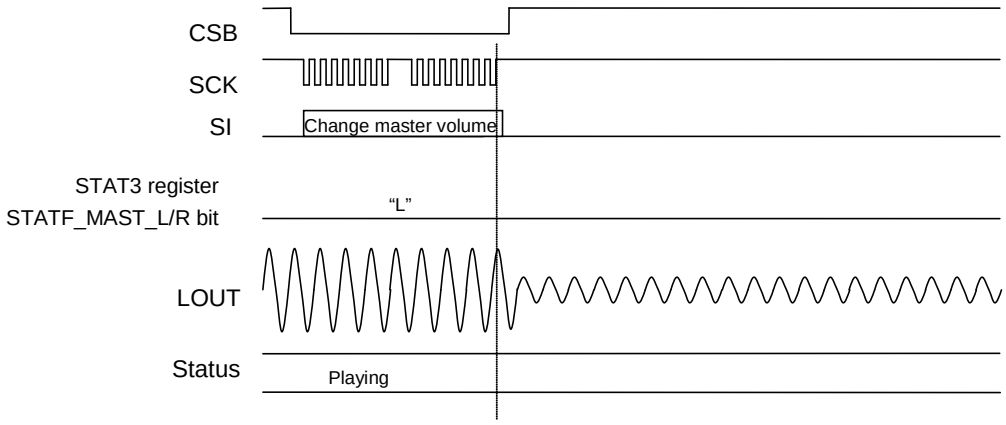
・To stop the playback of multiple channels, set the volume (VOL_SD_CHn) of the any CH to MUTE.
To stop playback of all channels, set the master volume (VOL_MASTL_L/H, VOL_MASTR_ L/H) to MUTE.
・To stop playback when playing a single channel, set the master volume (VOL_MASTL_L/H, VOL_MASTR_L/H) to MUTE.
・To restart playback after stopping playback in the PLAYCON_MAST register, refer to the SoundGenerator playback flow.

◆ SoundGenerator CH additional playback flow

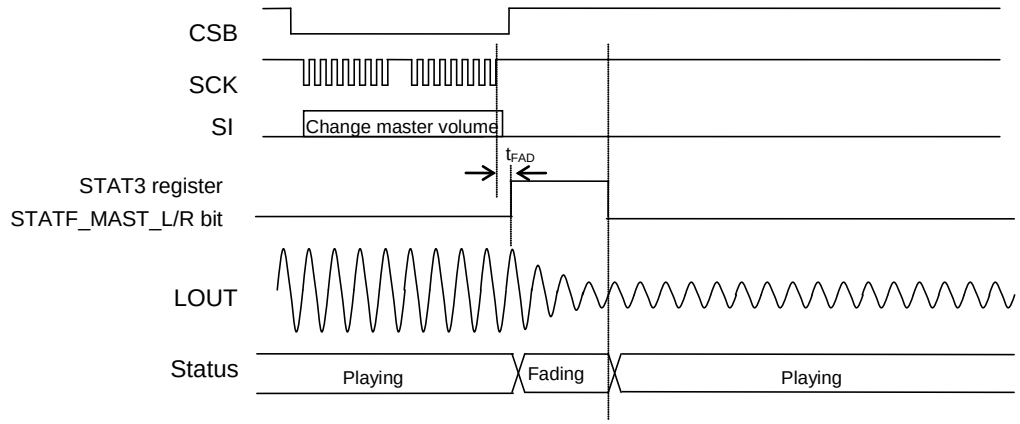
・When playing a CH that is not playing while playing any CH
(When playing the stopped CH after stopping the playback of only some CHs with the STOPCON_SD register while playing multiple CHs.)



◆ Volume change timing (all CHs) (without fade)



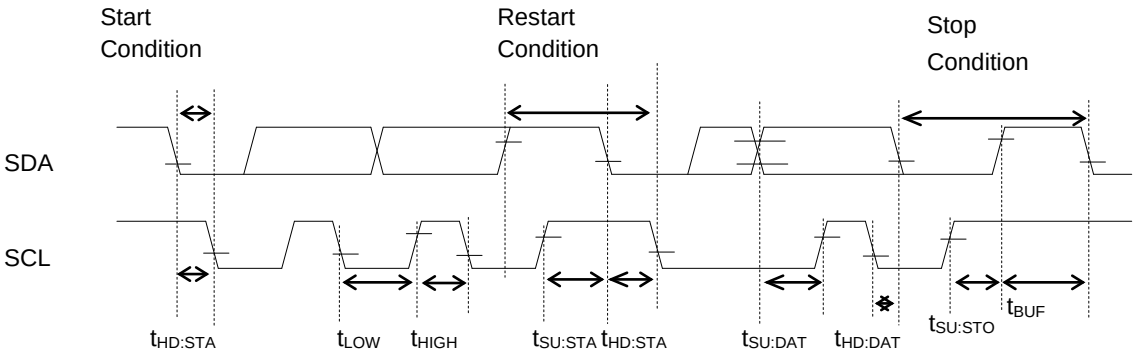
◆ Volume change timing (all CHs) (with fade)



*1 For the volume transition time, refer " VOLFADE_STEP register" in the registers.

● I^2C Interface (Slave)

◆ I^2C Interface Timing



■ Registers

● Register bank list

Registers are arranged in banks for each function.
Banks are switched using the BANKSEL register, which is a register common to all banks.

BANKSEL register [3:0]	Select registers section
0x0	SoundGenerator0 related registers
0x1	SoundGenerator1 related registers
0x2	EqualizerLch related registers
0x3	EqualizerRch related registers
0x4-0xF	Setting prohibited

Check the following pages for the registers of each bank.
Writing to banks and addresses not listed is prohibited. Write the initial value to the unused bit of each register.

● Registers list

◆ All banks common registers list（BANKSEL[3:0]= 0x0，0x1，0x2，0x3）

The address space from 0x00 to 0x3F is common to all banks and can be accessed from any bank.
Writing to addresses not listed is prohibited. Write the initial value to the unused bit of each register.

Address	Register name	Functions	R/W
0x00	BANKSEL	Access bank selection	R/W
0x01	CLKSEL	Reference clock selection	R/W
0x02	I^2CSEL	I^2C access mode selection	R/W
0x03	IFSEL	IF selection	R/W
0x04	LRSEL	Selection of Lch / Rch setting values	R/W
0x05~0x06	-	Write prohibited	R
0x07	ERROR	Notification of internal error status	R/W
0x08	STAT0	Notification of internal status	R
0x09	STAT1	Notification of playback status of CH 0 to 3	R
0x0A	STAT2	Notification of volume fade status of CH 0 to 3	R
0x0B	STAT3	Notification of master volume Lch/Rch fade status	R
0x0C~0x0F	-	Write prohibited	R
0x10	FLS_ACCS	Serial flash memory access control	W
0x11~0x15	-	Write prohibited	R
0x16	SAITCON	SerialAudioInterface transfer format setting	R/W
0x17	-	Write prohibited	R
0x18	-	Write prohibited	R
0x19	MCLKCON	SerialAudioInterface MCLK output control	R/W
0x1A	-	Write prohibited	R
0x1B	OUTDATA	Sound output data transfer channel setting	R/W
0x1C	OUTMODE	Sound output mode setting	R/W
0x1D	OUTCON	Sound output control	R/W
0x1E~0x1F	-	Write prohibited	R
0x20	OUTSTAT0_0	STATUS0 pin output setting of STAT0 register	R/W
0x21	OUTSTAT0_1	STATUS0 pin output setting of STAT1 register	R/W
0x22	OUTSTAT0_2	STATUS0 pin output setting of STAT2 register	R/W
0x23	OUTSTAT0_3	STATUS0 pin output setting of STAT3 register	R/W
0x24	-	Write prohibited	R
0x25	OUTSTAT0_5	STATUS0 pin output setting of ERROR register	R/W
0x26,0x27	-	Write prohibited	R
0x28	OUTSTAT1_0	STATUS1_MCLKO pin output setting of STAT0 register	R/W
0x29	OUTSTAT1_1	STATUS1_MCLKO pin output setting of STAT1 register	R/W
0x2A	OUTSTAT1_2	STATUS1_MCLKO pin output setting of STAT2 register	R/W
0x2B	OUTSTAT1_3	STATUS1_MCLKO pin output setting of STAT3 register	R/W
0x2C	-	Write prohibited	R
0x2D	OUTSTAT1_5	STATUS1_MCLKO pin output setting of ERROR register	R/W
0x2E	-	Write prohibited	R
0x2F	OUTSTAT2	STATUS2 pin output setting of ERROR register	R/W

Address	Register name	Functions	R/W
0x30~0x31	-	Write prohibited	R
0x32	PITFADE_STEP	Pitch fade step setting	R/W
0x33	PITFADE_CON	Pitch fade control	R/W
0x34,0x35	-	Write prohibited	R
0x36	VOLFADE_STEP	Volume fade step setting	R/W
0x37	VOLFADE_CON	Volume fade control	R/W
0x38	VOL_MASTL_L	Master volume Lch setting	R/W
0x39	VOL_MASTL_H		R/W
0x3A	VOL_MASTR_L	Master volume Rch setting	R/W
0x3B	VOL_MASTR_H		R/W
0x3C~0x3D	-	Write prohibited	R
0x3E	PLAYCON_MAST	Playback start / stop control	R/W
0x3F	-	Write prohibited	R

◆ SoundGenerator0 related registers list（BANKSEL[3:0]=0x0）

Writing to addresses not listed is prohibited. Write the initial value to the unused bit of each register.
The address space from 0x00 to 0x3F is common to all banks, so refer to "All banks common registers list".

Address	Register name	Functions	R/W
0x00~0x3F	-	All banks common registers	-
0x40	PITCHCON_SD	Pitch control of CH	R/W
0x41	VOLCON_SD	Volume control of CH	R/W
0x42	PLAYCON_SD	Playback control of CH	W
0x43	STOPCON_SD	Playback stop control of CH	W
0x44~0x4F	-	Write prohibited	R
0x50	PIT_SD_CH0_L	Pitch setting of CH0	R/W
0x51	PIT_SD_CH0_H		R/W
0x52	PIT_SD_CH1_L	Pitch setting of CH1	R/W
0x53	PIT_SD_CH1_H		R/W
0x54	PIT_SD_CH2_L	Pitch setting of CH2	R/W
0x55	PIT_SD_CH2_H		R/W
0x56	PIT_SD_CH3_L	Pitch setting of CH3	R/W
0x57	PIT_SD_CH3_H		R/W
0x58~0x5F	-	Write prohibited	R
0x60	VOL_SD_CH0_L	Volume setting of CH0	R/W
0x61	VOL_SD_CH0_H		R/W
0x62	VOL_SD_CH1_L	Volume setting of CH1	R/W
0x63	VOL_SD_CH1_H		R/W
0x64	VOL_SD_CH2_L	Volume setting of CH2	R/W
0x65	VOL_SD_CH2_H		R/W
0x66	VOL_SD_CH3_L	Volume setting of CH3	R/W
0x67	VOL_SD_CH3_H		R/W
0x68~0x7F	-	Write prohibited	R

◆ SoundGenerator1 related registers list（BANKSEL[3:0]=0x1）

Writing to addresses not listed is prohibited. Write the initial value to the unused bit of each register.
The address space from 0x00 to 0x3F is common to all banks, so refer to "All banks common registers list".

Address	Register name	Functions	R/W
0x00~0x3F	-	All banks common registers	-
0x40	PHRASE_SD_CH0	Phrase setting of CH0	R/W
0x41	PHRASE_SD_CH1	Phrase setting of CH1	R/W
0x42	PHRASE_SD_CH2	Phrase setting of CH2	R/W
0x43	PHRASE_SD_CH3	Phrase setting of CH3	R/W
0x44~0x47	-	Write prohibited	R
0x48	LOOPCON_SD	Loop playback control	R/W
0x49~0x7F	-	Write prohibited	R

◆ EqualizerLch related registers list（BANKSEL[3:0]=0x2）

Writing to addresses not listed is prohibited. Write the initial value to the unused bit of each register.
The address space from 0x00 to 0x3F is common to all banks, so refer to "All banks common registers list".

Address	Register name	Functions	R/W
0x00~0x3F	-	All banks common registers	-
0x40	EQLCON	EQ Lch enable control	R/W
0x41	EQLGAIN0	EQ Lch Band0 gain setting	R/W
0x42	EQLGAIN1	EQ Lch Band1 gain setting	R/W
0x43	EQLGAIN2	EQ Lch Band2 gain setting	R/W
0x44	EQLGAIN3	EQ Lch Band3 gain setting	R/W
0x45	EQLGAIN4	EQ Lch Band4 gain setting	R/W
0x46	EQLBAND0A0L	EQ Lch Band0 A0 coefficient setting	R/W
0x47	EQLBAND0A0H		R/W
0x48	EQLBAND0A1L	EQ Lch Band0 A1 coefficient setting	R/W
0x49	EQLBAND0A1H		R/W
0x4A	EQLBAND1A0L	EQ Lch Band1 A0 coefficient setting	R/W
0x4B	EQLBAND1A0H		R/W
0x4C	EQLBAND1A1L	EQ Lch Band1 A1 coefficient setting	R/W
0x4D	EQLBAND1A1H		R/W
0x4E	EQLBAND2A0L	EQ Lch Band2 A0 coefficient setting	R/W
0x4F	EQLBAND2A0H		R/W
0x50	EQLBAND2A1L	EQ Lch Band2 A1 coefficient setting	R/W
0x51	EQLBAND2A1H		R/W
0x52	EQLBAND3A0L	EQ Lch Band3 A0 coefficient setting	R/W
0x53	EQLBAND3A0H		R/W
0x54	EQLBAND3A1L	EQ Lch Band3 A1 coefficient setting	R/W
0x55	EQLBAND3A1H		R/W
0x56	EQLBAND4A0L	EQ Lch Band4 A0 coefficient setting	R/W
0x57	EQLBAND4A0H		R/W
0x58	EQLBAND4A1L	EQ Lch Band4 A1 coefficient setting	R/W
0x59	EQLBAND4A1H		R/W
0x5A-0x7F	-	Write prohibited	R

◆ EqualizerRch related registers list（BANKSEL[3:0]=0x3）

Writing to addresses not listed is prohibited. Write the initial value to the unused bit of each register.
The address space from 0x00 to 0x3F is common to all banks, so refer to "All banks common registers list".

Address	Register name	Functions	R/W
0x00~0x3F	-	All banks common registers	-
0x40	EQRCON	EQ Rch enable control	R/W
0x41	EQRGAIN0	EQ Rch Band0 gain setting	R/W
0x42	EQRGAIN1	EQ Rch Band1 gain setting	R/W
0x43	EQRGAIN2	EQ Rch Band2 gain setting	R/W
0x44	EQRGAIN3	EQ Rch Band3 gain setting	R/W
0x45	EQRGAIN4	EQ Rch Band4 gain setting	R/W
0x46	EQRBAND0A0L	EQ Rch Band0 A0 coefficient setting	R/W
0x47	EQRBAND0A0H		R/W
0x48	EQRBAND0A1L	EQ Rch Band0 A1 coefficient setting	R/W
0x49	EQRBAND0A1H		R/W
0x4A	EQRBAND1A0L	EQ Rch Band1 A0 coefficient setting	R/W
0x4B	EQRBAND1A0H		R/W
0x4C	EQRBAND1A1L	EQ Rch Band1 A1 coefficient setting	R/W
0x4D	EQRBAND1A1H		R/W
0x4E	EQRBAND2A0L	EQ Rch Band2 A0 coefficient setting	R/W
0x4F	EQRBAND2A0H		R/W
0x50	EQRBAND2A1L	EQ Rch Band2 A1 coefficient setting	R/W
0x51	EQRBAND2A1H		R/W
0x52	EQRBAND3A0L	EQ Rch Band3 A0 coefficient setting	R/W
0x53	EQRBAND3A0H		R/W
0x54	EQRBAND3A1L	EQ Rch Band3 A1 coefficient setting	R/W
0x55	EQRBAND3A1H		R/W
0x56	EQRBAND4A0L	EQ Rch Band4 A0 coefficient setting	R/W
0x57	EQRBAND4A0H		R/W
0x58	EQRBAND4A1L	EQ Rch Band4 A1 coefficient setting	R/W
0x59	EQRBAND4A1H		R/W
0x5A-0x7F	-	Write prohibited	R

● Description of Register Functions

◆ All banks common registers list (BANKSEL[3:0]= 0x0, 0x1, 0x2, 0x3)

• Access bank selection register（BANKSEL）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x00
Initial value : 0x00
Functions : Access bank selection

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3-0	BANK[3:0]	Access bank selection 0x0： SoundGenerator0 related registers 0x1： SoundGenerator1 related registers 0x2： EqualizerLch related registers 0x3： EqualizerRch related registers 0x4-0xF ： Setting prohibited	R/W	0000

It is a common register for all BANK registers.
Registers other than addresses 0x00 to 0x3F are independent registers for each bank.

- Clock selection register（CLKSEL）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x01
Initial value : 0x00
Funcrions : Reference clock selection

Bit	Bit name	Functions	R/W	Initial value
7-3	Unused	—	R	00000
2	XTSEL	Reference clock selection 0：Use RC4Mz 1：Use a crystal or ceramic oscillator or an external clock input	R/W	0
1-0	Unused	—	R	00

[Note]
・When using a crystal oscillator, ceramic oscillator, or external clock input, release the reset after turning on the power, check the power-up of the internal regulator (PUP bit of the STAT0 register is "1"), and then set it. Do not set during playback operation.
・If the XTSEL bit is set to "1", it will continue to be "1" even if it is set to "0".

- I^2C access mode selection register (I^2CSEL)

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x02
Initial value : 0x00
Functions : I^2C access mode selection

Bit	Bit name	Functions	R/W	Initial value
7-1	Unused	—	R	0000000
0	RANDOM	I^2C access mode selection 0: Use increment mode 1: Use random access mode	R/W	0

[Note]
・The setting of this register is valid when I^2C interface is performed with the MCU interface. When communication is performed by clock synchronous serial interface, only the increment mode is supported, and the setting of this register is invalid.
・After switching the RANDOM bit, be sure to restart from the start condition.

- IF selection register（IFSEL）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x03
Initial value : 0x00
Functions : IF seletion

Bit	Bit name	Functions	R/W	Initial value
7-5	Unused	—	R	000
4	TWSEL	Input mode selection 0：Use one-times input mode 1：Use two-times input mode	R/W	0
3-1	Unused	—	R	000
0	MCLKSEL	STATUS1_MCLKO pin selection 0：Select STATUS1 1：Select MCLKO	R/W	0

[Note]
・The TWSEL bit is set to “1”, shifts to two-times input mode. For details on how to input address or data, refer "Clock synchronous serial interface" and "I^2C interface" in the function description.
・After switching the TWSEL bit, be sure to return the CSB pin to the “H” level or restart from the start condition.

- LR selection register（LRSEL）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x04
Initial value : 0x00
Functions : Selection of Lch/Rch setting values

Bit	Bit name	Functions	R/W	Initial value
7-2	Unused	—	R	000000
1	LR_EQ	Selection of Rch setting value of equalizer 0: Apply Rch setting value(control independently) 1: Apply Lch setting value(control linked to Lch)	R/W	0
0	LR_VOL	Selection of Rch setting value of master volume 0: Apply VOL_MASTR_L/H(control independently) 1: Apply VOL_MASTL_L/H(control linked to Lch)	R/W	0

[Note]
・When the LR_EQ bit is set to “1”, the equalizer Rch is controlled by the EqualizerLch related registers. EqualizerRch related registers can be written / read.

・When the LR_VOL bit is set to “1”, the the master volume Rch is controlled by the VOL_MASTL_L/H register. The VOL_MASTR_L/H register can be written / read.

- Error register（ERROR）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x07
Initial value : 0x00
Functions : Notification of internal error status

Bit	Bit name	Functions	R/W	Initial value
7	Unused	—	R	0
6	ROMERR	Notification of the error of the flash memory read data during the internal reset process 0: No error 1: Error	R	0
5	Unused	—	R	0
4	TWERR	Notification of the error in the two-times input mode 0: No error 1: Error	R/W	0
3	Unused	—	R	0
2	CLKERR	Notification of stop error of crystal oscillator or ceramic oscillator or external clock input 0: No error 1: Error	R/W	0
1-0	Unused	—	R	00

[Note]
・The ROMERR bit is not cleared even if it is written to this register. Initialize this LSI by resetting with the RESETB.

・The TWERR bit notifies an error when a mismatch occurs between the first data input and the second data input with the TWSEL bit in the IFSEL register set to “1”. It is cleared by writing to this register.

・The CLKERR bit notifies an error when oscillation stop is detected with the XTSEL bit of the CLKSEL register set to “1”. The playback status continues, so take measures such as stopping playback as necessary. It is cleared by writing to this register. However, if oscillation is still stopped, the CLKERR bit is set to “1” again.

- Status register 0（STAT0）

Bank :0x0, 0x1, 0x2, 0x3
Address :0x08
Initial value :0x01
Functions :Notification of internal status

Bit	Bit name	Functions	R/W	Initial value
7-5	Unused	—	R	000
4	PUP_OUT	Notification of output status from LINE amplifier or SAI pin Notification of the status when the OUT_EN bit of the OUTCON register is changed. *1	R	0
3	Unused	—	R	0
2	PUP_XT	Notification of the status of the crystal oscillator or ceramic oscillator or external clock input 0：Waiting for oscillation stabilization or stopping 1：Oscillating	R	0
1	REG_SET	All banks common registers, SoundGenerator0 related registers, SoundGenerator1 related registers, EqualizerLch related registers, EqualizerRch related registers 0：Not set 1：Configured	R	0
0	PUP	Notification of internal regulator startup status 0：Internal regulator power down 1：Internal regulator power up	R	1

*1 Refer "Sound output power up and Sound output power down" in the timing chart.

[Note]
・When turn on the power and release the reset, be sure to check that the PUP bit is set to “1” before performing the following processing. Writing and reading to other registers with the PUP bit set to “0” is not guaranteed.
・The REG_SET bit becomes "1" by writing to all of the following registers. To set the REG_SET bit to "1", be sure to write the initial value even if the following registers are used as they are.

BANKSEL register[3:0]	register
0x0,0x1,0x2,0x3 (All banks common registers)	0x2D ： OUTSTAT1_5
0x0（SoundGenerator0 related registers）	0x67 ： VOL_SD_CH3_H
0x1（SoundGenerator1 related registers）	0x48 ： LOOPCON_SD
0x2（EqualizerLch related registers）	0x59 ： EQLBAND4A1H
0x3（EqualizerRch related registers）	0x59 ： EQRBAND4A1H

・The REG_SET bit is set to “0”, it means that the register has not been set or the register may have been initialized for some reason. In that case, reset all the registers before accessing the playback mode setting register and playback control register.
・Confirm that the PUP_OUT bit is “1” before playing.

- Status register 1（STAT1）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x09
Initial value : 0x00
Functions : Notification of playback status of CH 0 to 3

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3	STATP_SD_CH3	Notification of playback status of CH3 0：Playing stopped 1：Playing	R	0
2	STATP_SD_CH2	Notification of playback status of CH2 0：Playing stopped 1： Playing	R	0
1	STATP_SD_CH1	Notification of playback status of CH1 0：Playing stopped 1： Playing	R	0
0	STATP_SD_CH0	Notification of playback status of CH0 0：Playing stopped 1： Playing	R	0

- Status register 2（STAT2）

Bank : 0x0, 0x1, 0x2, 0x3,
Address : 0x0A
Initial value : 0x00
Functions : Notification of volume fade status of CH 0 to 3

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3	STATF_SD_CH3	Notification of fade status of CH3 0：Fading stopped 1：Fading	R	0
2	STATF_SD_CH2	Notification of fade status of CH2 0：Fading stopped 1：Fading	R	0
1	STATF_SD_CH1	Notification of fade status of CH1 0：Fading stopped 1：Fading	R	0
0	STATF_SD_CH0	Notification of fade status of CH0 0：Fading stopped 1：Fading	R	0

- Status register 3（STAT3）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x0B
Initial value : 0x00
Functions : Notification of master volume Lch/Rch fade status

Bit	Bit name	Functions	R/W	Initial value
7-2	Unused	—	R	000000
1	STATF_MAST_R	Notification of fade status of master volume Rch 0：Fading stopped 1：Fading	R	0
0	STATF_MAST_L	Notification of fade status of master volume Lch 0：Fading stopped 1：Fading	R	0

- Flash memory access control register（FLS_ACCS）

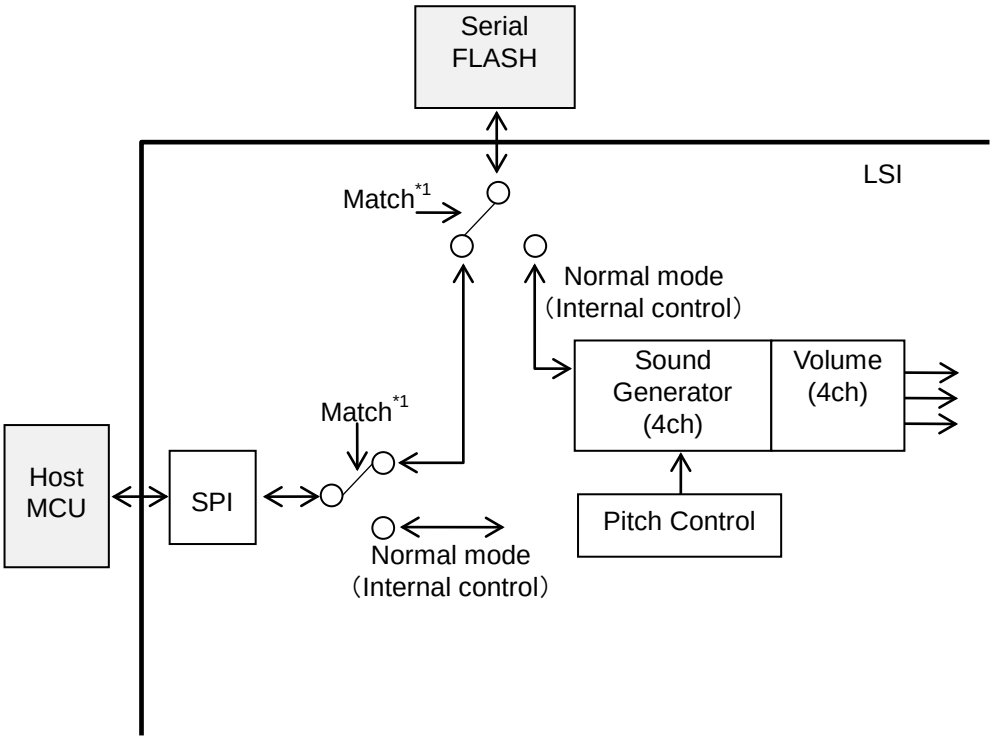
Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x10
Initial value : 0xXX
Functions : Serial flash memory access control

Bit	Bit name	Functions	R/W	Initial value
7-0	FLS_PRT[7:0]	Flash memory protect code	W	0xXX

[Note]
・It is necessary to set the flash memory protection release information in advance using the dedicated tool (SpeechLSIUtility).
・If the flash memory protection release information set by the dedicated tool (SpeechLSIUtility) is 0x69, the flash memory interface is not connected even if it matches the flash memory protection code set in the FLS_ACCS register.
・If the flash memory protection release information set by the dedicated tool (SpeechLSIUtility) is other than 0x69, the flash memory interface is connected when it matches the flash memory protection code set in the FLS_ACCS register.
・Once the clock synchronous serial interface and the flash memory interface are connected, the normal mode cannot be restored. To return to the normal mode, input the "L" level to the reset input pin (RESETB pin) to initialize this LSI.

・When rewriting the flash memory, input the "L" → "H" level to the reset input pin (RESETB pin), and then set it in the FLS_ACCS register. After inputting the “L” → “H” level to the RESETB pin, the FLS_ACCS register cannot be set after setting other than the FLS_ACCS register.

・The flash memory cannot be rewritten using the I^2C interface (slave), so do not write to this register.



*1：The write conditions to the flash memory access control register match

- SerialAudioInterface transfer format setting register（SAITCON）

Bank :0x0, 0x1, 0x2, 0x3
Address :0x16
Initial value :0x00
Functions :SerialAudioInterface transfer format setting

Bit	Bit name	Functions	R/W	Initial value
7	BWO	Bit width for transfer 0：16bit Straight PCM 1：8bit Straight PCM	R/W	0
6	Unused	—	R	0
5	FMTO	Transfer mode 0：LRCLK transfer mode 1：Frame synchronous transfer mode	R/W	0
4	MSBO	MSB first or LSB first in the transmit data. 0：MSB first 1：LSB first	R/W	0
3	ISSCKO	BCLK pin as 32gfs or 64gfs. 0：32gfs 1：64gfs	R/W	0
2	AFOO	Transmit data is left-aligned or right-aligned 0：Left-justify 1：Right-justify	R/W	0
1	DLYO	Transmit data has a 1-clock delay or not. 0：Serial data delay 1：No serial data delay	R/W	0
0	WSLO	LRCLK polarities 0：Lch is transmitted when LRCLK is "L" level, Rch is transmitted when LRCLK is "H" level 1：Lch is transmitted when LRCLK is "H" level, Rch is transmitted when LRCLK is "L" level	R/W	0

[Note]
・Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0" and the OUT_EN bit of the OUTCON register is "0").
・Set the WSLO bit to "1" in the frame synchronous transfer mode (set "1" for the FMTO bit).
・Set the AFOO bit to "0" in the frame synchronous transfer mode (set "1" to the FMTO bit).

- SerialAudioInterface MCLK control register（MCLKCON）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x19
Initial value : 0x00
Functions : SerialAudioInterface MCLK output control

Bit	Bit name	Functions	R/W	Initial value
7-3	Unused	—	R	00000
2-1	MCLK_FS	MCLKO output setting 00：128gfs 01：256gfs 1*：512gfs	R/W	00
0	MCLK_EN	MCLKO pin master clock output setting 0：Disable output 1：Enable output	R/W	0

*：0/1 Either is acceptable

MCLKSEL bit of the IFSEL register is "1" and the MCLK_EN of the MCLKCON register is "1", select playback from SAI pin by OUT_MD [1: 0] bits of the OUTMODE register. After setting the OUT_EN bit to “1”, when the PUP_OUT bit in STAT0 register becomes “1”, master clock output is started from the STATUS1_MCLKO pin.

[Note]
Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0" and the OUT_EN bit of the OUTCON register is "0").

- Sound output data transfer channel setting register（OUTDATA）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x1B
Initial value : 0x44
Functions : Sound output data transfer channel setting

Bit	Bit name	Functions	R/W	Initial value
7	Unused	—	R	0
6-4	OUT_RCH [2:0]	Setting the data to transmit to the Rch 000 : CH0 001 : CH1 010 : CH2 011 : CH3 1xx : Mixing CH0-3	R/W	100
3	Unused	—	R	0
2-0	OUT_LCH [2:0]	Setting the data to transfer to the Lch and LINE amplifiers 000 : CH0 001 : CH1 010 : CH2 011 : CH3 1xx : Mixing CH0-3	R/W	100

[Note]
Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0" and the OUT_EN bit of the OUTCON register is "0").

- Sound output mode setting register（OUTMODE）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x1C
Initial value : 0x01
Functions : Sound output mode setting

Bit	Bit name	Functions	R/W	Initial value
7	HPF	High-pass filter control 0：No use high-pass filter 1：Use high-pass filter with a cut-off frequency of 200Hz	R/W	0
6	GFS	Selection of a group (gfs) of sampling frequencies 0：a group of 12, 24, 48kHz（SAI output：gfs=48kHz） 1：a group of 8, 16, 32kHz（SAI output：gfs=32kHz）	R/W	0
5-3	Unused	—	R	000
2	POP	LINE amplifier Pop noise countermeasure control during power-up / down processing 0：Without pop noise suppression 1：With pop noise suppression	R/W	0
1-0	OUT_MD[1:0]	Playback mode setting*1	R/W	01

*1 If "00" is written to the OUT_MD [1: 0] bits, "01" is set to the OUT_MD [1: 0] bits.
The combinations of playback using the OUT_MD [1: 0] bits are as follows.

Playback mode	OUT_MD[1]	OUT_MD[0]
Play from LINE amplifier	0	1
Play from SAI pins	1	0
Play from LINE amplifier and SAI pins	1	1

[Note]
・OUTMODE register can be rewritten only when the OUT_EN bit of the OUTCON register is “0”.
・When using only SerialAudioInterface, it is recommended to set the POP bit to “0”.

- Sound output control register（OUTCON）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x1D
Initial value : 0x00
Functions : Sound output control

Bit	Bit name	Functions	R/W	Initial value
7-5	Unused	—	R	000
4	OUT_EN	Output control of playback mode set by OUT_MD [1: 0] 0：Output stopped 1：Output start	R/W	0
3-0	Unused	—	R	0000

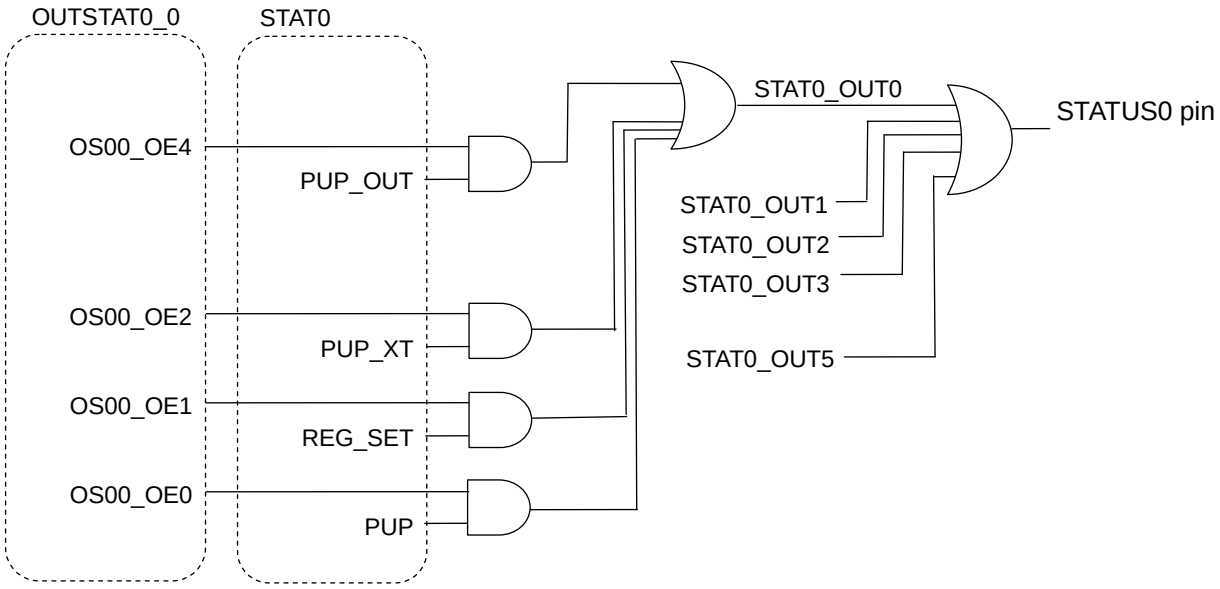
[Note]
When changing OUT_EN bit from “0” to “1”, wait for the PUP_OUT bit in the STAT0 register to become “1” before playing. When changing from "1" to "0", wait for the PUP_OUT bit in the STAT0 register to become "0" before performing the next processing.

- STATUS0 pin output setting register 0（OUTSTAT0_0）

Bank :0x0, 0x1, 0x2, 0x3
Address :0x20
Initial value :0x01
Functions :STATUS0 pin output setting of STAT0 register

Bit	Bit name	Functions	R/W	Initial value
7-5	Unused	—	R	000
4	OS00_OE4	Output of the PUP_OUT bit to the STATUS0 pin 0：No output 1：Output	R/W	0
3	Unused	—	R	0
2	OS00_OE2	Output of the PUP_XT bit to the STATUS0 pin 0：No output 1：Output	R/W	0
1	OS00_OE1	Output of the REG_SET bit to the STATUS0 pin 0：No output 1：Output	R/W	0
0	OS00_OE0	Output of the PUP bit to the STATUS0 pin 0：No output 1：Output	R/W	1

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS0 pin.

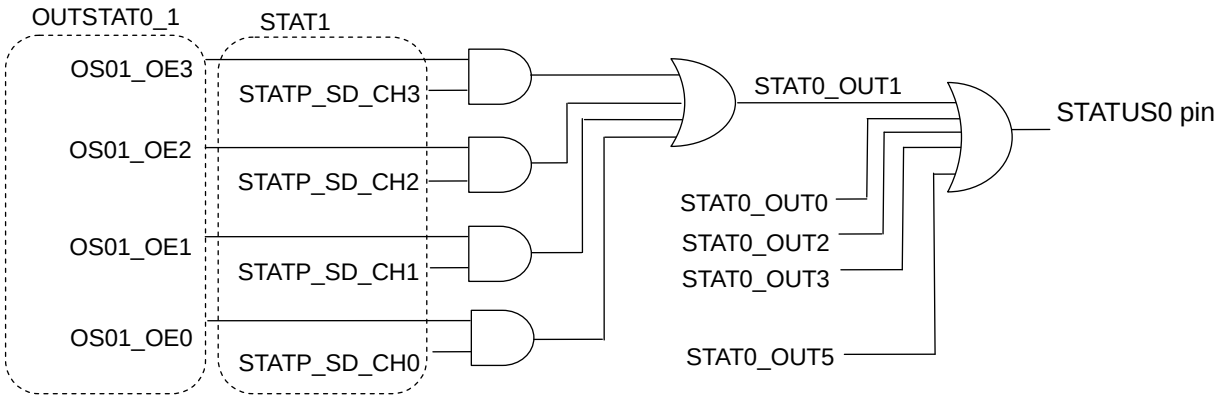


- STATUS0 pin output setting register 1（OUTSTAT0_1）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x21
Initial value : 0x00
Functions : STATUS0 pin output setting of STAT1 register

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3-0	OS01_OE3-0	Output of the playback status bit of CH0-3 to the STATUS0 pin 0：No output 1：Output	R/W	0000

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS0 pin.

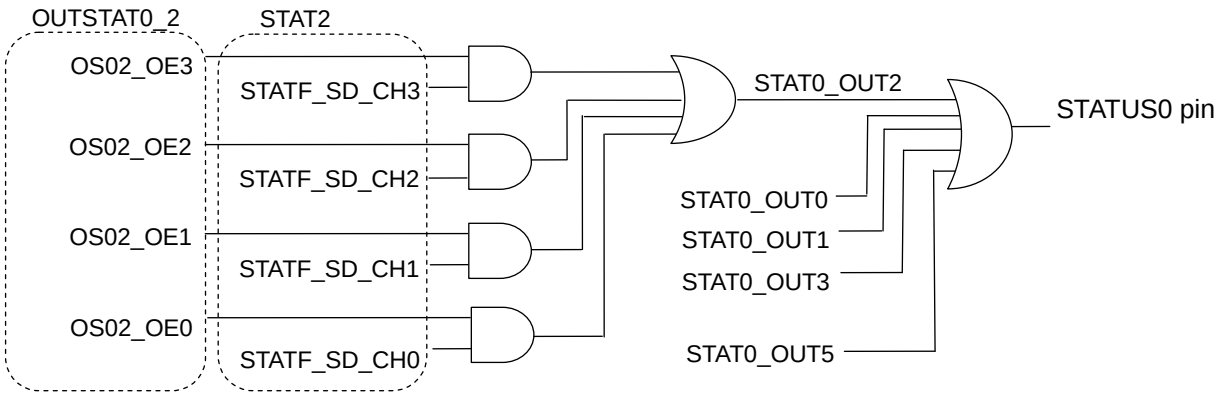


- STATUS0 pin output setting register 2（OUTSTAT0_2）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x22
Initial value : 0x00
Functions : STATUS0 pin output setting of STAT2 register

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3-0	OS02_OE3-0	Output of the volume fade status bit of CH0-3 to the STATUS0 pin 0：No output 1：Output	R/W	0000

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS0 pin.

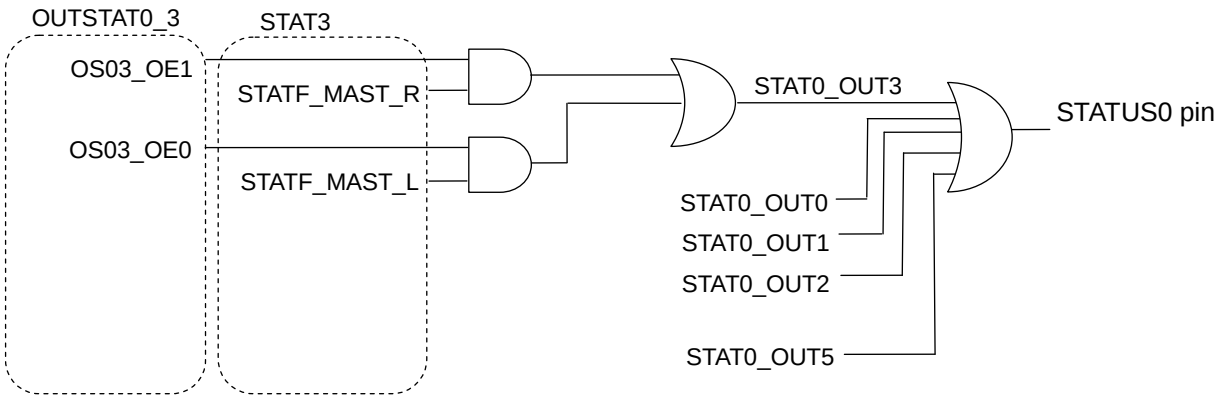


- STATUS0 pin output setting register 3（OUTSTAT0_3）

Bank :0x0, 0x1, 0x2, 0x3
Address :0x23
Initial value :0x00
Functions :STATUS0 pin output setting of STAT3 register

Bit	Bit name	Functions	R/W	Initial value
7-2	Unused	—	R	000000
1-0	OS03_OE1-0	Output of the volume fade status bit of master volume Lch/Rch to the STATUS0 pin 0：No output 1：Output	R/W	00

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS0 pin.

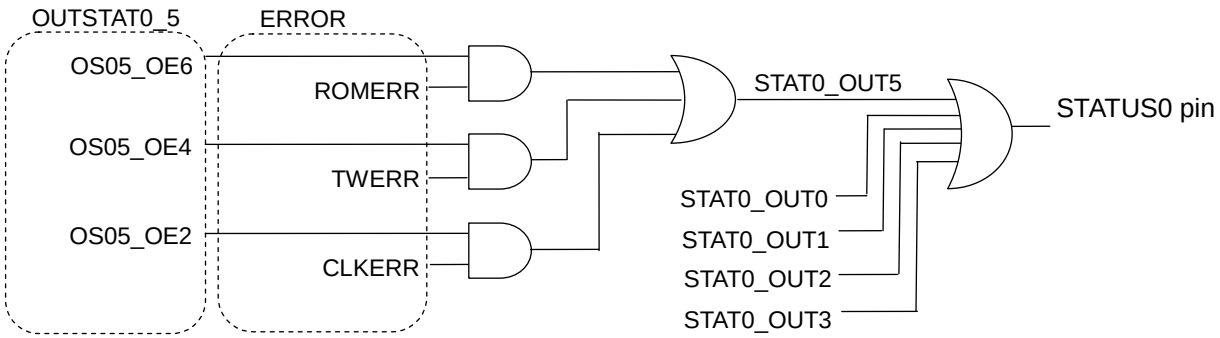


- STATUS0 pin output setting register 5（OUTSTAT0_5）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x25
Initial value : 0x00
Functions : STATUS0 pin output setting of ERROR register

Bit	Bit name	Functions	R/W	Initial value
7	Unused	—	R	0
6	OS05_OE6	Output of the ROMERR bit to the STATUS0 pin 0: No output 1: Output	R/W	0
5	Unused	—	R	0
4	OS05_OE4	Output of the TWERR bit to the STATUS0 pin 0: No output 1: Output	R/W	0
3	Unused	—	R	0
2	OS05_OE2	Output of the CLKERR bit to the STATUS0 pin 0: No output 1: Output	R/W	0
1-0	Unused	—	R	00

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS0 pin.

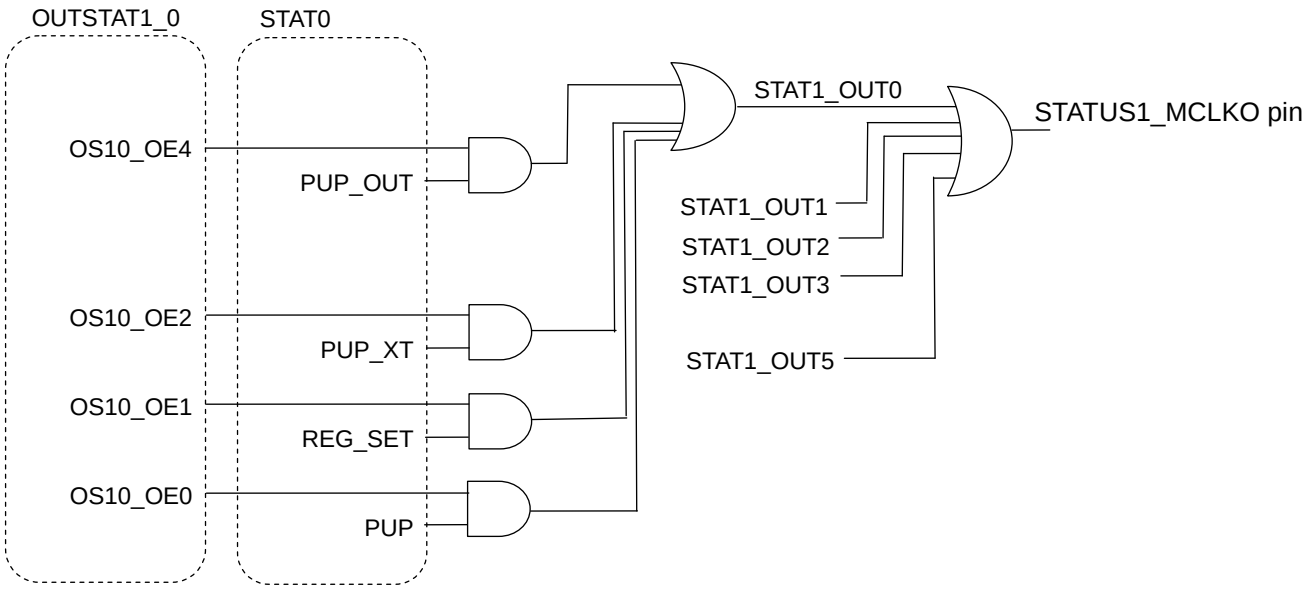


- STATUS1_MCLKO pin output setting register 0（OUTSTAT1_0）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x28
Initial value : 0x00
Functions : STATUS1_MCLKO pin output setting of STAT0 register

Bit	Bit name	Functions	R/W	Initial value
7-5	Unused	—	R	000
4	OS10_OE4	Output of the PUP_OUT bit to the STATUS1_MCLLKO pin 0：No output 1：Output	R/W	0
3	Unused	—	R	0
2	OS10_OE2	Output of the PUP_XT bit to the STATUS1_MCLLKO pin 0：No output 1：Output	R/W	0
1	OS10_OE1	Output of the REG_SET bit to the STATUS1_MCLLKO pin 0：No output 1：Output	R/W	0
0	OS10_OE0	Output of the PUP bit to the STATUS1_MCLLKO pin 0：No output 1：Output	R/W	0

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS1_MCLKO pin.

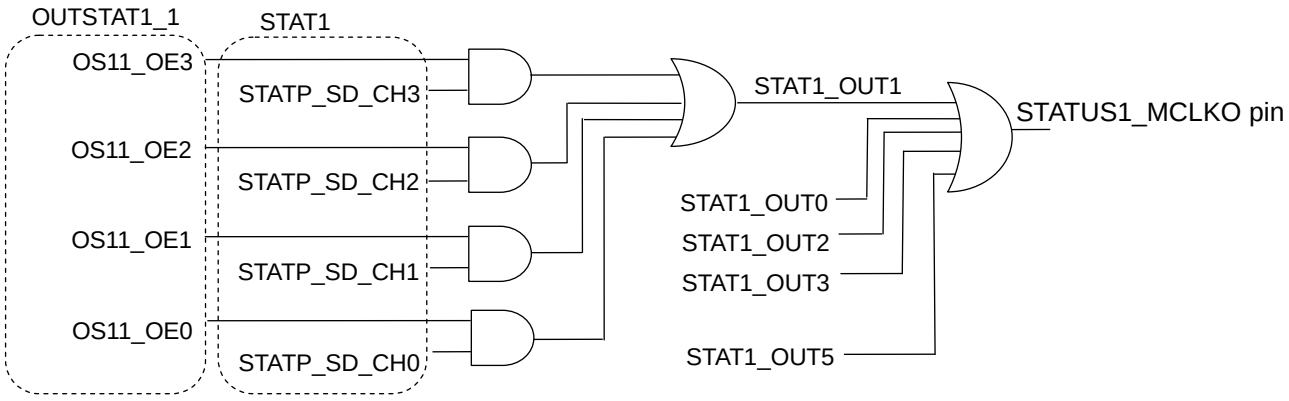


- STATUS1_MCLKO pin output setting register 1（OUTSTAT1_1）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x29
Initial value : 0x00
Functions : STATUS1_MCLKO pin output setting of STAT1 register

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3-0	OS11_OE3-0	Output of the playback status bit of CH0-3 to the STATUS1_MCLKO pin 0：No output 1：Output	R/W	0000

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS1_MCLKO pin.

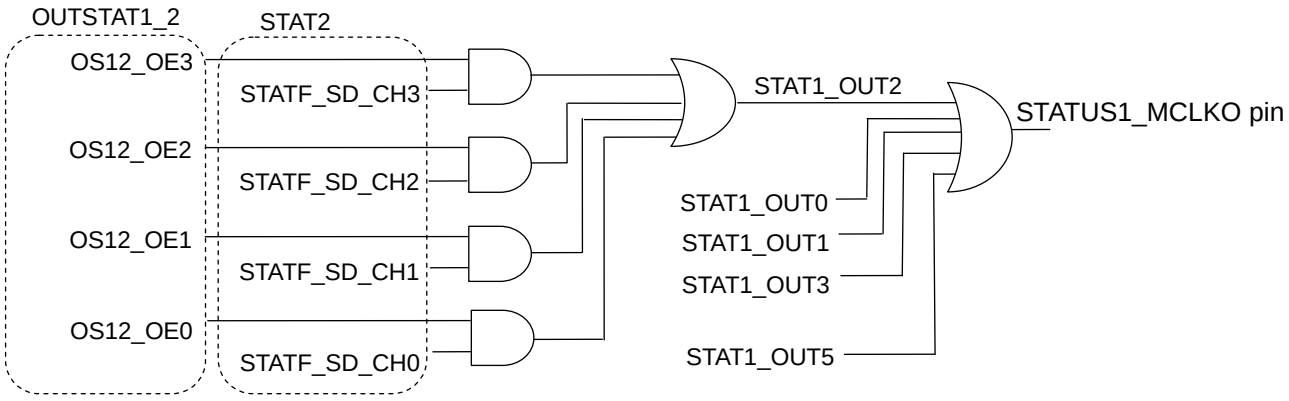


- STATUS1_MCLKO pin output setting register 2（OUTSTAT1_2）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x2A
Initial value : 0x00
Functions : STATUS1_MCLKO pin output setting of STAT2 register

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3-0	OS12_OE3-0	Output of the volume fade status bit of CH0-3 to the STATUS1_MCLKO pin 0：No output 1：Output	R/W	0000

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS1_MCLKO pin.

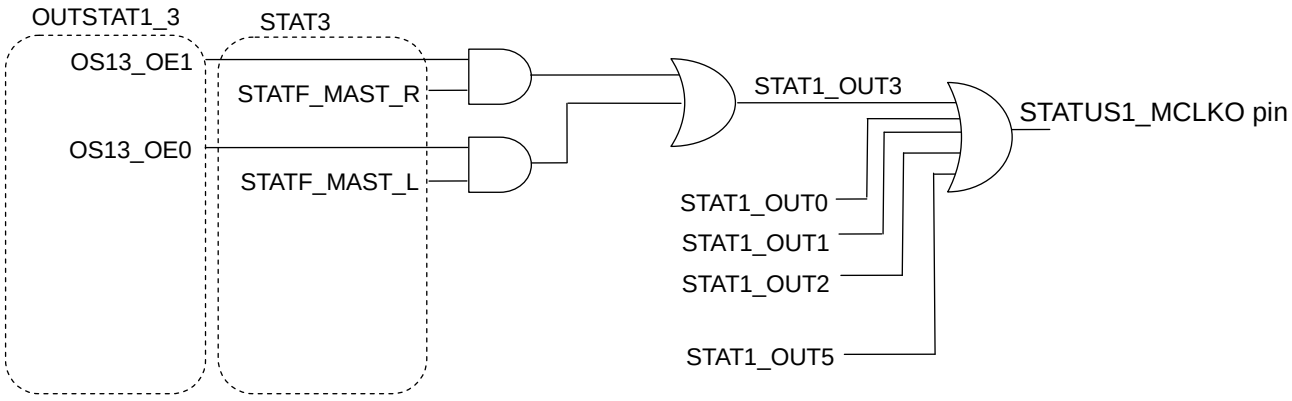


- STATUS1_MCLKO pin output setting register 3（OUTSTAT1_3）

Bank :0x0, 0x1, 0x2, 0x3
Address :0x2B
Initial value :0x00
Functions :STATUS1_MCLKO pin output setting of STAT3 register

Bit	Bit name	Functions	R/W	Initial value
7-2	Unused	—	R	000000
1-0	OS13_OE1-0	Output of the volume fade status bit of master volume Lch/Rch to the STATUS1_MCLKO pin 0：No output 1：Output	R/W	00

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS1_MCLKO pin.

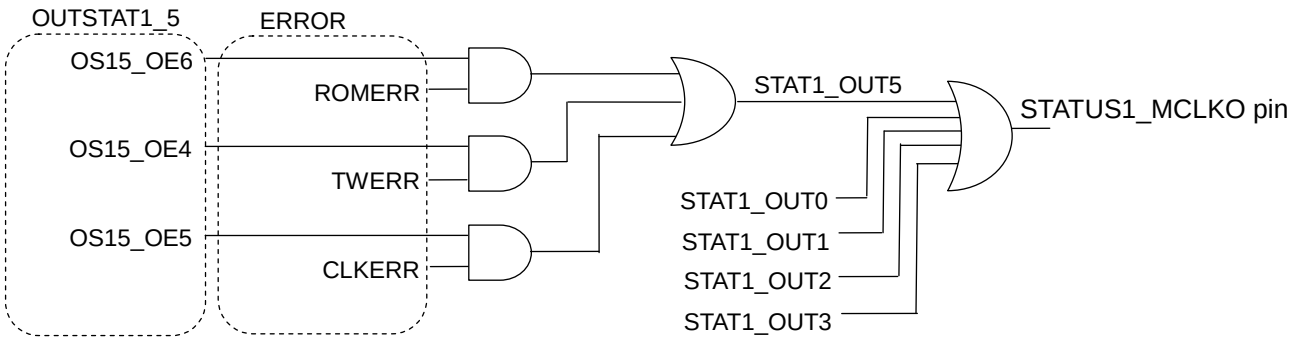


- STATUS1_MCLKO pin output setting register 5（OUTSTAT1_5）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x2D
Initial value : 0x54
Functions : STATUS1_MCLKO pin output setting of ERROR register

Bit	Bit name	Functions	R/W	Initial value
7	Unused	—	R	0
6	OS15_OE6	Output of the ROMERR bit to the STATUS1_MCLKO pin 0：No output 1：Output	R/W	1
5	Unused	—	R	0
4	OS15_OE4	Output of the TWERR bit to the STATUS1_MCLKO pin 0：No output 1：Output	R/W	1
3	Unused	—	R	0
2	OS15_OE2	Output of the CLKERR bit to the STATUS1_MCLKO pin 0：No output 1：output	R/W	1
1-0	Unused	—	R	00

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS1_MCLKO pin.

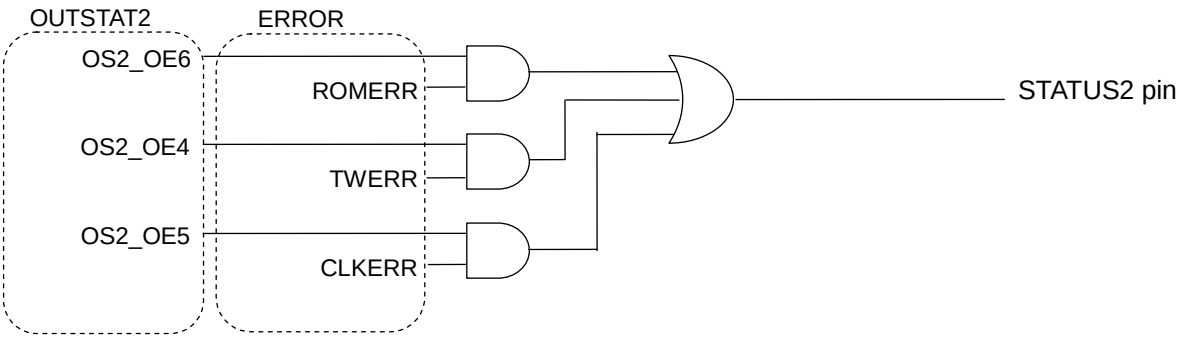


- STATUS2 pin output setting register（OUTSTAT2）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x2F
Initial value : 0x54
Functions : STATUS2 pin output setting of ERROR register

Bit	Bit name	Functions	R/W	Initial value
7	Unused	—	R	0
6	OS2_OE6	Output of the ROMERR bit to the STATUS2 pin 0: No output 1: Output	R/W	1
5	Unused	—	R	0
4	OS2_OE4	Output of the TWERR bit to the STATUS2 pin 0: No output 1: Output	R/W	1
3	Unused	—	R	0
2	OS2_OE2	Output of the CLKERR bit to the STATUS2 pin 0: No output 1: Output	R/W	1
1-0	Unused	—	R	00

[Note]
When “1” is set for multiple bits, the OR-processed signal is output from the STATUS2 pin.



- Pitch fade step setting register（PITFADE_STEP）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x32
Initial value : 0x00
Functions : Pitch fade step setting

Bit	Bit name	Functions	R/W	Initial value
7-0	PITFADE_STEP[7:0]	Setting the pitch change step time of the pitch fade function （0.00390625 times changing time）	R/W	0x00

The pitch changes by one step (0.00390625 times) of the pitch setting register every set time until the set pitch is reached. As shown below, the pitch transition time changes depending on the fade step setting value, pitch change amount, and sampling frequency (fs).

PITFADE_STEP [7:0]	fs conversion	fs：48kHz [ms] Step: 0.0625ms	fs：24kHz [ms] Step: 0.125ms	fs：12kHz [ms] Step: 0.25ms	fs：32kHz [ms] Step: 0.09375ms	fs：16kHz [ms] Step: 0.1875ms	fs：8kHz [ms] Step: 0.375ms
0x00	3/fs	0.0625	0.125	0.25	0.09375	0.1875	0.375
0x01	6/fs	0.125	0.25	0.5	0.1875	0.375	0.75
0x02	9/fs	0.1875	0.375	0.75	0.28125	0.5625	1.125
0x03	12/fs	0.25	0.5	1	0.375	0.75	1.5
:	:	:	:	:	:	:	:
0x7E	381/fs	7.9375	15.875	31.75	11.90625	23.8125	47.625
0x7F	384/fs	8	16	32	12	24	48
0x80	387/fs	8.0625	16.375	32.25	12.09375	24.1875	48.375
:	:	:	:	:	:	:	:
0xFE	765/fs	15.9375	31.875	63.75	23.90625	47.8125	95.625
0xFF	768/fs	16	32	64	24	48	96

The transition time until the set pitch is reached is expressed by the following formula.

Pitch transition time
＝｜[Current register value] － [New register value]｜× [PITFADE_STEP setting value+1] × 0.0625ms（fs:48kHz）

example）
Current register value（Pitch setting register value） : 0x100 = 256d
New register value（Pitch setting register value） : 0x200 = 512d
PITFADE_STEP[7:0] setting value : 0x07

Pitch transition time ＝ ｜[256] － [512]｜×（7＋1）× 0.0625ms ＝ 128[ms]

[Note]
By setting "1" in the PITFADE_CON register, the changed pitch is faded with the set value of this register.

- Pitch fade control register（PITFADE_CON）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x33
Initial value : 0x00
Functions : Pitch fade control

Bit	Bit name	Functions	R/W	Initial value
7-1	Unused	—	R	0000000
0	PITFADE_EN	Control fade 0：No use a fade 1：Use a fade	R/W	0

[Note]
When "1" is set, the pitch fades to the changed pitch with the setting value of the PITFADE_STEP register.

- Volume fade step setting regisger（VOLFADE_STEP）

Bank :0x0, 0x1, 0x2, 0x3
Address :0x36
Initial value :0x00
Functions :Volume fade step setting

Bit	Bit name	Functions	R/W	Initial value
7-0	VOLFADE_STEP[7:0]	Setting the volume change step time of the volume fade function （Time of change by 0.1 dB）	R/W	0x00

The volume changes by one step (0.1 dB) of the volume setting register every set time until the changed volume is reached. As shown below, the volume transition time changes depending on the fade step setting value, volume change amount, and sampling frequency (fs).

VOLFADE_STEP [7:0]	fs conversion	fs：48kHz [ms] Step: 0.0625ms	fs：24kHz [ms] Step: 0.125ms	fs：12kHz [ms] Step: 0.25ms	fs：32kHz [ms] Step: 0.09375ms	fs：16kHz [ms] Step: 0.1875ms	fs：8kHz [ms] Step: 0.375ms
0x00	3/fs	0.0625	0.125	0.25	0.09375	0.1875	0.375
0x01	6/fs	0.125	0.25	0.5	0.1875	0.375	0.75
0x02	9/fs	0.1875	0.375	0.75	0.28125	0.5625	1.125
0x03	12/fs	0.25	0.5	1	0.375	0.75	1.5
:	:	:	:	:	:	:	:
0x7E	381/fs	7.9375	15.875	31.75	11.90625	23.8125	47.625
0x7F	384/fs	8	16	32	12	24	48
0x80	387/fs	8.0625	16.375	32.25	12.09375	24.1875	48.375
:	:	:	:	:	:	:	:
0xFE	765/fs	15.9375	31.875	63.75	23.90625	47.8125	95.625
0xFF	768/fs	16	32	64	24	48	96

The transition time until the set volume is reached is expressed by the following formula.

Volume transition time
＝｜[Current dB value] － [New dB value]｜× [VOLFADE_STEP setting value＋1] × 0.0625ms（fs:48kHz）×10
or
＝｜[Current register value] － [New register value]｜× [VOLFADE_STEP setting value＋1] × 0.0625ms（fs:48kHz）

example）
Current dB value（Volume setting register value） :－51.2dB / 0x100 = 256d
New dB value（Volume setting register value） :－25.6dB / 0x200 = 512d
VOLFADE_STEP[7:0] setting value :0x07

Volume transition time ＝ ｜[－51.2] － [－25.6]｜×（7＋1）× 0.0625ms × 10 ＝ 128[ms]
Volume transition time ＝ ｜[256] － [512]｜×（7＋1）× 0.0625ms ＝ 128[ms]

[Note]
・By setting "1" in the VOLFADE_CON register, the changed volume is faded with the set value of this register.
・When the volume is changed in the VOL_MASTL_L/H register and VOL_MASTR_L/H register, it fades at 48kHz or 32kHz depending on the GFS bit of the OUTMODE register.

- Volume fade control register（VOLFADE_CON）

Bank :0x0, 0x1, 0x2, 0x3
Address :0x37
Initial value :0x00
Functions :Volume fade control

Bit	Bit name	Functions	R/W	Initial value
7-1	Unused	—	R	0000000
0	VOLFADE_EN	Control fade 0：No use a fade 1：Use a fade	R/W	0

[Note]
When "1" is set, the volume fades to the changed volume with the setting value of the VOLFADE_STEP register.

- Master Volume Lch setting register L（VOL_MASTL_L）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x38
Initial value : 0x00
Functions : Master volume Lch setting

Bit	Bit name	Functions	R/W	Initial value
7-0	VOLML_L[7:0]	Master volume Lch setting [7:0]	R/W	0x00

- Master Volume Lch setting register H（VOL_MASTL_H）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x39
Initial value : 0x03
Functions : Master volume Lch setting

Bit	Bit name	Functions	R/W	Initial value
7-2	Unused	—	R	000000
1-0	VOLML_H[1:0]	Master volume Lch setting[9:8]	R/W	11

[Note]
・The setting register L is updated by writing to the setting register H. To update the setting register L, write to the setting register H.
・This register is the volume adjustment after mixing. Therefore, the volume can be adjusted regardless of the VOL_SD_CHn registers.

The volume can be set from MUTE, -76.7 dB to +25.5 dB in 0.1 dB steps.

Volume [dB]	VOLML_H[9:8] VOLML_L[7:0]
MUTE	0x000
-76.7	0x001
-76.6	0x002
-76.5	0x003
:	:
-0.2	0x2FE
-0.1	0x2FF
0	0x300
+0.1	0x301
+0.2	0x302
:	:
+25.3	0x3FD
+25.4	0x3FE
+25.5	0x3FF

When setting the volume to -12dB, calculate using the following formula and write it to the register.
(-12（Volume dB value） ＋ 76.8) × 10 = 648d = 0x288
Write 0x88 to VOL_MASTL_L [7: 0] and 0x02 to VOL_MASTL_H [9: 8]

- Master Volume Rch setting register L（VOL_MASTR_L）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x3A
Initial value : 0x00
Functions : Master volume Rch setting

Bit	Bit name	Functions	R/W	Initial value
7-0	VOLMR_L[7:0]	Master volume Rch setting [7:0]	R/W	0x00

- Master Volume Rch setting register H（VOL_MASTR_H）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x3B
Initial value : 0x03
Functions : Master volume Rch setting

Bit	Bit name	Functions	R/W	Initial value
7-2	Unused	—	R	000000
1-0	VOLMR_H[1:0]	Master volume Rch setting [9:8]	R/W	11

[Note]
・The setting register L is updated by writing to the setting register H. To update the setting register L, write to the setting register H.
・This register is the volume adjustment after mixing. Therefore, the volume can be adjusted regardless of the VOL_SD_CHn registers.

The volume can be set from MUTE, -76.7 dB to +25.5 dB in 0.1 dB steps.

Volume [dB]	VOLMR_H[9:8] VOLMR_L[7:0]
MUTE	0x000
-76.7	0x001
-76.6	0x002
-76.5	0x003
:	:
-0.2	0x2FE
-0.1	0x2FF
0	0x300
+0.1	0x301
+0.2	0x302
:	:
+25.3	0x3FD
+25.4	0x3FE
+25.5	0x3FF

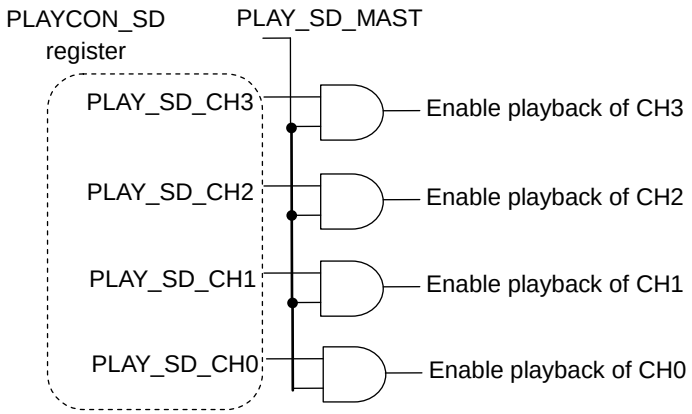
When setting the volume to -12dB, calculate using the following formula and write it to the register.
(-12（Volume dB value） ＋ 76.8) × 10 = 648d = 0x288
Write 0x88 to VOL_MASTL_L [7: 0] and 0x02 to VOL_MASTL_H [9: 8]

- Master playback control register（PLAYCON_MAST）

Bank : 0x0, 0x1, 0x2, 0x3
Address : 0x3E
Initial value : 0x00
Functions : Playback start / stop control

Bit	Bit name	Functions	R/W	Initial value
7-1	Unused	—	R	0000000
0	PLAY_SD_MAST	SoundGenerator playback control 0：stop 1：start	R/W	0

[Note]
・With the channel to be played set (the channel bit of the PLAYCON_SD register is set to “1”), set the PLAY_SD_MAST bit to “1” to start playback. If the PLAY_SD_MAST bit is set to “0” during playback, playback of all Sound Generator channels will stop immediately. At this time, the channel bit of the PLAYCON_SD register is not cleared.
・Read the STAT1 register to check the playback status of each channel.



◆ SoundGenerator0 related registers list（ BANKSEL[3:0]= 0x0 ）

• SoundGenerator pitch control register（PITCHCON_SD）

Bank : 0x00
Address : 0x40
Initial value : 0x00
Functions : Pitch control of CH

Bit	Bit name	Functions	R/W	Initial value
7-2	Unused	—	R	000000
1	PITCHEN_SD_CH1	Pitch control of CH1 0: Apply PIT_SD_CH1_L/H (control CH1 independently) 1: Apply PIT_SD_CH0_L/H (control linked to CH0)	R/W	0
0	Unused	—	R	0

For the pitch combinations of PITCHCON_SD, refer "Pitch settings" in the function description.

[Note]
Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0").

- SoundGenerator volume control register（VOLCON _SD）

Bank : 0x00
Address : 0x41
Initial value : 0x00
Functions : Volume control of CH

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3	VOLEN_SD_CH3	Volume control of CH3 0: Apply VOL_SD_CH3_L/H (control CH3 independently) 1: Apply VOL_SD_CH0_L/H (control linked to CH0)	R/W	0
2	VOLEN_SD_CH2	Volume control of CH2 0: Apply VOL_SD_CH2_L/H (control CH2 independently) 1: Apply VOL_SD_CH0_L/H (control linked to CH0)	R/W	0
1	VOLEN_SD_CH1	Volume control of CH1 0: Apply VOL_SD_CH1_L/H (control CH1 independently) 1: Apply VOL_SD_CH0_L/H (control linked to CH0)	R/W	0
0	Unused	—	R	0

For volume combinations, refer to "Volume settings" in the function description.

[Note]
Change the setting while playback is stopped(When all the channel bits of the STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0").

- SoundGenerator playback control register（PLAYCON_SD）

Bank : 0x00
Address : 0x42
Initial value : 0xXX
Functions : Playback control of CH

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3	PLAY_SD_CH3	Playback control of CH3 0：Keep current state 1：Playback	W	x
2	PLAY_SD_CH2	Playback control of CH2 0：Keep current state 1：Playback	W	x
1	PLAY_SD_CH1	Playback control of CH1 0：Keep current state 1：Playback	W	x
0	PLAY_SD_CH0	Playback control of CH0 0：Keep current state 1：Playback	W	x

[Note]
・When the bit of the channel to be played is “1” and the PLAY_SD_MAST bit of the master playback control register is “1”, playback of the channel is started. Read the STAT1 register to check the playback status of each channel.
・To stop playback, set the volume to MUTE in the VOL_SD_CHn registers, check that the fade has ended in the STAT2 register, and then set the STOPCON_SD register. Set the channel bit to be stopped to "1". Not affect the playback status of other channels. When the PLAY_SD_MAST bit in the master playback control register is set to “0”, playback of all channels is stopped immediately.

- SoundGenerator playback stop control register（STOPCON_SD）

Bank :0x00
Address :0x43
Initial value :0xXX
Functions :Playback stop control of CH

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	W	xxxx
3	STOP_SD_CH3	Playback control of CH3 0：Keep current state 1：Stop	W	x
2	STOP_SD_CH2	Playback control of CH2 0：Keep current state 1：Stop	W	x
1	STOP_SD_CH1	Playback control of CH1 0：Keep current state 1：Stop	W	x
0	STOP_SD_CH0	Playback control of CH0 0：Keep current state 1：Stop	W	x

[Note]
・By setting the bit of the channel to stop playback to “1”, playback of that channel is stopped. Playback can be confirmed by checking that the channel bit in the STAT1 register is "0".
・To stop playback, set the volume to MUTE in the VOL_SD_CHn registers, check that the fade has ended in the STAT2 register, and then set the STOPCON_SD register. Set the channel bit to be stopped to "1". Not affect the playback status of other channels. When the PLAY_SD_MAST bit in the master playback control register is set to “0”, playback of all channels is stopped immediately.

- SoundGenerator CHn pitch setting register L（PIT_SD_CHn_L） n=0 to 3

Bank : 0x00
Address : 0x50,0x52,0x54,0x56
Initial value : 0x00
Functions : Pitch setting of CH

Bit	Bit name	Functions	R/W	Initial value
7-0	PIT_SD_CH0_L PIT_SD_CH1_L PIT_SD_CH2_L PIT_SD_CH3_L	Address 0x50 : Pitch setting of CH0 [7:0] Address 0x52 : Pitch setting of CH1 [7:0] Address 0x54 : Pitch setting of CH2 [7:0] Address 0x56 : Pitch setting of CH3 [7:0]	R/W	0x00

- SoundGenerator CHn pitch setting register H（PIT_SD_CHn_H） n=0 to 3

Bank : 0x00
Address : 0x51,0x53,0x55,0x57
Initial value : 0x01
Functions : Pitch setting of CH

Bit	Bit name	Functions	R/W	Initial value
7-2	Unused	—	R	000000
1-0	PIT_SD_CH0_H PIT_SD_CH1_H PIT_SD_CH2_H PIT_SD_CH3_H	Address 0x51 : Pitch setting of CH0 [9:8] Address 0x53 : Pitch setting of CH1 [9:8] Address 0x55 : Pitch setting of CH2 [9:8] Address 0x57 : Pitch setting of CH3 [9:8]	R/W	01

[Note]
・The setting register L is updated by writing to the setting register H. To update the setting register L, write to the setting register H.

The pitch magnification of CH 0 to 1 can be set from 0.0625 times to 3.9960938 times in 0.00390625 times steps.
The pitch magnification of CH 2 to 3 can be set from 0.0625 times to 1 times in 0.00390625 times steps.

CH0 to1 Pitch magnification	PIT_SD_CHn_H[9:8] PIT_SD_CHn_L[7:0] (n=0~1)
3.9960938	0x3FF
3.9921875	0x3FE
3.9882813	0x3FD
3.984375	0x3FC
3.9804688	0x3FB
3.9765625	0x3FA
3.9726563	0x3F9
3.96875	0x3F8
3.9648438	0x3F7
3.9609375	0x3F6
3.9570313	0x3F5
3.953125	0x3F4
3.9492188	0x3F3
3.9453125	0x3F2
3.9414063	0x3F1
3.9375	0x3F0
:	:
3	0x300
:	:
2	0x200
:	:
1	0x100
:	:
0.0625	0x010
Setting prohibited (Set to “0.0625”)	0x00F
:	:
Setting prohibited (Set to “0.0625”)	0x000

CH2 to 3 Pitch magnification	PIT_SD_CHn_H[9:8] PIT_SD_CHn_L[7:0] (n=2~3)
Setting prohibited (Set to “1”)	0x3FF
	0x3FE
	0x3FD
	0x3FC
	0x3FB
	0x3FA
	0x3F9
	0x3F8
	0x3F7
	0x3F6
	0x3F5
	0x3F4
	0x3F3
	0x3F2
	0x3F1
	0x3F0
	:
	0x300
	:
	0x200
	:
1	0x100
:	:
0.0625	0x010
Setting prohibited (Set to “0.0625”)	0x00F
:	:
Setting prohibited (Set to “0.0625”)	0x000

When 0x000 to 0x00F is written, 0x010 is read.
When 0x101 to 0x3FF is written to channels 2 to 3, 0x100 is read.

To set the pitch magnification to 1.1875 times, use the following formula to calculate and write to the register.

1.1875（pitch magnification） × 256 = 304d = 0x130
Write 0x30 to PIT_SD_CHn_L[7:0], and 0x01 to PIT_SD_CHn_H[9:8].

[Note]
・For details on how to set the pitch for each channel, refer "Pitch settings" in the function description.

- Sound Generator CHn volume setting register L（VOL_SD_CHn_L） n=0 to 3

Bank :0x00
Address :0x60,0x62,0x64,0x66
Initial value :0x00
Functions :Volume setting of CH

Bit	Bit name	Functions	R/W	Initial value
7-0	VOL_SD_CH0_L[7:0] VOL_SD_CH1_L[7:0] VOL_SD_CH2_L[7:0] VOL_SD_CH3_L[7:0]	Address 0x60：Volume setting of CH0 [7:0] Address 0x62：Volume setting of CH1 [7:0] Address 0x64：Volume setting of CH2 [7:0] Address 0x66：Volume setting of CH3 [7:0]	R/W	0x00

- Sound Generator CHn volume setting register H（VOL_SD_CHn_H） n=0 to 3

Bank :0x00
Address :0x61,0x63,0x65,0x67
Initial value :0x03
Functions :Volume setting of CH

Bit	Bit name	Functions	R/W	Initial value
7-2	Unused	—	R	000000
1-0	VOL_SD_CH0_H[7:0] VOL_SD_CH1_H[7:0] VOL_SD_CH2_H[7:0] VOL_SD_CH3_H[7:0]	Address 0x61：Volume setting of CH0 [9:8] Address 0x63：Volume setting of CH1 [9:8] Address 0x65：Volume setting of CH2 [9:8] Address 0x67：Volume setting of CH3 [9:8]	R/W	11

[Note]
・The setting register L is updated by writing to the setting register H. To update the setting register L, write to the setting register H.
・For details on how to set the volume for each channel, refer "Volume settings" in the function description.

The volume can be set from MUTE, -76.7 dB to +25.5 dB in 0.1 dB steps.

Volume [dB]	VOL_SD_CHn_H[9:8] VOL_SD_CHn_L[7:0] (n=0 to 3)
MUTE	0x000
-76.7	0x001
-76.6	0x002
-76.5	0x003
:	:
-0.2	0x2FE
-0.1	0x2FF
0	0x300
+0.1	0x301
+0.2	0x302
:	:
+25.3	0x3FD
+25.4	0x3FE
+25.5	0x3FF

When setting the volume to -12dB, calculate using the following formula and write it to the register.
(-12（Volume dB value） ＋ 76.8) × 10 = 648d = 0x288
Write 0x88 to VOL_SD_CHn_L[7: 0] and 0x02 to VOL_SD_CHn_H[9: 8]

◆ SoundGenerator1 related registers list（BANKSEL[3:0]= 0x 1）

- SoundGenerator phrase setting register CH 0（PHRASE_SD_CH0）

Bank : 0x01
Address : 0x40
Initial value : 0x00
Functions : Phrase setting of CH 0

Bit	Bit name	Functions	R/W	Initial value
7-6	Unused	—	R	00
5-0	PHR_CH0[5:0]	Specify the playback phrase for CH 0 000000: Specify phrase 0 000001: Specify phrase 1 : 111110: Specify phrase 62 111111: Specify phrase 63	R/W	000000

- SoundGenerator phrase setting register CH 1（PHRASE_SD_CH1）

Bank : 0x01
Address : 0x41
Initial value : 0x00
Functions : Phrase setting of CH 1

Bit	Bit name	Functions	R/W	Initial value
7-6	Unused	—	R	00
5-0	PHR_CH1[5:0]	Specify the playback phrase for CH 1 000000: Specify phrase 0 000001: Specify phrase 1 : 111110: Specify phrase 62 111111: Specify phrase 63	R/W	000000

- SoundGenerator phrase setting register CH 2（PHRASE_SD_CH2）

Bank : 0x01
Address : 0x42
Initial value : 0x00
Functions : Phrase setting of CH 2

Bit	Bit name	Functions	R/W	Initial value
7-6	Unused	—	R	00
5-0	PHR_CH2[5:0]	Specify the playback phrase for CH 2 000000: Specify phrase 0 000001: Specify phrase 1 : 111110: Specify phrase 62 111111: Specify phrase 63	R/W	000000

- SoundGenerator phrase setting register CH 3（PHRASE_SD_CH3）

Bank : 0x01
Address : 0x43
Initial value : 0x00
Functions : Phrase setting of CH 3

Bit	Bit name	Functions	R/W	Initial value
7-6	Unused	—	R	00
5-0	PHR_CH3[5:0]	Specify the playback phrase for CH 3 000000: Specify phrase 0 000001: Specify phrase 1 : 111110: Specify phrase 62 111111: Specify phrase 63	R/W	000000

- SoundGenerator loop playback control register（LOOPCON_SD）

Bank : 0x01
Address : 0x48
Initial value : 0x0F
Functions : loop playback control

Bit	Bit name	Functions	R/W	Initial value
7-4	Unused	—	R	0000
3	LOOP_SD_CH3	Control loop playback of CH3 0：once playback 1：loop playback	R/W	1
2	LOOP_SD_CH2	Control loop playback of CH2 0：once playback 1：loop playback	R/W	1
1	LOOP_SD_CH1	Control loop playback of CH1 0：once playback 1：loop playback	R/W	1
0	LOOP_SD_CH0	Control loop playback of CH0 0：once playback 1：loop playback	R/W	1

[Note]
・To play once, set "0" to LOOP_SD_CHn bit of this register, and set PLAY_SD_CHn bit of the PLAYCON_SD register. And set the PLAY_SD_MAST bit in the PLAYCON_MAST register to "1". When play once is ended, the PLAY_SD_CHn bit in the PLAYCON_SD register is automatically cleared, but the PLAY_SD_MAST bit is not cleared. Not affect the playback status of other channels.

・To start loop playback, set "1" to LOOP_SD_CHn bit of this register, and set PLAY_SD_CHn bit of PLAYCON_SD register. And set the PLAY_SD_MAST bit in the PLAYCON_MAST register to "1".
・To stop loop playback, set the LOOP_SD_CHn bit of this register to “0” to switch to once playback, stop after play once. At this time as well, when play once is ended, the PLAY_SD_CHn bit in the PLAYCON_SD register is automatically cleared, but the PLAY_SD_MAST bit in the PLAYCON_MAST register is not cleared. Not affect the playback status of other channels.

・To stop playback immediately, set the volume to MUTE in the VOL_SD_CHn registers. Then, after confirming that the fade has ended in the STAT2 register, set STOP_SD_CHn bit in the STOPCON_SD register to “1”. Not affect the playback status of other channels.

◆ EqualizerLch related registers list（BANKSEL[3:0]=0x 2）

• EQ Lch equalizer control register（EQLCON）

Bank : 0x02
Address : 0x40
Initial value : 0x00
Functions : EQ Lch enable control

Bit	Bit name	Functions	R/W	Initial value
7-5	Unused	—	R	000
4	EQL4EN	Band4 equalizer setting 0：disable 1：enable	R/W	0
3	EQL3EN	Band3 equalizer setting 0：disable 1：enable	R/W	0
2	EQL2EN	Band2 equalizer setting 0：disable 1：enable	R/W	0
1	EQL1EN	Band1 equalizer setting 0：disable 1：enable	R/W	0
0	EQL0EN	Band0 equalizer setting 0：disable 1：enable	R/W	0

[Note]
Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0" and the OUT_EN bit of the OUTCON register is "0").

- EQ Lch Band n gain setting register（EQLGAINn） n=0 to 4

Bank : 0x02
Address : 0x41,0x42,0x43,0x44,0x45
Initial value : 0xE7
Functions : EQ Lch Band n gain setting

Bit	Bit name	Functions	R/W	Initial value
7-0	EQLGAIN0	Address 0x41 : Band 0 gain setting [7:0]	R/W	0xE7
	EQLGAIN1	Address 0x42 : Band 1 gain setting [7:0]		
	EQLGAIN2	Address 0x43 : Band 2 gain setting [7:0]		
	EQLGAIN3	Address 0x44 : Band 3 gain setting [7:0]		
	EQLGAIN4	Address 0x45 : Band 4 gain setting [7:0]		

The gain can be set in 0.5 dB steps from + 12 dB to MUTE.

EQLGAINn[7:0] (n=0~4)	Gain
0xFF	+12.0dB
0xFE	+11.5dB
0xFD ~ 0xE9	~(+0.5dB step)~
0xE8	+0.5dB
0xE7	0dB
0xE6	-0.5dB
0xE5 ~ 0x5A	~(+0.5dB step)~
0.59	-71.0dB
0x58	-71.5dB
0x57 ~ 0x00	MUTE

- EQ Lch Band n A0 coefficient setting register L（EQLBANDnA0L） n=0 to 4

Bank : 0x02
Address : 0x46,0x4A,0x4E,0x52,0x56
Initial value : 0x00
Functions : EQ Lch Band n A0 coefficien setting

Bit	Bit name	Functions	R/W	Initial value
7-0	EQLBAND0A0L	Address 0x46 : Band 0 A0 coefficient setting [7:0]	R/W	0x00
	EQLBAND1A0L	Address 0x4A : Band 1 A0 coefficient setting [7:0]		
	EQLBAND2A0L	Address 0x4E : Band 2 A0 coefficient setting [7:0]		
	EQLBAND3A0L	Address 0x52 : Band 3 A0 coefficient setting [7:0]		
	EQLBAND4A0L	Address 0x56 : Band 4 A0 coefficient setting [7:0]		

- EQ Lch Band n A0 coefficient setting register H（EQLBANDnA0H） n=0 to 4

Bank : 0x02
Address : 0x47,0x4B,0x4F,0x53,0x57
Initial value : 0x00
Functions : EQ Lch Band n A0 coefficient setting

Bit	Bit name	Functions	R/W	Initial value
7-0	EQLBAND0A0H	Address 0x47 : Band 0 A0 coefficient setting [15:8]	R/W	0x00
	EQLBAND1A0H	Address 0x4B : Band 1 A0 coefficient setting [15:8]		
	EQLBAND2A0H	Address 0x4F : Band 2 A0 coefficient setting [15:8]		
	EQLBAND3A0H	Address 0x53 : Band 3 A0 coefficient setting [15:8]		
	EQLBAND4A0H	Address 0x57 : Band 4 A0 coefficient setting [15:8]		

[Note]
・The setting register L is updated by writing to the setting register H. To update the setting register L, write to the setting register H.
・By setting the EQLBANDnA0L/H register and EQLBANDnA1L/H register, the center frequency and bandwidth of the equalizer can be set arbitrarily.
・Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0" and the OUT_EN bit of the OUTCON register is "0").
・Generate the setting value using the dedicated tool. Set that value in this register.

- EQ Lch Band n A1 coefficient setting register L（EQLBANDnA1L） n=0 to 4

Bank : 0x02
Address : 0x48,0x4C,0x50,0x54,0x58
Initial value : 0x00
Functions : EQ Lch Band n A1 coefficient setting

Bit	Bit name	Functions	R/W	Initial value
7-0	EQLBAND0A1L	Address 0x48 : Band 0 A1 coefficient setting [7:0]	R/W	0x00
	EQLBAND1A1L	Address 0x4C : Band 1 A1 coefficient setting [7:0]		
	EQLBAND2A1L	Address 0x50 : Band 2 A1 coefficient setting [7:0]		
	EQLBAND3A1L	Address 0x54 : Band 3 A1 coefficient setting [7:0]		
	EQLBAND4A1L	Address 0x58 : Band 4 A1 coefficient setting [7:0]		

- EQ Lch Band n A1 coefficient setting register H（EQLBANDnA1H） n=0 to 4

Bank : 0x02
Address : 0x49,0x4D,0x51,0x55,0x59
Initial value : 0x00
Functions : EQ Lch Band n A1 coefficient setting

Bit	Bit name	Functions	R/W	Initial value
7-0	EQLBAND0A1H	Address 0x49 : Band 0 A1 coefficient setting [15:8]	R/W	0x00
	EQLBAND1A1H	Address 0x4D : Band 1 A1 coefficient setting [15:8]		
	EQLBAND2A1H	Address 0x51 : Band 2 A1 coefficient setting [15:8]		
	EQLBAND3A1H	Address 0x55 : Band 3 A1 coefficient setting [15:8]		
	EQLBAND4A1H	Address 0x59 : Band 4 A1 coefficient setting [15:8]		

[Note]
・The setting register L is updated by writing to the setting register H. To update the setting register L, write to the setting register H.
・By setting the EQLBANDnA0L/H register and EQLBANDnA1L/H register, the center frequency and bandwidth of the equalizer can be set arbitrarily.
・Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0" and the OUT_EN bit of the OUTCON register is "0").
・Generate the setting value using the dedicated tool. Set that value in this register.

◆ EqualizerRch related registers list（BANKSEL[3:0]=0x 3）

• EQ Rch equalizer control register（EQRCON）

Bank : 0x03
Address : 0x40
Initial value : 0x00
Functions : EQ Rch enable control

Bit	Bit name	Functions	R/W	Initial value
7-5	Unused	—	R	000
4	EQR4EN	Band4 equalizer setting 0：disable 1：enable	R/W	0
3	EQR3EN	Band3 equalizer setting 0：disable 1：enable	R/W	0
2	EQR2EN	Band2 equalizer setting 0：disable 1：enable	R/W	0
1	EQR1EN	Band1 equalizer setting 0：disable 1：enable	R/W	0
0	EQR0EN	Band0 equalizer setting 0：disable 1：enable	R/W	0

[Note]
・Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0" and the OUT_EN bit of the OUTCON register is "0").

- EQ Rch Band n gain setting register（EQRGAINn） n=0 to 4

Bank : 0x03
Address : 0x41,0x42,0x43,0x44,0x45
Initial value : 0xE7
Functions : EQ Rch Band n gain settng

Bit	Bit name	Functions	R/W	Initial value
7-0	EQRGAIN0	Address 0x41 : Band 0 gain setting [7:0]	R/W	0xE7
	EQRGAIN1	Address 0x42 : Band 1 gain setting [7:0]		
	EQRGAIN2	Address 0x43 : Band 2 gain setting [7:0]		
	EQRGAIN3	Address 0x44 : Band 3 gain setting [7:0]		
	EQRGAIN4	Address 0x45 : Band 4 gain setting [7:0]		

The gain can be set in 0.5 dB steps from + 12 dB to MUTE.

EQRGAINn[7:0] (n=0~4)	Gain
0xFF	+12.0dB
0xFE	+11.5dB
0xFD ~ 0xE9	~(+0.5dB step)~
0xE8	+0.5dB
0xE7	0dB
0xE6	-0.5dB
0xE5 ~ 0x5A	~(+0.5dB step)~
0.59	-71.0dB
0x58	-71.5dB
0x57 ~ 0x00	MUTE

- EQ Rch Band n A0 coefficient setting register L（EQRBANDnA0L） n=0 to 4

Bank : 0x03
Address : 0x46,0x4A,0x4E,0x52,0x56
Initial value : 0x00
Functions : EQ Rch Band n A0 coefficient setting

Bit	Bit name	Functions	R/W	Initial value
7-0	EQRBAND0A0L	Address 0x46 : Band 0 A0 coefficient setting [7:0]	R/W	0x00
	EQRBAND1A0L	Address 0x4A : Band 1 A0 coefficient setting [7:0]		
	EQRBAND2A0L	Address 0x4E : Band 2 A0 coefficient setting [7:0]		
	EQRBAND3A0L	Address 0x52 : Band 3 A0 coefficient setting [7:0]		
	EQRBAND4A0L	Address 0x56 : Band 4 A0 coefficient setting [7:0]		

- EQ Rch Band n A0 coefficient setting register H（EQRBANDnA0H） n=0 to 4

Bank : 0x03
Address : 0x47,0x4B,0x4F,0x53,0x57
Initial value : 0x00
Functions : EQ Rch Band n A0 coefficient setting

Bit	Bit name	Functions	R/W	Initial value
7-0	EQRBAND0A0H	Address 0x47 : Band 0 A0 coefficient setting [15:8]	R/W	0x00
	EQRBAND1A0H	Address 0x4B : Band 0 A0 coefficient setting [15:8]		
	EQRBAND2A0H	Address 0x4F : Band 0 A0 coefficient setting [15:8]		
	EQRBAND3A0H	Address 0x53 : Band 0 A0 coefficient setting [15:8]		
	EQRBAND4A0H	Address 0x57 : Band 0 A0 coefficient setting [15:8]		

[Note]
・The setting register L is updated by writing to the setting register H. To update the setting register L, write to the setting register H.
・By setting the EQRBANDnA0L/H register and EQRBANDnA1L/H register, the center frequency and bandwidth of the equalizer can be set arbitrarily.
・Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0" and the OUT_EN bit of the OUTCON register is "0").
・Generate the setting value using the dedicated tool. Set that value in this register.

- EQ Rch Band n A1 coefficient setting register L（EQRBANDnA1L） n=0 to 4

Bank : 0x03
Address : 0x48,0x4C,0x50,0x54,0x58
Initial value : 0x00
Functions : EQ Rch Band n A1 coefficient L setting

Bit	Bit name	Functions	R/W	Initial value
7-0	EQRBAND0A1L	Address 0x48 : Band 0 A1 coefficient setting [7:0]	R/W	0x00
	EQRBAND1A1L	Address 0x4C : Band 1 A1 coefficient setting [7:0]		
	EQRBAND2A1L	Address 0x50 : Band 2 A1 coefficient setting [7:0]		
	EQRBAND3A1L	Address 0x54 : Band 3 A1 coefficient setting [7:0]		
	EQRBAND4A1L	Address 0x58 : Band 4 A1 coefficient setting [7:0]		

- EQ Rch Band n A1 coefficient setting register H（EQRBANDnA1H） n=0 to 4

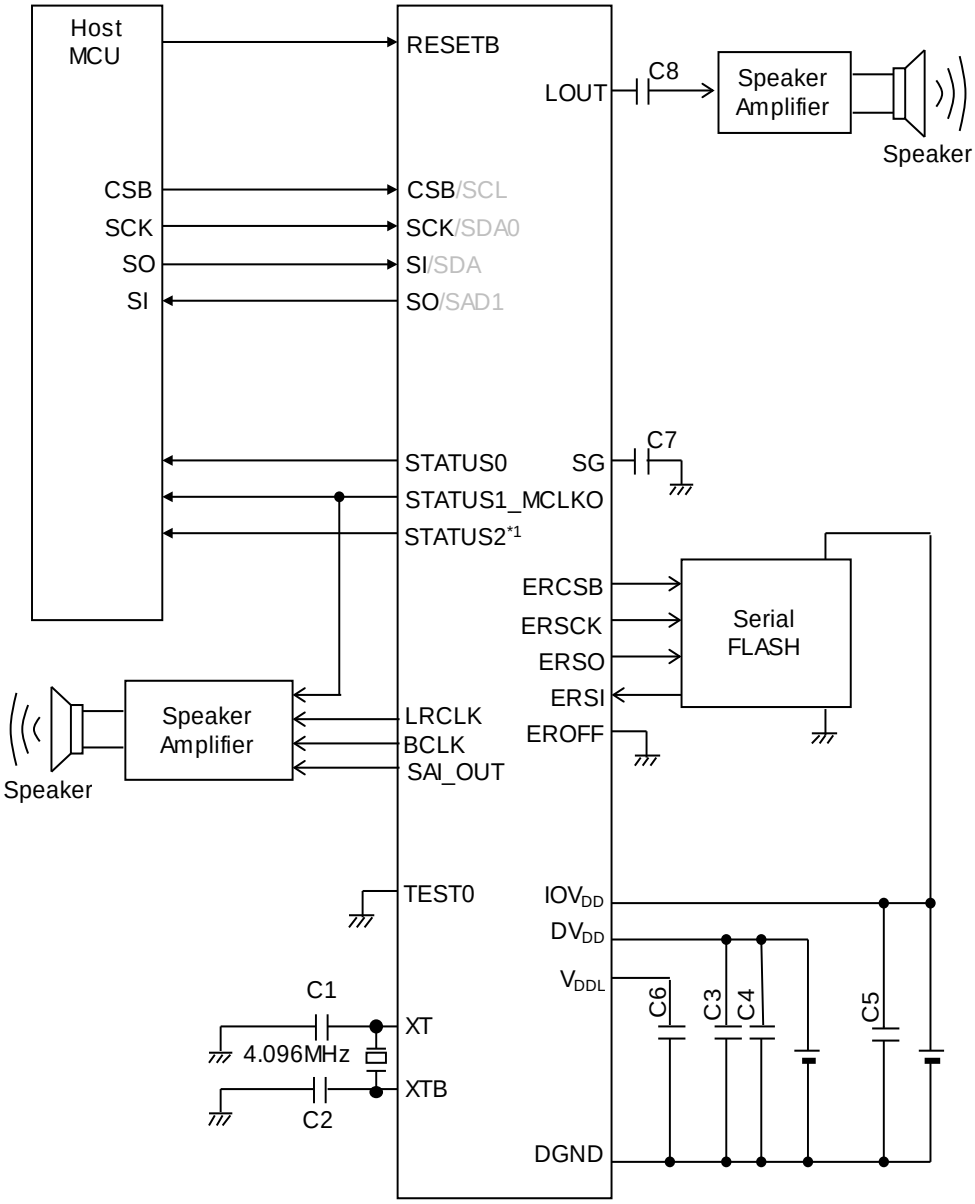
Bank : 0x03
Address : 0x49,0x4D,0x51,0x55,0x59
Initial value : 0x00
Functions : EQ Rch Band n A1 coefficient setting

Bit	Bit name	Functions	R/W	Initial value
7-0	EQRBAND0A1H	Address 0x49 : Band 0 A1 coefficient setting [15:8]	R/W	0x00
	EQRBAND1A1H	Address 0x4D : Band 1 A1 coefficient setting [15:8]		
	EQRBAND2A1H	Address 0x51 : Band 2 A1 coefficient setting [15:8]		
	EQRBAND3A1H	Address 0x55 : Band 3 A1 coefficient setting [15:8]		
	EQRBAND4A1H	Address 0x59 : Band 4 A1 coefficient setting [15:8]		

[Note]
・The setting register L is updated by writing to the setting register H. To update the setting register L, write to the setting register H.
・By setting the EQRBANDnA0L/H register and EQRBANDnA1L/H register, the center frequency and bandwidth of the equalizer can be set arbitrarily.
・Change the setting while playback is stopped(When all the channel bits of STAT1 register are "0" or when the PLAY_SD_MAST bit of the PLAYCON_MAST register is "0" and the OUT_EN bit of the OUTCON register is "0").
・Generate the setting value using the dedicated tool. Set that value in this register.

■ Application Circuit

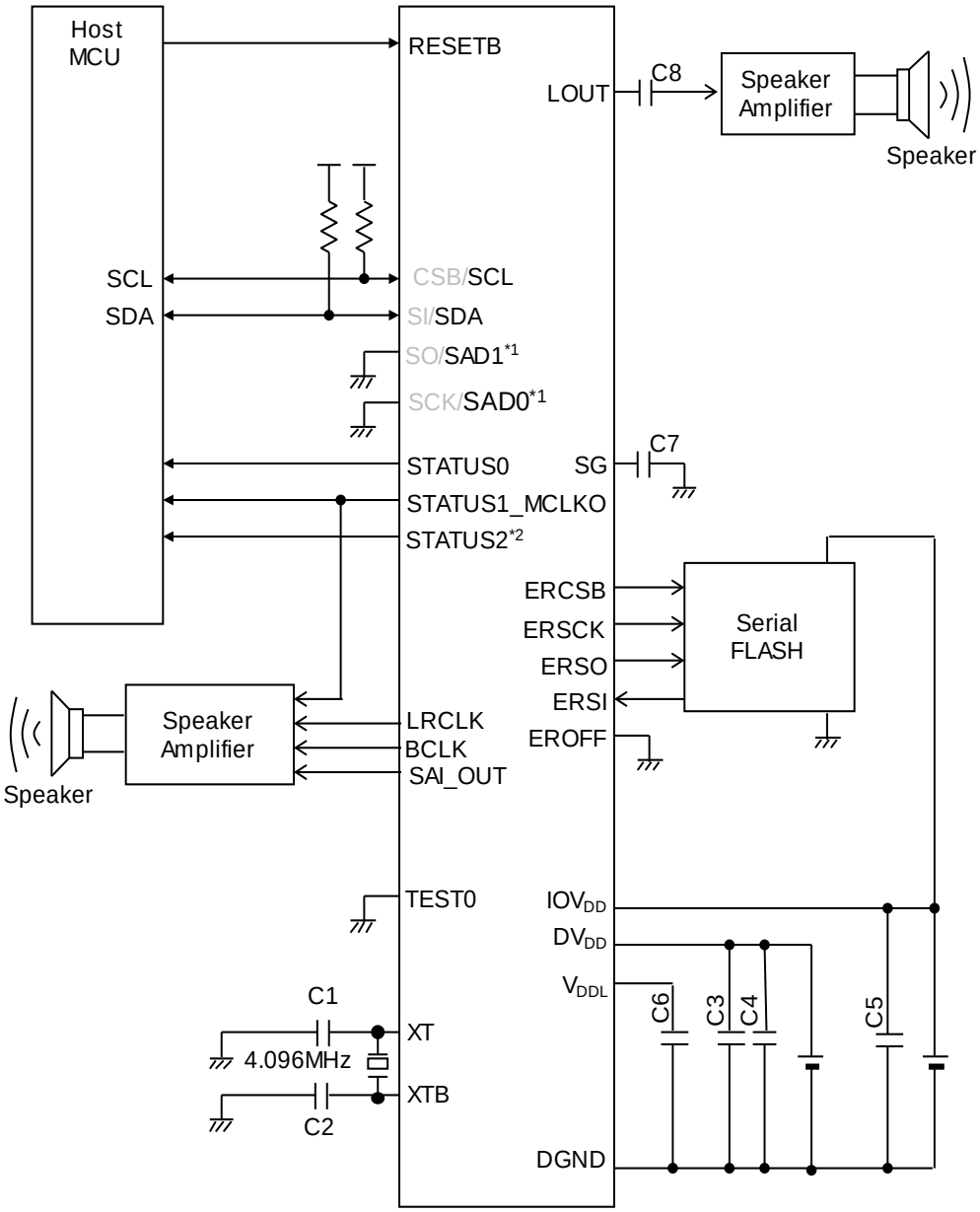
● Clock Synchronous Serial Interface



*1 : 24PIN version has no pin

Pin	Symbol	Recommended Constant
DV_{DD}	C3	3.3μF±20%
DV_{DD}	C4	0.1μF±20%
IOV_{DD}	C5	1μF±20%
V_{DDL}	C6	1uF±20%
SG	C7	0.1uF±20%
LOUT	C8	0.1uF±20%

● I^2C Interface (Slave)



*1 : When 100_0101 is selected as the slave address
*2 : 24PIN version has no pin

Pin	Symbol	Recommended Constant
DV_{DD}	C3	3.3μF±20%
DV_{DD}	C4	0.1μF±20%
IOV_{DD}	C5	1μF±20%
V_{DDL}	C6	1uF±20%
SG	C7	0.1uF±20%
LOUT	C8	0.1uF±20%

■ Recommended ceramic resonator

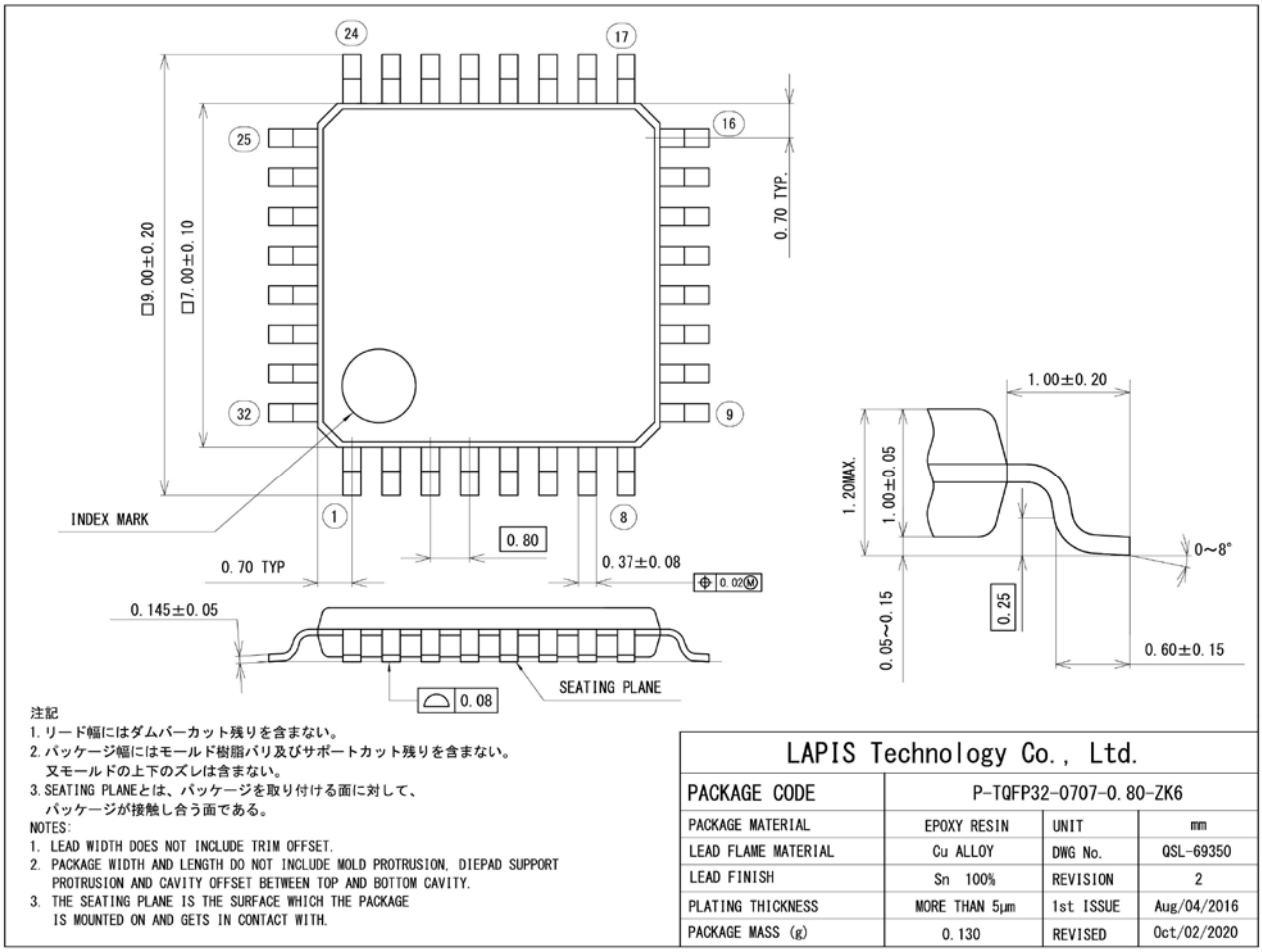
Recommended ceramic resonators are shown below.

● MURATA Corporation

Frequency [Hz]	Product Name	Built-in load capacity [pF]
4M	CSTCR4M00G55B-R0	39
4.096M	CSTCR4M09G55B-R0	

■ Package Dimensions

● ML22120TB （32pin TQFP）



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θJa) changes with the size and the number of layers of a substrate.

PCB	（W/L/t＝ 76.2 / 114.3 / 1.6 （mm））
PCB Layer	JEDEC 4 layers
Air cooling condition	No wind（0m/sec）
Heat resistance value（θJa）	59.04 [°C /W]
Chip power consumption PMax OutputPower	0.06 [W]

The TjMax of this LSI is 130 °C. TjMax is expressed by the following formula.

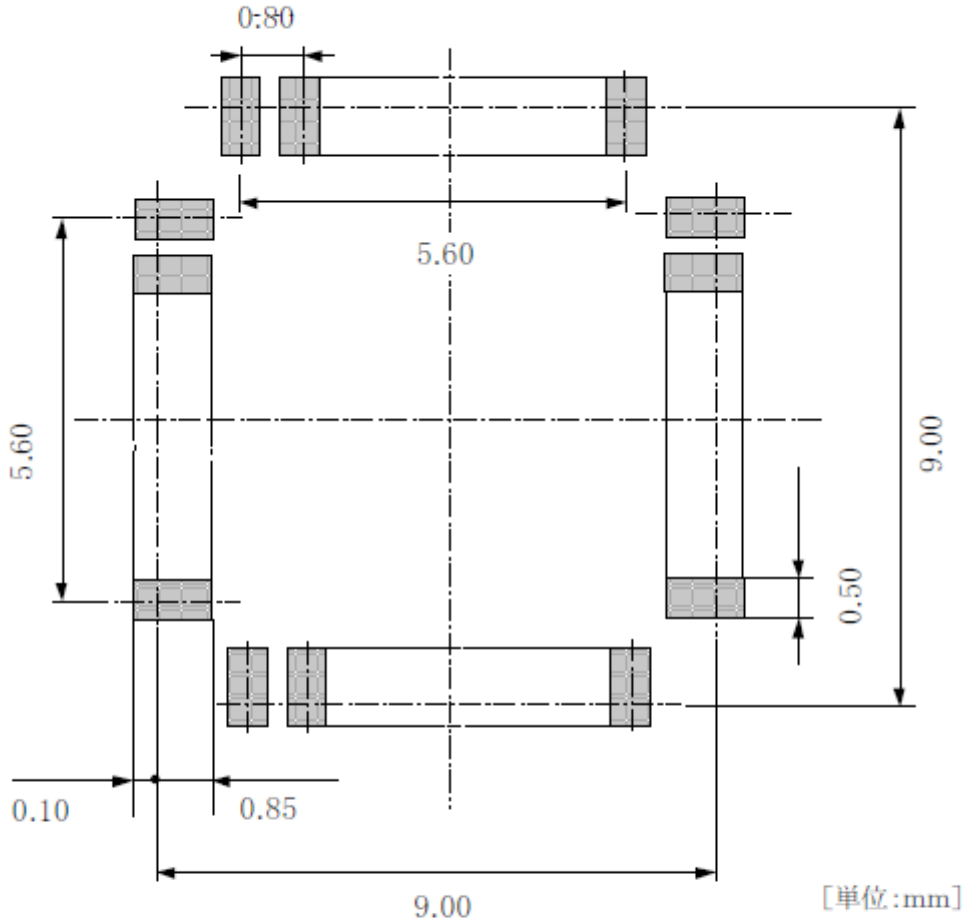
TjMax=TaMax + θJa×PMax

The mounting area for package lead soldering to PC boards is shown on the next page.

半田付け部端子存在範囲図

Figure of reference

Mounting area for package lead soldering to PC boards



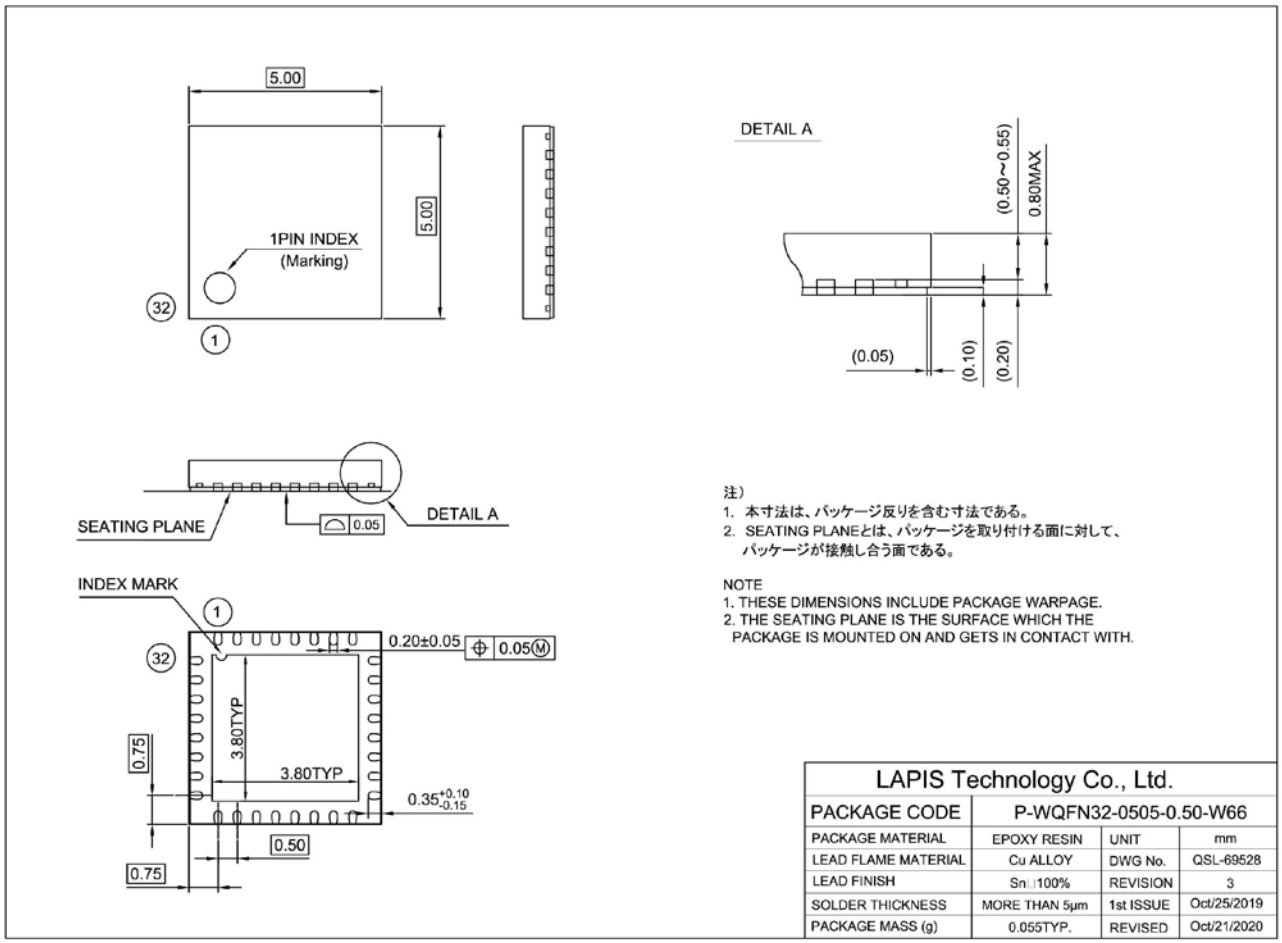
実装基板のフットパターンの設計の際には、実装の容易さ、接続の信頼性、配線の引き回し、半田ブリッジ発生のないことなどを十分考慮してください。

フットパターンの最適な設計は基板材質、使用する半田ペースト種類、厚み、半田付け方法などによって変わってきます。従って、本パッケージの端子の存在し得る範囲を「半田付け部端子存在範囲図」として示しますので、フットパターン設計の参考資料としてください。

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts,reliability, wiring,and elimination of solder bridges.

The optimum design for the foot pattern varies with the materials of the substrate,the sort and thickness of used soldering paste,and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering to PC boards.

● ML22120GD （32pin WQFN）



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN32-0505-0.50-W66		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69528
LEAD FINISH	Sn□100%	REVISION	3
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Oct/25/2019
PACKAGE MASS (g)	0.055TYP.	REVISED	Oct/21/2020

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θJa) changes with the size and the number of layers of a substrate.

PCB	（W/L/t＝ 76.2 / 114.3 / 1.6（mm））
PCB Layer	JEDEC 4 layers
Air cooling condition	No wind（0m/sec）
Heat resistance value（θJa）	31.76 [°C /W]
Chip power consumption PMax OutputPower	0.06 [W]

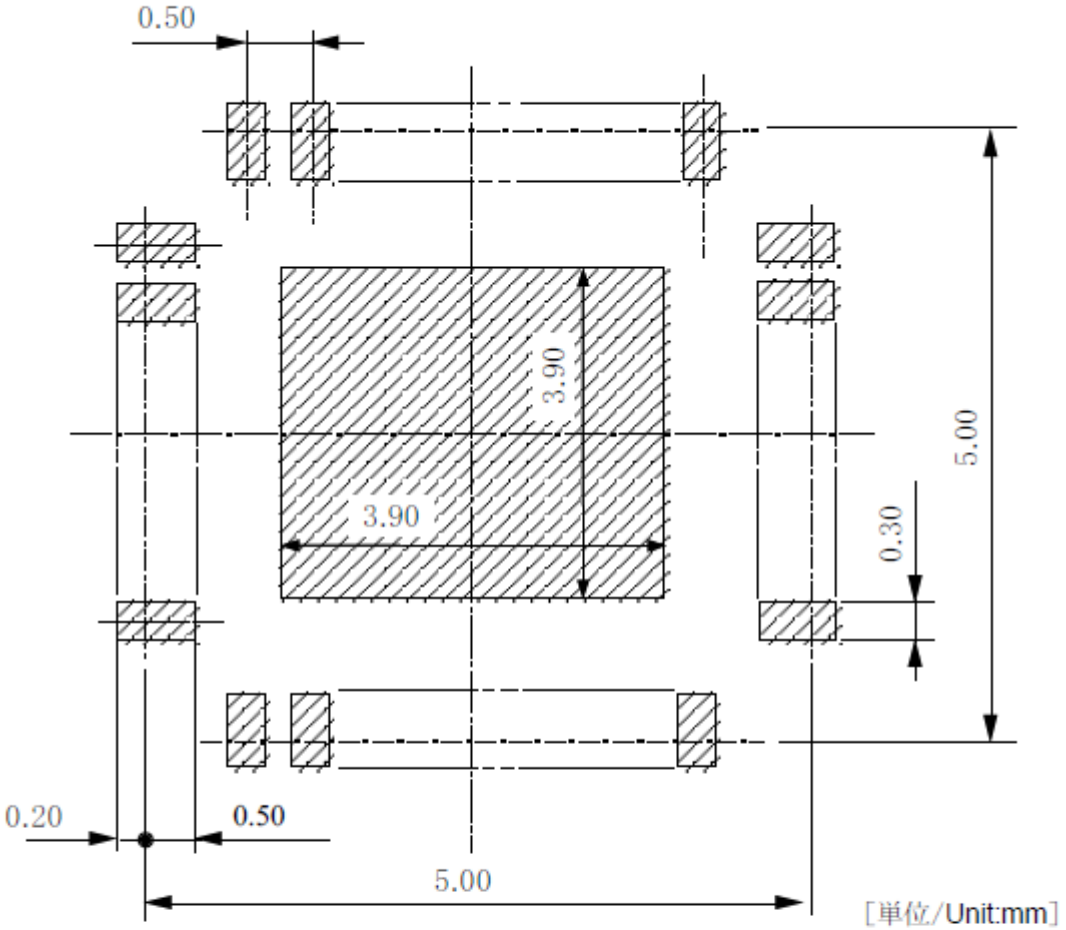
The TjMax of this LSI is 130 °C. TjMax is expressed by the following formula.
TjMax=TaMax + θJa×PMax

The heat sink area of the LSI solder open or GND on the board.
The mounting area for package lead soldering to PC boards is shown on the next page.

Figure of reference

半田付け端子存在範囲図

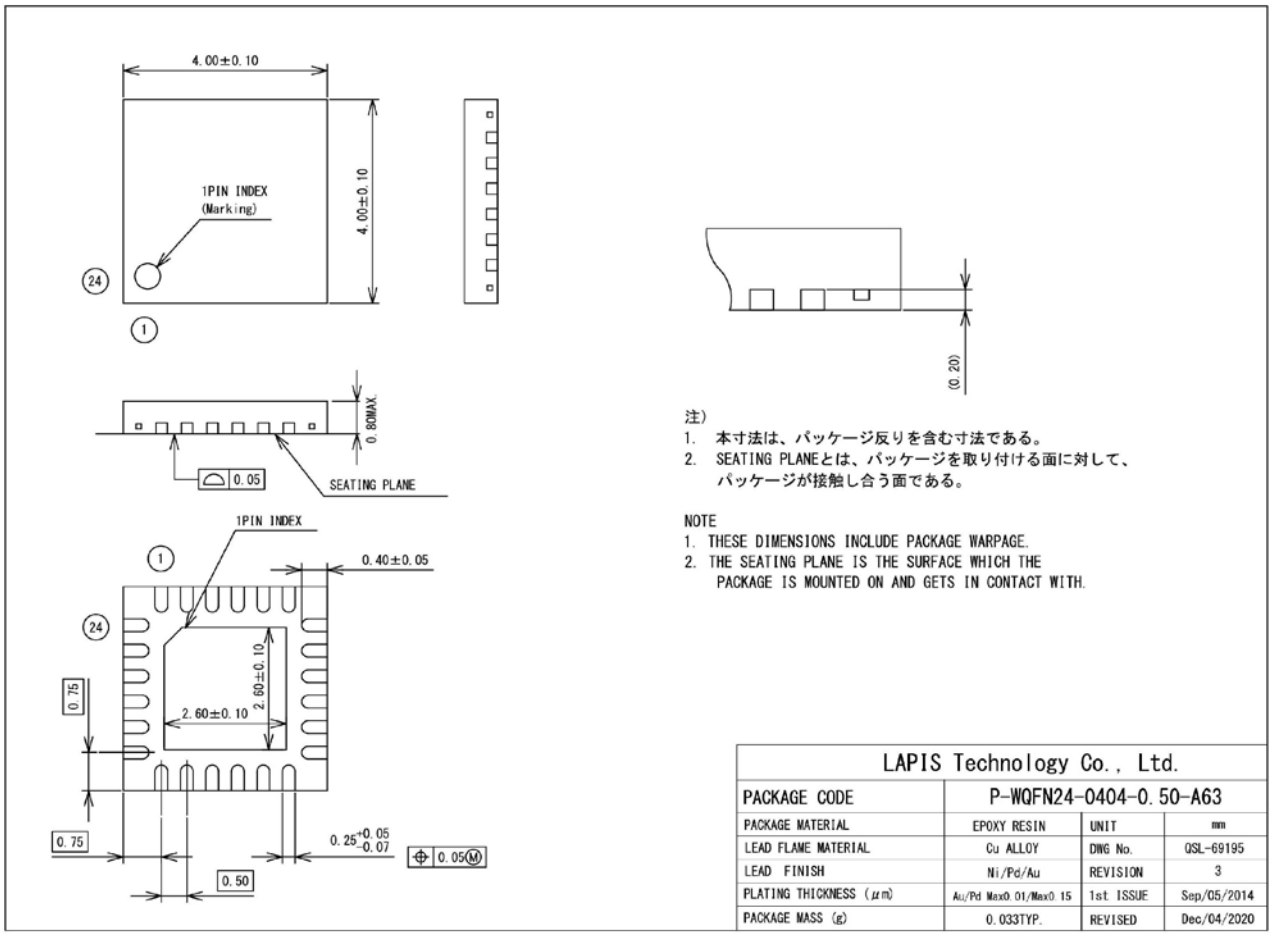
Mounting area for package lead soldering to PC boards



実装基板のフットパターンの設計の際には、実装の容易さ、接続の信頼性、配線の引き回し、半田ブリッジ発生のないことなどを十分考慮してください。
フットパターンの最適な設計は基板材質、使用する半田ペースト種類、厚み、半田付け方法などによって変わってきます。従って、本パッケージの端子の存在し得る範囲を「半田付け部端子存在範囲図」として示しますので、フットパターン設計の参考資料としてください。

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts,reliability, wiring,and elimination of solder bridges.
The optimum design for the foot pattern varies with the materials of the substrate,the sort and thickness of used soldering paste,and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering to PC boards.

● ML22120GP （24pin WQFN）



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN24-0404-0.50-A63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69195
LEAD FINISH	Ni/Pd/Au	REVISION	3
PLATING THICKNESS (μm)	Au/Pd Max0.01/Max0.15	1st ISSUE	Sep/05/2014
PACKAGE MASS (g)	0.033TYP.	REVISED	Dec/04/2020

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θJa) changes with the size and the number of layers of a substrate.

PCB	（W/L/t＝ 76.2 / 114.3 / 1.6 （mm））
PCB Layer	JEDEC 4 layers
Air cooling condition	No wind（0m/sec）
Heat resistance value（θJa）	36.53 [°C /W]
Chip power consumption PMax OutputPower	0.06 [W]

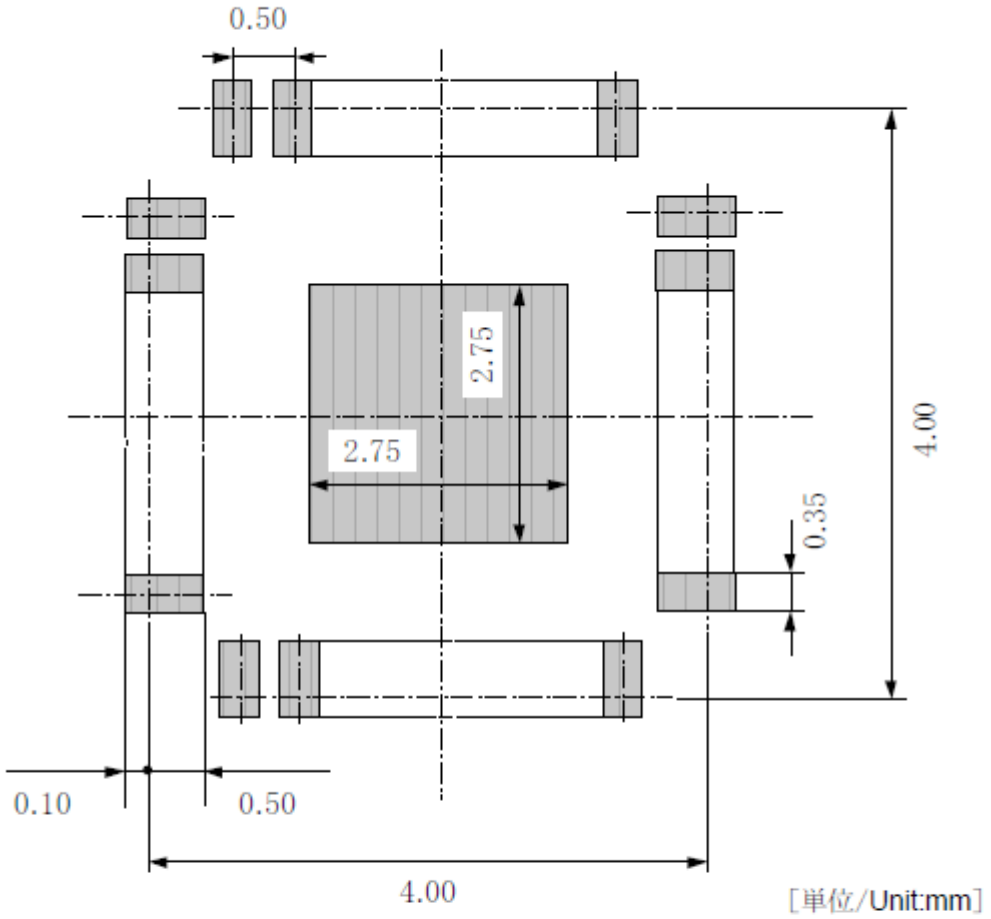
The TjMax of this LSI is 130 °C. TjMax is expressed by the following formula.
TjMax=TaMax + θJa×PMax

The heat sink area of the LSI solder open or GND on the board.
The mounting area for package lead soldering to PC boards is shown on the next page.

半田付け端子存在範囲図

Figure of reference

Mounting area for package lead soldering to PC boards



実装基板のフットパターンの設計の際には、実装の容易さ、接続の信頼性、配線の引き回し、半田ブリッジ発生のないことなどを十分考慮してください。
フットパターンの最適な設計は基板材質、使用する半田ペースト種類、厚み、半田付け方法などによって変わってきます。従って、本パッケージの端子の存在し得る範囲を「半田付け部端子存在範囲図」として示しますので、フットパターン設計の参考資料としてください。

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts,reliability, wiring,and elimination of solder bridges.
The optimum design for the foot pattern varies with the materials of the substrate,the sort and thickness of used soldering paste,and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering to PC boards.

■ Revision history

Document No.	Date	Page		Description
		Previous edition	Current edition	
FEDL22120-01	Mar 1, 2023	-	-	Formal 1st edition.

Notes

1) The information contained herein is subject to change without notice.

2) When using LAPIS Semiconductor Products, refer to the latest product information (data sheets, user's manuals, application notes, etc.), and ensure that usage conditions (absolute maximum ratings, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. You are responsible for evaluating the safety of the final products or systems manufactured by you.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Technology or any third party with respect to LAPIS Technology Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples, etc.). Therefore LAPIS Technology shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

5) The Products are intended for use in general electronic equipment (AV/OA devices, communication, consumer systems, gaming/entertainment sets, etc.) as well as the applications indicated in this document. For use of our Products in applications requiring a high degree of reliability (as exemplified below), please be sure to contact a LAPIS Technology representative and must obtain written agreement: transportation equipment (cars, ships, trains, etc.), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems, etc. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us. Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc.

6) The Products specified in this document are not designed to be radiation tolerant.
4
7) LAPIS Technology has used reasonable care to ensure the accuracy of the information contained in this document. However, LAPIS Technology does not warrant that such information is error-free and LAPIS Technology shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

8) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. LAPIS Technology shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

9) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

10) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or LAPIS Technology's Products.

11) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Technology.

(Note) "LAPIS Technology" as used in this document means LAPIS Technology Co., Ltd.

LAPIS Technology Co.,Ltd.

2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
https://www.lapis-tech.com/en/