

650V GaN Power Transistor (FET)

Features

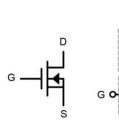
- Easy to use, compatible with standard gate drivers
- Excellent Q_G x R_{DS(on)} figure of merit (FOM)
- Low Q_{RR} , no free-wheeling diode required
- Low switching loss
- RoHS compliant and Halogen-free

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- High efficiency power supplies
- Telecom and datacom
- Automotive
- Servo motors

Packaging

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D		
	G	



Product Summary

 V_{DSS}

R_{DS(on), typ}

Q_{G, typ}

 $Q_{\text{RR, typ}}$

650

120

21

26

Schematic Symbol

Cascode Device Structure

V

mΩ

nC

nC

D

Part Number	Package	Packaging	Base QTY
RX65T125HS2A	DFN 8 x 8	Tape and Reel	2500

Maximum ratings, at $T_c=25 \$ °C, unless otherwise specified

Symbol	Parameter	Limit Value	Unit	
Continuous drain current @T _c =25℃			18	А
Ι _D	Continuous drain current @T _c =100°	11.5	А	
	Pulsed drain current @T _c =25℃ (puls	e width: 10us)	80	А
I _{DM}	Pulsed drain current @T _c =150℃ (pul	se width: 10us)	58	А
V _{DSS}	Drain to source voltage (T₁ = -55℃ to 150℃)		650	V
V _{TDSS}	Transient drain to source voltage ^a	800	V	
V _{GSS}	Gate to source voltage	±20	V	
P _D	Maximum power dissipation @T _c =25℃		67.5	W
T _c		Case	-55 to 150	°C
Tj	Operating temperature	Junction	-55 to 150	°C
Ts	Storage temperature	-55 to 150	°C	
T _{CSOLD}	Soldering peak temperature		260	°C



Thermal Resistance

Symbol	Parameter	Typical	Unit
Rojc	Junction-to-case	1.85	℃/W
Roja	Junction-to-ambient ^b	50	℃/W

Notes:

- a. Off-state spike duty cycle < 0.01, spike duration < 2us
- b. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70μm thickness)



Electrical Parameters, at T_J=25 ℃, unless otherwise specified

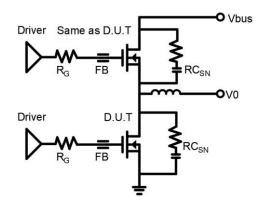
Symbol	Min	Тур	Max	Unit	Test Conditions
Forward Chara	cteristics	1	1	4	
V _{DSS-MAX}	650	-	-	V	V _{GS} =0V
BV _{DSS}	-	1000	-	V	V _{GS} =0V, I _{DSS} =250μA
$V_{GS(th)}$	3	4	5	V	$V_{DS}=V_{GS}$, $I_D=500\mu A$
- (-	120	150	mΩ	V _{GS} =8V, I _D =4A, T _J =25℃
$R_{DS(on)}$ c	-	240	-	- 11152	V _{GS} =8V, I _D =4A, T _J =150℃
1	-	5	20	μA	V _{DS} =700V, V _{GS} =0V, T _J =25℃
I _{DSS}	-	50	-	μA	V _{DS} =700V, V _{GS} =0V, T _J =150℃
1	-	-	150	nA	V _{GS} =20V
I _{GSS}	-	-	-150	nA	V _{GS} =-20V
C _{ISS}	-	606	-	pF	
C _{OSS}	-	40	-	pF	V _{GS} =0V, V _{DS} =650V, f=1MHz
C _{RSS}	-	3	-	pF	
C _{O(er)}	-	57	-	pF	
C _{O(tr)}	-	109	-	pF	- V _{GS} =0V, V _{DS} =0 - 650V
Q _G	-	21	-		
Q _{GS}	-	6.7	-	nC	V _{DS} =400V, V _{GS} =0 - 12V, I _D =10A
Q _{GD}	-	5	-	-	
t _{D(on)}	-	44	-		
t _R	-	16	-	-	
t _{D(off)}	-	40	-	ns	V_{DS} =400V, V_{GS} =0 - 12V, I_{D} =10A, R_{G} =40 Ω
t _F	-	12	-	_	
Reverse Chara	cteristics	1	1	1	
	-	1.3	-		V _{GS} =0V, I _S =5A, T _J =25℃
V _{SD}	-	1.9	-	v	V _{GS} =0V, I _S =10A, T _J =25℃
	-	3	-	1	V _{GS} =0V, I _S =10A, T _J =150℃
t _{RR}	-	16	_	ns	
Q _{RR}		26		nC	I _s =10A, V _{GS} =0V, d _i /d _t =1000A/us, V _{DD} =400V
~ KK		20		iic	

Notes:

C. Dynamic on-resistance; see Figure 17 and 18 for test circuit and configurations



Circuit Implementation



Recommended Single Ended Drive Circuit

Recommended gate drive: (0 V, 12 V) with $R_{G(tot)}$ = 34 Ω , where $R_{G(tot)}$ = R_{G} + R_{Driver}

Gate Ferrite Bead	Gate Resistance1	RC Snubber	
(FB)	(R _G)	(RC _{SN})	
MPZ1608S471ATA00	33 Ω	69 pF + 15 Ω	

Notes:

- d. RCsn should be placed as close as possible to the drain pin
- e. The layout and wiring of the drive circuit should be as short as possible



Typical Characteristics, at $T_c=25 \$ °C, unless otherwise specified

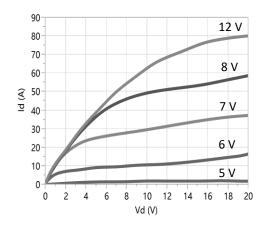
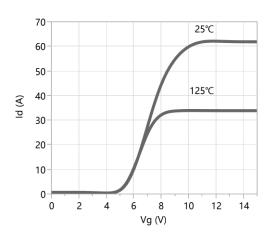
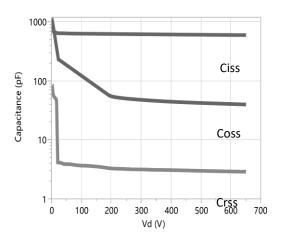


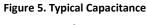
Figure 1. Typical Output Characteristics T_J=25℃











V_{GS}=0V, f=1MHZ

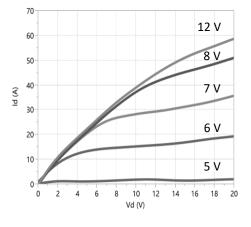


Figure 2. Typical Output Characteristics T₁=150℃

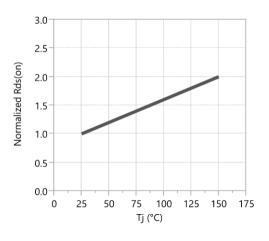
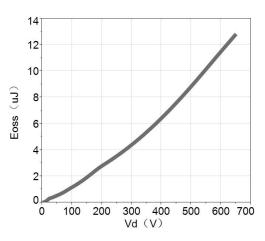


Figure 4. Normalized On-resistance

I_D=4A, V_{GS}=12V





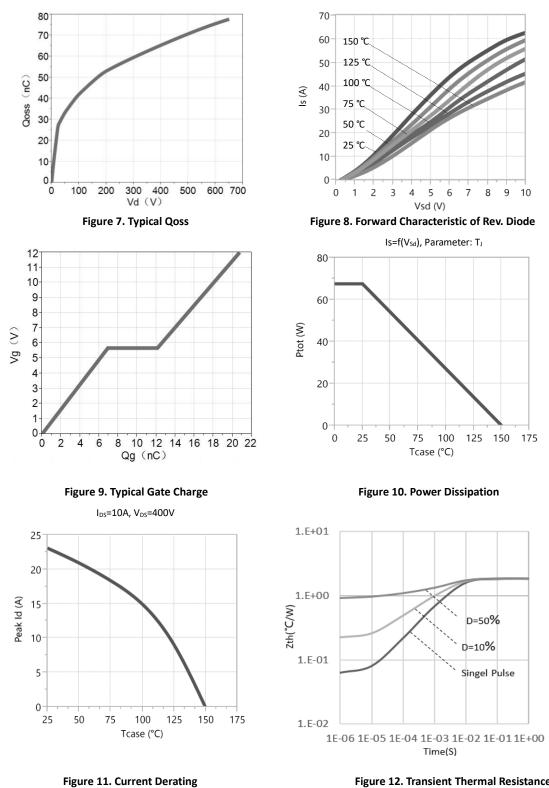
Rev. 1.2

5 / 11 This datasheet is subject to change without notice.

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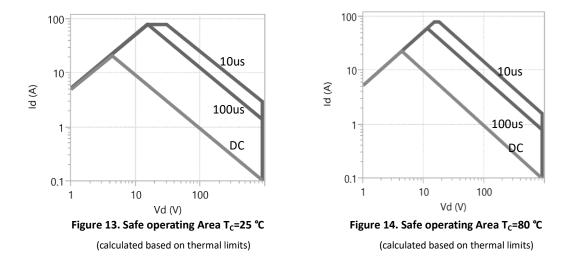


Typical Characteristics, at T_c=25 ℃, unless otherwise specified





Typical Characteristics, at $T_c=25 \$ °C, unless otherwise specified





Test Circuits and Waveforms

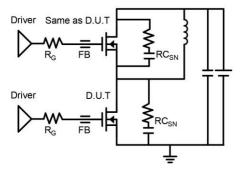


Figure 15. Switching Time Test Circuit

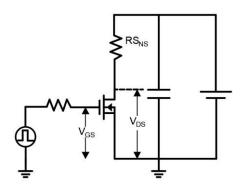


Figure 17. Dynamic R_{DS(on)} Test Circuit

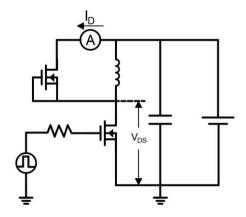


Figure 19. Diode Characteristic Test Circuit

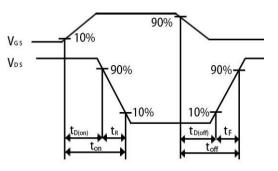


Figure 16. Switching Time Waveform

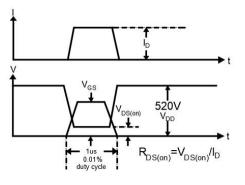


Figure 18. Dynamic R_{DS(on)} Waveform

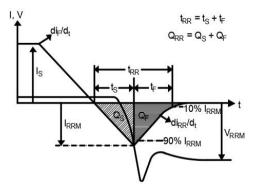


Figure 20. Diode Recovery Waveform



Design Considerations

Fast switching GaN device can reduce power conversion losses, and thus enable high frequency operations. Certain PCB design rules and instructions, however, need to be followed to take full advantages of fast switching GaN devices.

Before evaluating Runxin Micro's GaN devices, please refer to the table below which provides some practical rules that should be followed during the evaluation.

DO	DO NOT
Make sure the traces are as short as possible for both	Using Runxin Micro's devices in GDS board layouts
drive and power loops to minimize parasitic inductance	
Use the test tool with the shortest inductive loop, and	Use differential mode probe or probe ground clip with
make sure test points should be placed close enough	long wires
Minimize the lead length of TO packages when	Use long traces in drive circuit, or long lead length of
installing them to PCB	the devices

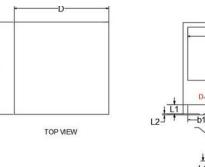
When Evaluating Runxin Micro's GaN Devices:



Package Outline

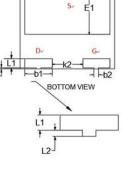
A2

G.



A1

D.



D1

k1

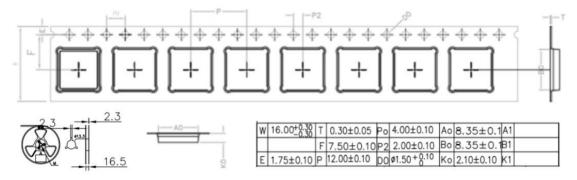
DFN 8 x 8mm (HS) Package

Combal	Dimensions in Millimeters				
Symbol	MIN	NOM	MAX		
A1	0.850	0.900	0.950		
A2	0.185	0.203	0.230		
D	7.000	8.000	9.000		
E	7.950	8.000	8.050		
D1	7.050	7.200	7.350		
E1	4.450	4.600	4.750		
K1	0.375	0.400	0.425		
K2	2.575	2.600	2.625		
b1	2.250	2.300	2.350		
b2	0.375	0.400	0.425		
L1	0.700	0.800	0.900		
L2	0.075	0.100	0.125		

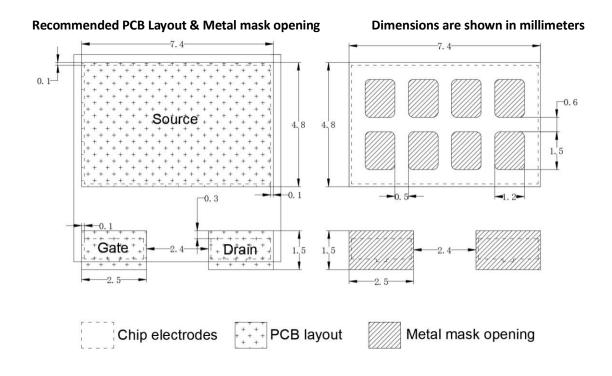
Tape and Reel Information

SIDE VIEW

Dimensions are shown in millimeters







Revision History

Version	Date	Change(s)
1.0	06/24/2021	Release formal datasheet
1.1	10/27/2022	Revise $C_{O(er)}$, $C_{O(tr)}$, Q_{G} , Q_{GS} , Q_{GD}
1.2	02/01/2023	Add BV _{DSS}

单击下面可查看定价,库存,交付和生命周期等信息

>>Runxin Micro