High Precision, Low Noise, Current Sensor IC With OCD

## 1 Features

- End-of-line programmable sensor
- Wide bandwidth up to 400 kHz
- Very short response time (2μs)
- High linearity down to ±0.5% full scale
- Measurement range up to 4500Gs
- Low thermal drift
- Offset drift (<5mV)
- Sensitivity drift (<1%)
- Supply voltage from 4.5 to 5.5 V
- AEC-Q100-Grade 0 Automotive Qualification
- Internal over-current detection
- 24 Bit customer ID
- Diagnostic capability
- OVD
- Broken wire
- SIP4-VB and SIP3-VB package

## 2 Applications

- High Voltage Traction Motor Inverter
- Smart Battery Junction Boxes
- Smart Fuse Overcurrent Detection
- DCDC Converter

## 3 Description

The SC4663 is a monolithic programmable Hall sensor IC featuring the planar Hall technology, which is sensitive to the flux density applied orthogonally to the IC surface. The sensor provides an output signal proportional to the applied magnetic flux density and is preferably suited for current measurement.

The transfer characteristic of the SC4663 is factory trimmed over temperature, and is programmable (offset, sensitivity, filtering, internal over-current threshold) during end-of-line customer calibration. With up to 400 kHz bandwidth and fast response time, it is particularly adapted for high speed applications such as inverters and converters where fast response time due to fast switching is required. The output clamping levels and on-chip filtering are also programmable as a function of application needs.

The sensor is designed for automotive and hostile industrial applications and operates with typically 5 V supply voltage in the ambient temperature range from -40 up to 150 ℃. The SC4663 is available in the very small leaded package SIP4 and SIP3.

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# Catalog



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# 4 Revision History

| Version | Date | Change | Name |
|---|---|---|---|
| Rev 1.0 | | | |

# 5 Device Information

| Part Number | Temperature | Package | Packing Form | OCD | Marking |
|---|---|---|---|---|---|
| SC4663 | L | SIP4-VB | Bulk | 120%FS | 4663 |
| SC4663 | L | SIP3-VB | Bulk | -- | 4663 |

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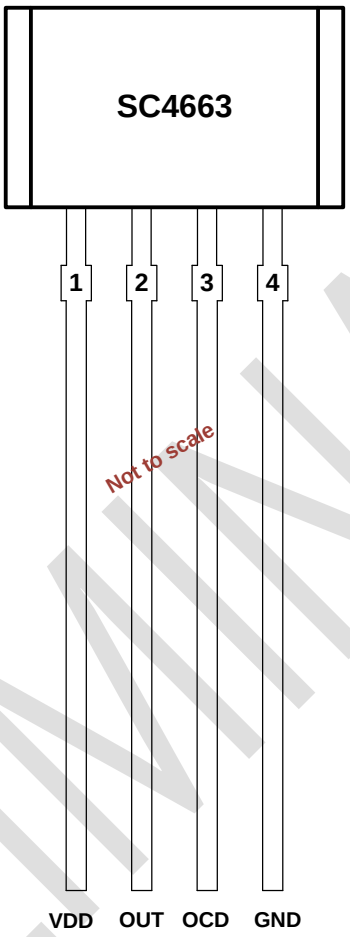
# 6 Pin configuration and Functions

## 6.1 SIP4-VB

4-Terminal SIP
VB Package
(Top View)




| Terminal | | Type | Description |
|---|---|---|---|
| Name | Number | | |
| VCC | 1 | PWR | 4.5V to 5.5V power supply. |
| OUT | 2 | Output | Output voltage |
| OCD | 3 | Output | Open-drain output. The open drain requires a pull-up resistor |
| GND | 4 | Ground | Ground terminal |

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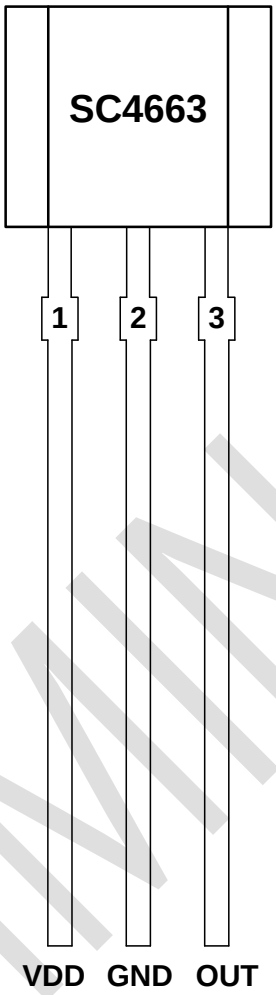
## 6.2 SIP3-VB

3-Terminal SIP
SA Package
(Top View)




| Terminal | | Type | Description |
|---|---|---|---|
| Name | Number | | |
| VCC | 1 | PWR | Supply voltage |
| GND | 2 | Ground | Ground terminal |
| OUT | 3 | Analog Output | Output voltage |

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# 7 Specification

## 7.1 Absolute Maximum Ratings

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

| Characteristic | Symbol | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Positive Supply Voltage(DC) | $V_{DD\_abs1}$ | VDD=0-->30V | - | 24 | V |
| Negtive Supply Voltage | $V_{DDR\_abs}$ | VDD=0-->-1.0V | -0.3 | - | V |
| Positive VOUT Voltage | $V_{OUT\_abs}$ | VOUT=0-->30V | - | 24 | V |
| Negtive VOUT Voltage | $V_{OUTR\_abs}$ | VDD=0-->-1.0V | -0.3 | - | V |
| VOUT Short Current to GND | $I_{Short\_GND}$ | VOUT=GND | - | 10 | mA |
| VOUT Short Current to VDD | $I_{Short\_VDD}$ | VOUT=VDD | - | 10 | mA |
| Output Sinking Current | $I_{out\_max}$ | | - | 10 | mA |
| Operating Temperature Range | $T_A$ | | -40 | 150 | ℃ |
| Storage Temperature Range | $T_{STG}$ | | -55 | 165 | ℃ |
| Maximum Junction Temperature | $T_{J(max)}$ | | - | 165 | ℃ |
| HBM ESD Rating | $ESD_{HBM}$ | | - | 1 | kV |

## 7.2 ESD Protection

*Human Body Model (HBM) tests according to: standard EIA/JESD22-A114-B HBM*

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| HBM ESD stress voltage | $V_{ESD}$ | -1000 | 1000 | V |

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## 7.3 Electrical /Magnetic Parameter

| valid through the full operate temperature range, VDD=5V, CBY=0.1uF, unless otherwise specified | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Electrical Specifications** | | | | | | |
| Supply Voltage | $V_{DD}$ | | 4.5 | 5 | 5.5 | V |
| Supply Current | $I_{DD}$ | No Res Load; VDD=4.5--5.5; All temp | - | 7.2 | - | mA |
| Power-On Delay | $t_{PO}$ | VDD=0-->5, VOUT=90% of FS | - | 100 | - | uS |
| Power-On Reset Voltage (High) | $V_{PORH}$ | VDD=0-->5.5 | - | 2.9 | - | V |
| Power-On Reset Voltage (Low) | $V_{PORL}$ | VDD=5.5-->0 | - | 2.5 | - | V |
| Under-voltage Protection(High) | $UVLO_H$ | VDD=0-->5.5V | - | 4 | - | V |
| High Voltage of OVP | $V_{OVPH}$ | VDD=5-->10V | - | 7.1 | - | V |
| Response Time | $t_{RES}$ | $C_{Load}$, Sen,$EE_{Noise}$, $EE_{BW}$ ,All temp | - | 2 | - | uS |
| Rise Time | $t_R$ | $C_{Load}$, Sen,$EE_{Noise}$, $EE_{BW}$ ,All temp | - | - | 3 | uS |
| VOUT Load Current | $I_{OUT}$ | VDD=4.5--5.5, $V_{OUT}$=0.5--4.5, Iload=-10--10mA | - | 10 | - | mA |
| VOUT Output Resistance | $R_{OUT}$ | $V_{OUT}$=VQ, $I_{LOAD}$=5mA | - | 1 | - | Ω |
| Output Capacitive Load | $C_{OUT}$ | $EE_{CL}$ = 0, Sen | 1 | - | 4.7 | nF |
| Output Capacitive Load | $C_{OUT}$ | $EE_{CL}$ = 1, Sen | 4.7 | - | 10 | nF |
| Output Leakage Current | $I_{LEAK}$ | High Impedance Mode | 0 | 6 | 20 | uA |
| Output Load Resistance(GND) | $R_{LoadL}$ | $R_L$=10k-->0.5k,B=+$B_{MAX}$ | 1 | - | - | kΩ |
| Output Load Resistance(VDD) | $R_{LoadH}$ | $R_L$=10k-->0.5k,B=-$B_{MAX}$ | 1 | - | - | kΩ |
| Clamped Output Low-level | Clamp_lo | B=-$B_{MAX}$, $R_L$=5k to VDD $EE_{CL}$=enable | 4 | 5 | 6 | %$V_{DD}$ |
| Clamped Output High-level | Clamp_hi | B=+$B_{MAX}$, $R_L$=5k to GND $EE_{CL}$=enable | 96 | 95 | 94 | %$V_{DD}$ |
| Clamped Output Accuracy | $CL_{ACC}$ | B=+$B_{MAX}$, $R_L$=5k to GND $EE_{CL}$=enable | - | - | 1 | %$V_{DD}$ |
| Output Slew Rate | SR | Sen, $C_L$ | 0.8 | - | - | V/uS |
| Cut-off Frequency | BW | Signal -3dB, $C_L$=4.7nF | 120 | - | 400 | kHz |

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| | | | | | | |
|---|---|---|---|---|---|---|
| VOUT Noise Peak-peak | $N_{p-p}$ | $C_{Load}$, Sen, TA, $EE_{Noise}$, $EE_{BW}$ | - | 6.3 | 124 | $mV_{p-p}$ |
| VOUT Noise RMS | $N_{RMS}$ | $C_{Load}$, Sen, TA, $EE_{Noise}$, $EE_{BW}$ | 1 | 5 | 10 | $mV_{RMS}$ |
| Chopping Frequency | $f_C$ | | - | 2 | - | MHz |
| Refresh rate | Trr | guaranteed by design | 0.8 | 1 | 2 | uS |
| **Magnetic Specifications** | | | | | | |
| Target Croase $V_Q$ | $V_{QT1}$ | EE=0,B=0, Sen=-Smax--+Smax | - | 50 | - | $\%V_{DD}$ |
| Target Croase $V_Q$ | $V_{QT2}$ | EE=1,B=0, Sen=-Smax--+Smax | - | 10 | - | $\%V_{DD}$ |
| Target Croase $V_Q$ | $V_{QT3}$ | EE=2,B=0, Sen=-Smax--+Smax | - | 0.5 | - | V |
| Target Croase $V_Q$ | $V_{QT4}$ | EE=3,B=0, Sen=-Smax--+Smax | - | 0.33 | - | V |
| $V_Q$ Programming Range | $V_{QPR}$ | B=0, Sen=Smax, EE=+-max | -0.2 | - | 0.2 | V |
| Bits for $V_Q$ Programming | $V_{QBits}$ | guaranteed by design | - | 10 | - | bit |
| Steps for $V_Q$ Programming | $V_{QStep}$ | Scan the EE for $V_Q$ | - | - | 0.8 | mV |
| $V_Q$ Accuracy After Programming | $V_{QAcc}$ | B=0, Sen=Smax, EE=+-max | -0.5 | 0 | 0.5 | mV |
| $V_Q$ Drift though Temperature Range | $V_{QTemp}$ | $T_A$=-40--150℃ | -0.5 | 0 | 0.5 | Gs |
| $V_Q$ Total Accuracy | $ACC_{VQ}$ | | -5 | 0 | 5 | mV |
| Linear Output Range | $VOUT_{LIN}$ | | 5 | - | 95 | % |
| Input Magnetic Range | $B_{RG}$ | guaranteed by design | ±450 | - | ±4500 | Gs |
| Sensitivity Mode with VDD | $M_{sen}$ | VDD=4.5--5.5V | - | - | 1 | % |
| Sensitivity Range | $S_{RG}$ | guaranteed by design | 0.4 | - | 4 | mV/Gs |
| Steps for Sen Programming | $S_{Step}$ | Scan the EE for Sen | - | 0.1 | - | % |
| Sen Accuracy After Programming | $S_{Acc}$ | Sen=Smax, EE=+-max | -1 | 0 | 1 | % |
| Sen Drift though Temperature Range | $S_{Temp}$ | $T_A$=-40--150℃ | -0.5 | 0 | 0.5 | % |
| Sen Total Accuracy | $ACC_S$ | | -1 | 0 | 1 | % |
| Linearity Error | LN | | -0.2 | 0 | 0.2 | % |
| PSRR | PSRR1 | 0-1kHz, 100mV pk-pk ripple on VCC B=0 | - | 55 | - | dB |
| PSRR | PSRR2 | 1k-100kHz, 100mV pk-pk ripple on VCC B=0 | - | 25 | - | dB |
| **Diagnostic Specifications** | | | | | | |

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| | | | | | | |
|---|---|---|---|---|---|---|
| DIAG_Level LOW | $DIAG_L$ | | 0 | 0.5 | 4 | %VDD |
| DIAG_Level HIGH | $DIAG_H$ | | 96 | 99.5 | 100 | %VDD |
| Broken GND | | | 0 | 0.5 | 4 | %VDD |
| Broken VDD | | | 96 | 99.5 | 100 | %VDD |
| **OCD Specifications (SIP4 only)** | | | | | | |
| OCD Internal ON Resistance | $R_{ON\_OCD}$ | B=400,$R_L$=5k to VDD | - | 100 | - | Ω |
| OCD Accuracy | $ACC_{OCD}$ | B=200G-->400G | -10 | 0 | 10 | %Thr |
| OCD Response Time | $t_{FR}$ | B=200G-->400G,tr=10ns | - | 1 | 2 | us |
| OCD Release Time | $t_{FC}$ | B=400G-->200G,tf=10ns | - | 1 | 2 | us |
| OCD Input Holding Time | $t_{OCD\_Hold}$ | guaranteed by design | - | 0.5 | - | us |
| OCD Output Dwell Time | $t_{OCD\_DW}$ | B=400G-->200G,tf=10ns | - | 10 | - | us |
| OCD Programming Rage | $OCD_{RG}$ | | 50 | - | 250 | %FS |

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# 8 Detail Description

## 8.1 Overview

The SC4663 is a monolithic programmable Hall sensor, featuring <1% sensitivity drift across temperature, <0.5% full-scale linear error across temperature and device options providing both



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unidirectional and bidirectional magnetic field sensing. The SC4663 can measure magnetic field range up to 4500Gs and be applied from -40℃ to 150℃. The magnetic field is sensed by a Hall sensor and is amplified by a precision signal chain. The SC4663 has a very fast response time (2μs) and a bandwidth of 400kHz. The SC4663 can operate with a voltage supply from 4.5 V to 5.5 V. The SC4663 is optimized for high accuracy and temperature stability, with both offset and sensitivity compensated across the entire operating temperature range.

## 8.2 Functional Block Diagram

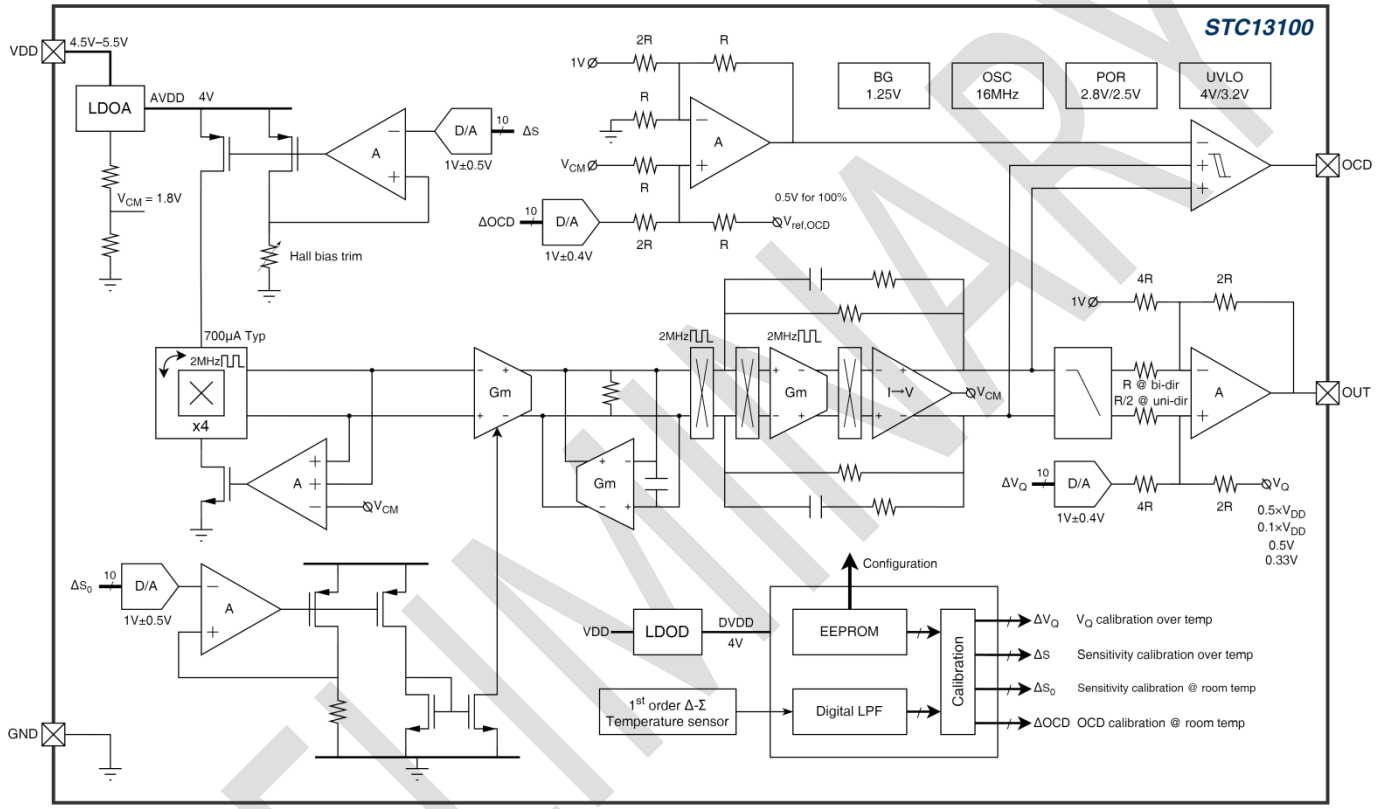


**Figure 8-1. Functional Block Diagram**

## 8.3 Feature Description

The descriptions in this section assume: TA = 25°C, no output load (RL, CL).

### 8.3.1 Power-On and Power-down

#### 8.3.1.1 Power On

At power-up, as VCC ramps up, the output is in a high-impedance state. When VCC crosses $V_{PORH}$ [1]/[1'], the POR Release counter starts counting for $t_{PORR}$. At this point, if VCC exceeds $V_{UVLOH}$ [2'], the output will go to the default after $t_{UVLOD}$ [3']. If VCC does not exceed $V_{UVLOH}$ [2], the output will stay in the high-impedance state until VCC reaches $V_{UVLOH}$ [3] and then go to setting output after

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$t_{UVLOD}$ [4].

VCC drops below $VCC_{(min)}$= 4.5 V If VCC drops below $V_{UVLOL}$ [4']/[5], the UVLO Enable Counter starts counting. If VCC is still below $V_{UVLOL}$ when the counter reaches $t_{UVLOE}$, the UVLO function will be enabled and the output will be pulled near GND [6]. If VCC exceeds VUVLOL before the UVLO Enable Counter reaches $t_{UVLOE}$ [5'], the output will continue to be the default.

Coming out of UVLO While UVLO is enabled [6], if VCC exceeds $V_{UVLOH}$ [7], UVLO will be disabled after $t_{UVLOD}$ , and the output will be the default [8].

### 8.3.1.2 Power Down

As VCC ramps down below $V_{UVLOL}$ [6']/[9], the UVLO Enable Counter will start counting. If VCC is higher than $V_{PORL}$ when the counter reaches $t_{UVLOE}$ , the UVLO function will be enabled and the output will be pulled near GND [10]. The output will enter a high-impedance state as VCC goes below $V_{PORL}$ [11]. If VCC falls below $V_{PORL}$ before the UVLO Enable Counter reaches $t_{UVLOE}$, the output will transition directly into a high-impedance state [7'].

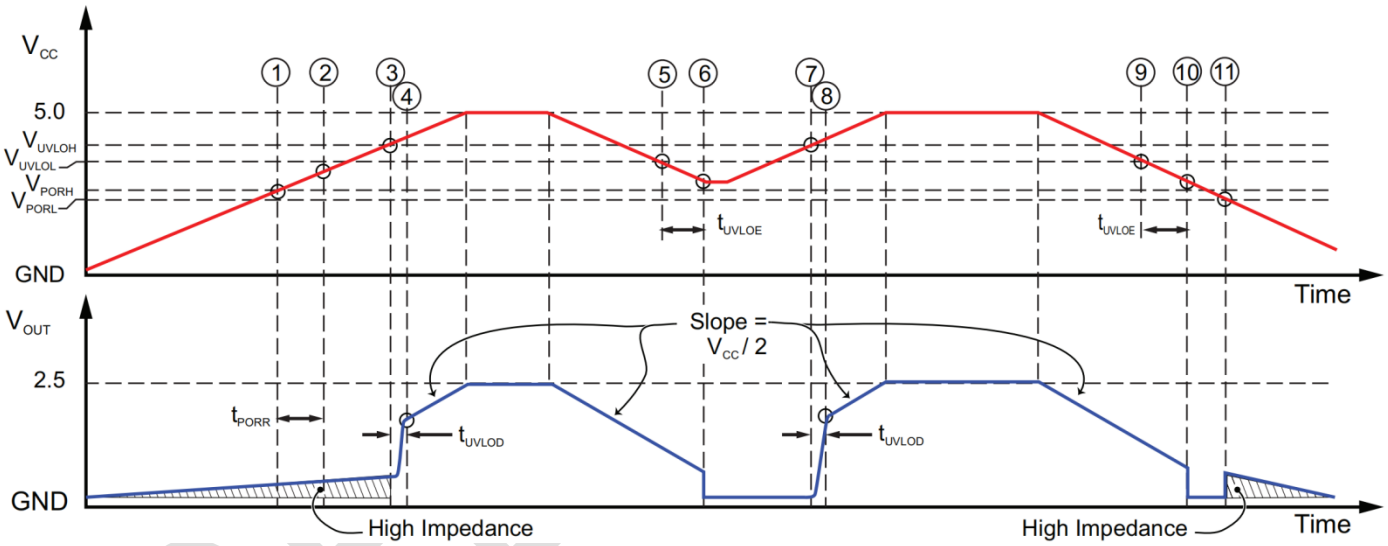


**Figure 8-2. POR and UVLO Operation – Slow Rise Time Case**



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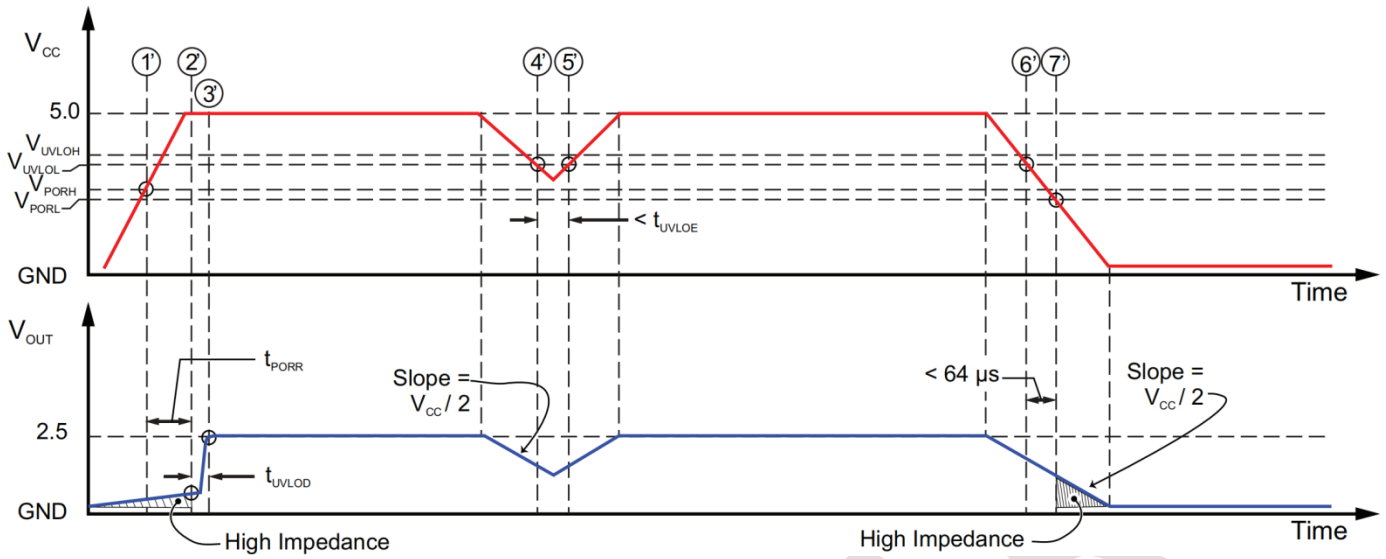


**Figure 8-3. POR and UVLO Operation – Fast Rise Time Case**

### 8.3.2 CLAMP

The SC4663 has a Clamp function used to limit the output voltage. When sensing a large magnetic field, the maximum output is limited at 95%VDD and the minimum output is limited at 5%VDD.

### 8.3.3 Over-Current Detection (OCD)

#### 8.3.3.1 Fast Over-Current Detection (OCD)

The Over-Current Detection (OCD) function allows fast detection of over-current events. The raw analog output of the Hall probes is fed directly into comparators with programmable switching thresholds. A user programmable deglitch filter is implemented to enable the suppression of fast switching transients. The two different open-drain OCD pins are active low and can be directly combined into a wired-AND configuration on board level to have a general over-current detection signal.

The OCD pins are providing a very fast response, thanks to independence from the main signal path. They can be used as a trap functionality to quickly shut down the current source as well as for precise detection of soft overload conditions.

#### 8.3.3.2 OCD pins external connection

The OCD pins can be connected to a logic input pin of the micro-controller and/or the gate-driver to quickly react to over-current events. They are designed as open-drain outputs to easily setup a wired-AND configuration and allow monitoring of several current sensors outputs via only one micro-controller pin.

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#### 8.3.3.3 OCD thresholds

The symmetric threshold level of the OCD outputs is adjustable and triggers an over-current event in case of a positive or negative over-current. The instruction for the settings is documented in the SC4663 programming guide and the SC4663 addendum.

### 8.3.4 OTP

The SC4663 has a over-temperature protection function. When temperature raising over the thresholds, the SC4663 will enter the fault mode and the performance of the output voltage is according to the setting of the F_OTP_MO in the EEPROM.

### 8.3.5 OVP

The SC4663 has a over-voltage protection function. When voltage of VDD raising over the thresholds, the SC4663 will enter the fault mode and the performance of the output voltage is according to the setting of the F_OV_MO in the EEPROM.

### 8.3.6 Low-pass filter

Low-pass filter allows signals with frequencies below a certain cutoff frequency to pass through while attenuating signals with frequencies above that cutoff. Low-pass filters help to ensure that only the desired frequency range of the signal is transmitted, reducing interference and improving overall signal quality. Overall, low-pass filters improve the overall performance and reliability of the system.

### 8.3.7 Fast response circuitry

Fast response circuitry is designed to react promptly to step signals. This ensures that critical transients or rapid changes in the system are captured and responded to in a timely manner, even if they fall outside the frequency range typically allowed by the filter.

### 8.3.8 temperature-coefficient

SC4663 use 16-segment temperature compensation algorithm. It improves the sensitivity drift and zero-point voltage drift at full temperature range. Each segment can adjust sensitivity and output voltage independently. The user can read the temperature through the temperature sensor. The temperature node of each segment can be freely set by the user.

## 8.4 EEPROM Programming Information

### 8.4.1 Programming Serial Interface

The SC4663 incorporates a serial interface that allows an external controller to read and write

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registers in the EEPROM and volatile memory. Each transaction is initiated by a command from the controller; the SC4663 does not initiate any transactions. Three commands are recognized by the device: Write Access Code, Write, and Read. As shown in Figure 8-4, the SC4663 receives all commands via the OUT pin. It responds to Read commands via the VOUT pin. This implementation of Manchester encoding requires the communication pulses be within a high and low range of voltages for the VOUT line. The Write command to EEPROM is supported by two high voltage pulses on the VOUT line.

### 8.4.2 Writing The Access Code

In order for the external controller to write or read from the SC4663 memory during the current session, it must establish serial communication with the SC4663 by sending a Write command including the Access Code within Access Code Time Out from power-up.

### 8.4.3 Writing to Volatile Memory

In order for the external controller to write to volatile memory, a Write command must be transmitted on the VDD pin. Successive Write commands to volatile memory must be separated by $t_{WRITE}$.

### 8.4.4 Writing To EEPROM

In order for the external controller to write to non-volatile EEPROM, a Write command must be transmitted on the VDD pin. The controller must also send two Programming pulses, long high-voltage strobes via the VOUT pin. These strobes are detected internally, allowing the SC4663 to boost the voltage on the EEPROM gates.

### 8.4.5 Reading From EEPROM Or Volatile Memory

In order for the external controller to read from EEPROM or volatile memory, a Read command must be transmitted on the VDD line. Within time $t_{start\_read}$, the VOUT line will stop responding to the magnetic field and the Read Acknowledge frame will transmitted on the VOUT line. The Read Acknowledge frame contains Read data.

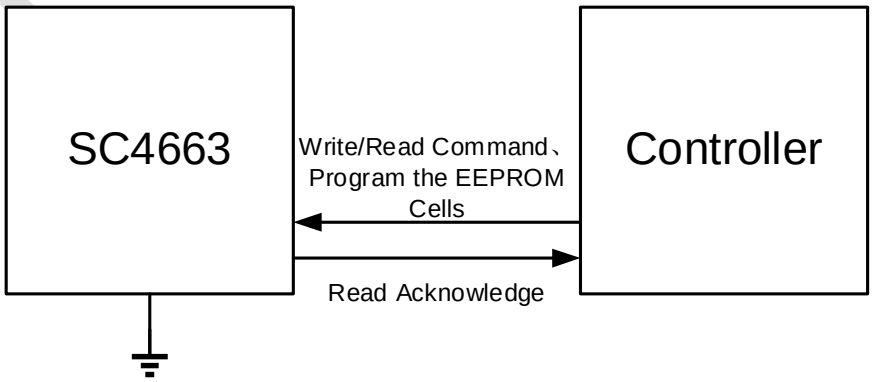


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**Figure 8-4. Programming Interface**

### 8.4.6 Register map

The following Figure 8-5. and 8-6. shows the Register map of SC4663. Figure 8-5. shows the functions of the SC4663. SC4663 has a 16-segment temperature compensation algorithm. Each segment register map is as Figure 8-6. showed.

| A[7:0] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
|---|---|---|---|---|---|---|---|---|
| 0x00 | ID_CUST[23:16] | | | | | | | |
| 0x01 | ID_CUST[15:8] | | | | | | | |
| 0x02 | ID_CUST[7:0] | | | | | | | |
| 0x03 | LK_CUST | | UD_OUT | VQ | | | T_OCD_HLD | |
| 0x04 | OCD_TH | | | T_OCD_MSK | | NO_OCD | NO_CLMP | USE_BK |
| 0x05 | G1 | | G2 | | NO_NOTCH | NO_F_RSP | F_RSP_TH | |
| 0x06 | COMM_WIN | | CL | | MO_3V3 | REF_IN | G_RT[9:8] | |
| 0x07 | 0 | ECC_0306 | | | | | | |
| 0x08 | G_RT[7:0] | | | | | | | |
| 0x09 | OTP_H[11:4] | | | | | | | |
| 0x0A | OTP_H[3:0] | | | | OTP_L[11:8] | | | |
| 0x0B | OTP_L[7:0] | | | | | | | |
| 0x0C | 0 | ECC_080B | | | | | | |
| 0x0D | F_OV_MO | | F_OTP_MO | | F_EE_MO | | F_GAIN_MO | |
| 0x0E | F_OCD_MO | | F_HL_MO | | F_TEMP_MO | | F_UVLO_MO | |
| 0x0F | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x10 | CLMP_LVL | OW_OD | SWP_DIR_M | SWP_DIR_S | CL_MO | 0 | T_TRK | |
| 0x11 | 0 | ECC_0D10 | | | | | | |
| 0x12 | CAL_T[0] | | | | | | | |
| 0x13 | | | | | | | | |
| 0x14 | | | | | | | | |
| 0x15 | | | | | | | | |
| 0x16 | | | | | | | | |
| 0x17 | | | | | | | | |

**Figure 8-5. Register map of function**

| A[7:0] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
|---|---|---|---|---|---|---|---|---|
| 0xXX+0x00 | TJ[11:4] | | | | | | | |
| 0xXX+0x01 | dVQ[9:2] | | | | | | | |
| 0xXX+0x02 | dS[9:2] | | | | | | | |
| 0xXX+0x03 | dVREF[8:1] | | | | | | | |
| 0xXX+0x04 | dVREF[0] | ECC_CAL[6:0] | | | | | | |
| 0xXX+0x05 | TJ[3:0] | | | | dVQ[1:0] | | dS[1:0] | |

**Figure 8-6. Register map of each segment CAL_T**

### 8.4.7 Induction Magnetic Field

**UD_OUT** locates at bit[5] in Address 0x03. It defines the unidirectional output of SC4663. By setting this bit, SC4663 will be affected only by unidirectional magnetic field. The default setting is 0.

**SWP_DIR_M** locates at bit[5] in Address 0x10. By setting this bit, the polarity of magnetic field that SC4663 induces will change. The default setting is 0.



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### 8.4.8 Quiescent Voltage

**VQ** locates at bit[2] to bit[4] in Address 0x03. They define the output voltage without external magnetic field. It has four stages. When its code is 000 or 001, the output voltage is proportional to the VDD. When its code is 010 or 011, the output is a constant voltage. The default setting is 3b'000.

**Table 8-1. VQ code**

| VQ | Code |
|---|---|
| 0.5x VDD | 000 |
| 0.1x VDD | 001 |
| 0.5V | 010 |
| 0.33V | 011 |

### 8.4.9 OCD

**T_OCD_HLD** locates at bit[0] and bit[1] in Address 0x03. They define OCD duration time. When the OCD is triggered, the OCD alarm will hold at least a period of time according to the setting even if OCD is clear. The default code is 00.

**T_OCD_MSK** locates at bit[3] and bit[4] in Address 0x04. They define OCD delay time. When the OCD is triggered, the OCD alarm will delay according to the setting even if OCD is clear. The default code is 00.

**Table 8-2. Time of T_OCD_HLD and T_OCD_MSK code**

| OCD hold time | Code | OCD mask time | Code |
|---|---|---|---|
| 0 us | 00 | 0ns | 00 |
| 10 us | 01 | 250ns | 01 |
| 2.05 us | 10 | 500ns | 10 |
| 5.12 us | 11 | 750ns | 11 |

**OCD_TH** bits locates at bit[5] to bit [7] in Address 0x04. They define OCD threshold. It stands for Over-current Detection Threshold and decide the limit of the strength of the magnetic field that OCD will take action to open alarm. The default code is 3b'000.

**Table 8-3. OCD_TH code**

| OCD threshold | Code | OCD threshold | Code |
|---|---|---|---|



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| | | | |
|---|---|---|---|
| | | 120%FS | 100 |
| 250%FS | 001 | 100%FS | 101 |
| 200%FS | 010 | 80%FS | 110 |
| 150%FS | 011 | 50%FS | 111 |

**NO_OCD** locates at bit[2] in Address 0x04. By setting this bit, the OCD function will be disabled and no longer respond to the over-current. The default setting is 0.

### 8.4.10 CLAMP

**No_CLAMP** locates at bit[1] in Address 0x04. By setting this bit, the CLAMP function will be disabled. The default setting is 0.

### 8.4.11 GAIN

Gain bits define the multiplier of the SC4663 induced magnetic field. SC4663 has two Gain, GAIN 1 and GAIN 2. The total Gain equals to the product of GAIN 1 and GAIN 2.

**GAIN 1** locates at bit[6] and bit[7] in Address 0x05 while **GAIN 2** locates at bit[4] and bit[5] in Address 0x05. The default setting of **GAIN 1** and **GAIN 2** are all 00.

**Table 8-4. Multiplier of GAIN code**

| GAIN 1 | Code | GAIN 2 | Code |
|---|---|---|---|
| 1x | 00 | 1x | 00 |
| 2x | 01 | 2x | 01 |
| 4x | 10 | 4x | 10 |
| 8x | 11 | 8x | 11 |

**G_RT** is 10 bits, which define the GAIN of SC4663 at 25℃. It locates at Address 0x08 and bit[0] and bit[1] in Address 0x06. The $G\_RT_{maxcode}$ is 511, and $G\_RT_{mincode}$ is 512. The default setting of this code is 10h'000.

### 8.4.12 Low-pass Filter

**No_NOTCH** locates at bit[3] in Address 0x05. By setting this bit, low-pass filter will be disabled. And



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it will enlarge high-frequency noise and shorten the response time of SC4663. The default setting is 0.

### 8.4.13 Fast Response Circuitry

**NO_F_RSP** locates at bit[2] in Address 0x05. By setting this bit, fast response circuitry will be disabled. Whether the step signal will be filtered by the low-pass filter depends on its frequency. The default setting is 0.

**F_RSP_TH** locates at bit[0] and bit[1] in Address 0x05. They define the threshold of fast response. The default setting is 0.

### 8.4.14 Communication Window

**COMM_WIN** locates at bit[6] and bit[7] in Address 0x06. They define the duration startup that enables to input protocol via OUT pin. If it is over time, SC4663 cannot be communicated. If it is set 11, the SC4663 will be locked and can never be communicated. The default setting of this code is 00.

**Table 8-5. Duration Time of Communication Window**

| COMM_WIN | Code |
|---|---|
| 100ms | 00 |
| 50ms | 01 |
| 20ms | 10 |
| 0ms | 11 |

### 8.4.15 Output

**CL** locates at bit[4] and bit [5] in Address 0x06. They define the external capacitor range that should be used. If external capacitor used is out of range, it will cause output shocking. The default code is 00.

**Table 8-6. external capacitor range of CL code**

| OUT capacitor | Code |
|---|---|
| 1nf - 4.7nf | 00 |
| | 01 |
| 4.7nf - 10nf | 10 |

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| | |
|---|---|
| | 11 |

**CL_MO** locates at bit[3] in Address 0x10. It defines the function of OCD self-recovery. By setting this bit, SC4663 will recover when over-current is removed. The default setting is 0.

### 8.4.16 Over-temperature Protection

**OTP_H** is 12 bits, which locates at Address 0x09 and bit[4] to bit[7] in Address 0x0A. They define the trip point of over-temperature protection. The $OTP\_H_{maxcode}$ is 2047, and $G\_RT_{mincode}$ is 4095. The default setting of this code is 12h'000.

**OTP_L** is 12 bits, which locates at Address 0x0B and bit[0] to bit[3] in Address 0x0A. They define the recovery point of over-temperature protection. The $OTP\_H_{maxcode}$ is 2047, and $G\_RT_{mincode}$ is 4095. The default setting of this code is 12h'000.

### 8.4.17 Self-test Mode

SC4663 has many self-test modes that are listed as follows.

**F_OV_MO** locates at bit[6] and bit[7] in Address 0x0D, about fault mode of Over-voltage protection.

**F_OTP_MO** locates at bit[4] and bit[5] in Address 0x0D, about fault mode of Over-temperature protection.

**F_EE_MO** locates at bit[2] and bit[3] in Address 0x0D, about fault mode of ECC.

**F_GAIN_MO** locates at bit[0] and bit[1] in Address 0x0D, about fault mode of Gain stage self-test.

**F_OCD_MO** locates at bit[6] and bit[7] in Address 0x0E, about fault mode of Over-current detection.

**F_HL_MO** locates at bit[4] and bit[5] in Address 0x0E, about fault mode of Hall bias self-test.

**F_TEMP_MO** locates at bit[2] and bit[3] in Address 0x0E, about fault mode of Temperature sensor self-test failure.

**F_UVLO_MO** locates at bit[0] and bit[1] in Address 0x0E, about fault mode of UVLO.

By setting each of these fault modes to 00, it will disable this function. The other settings are listed in TABLE. The default code is 00.

**Table 8-7. Fault mode of self-test**

| Default mode | Code |
|---|---|
| Disabled | 00 |
| HZ | 01 |



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| | |
|---|---|
| Pull OUT L | 10 |
| Pull OUT H | 11 |

### 8.4.18 OW_OD

**OW_OD** locates at bit[6] in Address 0x10. It defines the function of one-wire open-drain output. By setting this bit, the OUT current will be open. The default setting of this code is 0.

### 8.4.19 CAL_T[15:0]

**CAL_T** includes temperature of segment point, temperature-coefficient effects of VQ & GAIN calibration.

**$T_J$** is used to locate the temperature, while the value of $T_J$ is according to the temperature sensor.

**dVQ** has 10 bits used to calibrate. $VQ_{maxcode}$ is 511, and $VQ_{mincode}$ is 512.

**dS** has 10 bits used to calibrate. $GAIN_{maxcode}$ is 511, and $GAIN_{mincode}$ is 512.

### 8.4.20 ECC

**ECC** is used to correct the single bit or detect the fault of double bits error in the EEPROM. SC4663 has three ECC for Address 0x03-0x06, Address 0x08-0x0B and Address 0x0D-0x10. Furthermore, Each segment of temperature coefficient has one ECC.

## 9 Characteristic Definitions

### 9.1 Power-On Time ($t_{PO}$)

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time ($t_{PO}$) is defined as: the time it takes for the out- put voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage ($V_{CC(min)}$) as shown in Figure 9-1.

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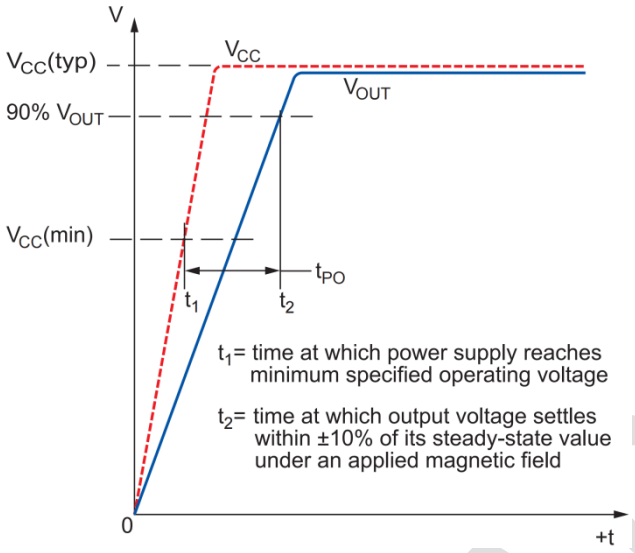


**Figure 9-1. Power-On Time Definition**

### 9.2 Temperature Compensation Power-On Time ($t_{TC}$)

After Power-On Time ($t_{PO}$) elapses, $t_{TC}$ is also required before a valid temperature compensated output.

### 9.3 Propagation Delay ($t_{pd}$)

The time interval between a) when the applied magnetic field reaches 20% of its final value, and b) when the output reaches 20% of its final value (see Figure 6).

### 9.4 Rise Time ($t_r$)

The time interval between a) when the sensor IC reaches 10% of its final value, and b) when it reaches 90% of its final value (see Figure 9-2). Both $t_r$ and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

### 9.5 Response Time ($t_{RESPONSE}$)

The time interval between a) when the applied magnetic field reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied magnetic field (see Figure 9-3).

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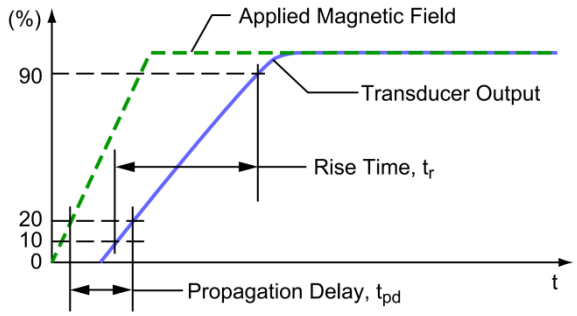


**Figure 9-2. Propagation Delay and Rise Time Definitions**

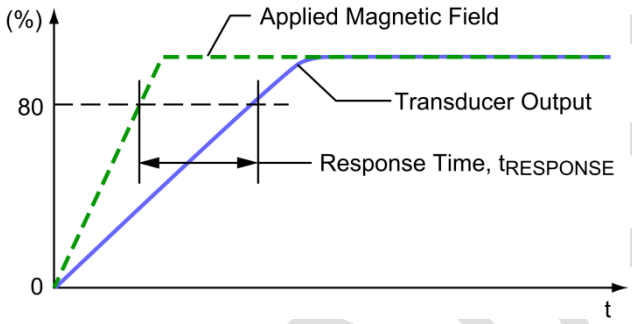


**Figure 9-3. Response Time Definition**

## 9.6 Delay to Clamp ($t_{CLP}$)

A large magnetic input step may cause the clamp to overshoot its steady-state value. The Delay to Clamp ($t_{CLP}$) is defined as: the time it takes for the output voltage to settle within steady-state clamp voltage ±1% of Clamp Voltage Dynamic Range, after initially passing through its steady-state voltage, as shown in Figure 9-4. Clamp Voltage Dynamic Range is defined as $V_{CLP(HIGH)min}$ - $V_{CLP(LOW)max}$.

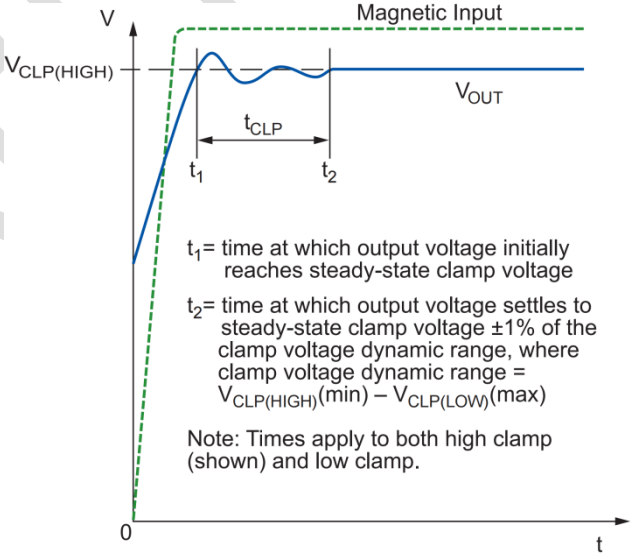


**Figure 9-4. Delay to Clamp Definition**

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### 9.7 Quiescent Voltage Output ($V_{OUT(Q)}$)

In the quiescent state (no significant magnetic field: B = 0 G), the output ($V_{OUT(Q)}$ ) is a constant voltage or has a constant ratio to the supply voltage (VCC) throughout the entire operating ranges of VCC and ambient temperature ($T_A$).

### 9.8 Initial Unprogrammed Quiescent Voltage Output ($V_{OUT(Q)init}$)

Before any programming, the Quiescent Voltage Output ($V_{OUT(Q)}$) has a nominal value of VCC / 2.

### 9.9 Quiescent Voltage Output Temperature Coefficient ($TC_{QVO}$)

Device $V_{OUT(Q)}$ changes as temperature changes, with respect to its programmed Quiescent Voltage Output Temperature Coefficient, $TC_{QVO}$ . $TC_{QVO}$ is programmed at 150°C and is calculated relative to the nominal $V_{OUT(Q)}$ programming temperature of 25°C. $TC_{QVO}$ (mV/°C) is defined as:

$$TC_{QVO} = \frac{[V_{OUT(Q)T2} - V_{OUT(Q)T1}]}{T2 - T1} \quad (1)$$

where T1 is the nominal $V_{OUT(Q)}$ programming temperature of 25°C, and T2 is the $TC_{QVO}$ programming temperature of 150°C. The expected $V_{OUT(Q)}$ through the full ambient temperature range ($V_{OUT(Q)EXPECTED(TA)}$) is defined as:

$$V_{OUT(Q)EXPECTED(T_A)} = V_{OUT(Q)T_1} + TC_{QVO}(T_A - T_1) \quad (2)$$

$V_{OUT(Q)EXPECTED(TA)}$ should be calculated using the actual measured values of $V_{OUT(Q)}$T1 and $TC_{QVO}$ rather than programming target values.

### 9.10 Quiescent Voltage Output Drift Through Temperature Range ($V_{OUT(Q)TC}$)

Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output ($V_{OUT(Q)}$) may drift from its nominal value through the operating ambient temperature ($T_A$). The Quiescent Voltage Output Drift Through Temperature Range ($V_{OUT(Q)TC}$) is defined as:

$$D_{V_{OUT(Q)}TC} = V_{OUT(Q)(T_A)} - V_{OUT(Q)EXPECTED(T_A)} \quad (3)$$

$\Delta V_{OUT(Q)TC}$ should be calculated using the actual measured values of $\Delta V_{OUT(Q)(TA)}$ and $\Delta V_{OUT(Q)EXPECTED(TA)}$ rather than programming target values.

### 9.11 Sensitivity (Sens)

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, the application of a north polarity field decreases the output voltage from its quiescent



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value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device, and it is defined as:

$$\text{Sens} = \frac{V_{OUT(B_{POS})} - V_{OUT(B_{NEG})}}{B_{POS} - B_{NEG}} \quad (4)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

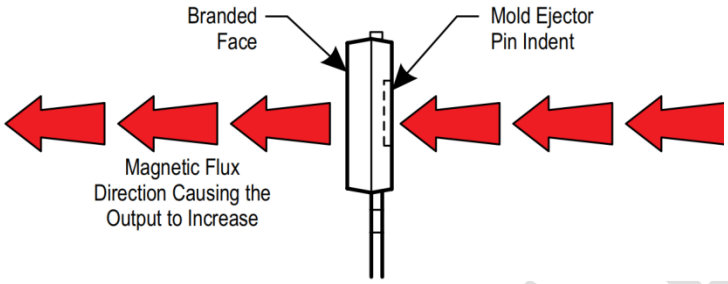


**Figure 9-5. Magnetic Flux Polarity**

### 9.12 Initial Unprogrammed Sensitivity ($Sens_{init}$)

Before any programming, Sensitivity has a nominal value that depends on the GAIN_STAGE_COARSE bits and G_RT bits setting.

### 9.13 Sensitivity Programming Range ($Sens_{PR}$)

The magnetic sensitivity (Sens) can be programmed around its initial value within the sensitivity range limits: $Sens_{PR(min)}$ and $Sens_{PR(max)}$. Exceeding the specified Sensitivity Range will cause Sensitivity Drift Through Temperature Range $Sens_{TC}$ to deteriorate beyond the specified values.

### 9.14 Average Fine Sensitivity Programming Step Size ($Step_{SENS}$)

The Average Quiescent Voltage Output Programming Step Size ($Step_{Sens}$ ) is determined using the following calculation:

$$\text{Step}_{\text{Sens}} = \frac{\text{Sens}_{\text{maxcode}} - \text{Sens}_{\text{mincode}}}{2^n - 1} \quad (5)$$

where n is the number of available programming bits in the trim range, 10 bits, $Sens_{maxcode}$ is at decimal code 511, and $Sens_{mincode}$ is at decimal code 512.

### 9.15 Sensitivity Temperature Coefficient ($TC_{SENS}$)

Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, $TC_{SENS}$. $TC_{SENS}$ is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. $TC_{SENS}$ (%/°C) is defined as:

$$TC_{Sens} = \frac{Sens_{T_2} - Sens_{T_1}}{Sens_{T_1} \times (T_2 - T_1)} \times 100\% \quad (6)$$



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where T1 is the nominal Sens programming temperature of 25°C, and T2 is the $TC_{SENS}$ programming temperature of 150°C. The expected value of Sens over the full ambient temperature range, $Sens_{EXPECTED(TA)}$, is defined as:

$$Sens_{EXPECTED(T_A)} = Sens_{T_1} \times [100\% + \frac{TC_{Sens}(T_A - T_1)}{100}] \quad (7)$$

$Sens_{EXPECTED(TA)}$ should be calculated using the actual measured values of SensT1 rather than programming target values.

### 9.16 Sensitivity Drift Through Temperature Range ($Sens_{TC}$)

Temperature-coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range ($T_A$). The Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$) is defined as:

$$\Delta\,\mathrm{Sens_{TC}} = \frac{\mathrm{Sens_{T_A}} - \mathrm{Sens_{EXPECTED(T_A)}}}{\mathrm{Sens_{EXPECTED(T_A)}}} \times 100\% \quad (8)$$

### 9.17 Sensitivity Drift Due to Package Hysteresis ($Sens_{PKG}$)

Package stress and relaxation can cause the device sensitivity at TA = 25°C to change during and after temperature cycling. The sensitivity drift due to package hysteresis ($\Delta Sens_{PKG}$) is defined as:

$$\Delta\,\mathrm{Sens_{PKG}} = \frac{\mathrm{Sens_{(25℃)2}} - \mathrm{Sens_{(25℃)1}}}{\mathrm{Sens_{(25℃)1}}} \times 100\% \quad (9)$$

where Sens(25°C)1 is the programmed value of sensitivity at TA = 25°C, and Sens(25°C)2 is the value of sensitivity at TA = 25°C, after temperature cycling TA up to 150°C and back to 25°C.

### 9.18 Linearity Sensitivity Error ($Lin_{ERR}$)

The SC4663 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

### 9.19 Linearity Error

Linearity error is calculated separately for the positive ($Lin_{ERRPOS}$) and negative ($Lin_{ERRNEG}$) applied magnetic fields. Linearity Error (%) is measured and defined as:

$$\mathrm{Lin_{ERR_{POS}}} = (1 - \frac{\mathrm{Sens_{B_{POS2}}}}{\mathrm{Sens_{B_{POS1}}}}) \times 100\% \quad (10)$$

$$Lin_{ERR_{NEG}} = (1 - \frac{Sens_{B_{NEG2}}}{Sens_{B_{NEG1}}}) \times 100\% \quad (11)$$

where:



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$$Sens_{B_x} = \frac{|V_{OUT(B_x)} - V_{OUT(Q)}|}{B_x} \quad (12)$$

and $B_{POSx}$ and $B_{NEGx}$ are positive and negative magnetic fields, with respect to the quiescent voltage output such that $|B_{POS2}| = 2 \times |B_{POS1}|$ and $|B_{NEG2}| = 2 \times |B_{NEG1}|$.

Then:

$$\text{LinERR} = \max(\text{LinERR}_{\text{POS}}, \text{LinERR}_{\text{NEG}}) \quad (13)$$

### 9.20 Symmetry Sensitivity Error ($Sym_{ERR}$)

The magnetic sensitivity of an SC4663 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry Error, $Sym_{ERR}$ (%), is measured and defined as:

$$Sym_{ERR} = (1 - \frac{Sens_{B_{POS}}}{Sens_{B_{NEG}}}) \times 100\% \quad (14)$$

where SensBx is as defined in equation 12, and $B_{POSx}$ and $B_{NEGx}$ are positive and negative magnetic fields such that $|B_{POSx}| = |B_{NEGx}|$.

### 9.21 Ratiometry Error (RatERR)

The SC4663 device features ratiometric output. This means that the Quiescent Voltage Output ($V_{OUT(Q)}$) magnetic sensitivity, Sens, and Output Voltage Clamp ($VCLP_{(HIGH)}$ and $VCLP_{(LOW)}$) are proportional to the Supply Voltage (VCC). In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in Quiescent Voltage Output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage (VCC) is defined as:

$$Rat_{ERRV_{OUT(Q)}} = (1 - \frac{V_{OUT(Q)(VCC)}/V_{OUT(Q)(5V)}}{V_{cc}/5V}) \times 100\% \quad (15)$$

The ratiometric error in magnetic sensitivity, $Rat_{ERRSens}$ (%), for a given Supply Voltage (VCC) is defined as:

$$Rat_{ERRSens} = (1 - \frac{Sens_{(VCC)}/Sens_{(5V)}}{VCC/5V}) \times 100\% \quad (16)$$

The ratiometric error in the clamp voltages, $Rat_{ERRCLP}$ (%), for a given supply voltage (VCC) is defined as:

$$Rat_{ERRCLP} = (1 - \frac{V_{CLP(VCC)}/V_{CLP(5V)}}{VCC/5V}) \times 100\% \quad (17)$$

where VCLP is either VCLP(HIGH) or VCLP(LOW).

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### 9.22 Power-On Reset Voltage ($V_{POR}$)

On power-up, to initialize to a known state and avoid current spikes, the SC4663 is held in Reset state. The Reset signal is disabled when VCC reaches $V_{UVLOH}$ and time $t_{PORR}$ has elapsed, allowing the output voltage to go from a high-impedance state into normal operation. During power-down, the Reset signal is enabled when VCC reaches $V_{PORL}$, causing the output voltage to go into a high-impedance state. (Note that a detailed description of POR and UVLO operation can be found in the Functional Description section).

### 9.23 Power-On Reset Release Time ($t_{PORR}$)

When VCC rises to $V_{PORH}$ , the Power-On Reset Counter starts. The SC4663 output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached $t_{PORR}$ and VCC has exceeded $V_{UVLOH}$. Under-voltage Lockout Threshold ($V_{UVLO}$) If VCC drops below $V_{UVLOL}$, the output voltage will be pulled to GND. If VCC starts rising, the SC4663 will come out of this lock state when VCC reaches $V_{UVLOH}$.

### 9.24 UVLO Enable/Disable Delay Time ($t_{UVLO}$)

When a falling VCC reaches $V_{UVLOL}$, time $t_{UVLOE}$ is required to engage the Undervoltage Lockout state. When VCC rises above $V_{UVLOH}$, time $t_{UVLOD}$ is required to disable UVLO and to have a valid output voltage.

### 9.25 Output Saturation Voltage ($V_{SAT}$)

When output voltage clamps are disabled, the output voltage can swing to a maximum of $V_{SAT(HIGH)}$ and to a minimum of $V_{SAT(LOW)}$ .

### 9.26 Broken Wire Voltage ($V_{BRK}$)

If the GND pin is disconnected (broken wire event), output voltage will go to $V_{BRK(HIGH)}$ if a load resistor is connected to VCC, or to $V_{BRK(LOW)}$ if a load resistor is connected to GND.

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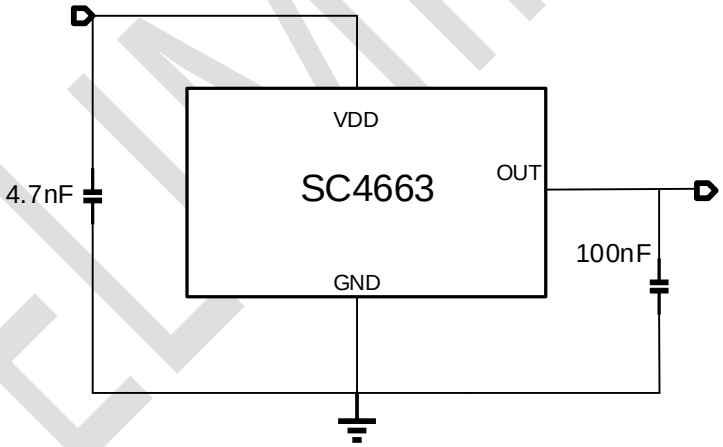
## 10 Typical Application Diagram

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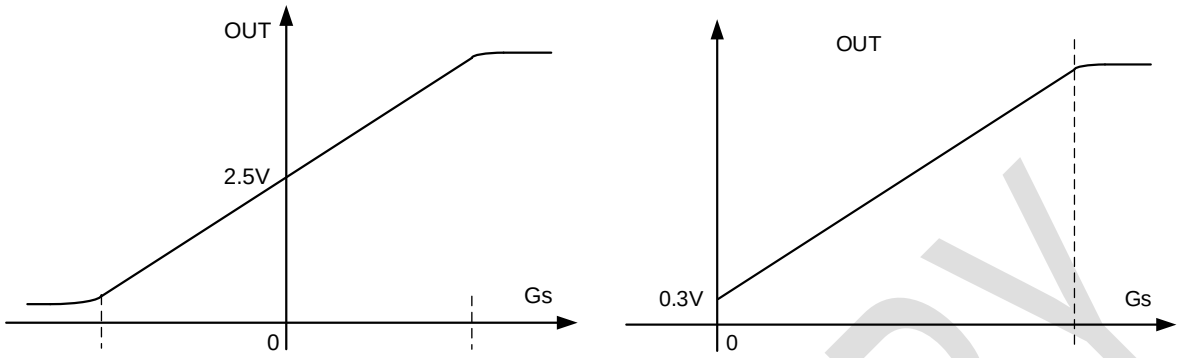
# 11 Transfer Function




# 12 Package Designator

## 12.1 Package(SIP4-VB)

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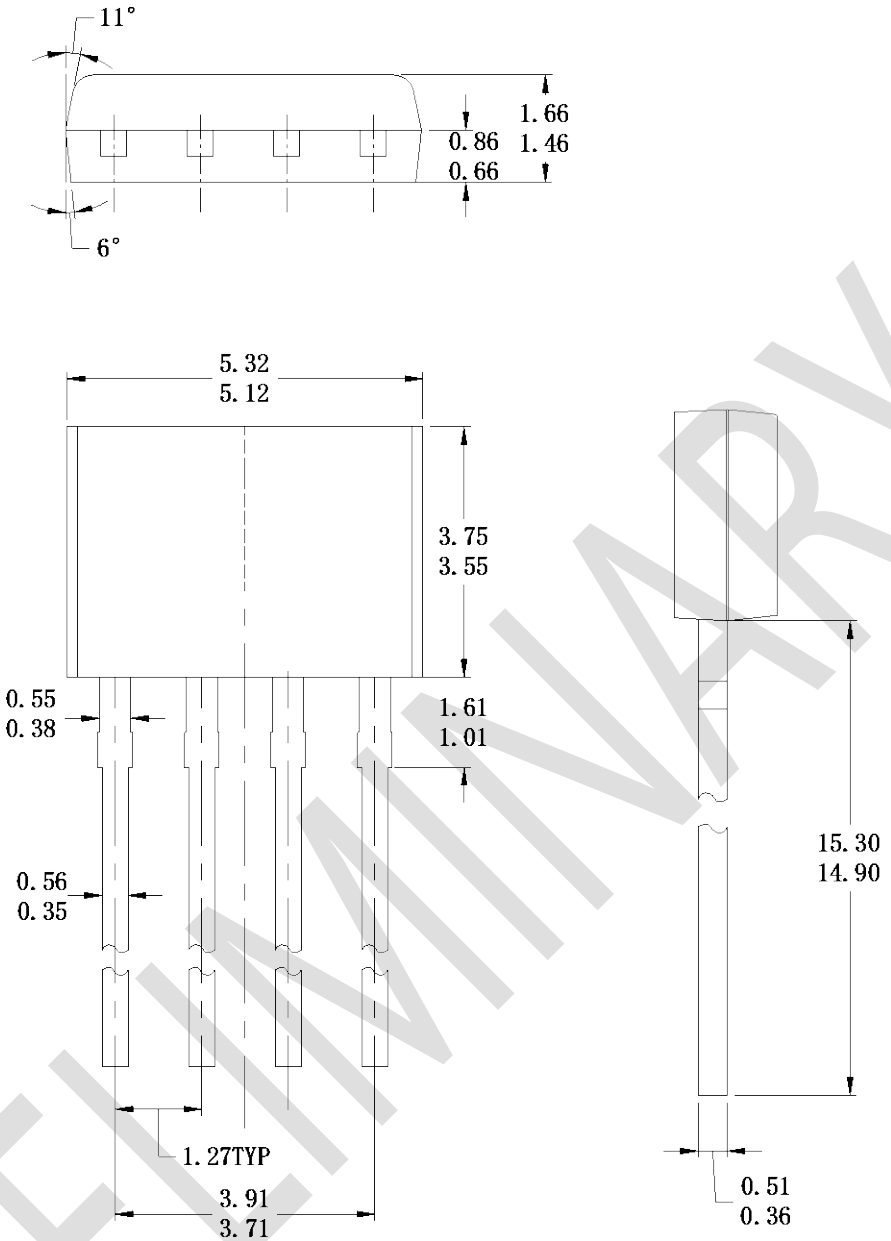


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## 12.2 Package(SIP3-VB)

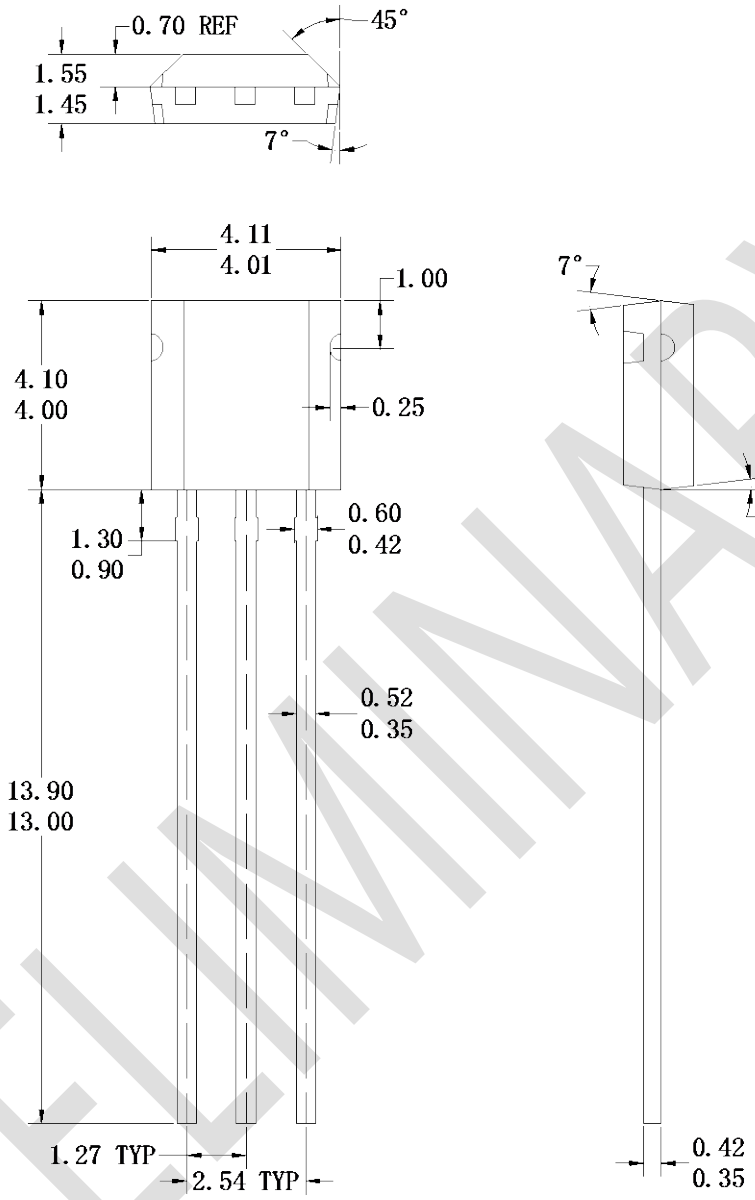


Figure: TO-92S-U Package Shape and Dimension in millimeters

Notes: A. All linear dimensions are in millimeters.

B. Body dimension do not include mold flash

C. This package complies to JEDEC MS-012 variation BA

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