100V Three-Phase Half-Bridge Gate Driver

Features

- Driver for three-phase N-channel MOS or IGBT
- High-side floating bootstrap power supply, operating voltage up to 120V
- Integrated bootstrap diode
- Integrated sink-source balancing circuit, no resistors or diodes required at the gate of the power transistor
- Output equivalent current capability of 2.5A
- Maximum operating frequency 500kHz
- Logic input levels compatible with 3.3V / 5V
- High-side undervoltage protection
- Adaptive dead-time control circuit
- Built-in lockout to prevent shoot-through
- Packaging forms: QFN24, TSSOP20

Description

The ZH639D0 is a high-voltage, high-speed half-bridge gate driver for power MOSFETs and IGBTs. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in a high-side configuration, with an operating voltage of 120V. The three output channels builds internal adaptive dead-time to avoid cross-conduction. The output module integrates a sink-source balancing circuit, eliminating the need for resistors and diodes between the IC and the gate of the power transistor. The high and low-side outputs are independently controlled by the input, and the high-side is equipped with undervoltage protection.

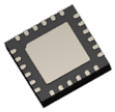
The 24-pin package has separate power GND and logic GND pins for convenient PCB layout reducing interference.

Applications

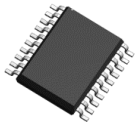
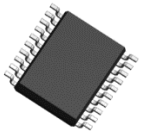
- Drones
- Power tools
- Motor drives
- Wireless charger

Package

QFN24

TSSOP20

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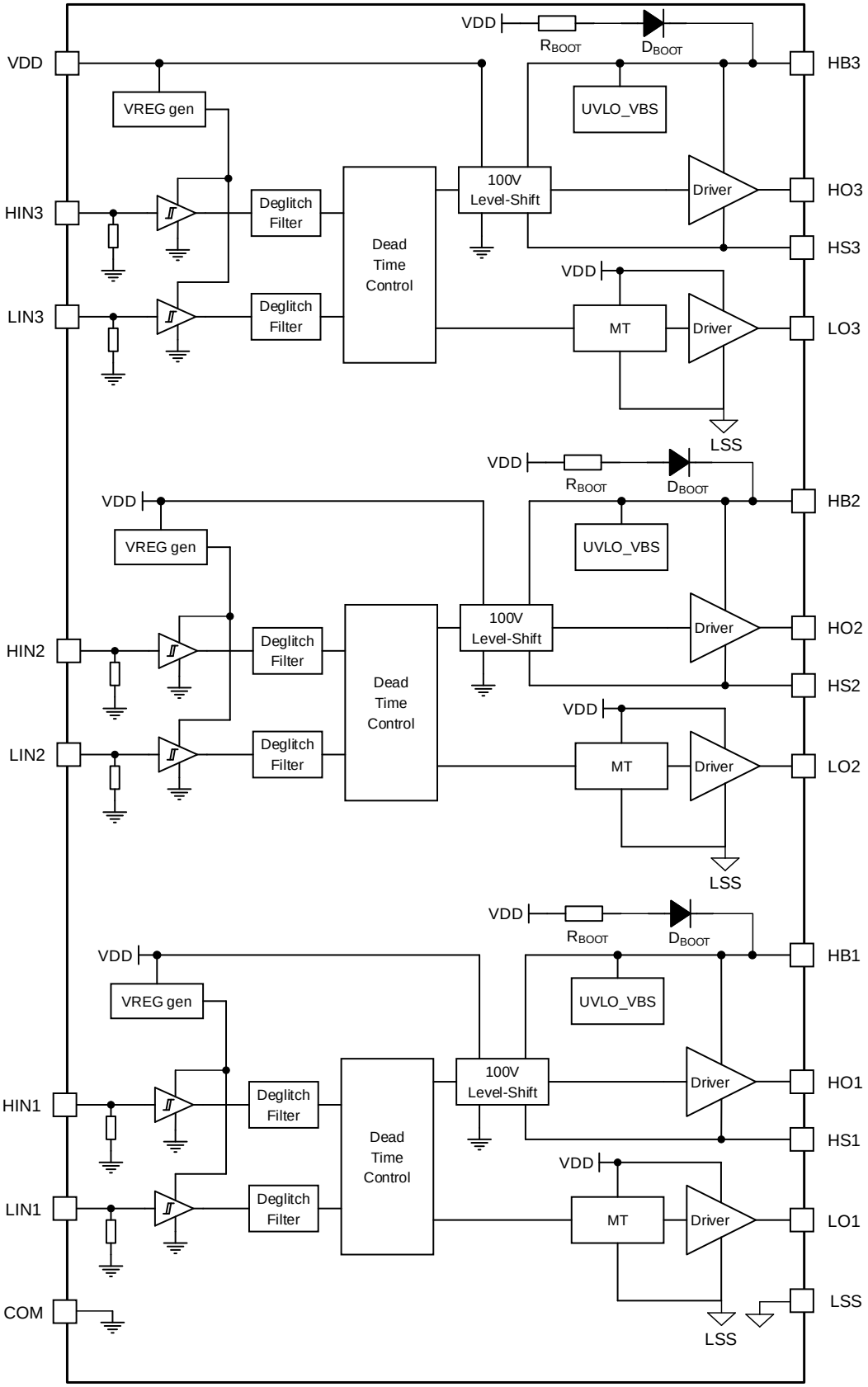
Functional Block Diagram



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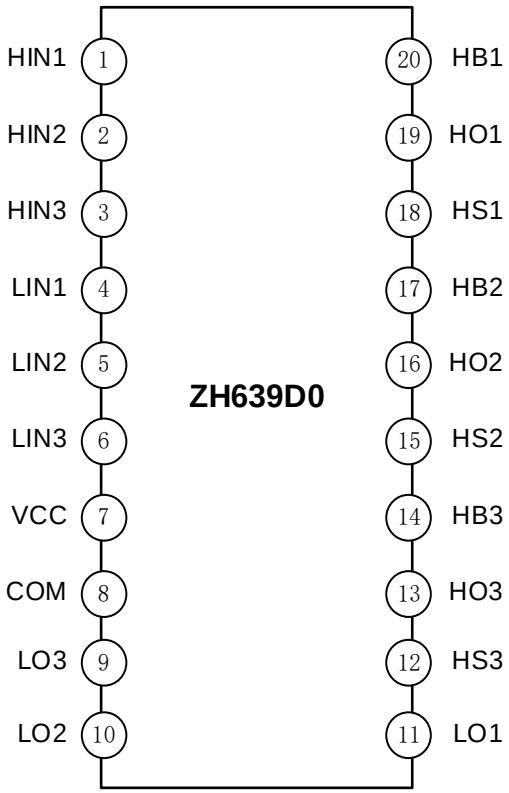
Pin Definitions

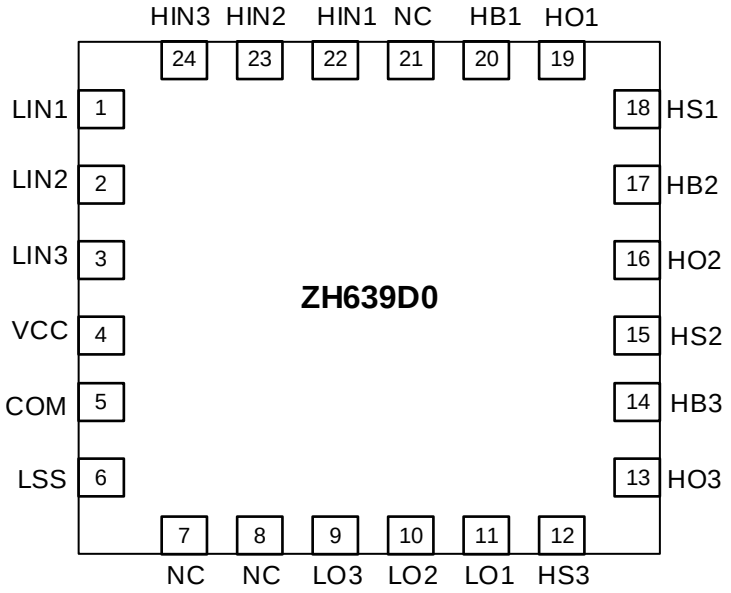
TSSOP20



Pin Name	Pin Number	Type	Description
HIN1、HIN2、HIN3	1、2、3	Input	High-side logic input control signals
LIN1、LIN2、LIN3	4、5、6	Input	Low-side logic input control signals
COM(LSS)	8	Ground	Chip ground
VCC	7	Power	Chip power supply
LO3、LO2、LO1	9、10、11	Output	Low-side power output
HS3、HS2、HS1	12、15、18	Output	High-side floating ground
HO3、HO2、HO1	13、16、19	Output	High-side power output
HB3、HB2、HB1	14、17、20	Power	High-edge suspended power supply

100V Three-Phase Half-Bridge Gate Driver

QFN24



Pin Name	Pin Number	Type	Function Description
HIN1, HIN2, HIN3	22, 23, 24	Input	High-side logic input control signal
LIN1, LIN2, LIN3	1, 2, 3	Input	Low-side logic input control signal
COM	5	Ground	Logic reference ground, shared with the microcontroller
LSS	6	Ground	Power reference ground, shared with the power transistor
VCC	4	Power	Chip power supply
LO3, LO2, LO1	9, 10, 11	Output	Low-side power output
HS3, HS2, HS1	12, 15, 18	Output	High-side floating ground
HO3, HO2, HO1	13, 16, 19	Output	High-side power output
HB3, HB2, HB1	14, 17, 20	Power	High-side floating power supply
	7, 8, 21	NC	No connection

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Ordering Information

Part Number	Package	Packing	Quantity per Reel
ZH639D0JT	TSSOP20	Reel	4000
ZH639D0NU	QFN24	Reel	4000

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
HBx	High-Side Floating Supply	–	-0.3	120	V
HSx	High-Side Floating Ground	–	-5	100	V
		1us	-10	110	V
HBx-HSx	Floating Supply Voltage	–	-0.3	20	
HOx	High-Side Output	–	HS – 0.3	HB + 0.3	V
LOx	Low-Side Output	–	–0.3	VCC + 0.3	V
VCC	Supply Voltage	–	–0.3	20	V
HINx	High-Side Logic Input Voltage	–	–0.3	6	V
LINx	Low-Side Logic Input Voltage	–	–0.3	6	V
T_A	Ambient Temperature		–40	125	°C
T_{stg}	Storage Temperature		–55	150	°C

ESD

Symbol	Parameter	Test Conditions	Typical Value	Unit
VESD	Electrostatic Discharge	Human Body Model (HBM)	±2000	V
		Negative discharge to GND at HSx pin	1000	V

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{HBx}	High-Side Floating Supply Voltage	VS + 5	VS + 12	V
V_{HSx}	High-Side Floating Ground Voltage	–5	100	V
V_{HOx}	High-Side Floating Output Voltage	V_{HSx}	V_{HBx}	V
VCC	Supply Voltage	5	12	V
V_{LOx}	Low-Side Output Voltage	0	VCC	V
V_{INx}	Logic Input Voltage (HINx & LINx)	0	5	V

T_A	Ambient Temperature	–40	125	°C

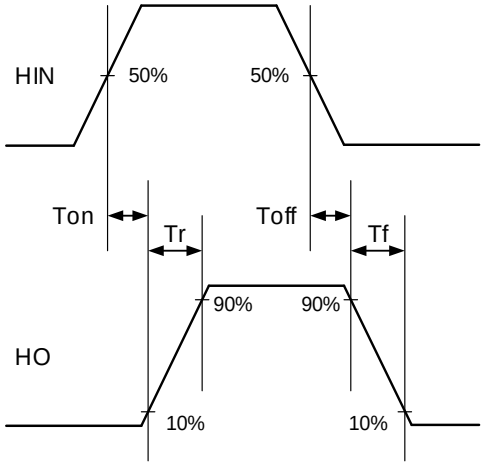
Electrical Characteristics

(Unless otherwise specified, test conditions are 25°C, VCC=8V, VM=80V)

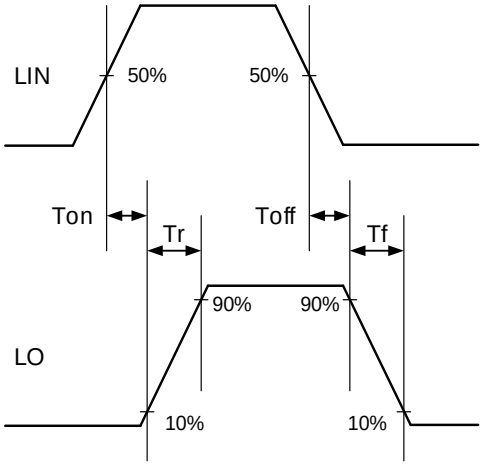
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Section						
V_{VHBR}	HBx Rising Threshold	$V_{HBRx} = V_{HBx} - V_{HSx}$		3.8		V
V_{VHBF}	HBx Falling Threshold			2.2		V
V_{VHBH}	HBx Threshold Hysteresis			1.6		V
I_{Q-VCC}	VCC Quiescent Current	HINx = LINx = 0，VSx=0		50	200	μA
		HINx=1，LINx=0				uA
		HINx=0，LINx=1				uA
I_{BL}	Bootstrap Supply Leakage Current	HBx = HSx = 100 V			50	μA
		150℃			150	uA
I_{OP}	Dynamic Operating Current	Complementary 25k, 50%, PWM, No Load		1.8	2.9	mA
Input Section						
V_{IH}	High-Level Input Threshold Voltage		2.2			V
V_{IL}	Low-Level Input Threshold Voltage				0.7	V
V_{IN-Hys}	Input Pin Threshold Voltage Hysteresis		0.7			V
R_{IN}	Input Pin Pull-Down Resistance			200		kΩ
Output Section						
I_{HPU}	High-Side Pull-Up Current	HOx = HSx，HINx=1		170		mA
I_{HPD}	High-Side Pull-Down Current	HOx = HBx，HINx=0		150		mA
I_{HPDST}	High-Side Strong Pull-Down Current	HINx=0，HOx=HSx+5V		2.5		A
I_{LPU}	Low-Side Pull-Up Current	LOx=0，LINx=1		140		mA
I_{LPD}	Low-Side Pull-Down Current	LOx=VCC，LINx=0		150		mA
I_{HPDST}	Low-Side Strong Pull-Down Current	LINx=0，LOx=LSS+5V		2.5		A

R_{HPD}	HO Output Strong Pull-Down Resistance	HOx=HSx+100mV，HINx=0		0.8	1	Ω
R_{LPD}	LO Output Strong Pull-Down Resistance	LOx=100mV，LINx=0		0.8	1	Ω
Dynamic Parameters						
t_{PDLH}	Turn-On Propagation Delay Time			100	250	ns
t_{PDHL}	Turn-Off Propagation Delay Time			100	250	ns
t_{PDRM}	Low-to-High Propagation Delay Matching				60	ns
t_{PDFM}	High-to-Low Propagation Delay Matching				60	ns
t_{RISE}	Output Rise Time	10% ~ 90%, C_L = 1nF		100	170	ns
t_{FALL}	Output Fall Time	10% ~ 90%, C_L = 1nF		50	90	ns
DT	Dead Time	C_L = 1nF	50	100	150	ns

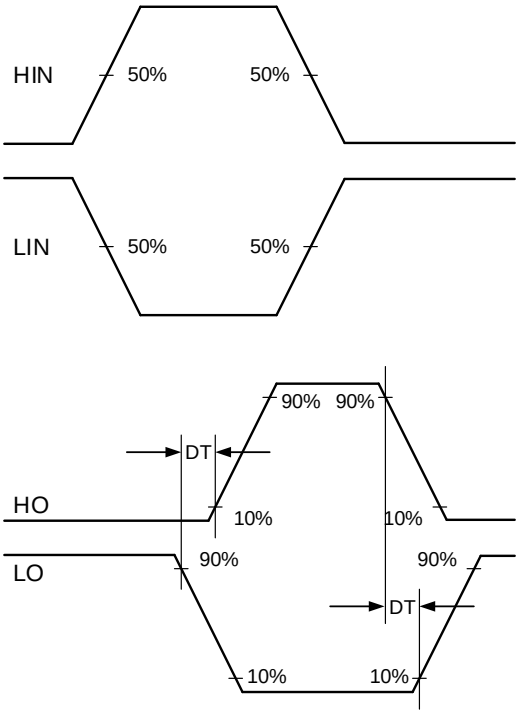
Switching Characteristics Diagram



High-Side Output HOx Switching Time Waveform



Low-Side Output LOx Switching Time Waveform

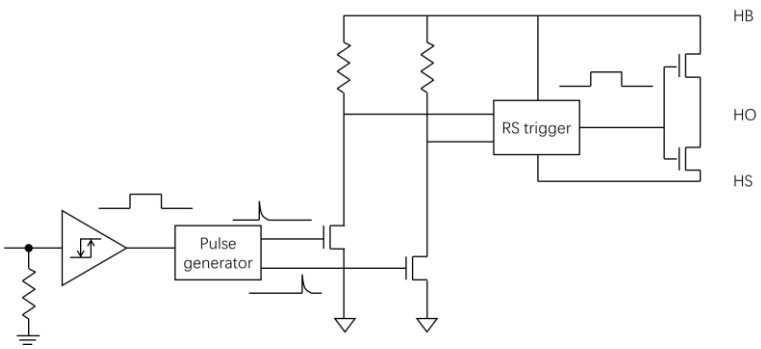


Dead Time Waveform Diagram

Level Shifter

A level shifter circuit is required as an interface from the input (HINx) to the high-voltage side drive (HOx), which is referenced to the switching node (HSx). This allows the control of the HOx output with respect to the HSx pin and provides low-latency matching with the low-side input.

Traditional level shifting circuits use a " level reconstruction" driving method (as shown in the figure below). The drive signal first passes through a pulse generator that generates two short pulses at the rising and falling edges. These short pulses are transmitted to the high rail and then reconstructed to a drive signal through an RS flip-flop. This approach is prone to RS flip-flop false-trigger or miss-trigger due to interference, and the system cannot detect or correct the fault once it occurs.



Traditional Level Shifter Scheme

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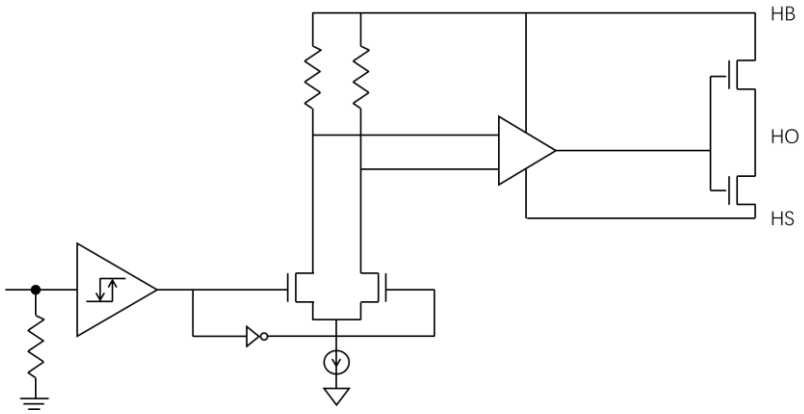
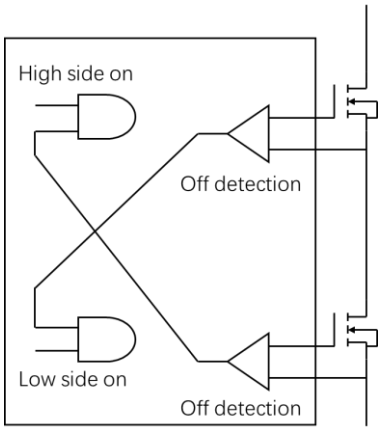
The ZH639D0 achieves level shifting using a real-time differential level shifter, avoiding false triggering, miss triggering caused by high-speed dv/dt and RS flip-flops. At the same time, the system's maximum frequency can be increased, maintaining correct logical output even under strong interference.



ZH639D0 Level Shifter Scheme

Adaptive Dead Time

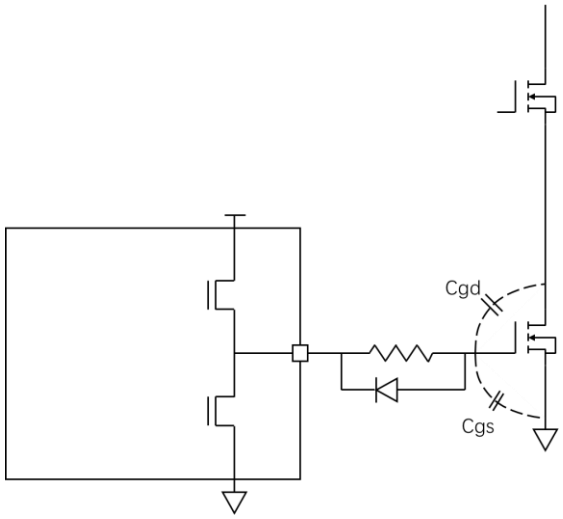
Under different load power transistor parameters, working voltages, and operating temperatures, the rise and fall times of the gate voltage will change. Traditional dead time generation methods use fixed dead time and cannot adapt to these parameter changes. This results in wasted dead space under light loads, causing output waveform distortion, while insufficient dead time under heavy loads, causing potential cross-conduction between the upper and lower transistors. The ZH639D0 uses feedback-based adaptive dead time control. During the turn-off process of the upper transistor, the driver chip continuously monitors the completion status of the upper transistor. Once the turn-off is fully completed, it notifies the lower transistor's drive signal to turn on. Similarly, during the turn-off process of the lower transistor, the driver chip continuously monitors the completion status of the lower transistor. Once the turn-off is fully completed, it notifies the upper transistor's drive signal to turn on. This design aims to minimize the dead time as much as possible while ensuring safety.



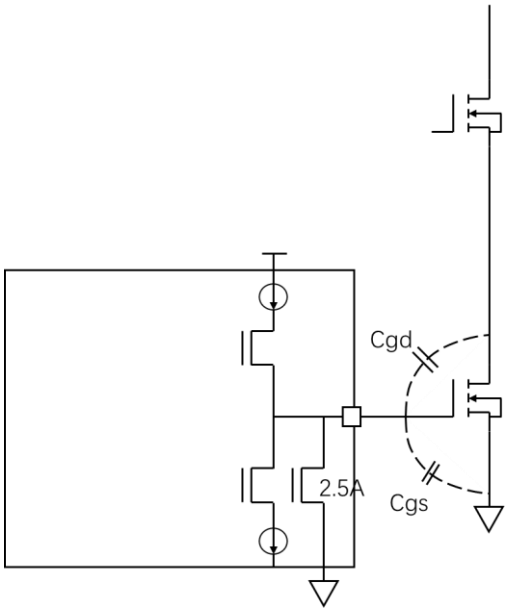
Adaptive Dead Time

Driving Capability

Traditional driving circuits apply voltage output, use external resistor for current limiting, and diode conducting (as shown in the diagram below). The use of resistor is to slow down the dv/dt and di/dt during the power transistor's conduction, improving EMI and avoiding interference or false triggering caused by rapid changes in voltage and current. The use of diode ensures that during the power transistor's turn-off, the gate has low-impedance pull-down capability to prevent false turn-on of the power transistor, due to coupling of the Cgd capacitance.



Traditional Driving Circuit



Dual-stage driving circuit

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ZH639D0 adopts current-limiting output. Its shutdown logic employs dual-stage driving: the first stage ensures appropriate shutdown dv/dt and di/dt, while the second stage guarantees low impedance in fully shutdown state. Users do not need to connect external resistors or diodes; ZH639D0 reliably achieves switching on and off operations.

Based on I_{HPU}，I_{HPD}，I_{LPU}，I_{LPD}, and the value of Cgd or Qgd of the power transistors. The rising slope, falling slope, rising time, and falling time of the HS node during system operation can be calculated. The formulas are:

dv/dt = I/Cgd

dt = Qgd/I

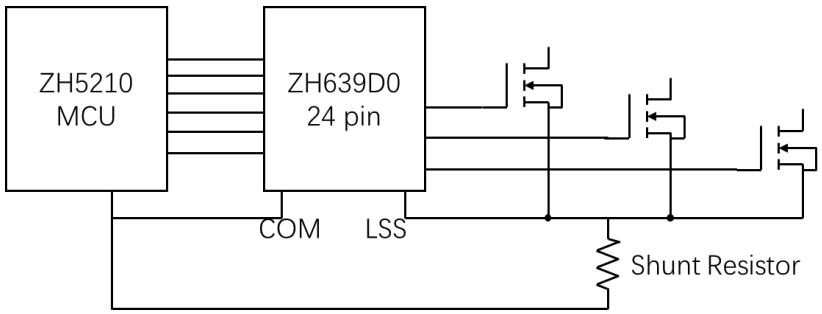
For a 100A MOS transistor with Qgd approximately 40nC, the rise time and fall time can be calculated to be approximately 200ns.

Startup and Undervoltage Protection

The high-side integrates an undervoltage protection circuit, which monitors the bootstrap voltage (HBx-HSx). When the bootstrap voltage is insufficient, the high-side output ignores the input (HINx) logic and remains low (turning off the power transistor). After the voltage on the bootstrap capacitor is sufficient to safely turn on the upper drive transistor, HOx begins to respond to the logic of HINx. During high-side undervoltage conditions, the low-side can operate normally.

Dual GND Design

Gate drivers are used between the MCU and power transistors (MOS or IGBT). During operation, gate currents and the source-drain currents of the power transistors cause fluctuations in the system's ground (GND), affecting normal operation of the system. The ZH639D0 (24-pin version) is designed with a dual GND configuration: COM serves as the logical reference ground, sharing the same potential as the MCU ground, ensuring undisturbed transmission of input signals LINx and HINx logic. LSS stands for low-side source (LSS), connected to the low-side source of the power transistor, ensuring a minimal path for gate drive current. In PCB design, for the 20-pin version, it is recommended to connect COM preferably to the power ground; for the 24-pin version, connecting the bottom heat sink pad to the COM pin and LSS to the power ground is recommended.



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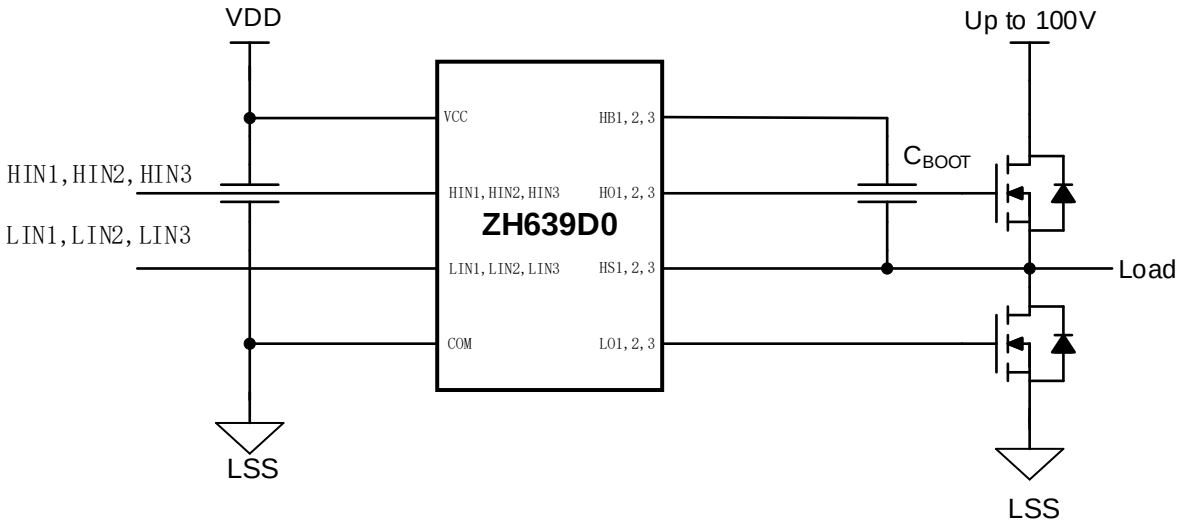
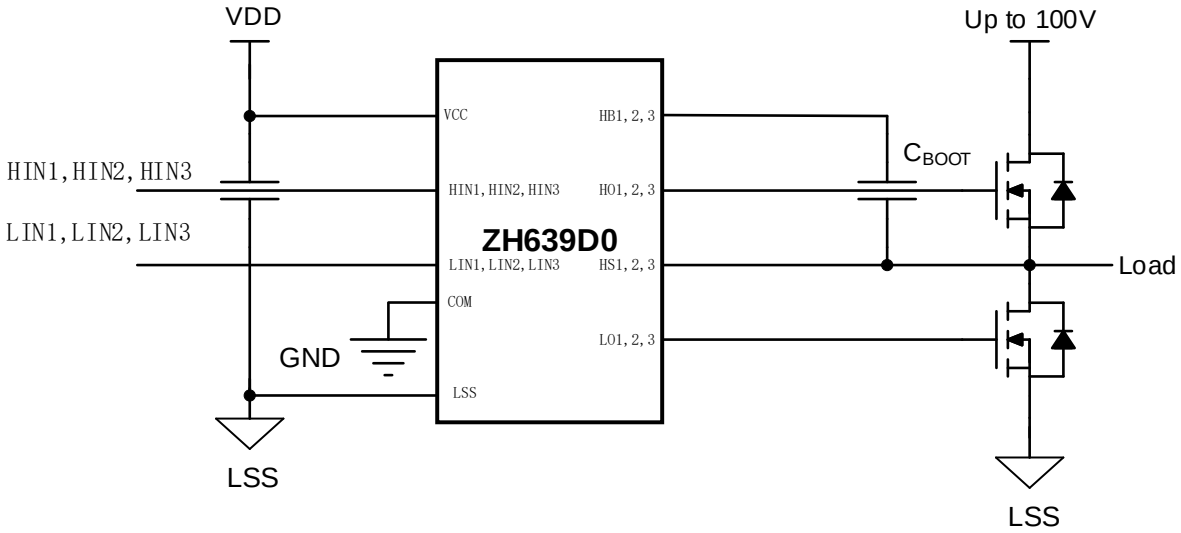
100V Three-Phase Half-Bridge Gate Driver

Typical Applications

TSSOP20



QFN24



Truth Table Inputs and Outputs

Inputs		Outputs	
HINx	LINx	HOx	LOx
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L
Floating	Floating	L	L

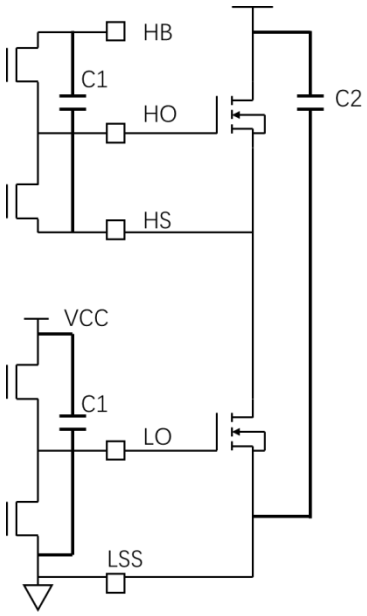
Application Notes

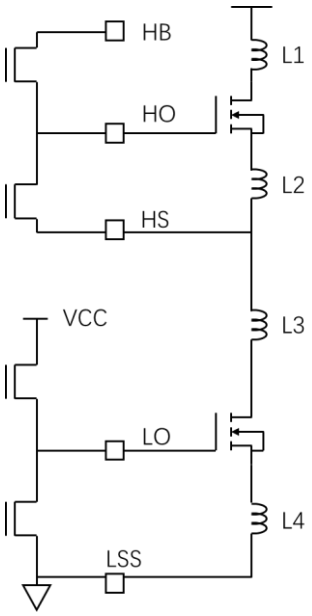
Circuit board layout is crucial to achieve optimal performance of high-side and low-side gate drivers. Please follow the following notes (using MOSFETs as an example):

1.Low ESR / ESL capacitors between VCC and COM pins, and HBx and HSx pins, must be placed close to the chip pins to support peak currents drawn from VCC and HBx during external MOSFET turn-on (see C1 in the lower left figure).

2.To prevent large voltage transients at the Drain of the top MOSFET, connect a low ESR electrolytic capacitor and a high-quality ceramic capacitor between the Drain and Ground (LSS) of the MOSFET (see C2 in the lower left figure).

3.Minimize parasitic inductance between the Source of the top MOSFET and the Drain of the bottom MOSFET (synchronous rectifier) to avoid large negative transients on the switch node (HSx pin) (see lower right figure).

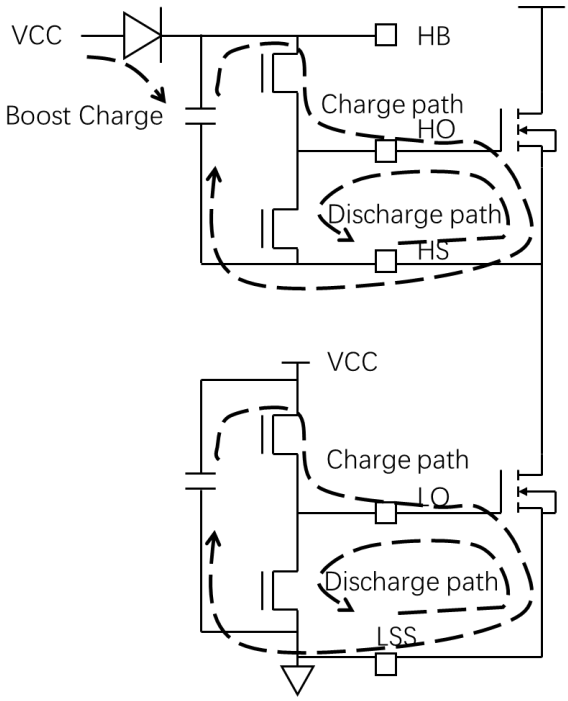




Grounding Considerations:

1 The primary consideration in designing grounding connections is to confine the current loop for charging and discharging MOSFET gates within the smallest physical area possible. This minimizes circuit inductance and reduces noise issues on MOSFET gate terminals. Gate drivers should be placed as close as possible to the MOSFETs.

2 The second consideration involves high-current paths, including bootstrap capacitors, local ground reference bypass capacitors, and body diodes of low-side MOSFETs. Bootstrap capacitors charge cyclically via bootstrap diodes (internal), bypassing capacitors from the ground reference VCC. These charging intervals are brief but entail high peak currents. Minimizing circuit board loop lengths and areas is crucial for ensuring reliable operation.



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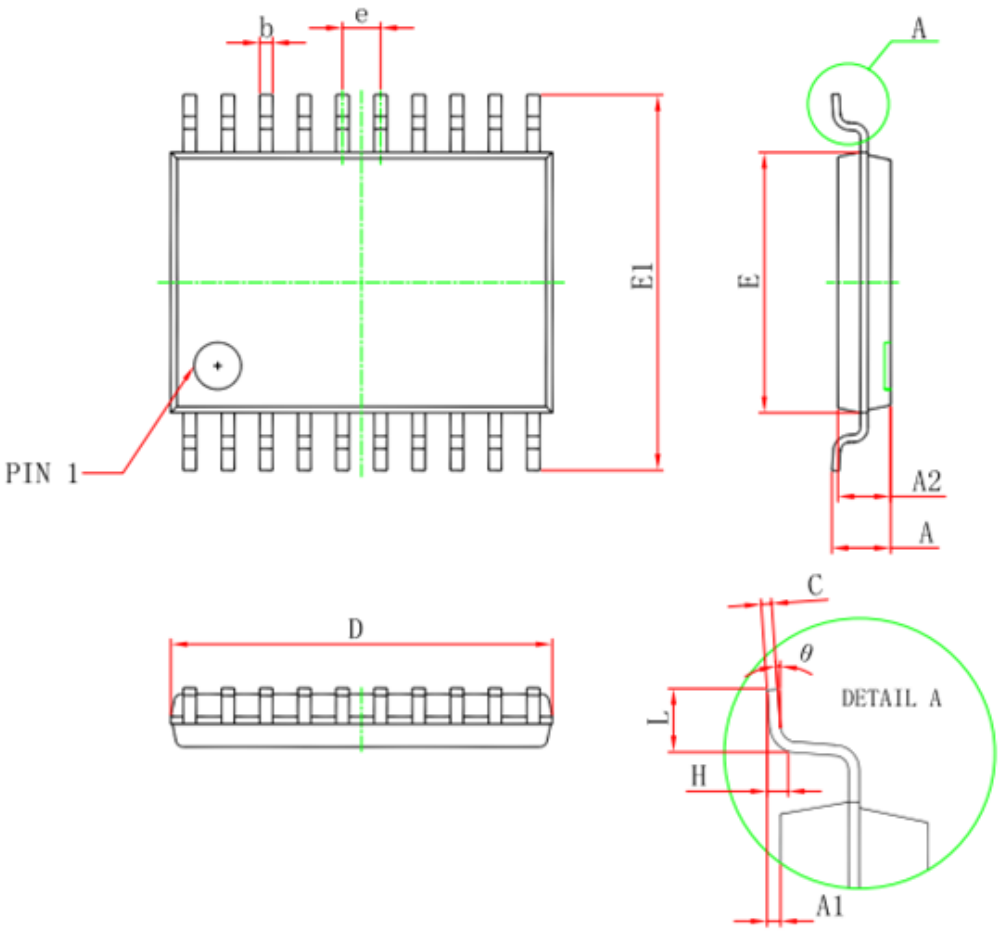
Package

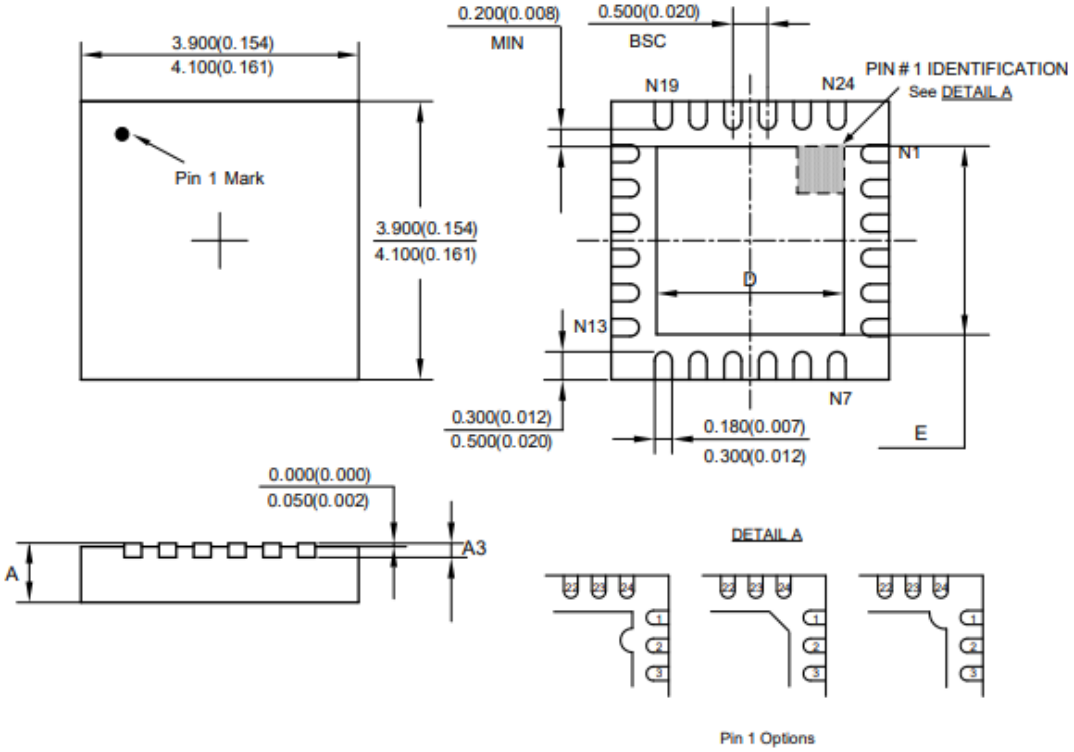
TSSOP20



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

100V Three-Phase Half-Bridge Gate Driver

QFN24



Symbol	D=E				A				A3			
	min(mm)	max(mm)	min(inch)	max(inch)	min(mm)	max(mm)	min(inch)	max(inch)	min(mm)	max(mm)	min(inch)	max(inch)
Option1	2.600	2.800	0.102	0.110	0.700	0.850	0.028	0.033	0.153	0.253	0.006	0.010
Option2	2.350	2.550	0.093	0.100	0.700	0.850	0.028	0.033	0.153	0.253	0.006	0.010
Option3	2.600	2.800	0.102	0.110	0.550	0.650	0.022	0.026	0.125	0.175	0.005	0.007

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Revision History

Version	Modification Date	Modification Details
V1.6	2024.06.18	Generates the English Version Datasheet.

单击下面可查看定价，库存，交付和生命周期等信息

>>Semiment (赛卓电子)