SC69401

Hall Effect Angle Position Sensors

Product Features

- High-precision rotary absolute angle position detection
- Simple magnetic circuit design
- Wide operating temperature range: -40° C to +160° C
- Selectable output modes: Analog, PWM, SPI
- Programmable angular measuring range (angles up to 360 degrees)
- Programmable linear transmission characteristics (any 4-point, 8-point, or range-selectable 16-segment, 32-segment equally divide curves)
- 32-bit programmable user ID
- Differential Hall sensing to resist stray magnetic field interference
- Rich on-chip diagnostic capabilities
- Disconnect diagnostics (broken V_{DD}, broken V_{SS})
- Over-current and over-voltage protection; under-voltage detection
- Conforms to AEC_Q100
- Conforms to ISO26262 Functional Safety ASIL Ready
- Single chip SOP-8 and dual redundant chip eTSSOP-16L packages - lead-free, both comply with EU RoHS hazardous substance requirements

Product Applications

- Non-contact absolute angular position detection
- Accelerator pedal sensor
- Steering wheel angle sensor
- Shifter gear position detection
- Throttle and exhaust gas recirculation valve
- Ride height of vehicle
- Rotary switch

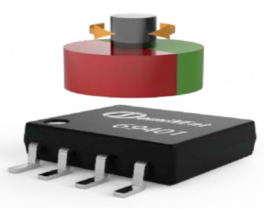
Product Description

The SC69401 is an angular position sensor chip based on the principle of differential Hall magnetic sensing from Semiment Electronics. A full differential Hall sensing matrix is built into the center of the chip, which generates a corresponding sine-cosine position signal by sensing a pair of polar S/N magnets above it. The signal is amplified by a preamplifier and then sampled by the internal analog-to-digital converter circuitry. The chip's proprietary DSP circuitry performs angular arithmetic, and finally outputs the absolute position information (0-360 degrees) of the magnet's rotation in a variety of interface formats.

The SC69401 provides a variety of output methods: analog output proportional to the rotation angle, PWM output, and 4-wire SPI bus. The output curve can be selected from any 4-point, 8-point, or 16-segment, 32-segment, or any other programming method.

The SC69401, a sensor chip primarily for automotive applications, provides a rich set of on-chip diagnostic functions. The chip was designed and developed following the ISO 26262 standard and is ASIL-B Level.

The SC69401 is suitable for non-contact detection of the mounting position on the axle and is suitable for applications such as automotive gas pedals, electronic throttles, EGR valves, gear shifters, body heights and steering wheel angle.



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Ordering Information

Product Code	Package Form	Package	Operating temperature	Description
SC69401	Tape & Reel, 3000pcs/reel	SOP-8	-40°C ~ 160°C	Default Analog Output
SC69401-SPI	Tape & Reel, 3000pcs/reel	SOP-8	-40°C ~ 160°C	Default SPI Interface
SC69401D	Tape & Reel, 3000pcs/reel	eTSSOP-16L	-40°C ~ 160°C	Default Analog Output
SC69401D-SPI	Tape & Reel, 3000pcs/reel	eTSSOP-16L	-40°C ~ 160°C	Default SPI Interface

Pin Description

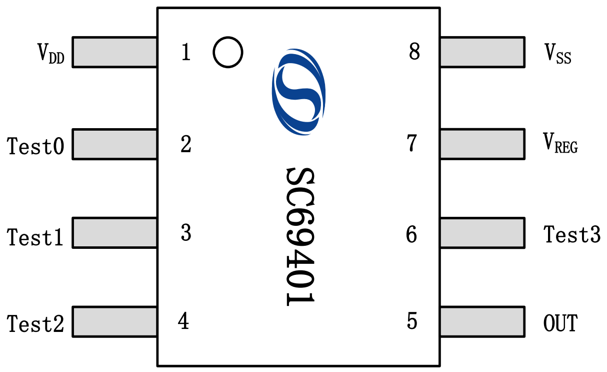

Figure-1: SOP-8 Package

PIN		Type	Description
Symbol	Number		
V_{DD}	1	Power supply	Power Input
Test0	2	Test/Digital Output	Test pin, connect to Ground; SPI_MISO: Master in Slave out data pin for SPI
Test1	3	Test	Test Pins, connect to ground

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Test2	4	Test/Digital Inputs	Test pin, connect to ground; SPI_SCLK: SPI clock signal input.
OUT	5	Outputs/Digital Inputs	Analog output; PWM; SPI_CS: SPI enable input pin
Test3	6	Test/Digital Inputs	Test pin, connect to ground; SPI_MOSI: SPI master-out slave-in data pin
V_{REG}	7	Power output	Internal power supply
V_{SS}	8	Ground	Ground

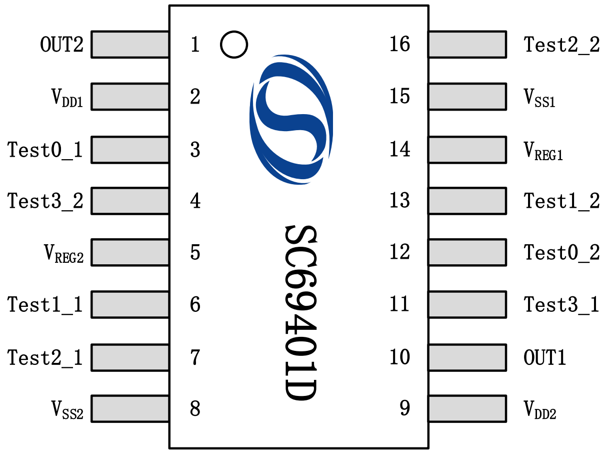

Figure-2: eTSSOP-16 Package

PIN		Type	Description
Symbol	Number		
OUT2	1	Outputs/Digital Inputs	Chip 2 - analog output; PWM; SPI_CS: SPI enable input pin
V_{DD1}	2	Power supply	Chip 1 - Power Input
Test0-1	3	Test/Digital Output	Chip 1 - test pin, connect to ground; SPI_MISO: master-in slave-out data pin for SPI
Test3-2	4	Test/Digital Inputs	Chip 2 - test pin, connect to ground; SPI_MOSI: master-out slave-in data pin for SPI
V_{REG2}	5	Power output	Chip 2 - Internal Power Supply
Test1-1	6	Test	Chip 1 - test pin, connect to ground
Test2-1	7	Test/Digital Inputs	Chip 1 - test pin, connect to ground; SPI_SCLK: SPI clock signal input.
V_{SS2}	8	Ground	Chip 2 - Ground
V_{DD2}	9	Power supply	Chip 2 - Power Input
OUT1	10	Outputs/Digital	Chip 1 - analog output; PWM; SPI_CS: SPI enable input pin

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		Inputs	
Test3-1	11	Test/Digital Inputs	Test pin, connect to ground; SPI_MOSI: SPI master-out slave-in data pin
Test0-2	12	Test/Digital Output	Chip 2 - test pin, connect to ground; SPI_MISO: master-in slave-out data pin for SPI
Test1-2	13	Test	Chip 2 - test pin, connect to ground
V_{REG1}	14	Power output	Chip 1 - Internal Power Supply
V_{SS1}	15	Ground	Chip 1 - Ground
Test2-2	16	Test/Digital Inputs	Chip 2 - test pin, connect to ground; SPI_SCLK: SPI clock signal input.

Functional block diagram

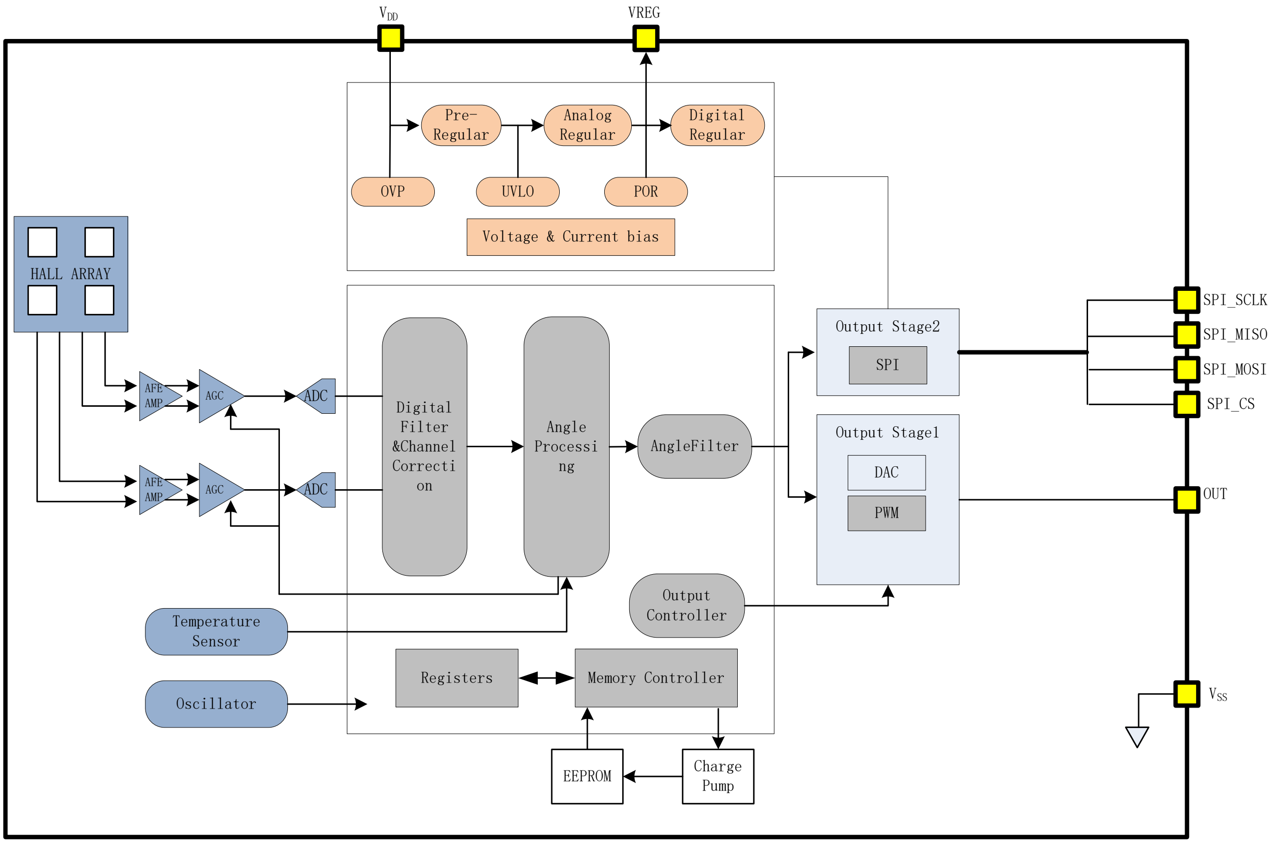

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Figure-3: Functional block diagram of the chip

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Limit parameters

Parameters	Symbol	Test Conditions	MIN	MAX	Unit
Supply Voltage	V_{DD}	<60S	-14	28	V
Analog Output Voltage	V_{OUT}	<60S	-6	18	V
Reverse Output Current	I_R			40	mA
Operating Temperature	T_A		-40	160	℃
Storage Temperature	T_S		-40	160	℃
Magnetic Field Strength	H		-1	1	T

Exceeding the absolute maximum ratings may result in permanent damage to the device, and prolonged operation at the absolute maximum ratings may affect the reliability of the device.

ESD

Human body model (HBM) testing according to EIA/JESD22-A114-B HBM

Type	Symbol	MIN	MAX	Unit
HBM	V_{ESD}	-4	4	kV

Dual Chip Isolation Parameters

Parameters	Symbol	MIN	MAX	Unit
Isolation Resistor	IsoR	4		MΩ

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Electrical parameter

Parameters	Symbol	Test Conditions	MIN	Typ	MAX	Unit
Supply Voltage	V_{DD}	5V Mode	4.5	5.0	5.5	V
	$V_{DD\_3.3V}$	V_{REG} and V_{DD} are connected to 3.3V UVLO_3P5EN=1	3.15	3.3	3.6	V
Supply Current	I_{DD}	Single die SOP-8		8	10	mA
Isurge Current	Isurge	Single die SOP-8			50	mA
Overcurrent Alarm	I_{OCP}	Single die SOP-8		25	35	mA
Regulated Voltage	V_{REG}		3.1	3.37	3.5	V
Regulated Voltage Overdrive Detection	V_{REGOVP}		3.65	3.75	3.85	V
Regulated Voltage Low Detection	V_{REGUVL}		2.7	2.8	2.9	V
Undervoltage Detection Voltage	V_{UVLO}	UVLO_3P5EN = 0	3.4	3.7	4.2	V
		UVLO_3P5EN = 1	2.6	2.8	3.1	V
Undervoltage Detection Hysteresis	$V_{UVLOHYS}$		150		350	mV
Overvoltage Protection Voltage	V_{OVP}		5.8	6.2	6.6	V
Overvoltage Detection Hysteresis	$V_{OVPHYST}$		100		600	mV
Output Short-circuit Current	Ishort	Shorted to Ground, Analog Output			15	mA
		Short to Ground, PWM Push-Pull Outputs			50	mA
		Shorted to V_{DD} Analog Output			15	mA
		Shorted to V_{DD}, PWM Push-Pull Outputs			50	mA
Analog Output Load Resistance	R_L	Pull-up resistor, connected to V_{DD}	4.7		470	KΩ
		Pull-down resistor, connected to ground	4.7		470	KΩ
PWM Output Load Resistance	R_{L_PWM}	Pull-up resistor, connected to V_{DD}	1			KΩ
		Pull-down resistor,	1			KΩ

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		connected to ground				
Analog Output Saturation Level	Vsat_lo	Pull-up resistor R=10k, connected to V_{DD}		0.5	2	$\%V_{DD}$
		Pull-up resistor R=4.7k, connected to V_{DD}		2.5	3	$\%V_{DD}$
	Vsat_hi	Pull-down resistor R=4.7k, connected to ground	96.5	97.5		$\%V_{DD}$
		Pull-down resistor R=10k, connected to ground	97.5	98		$\%V_{DD}$
Active Diagnostic Output Level	Dsat_lo	Pull-down resistor $R\leq470k$		1	2	$\%V_{DD}$
		Pull-down resistor $R\leq10k$		0.5	1	$\%V_{DD}$
	Dsat_hi	Pull-up resistor $R\leq10k$	97.5	98		$\%V_{DD}$
Passive Diagnostic Output Level (broken)	BV_{SS} PD	Broken V_{SS}, pull-down resistor, $4.7K\leq R\leq100k$		0	3	$\%V_{DD}$
	BV_{SS} PU	Broken V_{SS}, pull-up resistor, $4.7K\leq R\leq100k$	97	98		$\%V_{DD}$
	BV_{DD} PD	Broken V_{DD}, pull-down resistor, $4.7K\leq R\leq100k$		0	1	$\%V_{DD}$
	BV_{DD} PU	Broken V_{DD}, pull-up resistor, $4.7K\leq R\leq100k$	96.5	98		$\%V_{DD}$
Programmable Clamp Voltage	Clamp_lo	Programmable	0		100	$\%V_{DD}$
	Clamp_hi	Programmable	0		100	$\%V_{DD}$

Based on the description in the table above, the SC69401 can meet the output range settings for the typical application of Figure-4

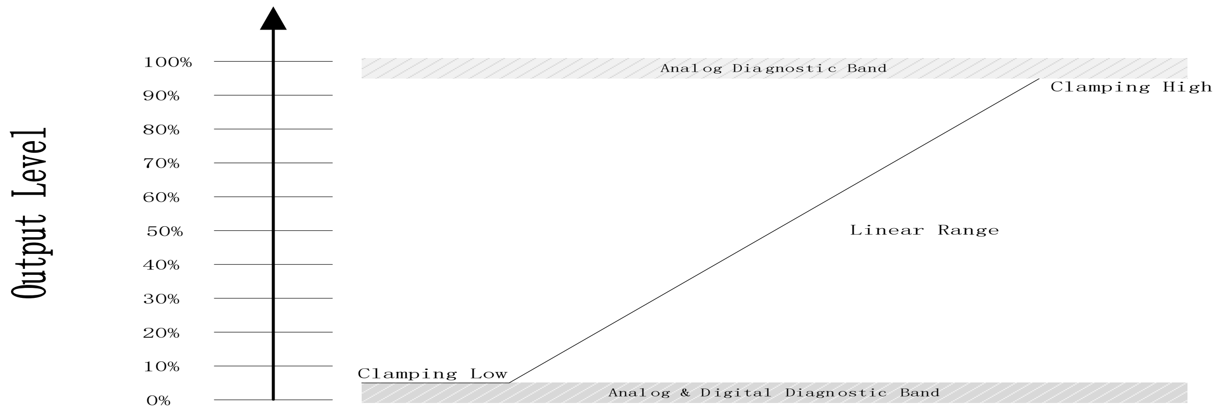

Figure-4: Example of Output Range for Typical Application

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Timing parameter

◆ Basic timing

Parameters	Symbol	Test Conditions	MIN	Typ	MAX	Unit
Main Clock Frequency	F_{CK}	Full Temperature Test	7.8	8.2	8.5	MHz
Main Clock Frequency Temperature Offset	$\Delta_{FCK,T}$		-3		3	$\%F_{CK}$
Data Refresh Frequency	Tper		121	128	134	us
Step Response Time	Ts			128		us
Power-on Reset	T_{POR}			40		us
Initialization Time	T_{INIT}			16.384		ms
Analog Output Slew-rate	SR	C_{OUT} =100nF		60		V/ms
		C_{OUT} =10nF		80		V/ms
		C_{OUT} =47nF		85		V/ms
		C_{OUT} =330nF		20		V/ms

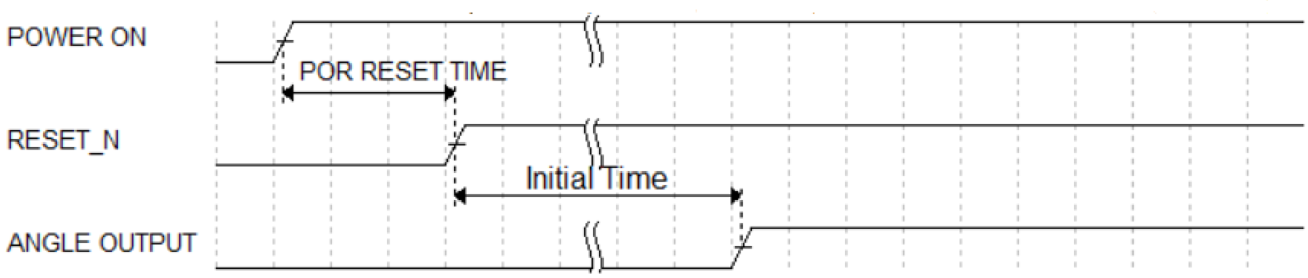

Figure-5: Power-on reset timing

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◆ EEPROM Timing

Parameters	Symbol	Test Conditions	MIN	Typ	MAX	Unit
Power-on Reset Time	t_{PS}			100		us
	t_{PW}			100		us
Standby Time	TIDLE			20		ms

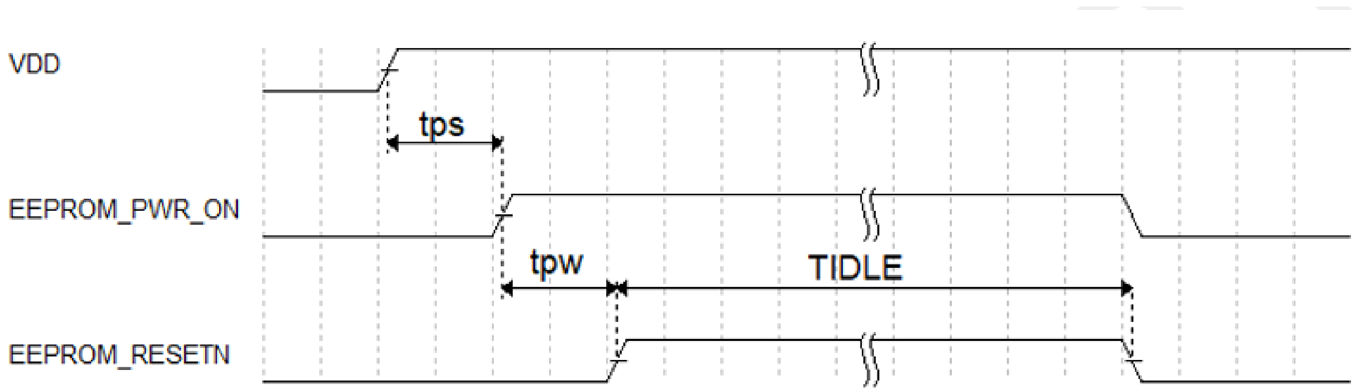

Figure-6: EEPROM Timing

◆ PWM output

Parameters	Symbol	Test Conditions	MIN	Typ	MAX	Unit
PWM Frequency	F_{PWM}	Frequency range	125, 250, 500, 1000, 2000			Hz
PWM Frequency Initial Tolerances	F_{PWM_Init}	25°C			±2%	F_{PWM}
PWM Frequency Thermal Drift	ΔF_{PWM}	PWM frequency temperature drift			±3%	F_{PWM}
PWM Output Rise Time (open-drain output)	Trise_LSD	4.7nF, R_L=1KΩ pull-up		10		us
		4.7nF, R_L=10KΩ pull-up		100		us
		10nF, R_L=1KΩ pull-up		20		us
PWM Output Rise Time (push-pull	Trise_PP	4.7nF, R_L=1KΩ pull-up		3		us
		4.7nF, R_L=10KΩ pull-up		3		us

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output)		10nF, R_L=1KΩ pull-up		4		us
PWM Output Fall Time (open-drain output)	Tfall_LSD	4.7nF, R_L=1KΩ pull-up		2		us
		4.7nF, R_L=10KΩ pull-up		2		us
		10nF, R_L=1KΩ pull-up		4		us
PWM Output Fall Tme (push-pull output)	Tfall_PP	4.7nF, R_L=1KΩ pull-up		2		us
		4.7nF, R_L=10KΩ pull-up		2		us
		10nF, R_L=1KΩ pull-up		4		us

* The SC69401 can support the remaining PWM frequency settings in the form of parameter adjustments, please consult the technical support team at Semiment.

◆ SPI output

Parameters	Symbol	Test Conditions	MIN	Typ	MAX	Unit
High Level Input Voltage	V_{IH}		0.7*V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}		0		0.3*V_{DD}	V
High Level Output Voltage	V_{IH}		V_{DD}-0.35		V_{DD}	V
Low Level Output Voltage	V_{IL}		0		V_{SS}+0.35	V
Clock Cycle	tSCLK	EE_PINFILTER = 1	450	500		ns
		EE_PINFILTER = 2	900	1000		ns
		EE_PINFILTER = 3	1800	2000		ns
Clock Low	tSCLK_LO	EE_PINFILTER = 1	225			ns
		EE_PINFILTER = 2	450			ns
		EE_PINFILTER = 3	900			ns
Clock High	tSCLK_HI	EE_PINFILTER = 1	225			ns
		EE_PINFILTER = 2	450			ns
		EE_PINFILTER = 3	900			ns
Output Data Delay Time	tMISO	EE_PINFILTER = 1, C_L = 30pF			210	ns
		EE_PINFILTER = 2, C_L = 30pF			300	ns

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		EE_PINFILTER = 3, C_L = 30pF			510	ns
Data Capture Establishment Time	tMOSI			30		ns
Initial Clock Delay Time	t1	EE_PINFILTER = 1	225			ns
		EE_PINFILTER = 2	450			ns
		EE_PINFILTER = 3	900			ns
Initial Output Data Setup Time	t2	EE_PINFILTER = 1		90	120	ns
		EE_PINFILTER = 2		180	210	ns
		EE_PINFILTER = 3		370	420	ns
Communication Completion Enable Hold Time	t3		225			ns
Communication Completion Output Hold Time	t4	EE_PINFILTER = 1		90	120	ns
		EE_PINFILTER = 2		180	210	ns
		EE_PINFILTER = 3		370	420	ns
Synchronized Pulse Period	tSyncPulse	EE_PINFILTER = 1	520		10000	ns
		EE_PINFILTER = 2	610		10000	ns
		EE_PINFILTER = 3	820		10000	ns

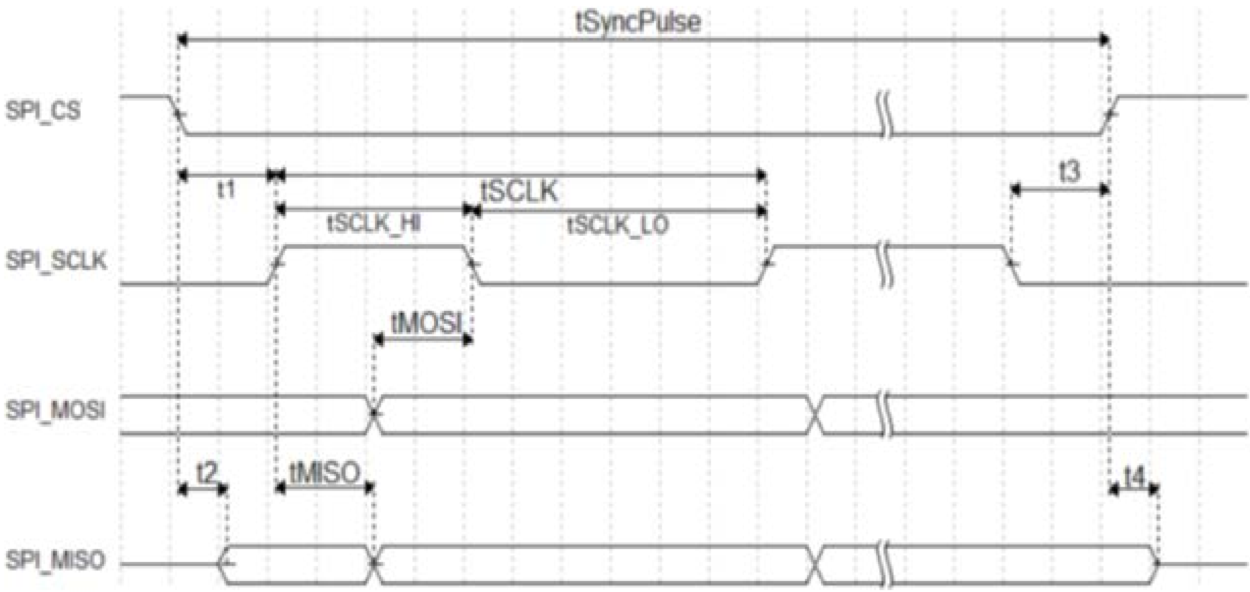

Figure-7: SPI Timing

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Precision parameters

◆ Analog output

Parameters	Symbol	Test Conditions	MIN	Typ	MAX	Unit
ADC Resolution	R_{ADC}			15		bits
Analog Output Resolution	R_{DAC}			12		bits
DAC Intrinsic Nonlinearity Error	INL			5		LSB
DAC Differential Nonlinear Error	DNL		0.05	1	3	LSB
Angular Offset Error	ΔE_{ang}		-1.2		1.2	Deg
Nonlinearity Error	ΔE_{L}		-1		1	Deg
Angular Temperature Drift Error	ΔE_{temp}		-0.5		0.5	Deg
Proportional Output Error	ΔE_{ratio}	$4.5V \leq V_{DD} \leq 5.5V$	-0.05	0	0.5	$\%V_{DD}$
Output Pole Noise	$N_{pk\text{-}pk}$			0.18	0.27	Deg

◆ PWM output

Parameters	Symbol	Test Conditions	MIN	Typ	MAX	Unit
PWM output resolution	RSP			12		bits
PWM % Duty Cycle Jitter (open-drain output)	J_{DC}	125Hz,4.7nF,R_L =1Kohm, Resistor Pull-Up		±0.003	±0.016	%DC
		250Hz,4.7nF,R_L =1Kohm, Resistor Pull-Up		±0.005	±0.02	%DC
		500Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up		±0.009	±0.035	%DC
		1000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up		±0.003	±0.016	%DC
		2000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up		±0.005	±0.02	%DC

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PWM % Duty Cycle Jitter (push-pull output)	J_{DC}	125Hz,4.7nF,R_L =1Kohm, Resistor Pull-Up		±0.003	±0.016	%DC
		250Hz,4.7nF,R_L =1Kohm, Resistor Pull-Up		±0.005	±0.02	%DC
		500Hz,4.7nF,R_L =1Kohm, Resistor Pull-Up		±0.009	±0.035	%DC
		1000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up		±0.003	±0.016	%DC
		2000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up		±0.005	±0.02	%DC
PWM Frequency Jitter (open-drain output)	J_{PWM}	125Hz-2000Hz,4.7nF,R_L =1Kohm,Resistor Pull-Up		±0.04	±0.15	Hz
PWM Frequency Jitter (push-pull output)	J_{PWM}	125Hz-2000Hz,4.7nF,R_L =1Kohm,Resistor Pull-Up		±0.04	±0.15	Hz

Jitter is defined as ±3σ , σ is the standard deviation of 1000 normal waveforms. %DC: %Duty Cycle

Magnetic parameter

Parameters	Symbol	Test Conditions	MIN	Typ	MAX	Unit
Magnetic Field Strength	H_{EXT}		10		120	mT
Magnet Diameter	D_{mag}			6		mm
Magnet thickness	H_{mag}			2.5		mm
Airgap Between Magnet and Chip	AG		0.5		3	mm
Magnet Material				NdFeB 35		

*The magnet is a radially magnetized pair of pole disc magnet.

*Magnetic parameter measurements in this datasheet were obtained using the magnet conditions described above.

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User programmable parameters

Parameters	Description	default	Bits
OUT mode	output mode	0	2
PWM POL	PWM Polarity	0	1
PWMT	PWM frequency	0	3
OUT_CONFIG	PWM Output Configuration	0	2
GAIN_G	Analog op amp first stage gain setting	0	2
AGC	Automatic gain control of the second stage of an analog op amp	1	1
GAIN_F	Analog op amp second stage gain setting	1	5
SEMI_ID1	Semiment Factory ID	xxx	8
SEMI_ID2	Semiment Factory ID	xxx	8
SEMI _ID3	Semiment Factory ID	xxx	8
SEMI _ID4	Semiment Factory ID	xxx	8
USER_ID1	user ID	0	8
USER_ID2	user ID	0	8
USER_ID3	user ID	0	8
USER_ID4	user ID	0	8
EEPROM_LOCK_CODE	EEPROM_LOCK Bit Valid Judgment Code	0	7
EEPROM_LOCK	EEPROM Lock Bit	0	1
DIAG_EN	Diagnostic Enable Bit	1	1
DIAG_MASK	Diagnostic Mask Register	128	8
GAIN_THRESHOLD_LOW	Analog op amp second stage gain low thresholds	0	5
GAIN_THRESHOLD_HIGH	Analog op amp second stage gain high thresholds	31	5
FIELDTHOLD_LOW	low field strength threshold	0	8
FIELDTHOLD_HIGH	High field strength threshold	255	8
TEMPTHRESHOLD_LOW	Low temperature threshold	0	7
TEMPTHRESHOLD_HIGH	elevation threshold	127	7
DIAG_DEBOUNCE	Diagnostic debounce time	0	3
CLAMP_HIGH	Output High Clamp	60296	16

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CLAMP_LOW	Output Low Clamp	6653	16
DP	Break point/Zero Point	0	16
CW	direction of rotation	0	1
WORK_RANGE_GAIN	16-point/32-point calibrated operating angle range (degrees)	360	16
LNR_POINTS	Calibration point selection	3	2
LNR_A_X	4-point calibration , X-axis coordinates (angle)	0	16
LNR_B_X		0	16
LNR_C_X		0	16
LNR_D_X		0	16
LNR_A_Y	4-point calibration , Y-axis coordinates (%V_{DD})	0	16
LNR_B_Y		0	16
LNR_C_Y		0	16
LNR_D_Y		0	16
LNR_A_S	4-point calibration, slope of each segment	0	16
LNR_B_S		0	16
LNR_C_S		0	16
LNR_D_S		0	16
LNR4_S0	4-point calibration, initial slope	0	16
LNR4_Y5	4-point calibration, endpoint Y coordinate	0	16
LNR_Y0	4-point, 16-point/32-point calibration of the initial point Y-coordinate	0	16
LNR9_Yn	8-point calibration, Y-axis coordinates (n=0~8)	0	9x16
LNR9_Xn	8-point calibration, X-axis coordinates (n=0~8)	0	9x16
LNR17_Yn	16-point calibration, Y-axis coordinates (n=0~15)	0	17x16
LNR_DELTAYn	32-point calibration, Y-axis coordinates (offset %) (n=0~31)	0	32x8
LNR_DELTA_Y_EXPAND	32-point calibration, Y-axis coordinate deviation range setting	3	2

◆ Output mode

The SC69401 provides three output modes: proportional analog output, PWM output, and SPI bus output. PWM supports PMOS or NMOS open drain output and push-pull output, SPI only supports push-pull output.

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- **Analog Output Mode**

Parameters	Value	Description
OUT mode[1:0]	0	analog output
	1	PWM output
	2	reserve
	3	SPI output

- **PWM output mode**

PWM output polarity setting

Parameters	Value	Description
PWM POL	0	Active High
	1	Active Low

PWM output frequency setting

Parameters	Value	Description
PWMMT [2:0]	000	125
	001	250
	010	500
	011	1000
	others	2000

PWM output mode setting

Parameters	Value	Description
OUT_CONFIG [2:0]	0	Digital Output NMOS OpenDrain
	1	Digital Output PMOS OpenDrain
	2	digital push-pull output
	3	Digital High Resistance State Output

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PWM Output Waveform

PWM is set to PWM_POL=0, PWMT=011, and output duty cycle 0.0244%

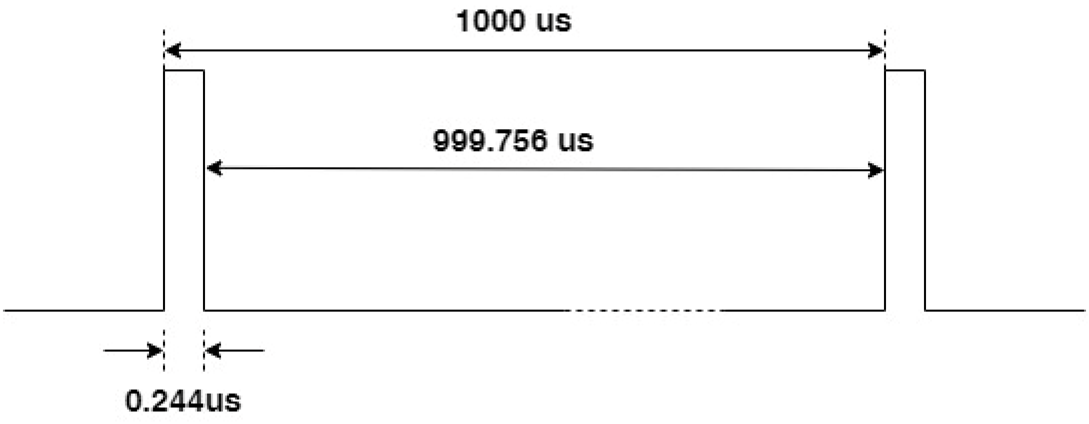

Figure-8: PWM output waveform when PWM_POL=0

PWM is set to PWM_POL=1, PWMT=011, output duty cycle 0.0244%

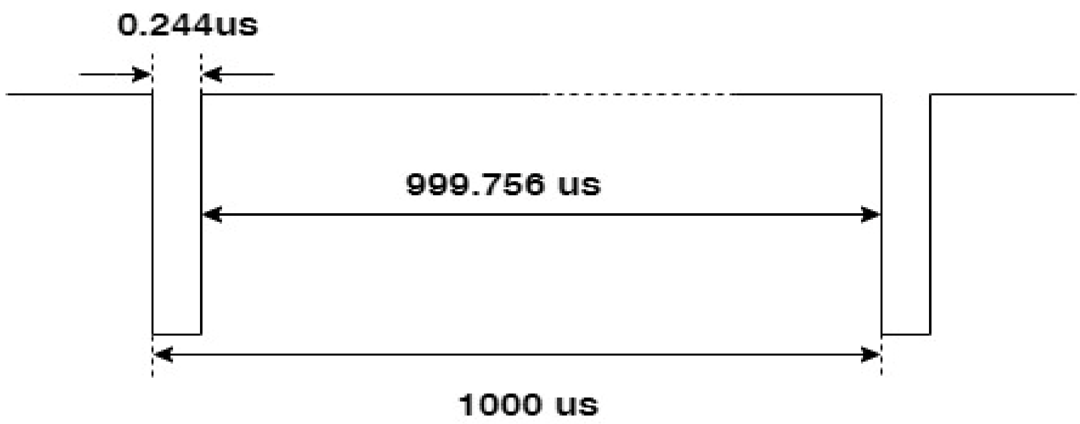

Figure-9: PWM output waveform when PWM_POL=1

- **Four-wire SPI protocol output (slave)**

SC69401 SPI is used as a full-duplex serial communication, in which the host can send commands and receive the result of the last command at the same time in one master-slave communication.SC69401 is used as a slave and controlled by the chip select signal SPI_CS.SPI communication is activated when SPI_CS is set to low level, and ends when SPI_CS is set to high level. SPI_SCLK is used as a clock for SPI communication, which is sent by the host to SC69401.MISO and MOSI signals are changed on the rising edge of the clock and captured on the

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falling edge of the clock.

Communications format

Command	Data transmission direction	Byte 0	Byte 1	Byte 2	Byte 3
Reads 16-bit angle values	master-to-slave	0x9C	0x00	0x00	CRC8
	slave to master	0x9C	AngleH	AngleL	CRC8
Read temperature and magnetic field strength values	master-to-slave	0xBC	0x00	0x00	CRC8
	slave to master	0xBC	Temp	FiledStrength	CRC8
Write Register Value	master-to-slave	0xCC	RegAddr	RegValue	CRC8
	slave to master	0xCC	RegAddr	RegValue	CRC8
Read Register Value	master-to-slave	0xC4	RegAddr	0x00	CRC8
	slave to master	0XC4	RegValue	(RegAddr+1)Value	CRC8

Output angle Angle = (AngleH<< 8 + AngleL)/65536 * 360

◆ Sensor Front End Setup

● First stage gain setting

Parameters	Value	Description
GAIN_G [2:0]	0	2.5
	1	5
	2	10
	3	10

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- **Second stage gain setting**

AGC enable is used to set the automatic gain control enable for the second stage gain. AGC =1 enables automatic gain control; AGC =0 disables automatic gain control.

If the AGC control bit is disenabled the second stage gain is set directly through the registers

Parameters	Value	Description
AGC	0	Disable automatic gain control
	1	Enable automatic gain control
GAIN_F [4:0]	0	1
	1	1.1
	2	1.21
	...	...
	29	15.86
	30	17.4
	31	20

◆ Traceable information

At the factory, each device contains the Semiment factory ID and user ID for traceable purposes

Parameters	Value
SEMI_ID1 [7:0]	0-255
SEMI_ID2 [7:0]	0-255
SEMI_ID3 [7:0]	0-255
SEMI_ID4 [7:0]	0-255
USER_ID1 [7:0]	0-255
USER_ID2 [7:0]	0-255
USER_ID3 [7:0]	0-255
USER_ID4 [7:0]	0-255

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◆ EEPROM write protection

Parameters	Value	Description
EEPROM_LOCK_CODE [6:0]	0x3A	EEPROM_LOCK bit active
	Other values	EEPROM_LOCK bit is invalid
EEPROM_LOCK	0	EEPROM can be read, written and erased.
	1	EEPROM read-only

◆ Diagnostic

- **Diagnostic Enable**

Parameters	Value	Description
DIAG_EN	0	Enable Diagnostics
	1	Disable Diagnostics

- **Diagnostic Mask Register: corresponding to mask bit to be 0, the fault will not trigger diagnosis; corresponding to mask corresponding to mask bit to be 1, the fault will trigger diagnosis.**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CRC Checksum Error	GAINF overflow	Current diagnosis	Digital Voltage Fault	CORDIC overflow	field strength overflow	-	temperature overflow

- **Diagnostic threshold**

Parameters	Value	Description
GAIN_THRESHOLD_LOW [4:0]	0-31	Second-stage analog op-amp gain low thresholds
GAIN_THRESHOLD_HIGH [4:0]	0-31	Second-stage analog op-amp gain high thresholds
TEMPTHRESHOLD_LOW [6:0]	0-127	Low-temperature threshold

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TEMPTHRESHOLD_HIGH [6:0]	0-127	High-temperature threshold
FIELDTHOLD_LOW [7:0]	0-255	low field strength threshold
FIELDTHOLD_HIGH [7:0]	0-255	High field strength threshold

- **Diagnostic debounce time setting**

Parameters	Value	STEP_UP TIME(ms)	STEP_DOWN TIME(ms)
DIAG_DEBOUNCE [2:0]	0	20	20
	1	20	30
	2	20	40
	3	40	40
	4	60	80
	5	80	100
	6	100	120
	7	120	140

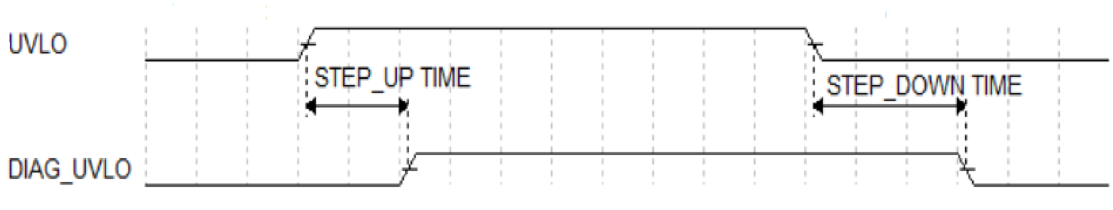

Figure-10: Diagnostic debounce timings

◆ Output parameter setting

- **Breakpoint/Zero-DP**

The breakpoint and zero point of the SC69401 are the same point, which can be programmed at any point on the circumference, and all angles are based on the breakpoint or zero point.DP is the jump point between 0 and 360 degrees, for applications with less than 360 degrees of travel, DP should not be set in the same position as the start of the working travel, but must be set outside the working travel.

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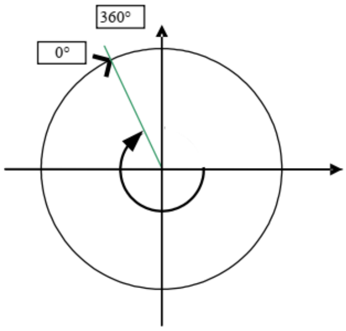

Figure-11: Schematic diagram of DP points

Parameters	Value	Description
DP	0-360	Breakpoint/Zero (degrees)

- **Direction of rotation**

The CW parameter defines the direction of rotation of the magnet.

Counterclockwise is defined as rotation in 1-4-5-8 pin order (SOP-8 package) or 1-8-9-16 pin order (eTSSOP-16L package); clockwise is defined as the opposite direction, rotation in 8-5-4-1 pin order (SOP-8 package) or 16-9-8-1 pin order (eTSSOP-16L package);

Parameters	Value	Description
CW	0	Counterclockwise
	1	Clockwise

- **Output clamp setting**

The output clamp setting is used to limit the output voltage range. CLAMP_LOW sets the minimum output voltage value and CLAMP_HIGH sets the maximum output voltage value. Both parameters work for 4-point, 8-point, 16-point, and 32-point correction modes.

Parameters	Value	Description
CLAMP_LOW	0-100	Low clamping
CLAMP_HIGH	0-100	High clamping

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- **4-point calibration mode**

The SC69401 allows the user to divide the output curve through 4 points into up to 5 segments using the 4-point calibration mode, allowing the number of calibration points to be reduced to 2 or 3. The Y coordinate (-50%~100%) and X coordinate (0°~360°) of the 4 calibration points, and the slope of the 5 segments (LNR_S0,LNR_S1,LNR_S2,LNR_S3,LNR_S4) are fully set by the user. . To calculate the slope, two endpoints of the curve, 0 degree start and 360 degree end, are needed to calculate LNR_S0 and LNR_D_S.

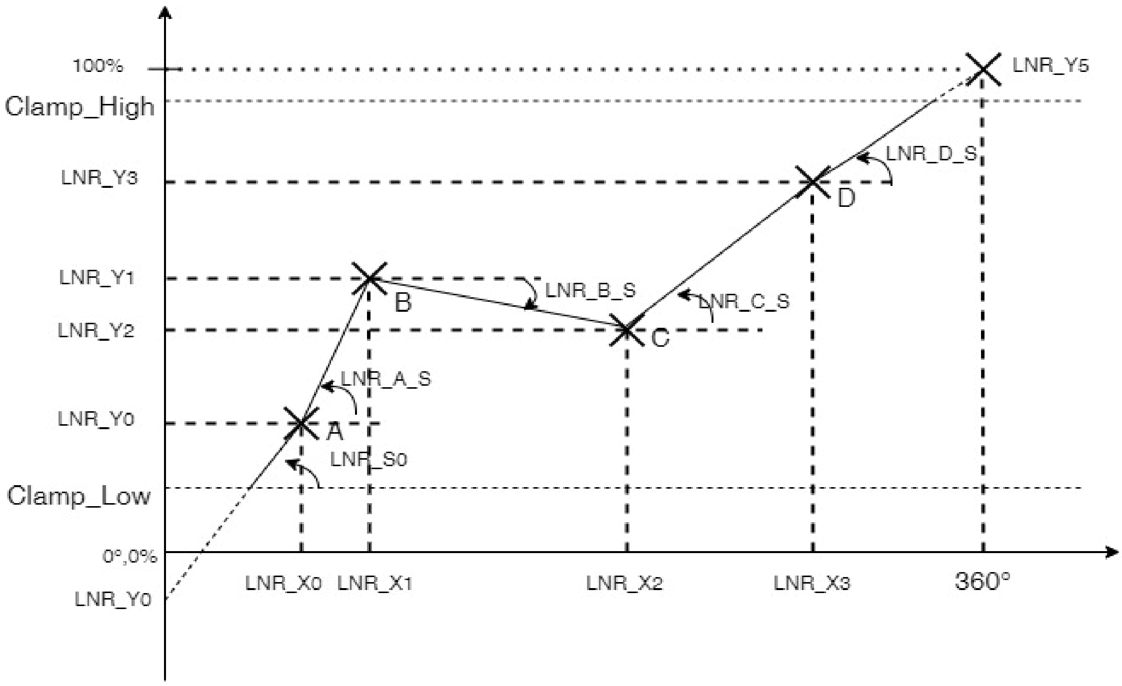

Figure-12: 4-point calibration parameters description

- **8-point arbitrary point calibration mode**

The SC69401 allows the user to program the output curve desired by the user by customizing the X-coordinate (0°~ 360°) and Y-coordinate (0%~100%) of any 8 calibration points. However, the slope cannot be set and can only be calculated from two neighboring points. A default fixed calibration point [0°, 0%] is also required as a starting point.

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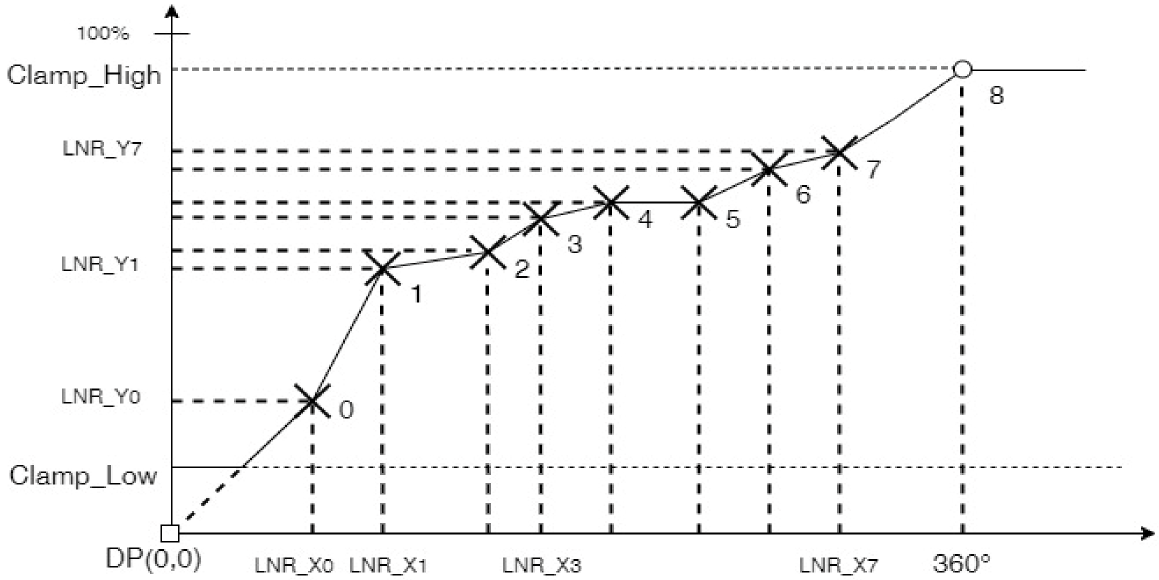

Figure-13: 8-point calibration parameters description

- **16-point calibration mode**

The 16-point calibration mode allows the user to set only the Y-axis value of the coordinate point. x-axis coordinates are defined by the W value and are divided into 16 segments within the WORK_RANGE range. y-point coordinates are allowed to range from -50% to +150% of the clamped voltage, which allows the clamped voltage to be in-between a certain segment (as shown in the following figure). But the output is still clamped voltage.

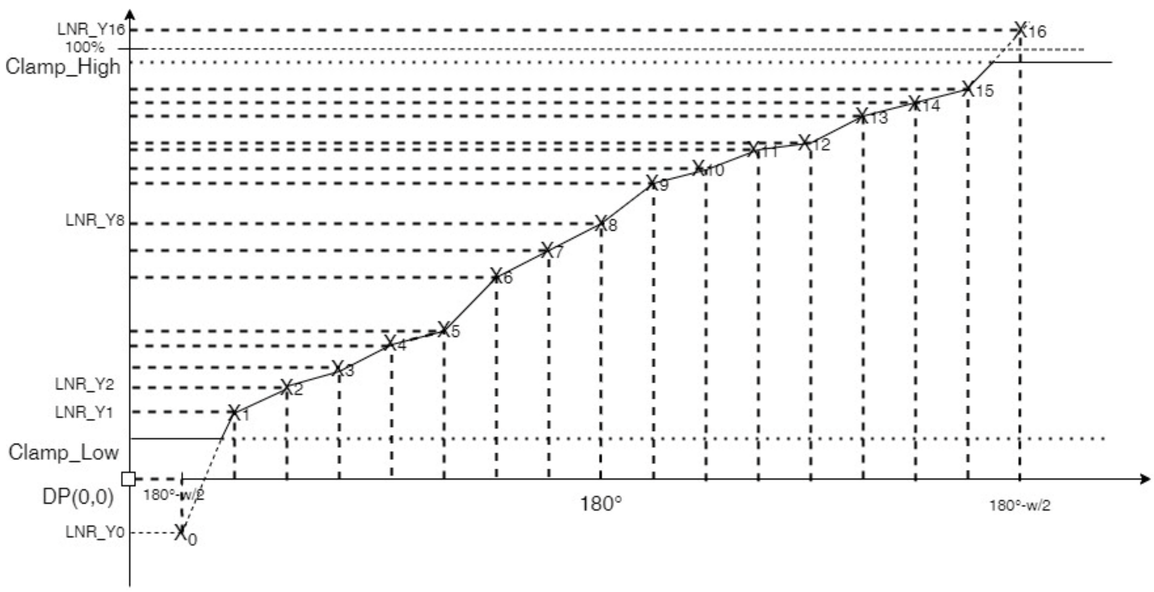

Figure-14: 16-point calibration parameters description

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- **32-point calibration mode**

The work range W is defined by Workrange and is divided into 32 segments centered at 180°. The Y-axis coordinates consist of only 8 bits of data, so they are not absolute values but incremental coordinates. The two endpoints are (180°-w/2, 0%) and (180°+w/2,100%) to define an ideal curve, and ΔY is the fine-tuned value of Y corresponding to the X coordinate of the horizontal axis.

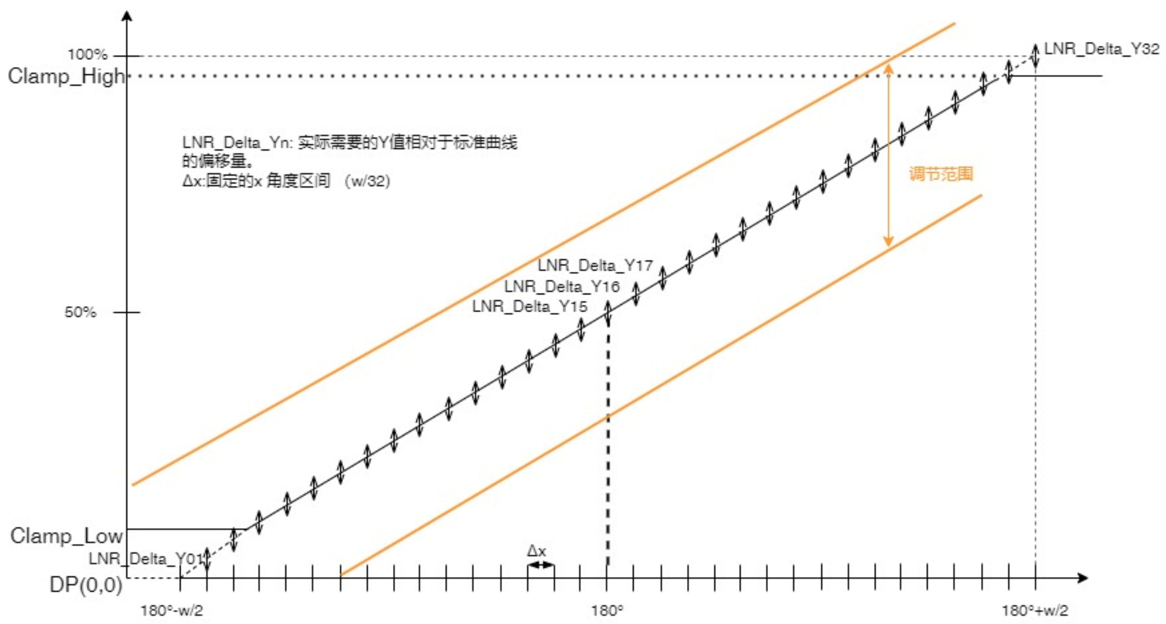

Figure-15: 32-point calibration parameters description

32-point calibration, Y-axis coordinate deviation range setting

Parameters	Value	Description
LNR_DELTA _y_expand [1:0]	0	Tolerance range ±3.125%
	1	Tolerance range ±6.25%
	2	Tolerance range ±12.5%
	3	Tolerance range ±25%

- **Angle range se**lection

$$W=\frac{WORK\_RANGE\_GAIN\times 360°}{0XFFFF}$$

Angular range $\theta_{min}=\frac{360°-w}{2}$ $\theta_{max}=\frac{360°+w}{2}$

θmin indicates the angle at 0% output, and θmax indicates the angle at 100% output. In order to

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correct the output properly, the angle range needs to be set to an integer multiple greater than 16.

Example of angular range setting:

WORK_RANGE_GAIN	W (degrees)	θmin (degrees)	θmax (degrees)	Δx,16pts (degrees)	Δx,32pts (degrees)
0x1000	22.50034	168.7498	191.2502	1.406271	0.703136
0x1100	23.90661	168.0467	191.9533	1.494163	0.747082
0x1200	25.31289	167.3436	192.6564	1.582055	0.791028
0x1300	26.71916	166.6404	193.3596	1.669947	0.834974
0x2000	45.00069	157.4997	202.5003	2.812543	1.406271
0x2100	46.40696	156.7965	203.2035	2.900435	1.450217
0x2200	47.81323	156.0934	203.9066	2.988327	1.494163
0x2300	49.2195	155.3902	204.6098	3.076219	1.538109
0x3000	67.50103	146.2495	213.7505	4.218814	2.109407
0x3100	68.9073	145.5463	214.4537	4.306706	2.153353
0x3200	70.31357	144.8432	215.1568	4.394598	2.197299
0x3300	71.71984	144.1401	215.8599	4.48249	2.241245
0x4000	90.00137	134.9993	225.0007	5.625086	2.812543
0x4100	91.40764	134.2962	225.7038	5.712978	2.856489
0x4200	92.81392	133.593	226.407	5.80087	2.900435
0x4300	94.22019	132.8899	227.1101	5.888762	2.944381
0xFA00	351.5679	4.216068	355.7839	21.97299	10.9865
0xFB00	352.9741	3.512932	356.4871	22.06088	11.03044
0xFC00	354.3804	2.809796	357.1902	22.14878	11.07439
0xFD00	355.7867	2.106661	357.8933	22.23667	11.11833
0xFE00	357.193	1.403525	358.5965	22.32456	11.16228
0xFF00	358.5992	0.700389	359.2996	22.41245	11.20623
0xFFFF	360	0	360	22.5	11.25

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Typical Application Circuit

◆ Analog/PWM SOP-8 Package Application Circuits

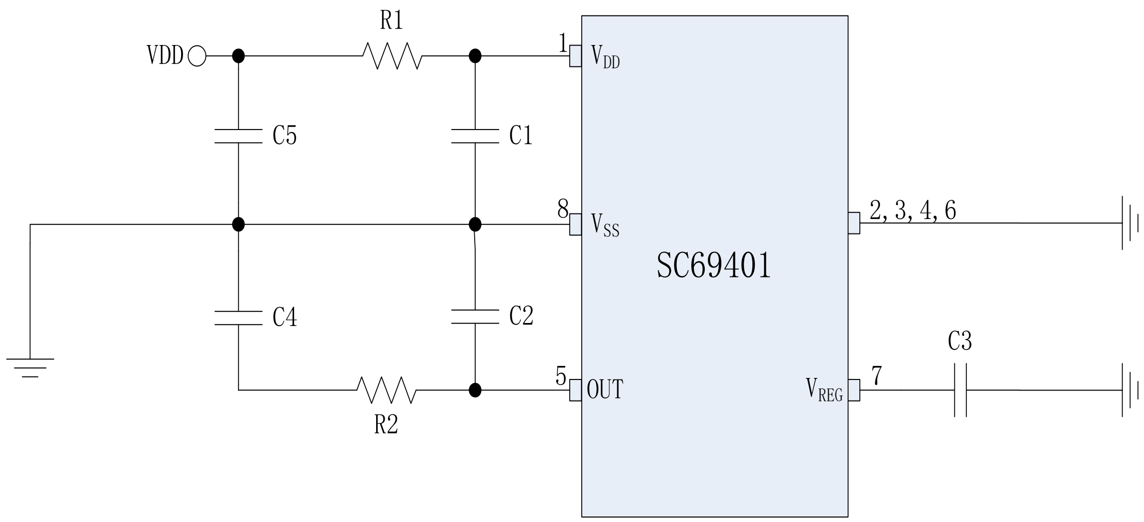

Figure-16: Analog/PWM SOP-8 Reference Circuit Diagram

Analog Output Reference

Component	MIN	Typ	MAX	Description
R1	-	0Ω	33Ω	Reduces EMC effects and increases measurement error
R2	-	0Ω	100Ω	Reduces EMC effects
C1	47nF	100nF	1uF	Placement near pins
C2	47nF	100nF	-	Placement near pins
C3	47nF	100nF	220nF	Placement near pins
C4	-	-	10nF	Reduced EMC impact, placed close to the connector end
C5	-	-	10nF	Reduced EMC impact, placed close to the connector end

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Digital output (PWM) reference

Component	MIN	Typ	MAX	Description
R1	-	0Ω	33Ω	Reduces EMC effects affecting the output high level
R2	-	0Ω	100Ω	Reduces EMC effects, affecting output high and low levels
C1	47nF	100nF	1uF	Placement near pins
C2	2.2nF	4.7nF	22nF	Placement near pins
C3	47nF	100nF	220nF	Placement near pins
C4	-	-	10nF	Reduced EMC impact, placed close to the connector end
C5	-	-	2.2nF	Reduced EMC impact, placed close to the connector end

◆ Analog/PWM eTSSOP-16L Package

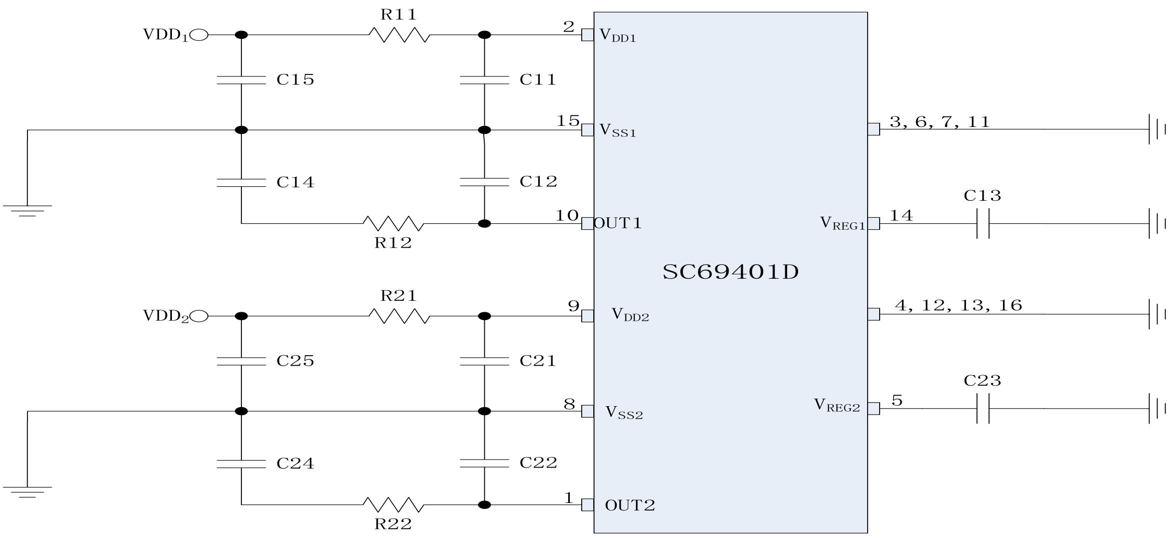

Figure-17: Analog/PWM eTSSOP-16L Reference Circuit Diagram

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Analog Output Reference

Component	MIN	Typ	MAX	Description
R11, R21	-	0Ω	33Ω	Reduces EMC effects and increases measurement error
R12, R22	-	0Ω	100Ω	Reduces EMC effects and increases measurement error
C11, C21	47nF	100nF	1uF	Placement near pins
C12, C22	47nF	100nF	-	Placement near pins
C13, C23	47nF	100nF	220nF	Placement near pins
C14, C24	-	-	10nF	Reduced EMC impact, placed close to the connector end
C15, C25	-	-	10nF	Reduced EMC impact, placed close to the connector end

Digital output (PWM) reference

Component	MIN	Typ	MAX	Description
R11, R21	-	0Ω	33Ω	Reduces EMC effects affecting the output high level
R12, R22	-	0Ω	100Ω	Reduces EMC effects, affecting output high and low levels
C11, C21	47nF	100nF	1uF	Placement near pins
C12, C22	2.2nF	4.7nF	22nF	Placement near pins
C13, C23	47nF	100nF	220nF	Placement near pins
C14, C24	-	-	10nF	Reduced EMC impact, placed close to the connector end
C15, C25	-	-	2.2nF	Reduced EMC impact, placed close to the connector end

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◆ SPI SOP-8 Package Application Circuit

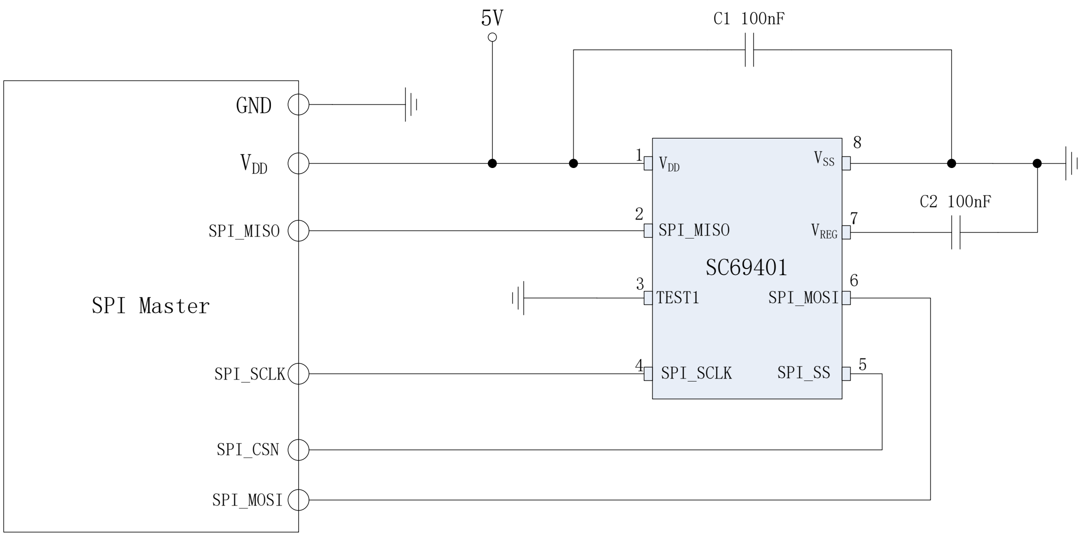

Figure-18: SPI SOP-8 Reference Circuit Diagram

◆ SPI eTSSOP-16L Package Application Circuits

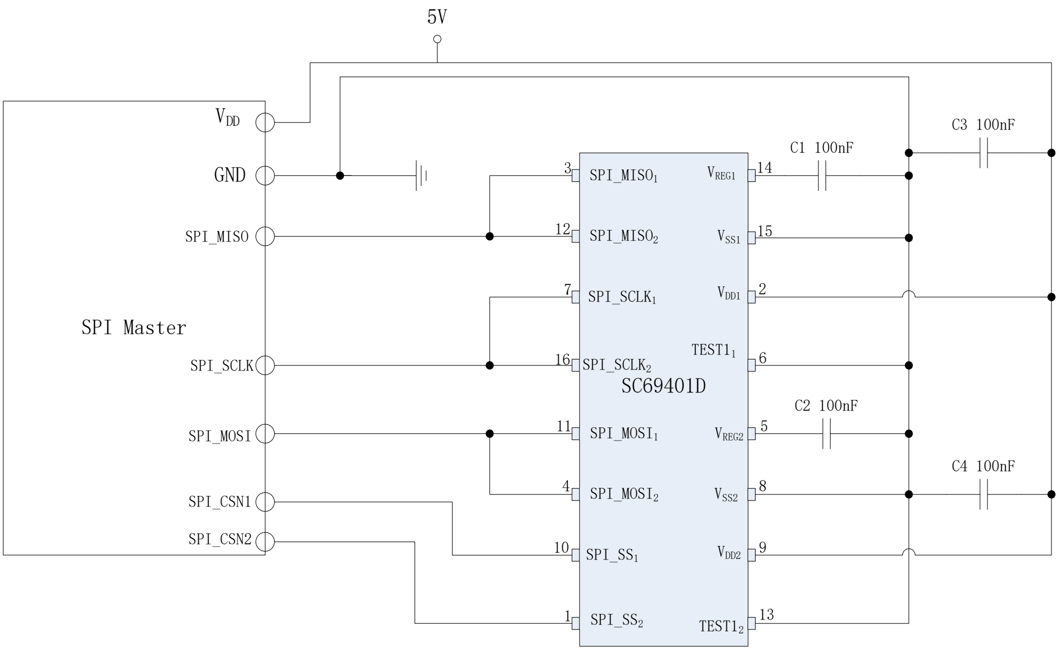

Figure-19: SPI eTSSOP-16L Reference Circuit Diagram

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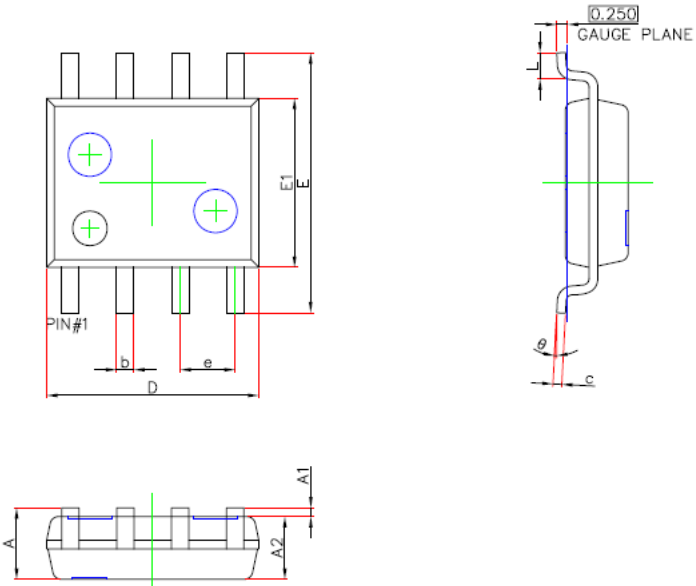
Package Information

◆ SOP-8 package form



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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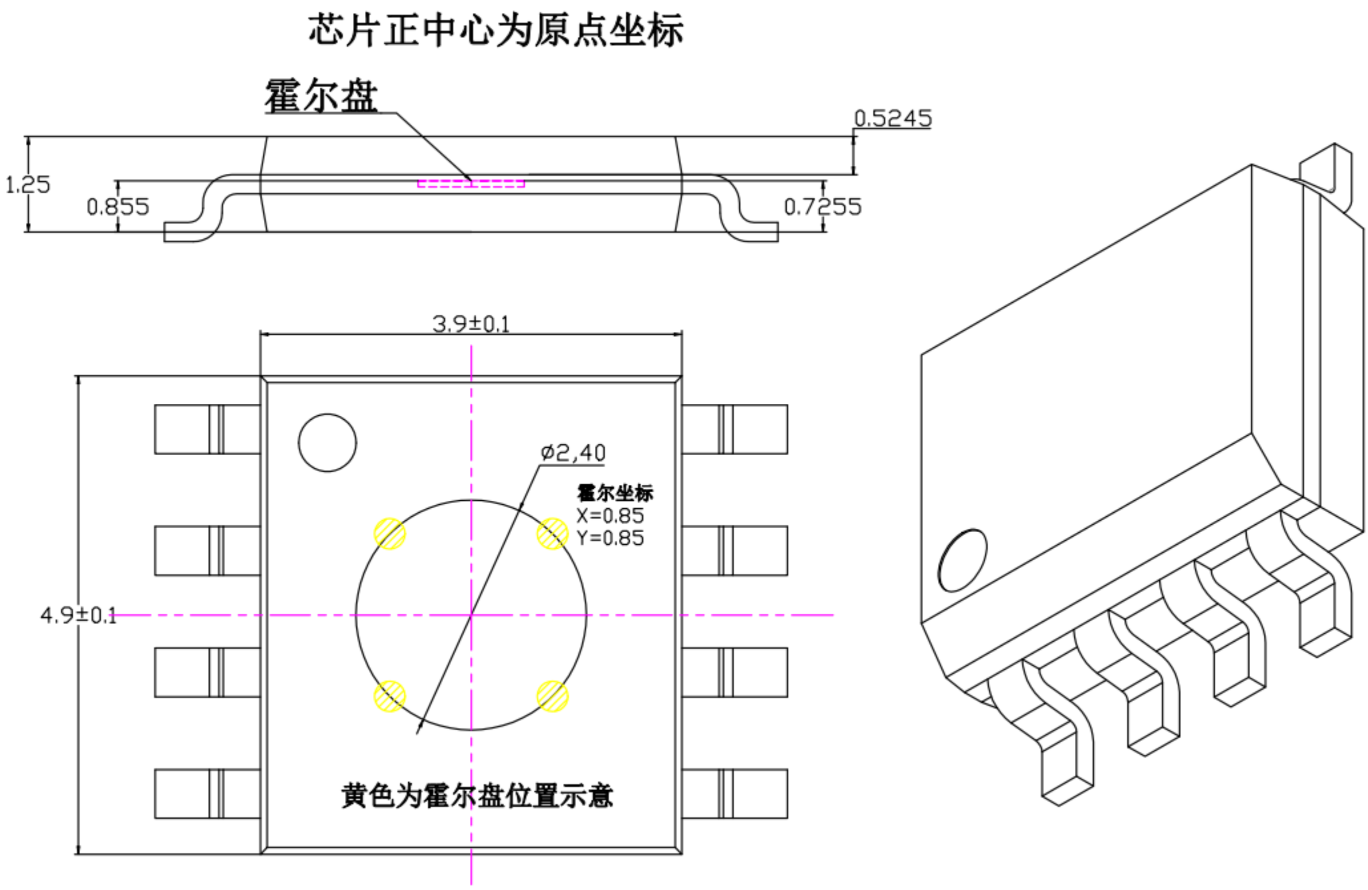
◆ SOP-8 Package Hall Disk Location



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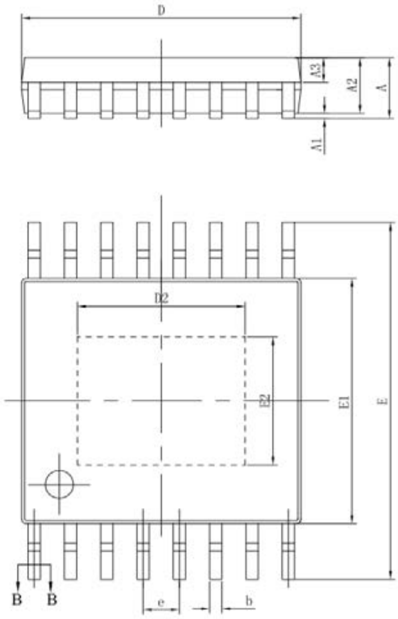
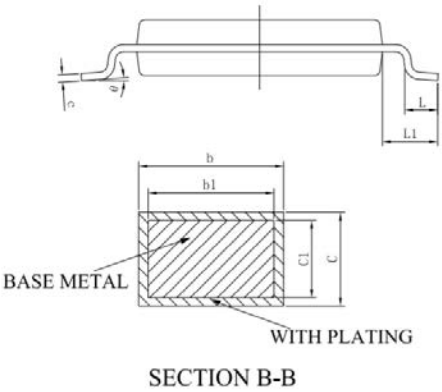
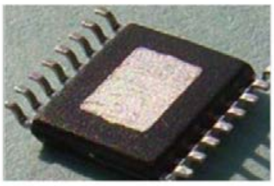
◆ eTSSOP-16L Package Format







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	—	0.75
L1	1.00BSC		
θ	0	—	8°

Size(mm) / L/F Size (mil)	D2	E2
91*118	2.80REF	2.10REF
118*118	2.80REF	2.80REF

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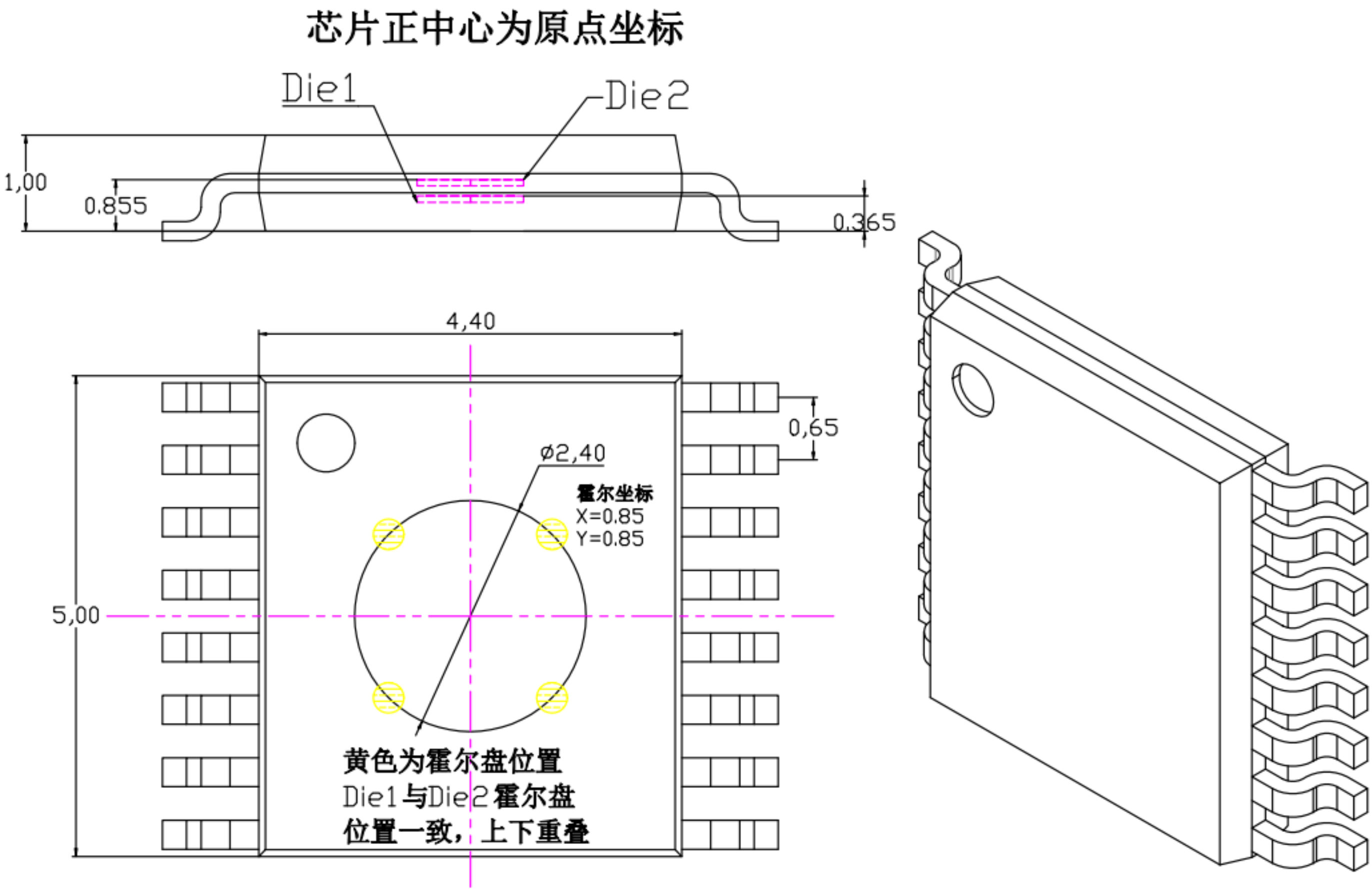
◆ **eTSSOP-16L Package Hall Disk Location**



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Revision information

version number	Update Date	Description
E1.0	2023-07-27	Initialization version
A1.0	2024-02-20	Official release version

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