STK8BA53

Digital Output 3-axis MEMS Accelerometer

Datasheet

Version – 1.3

2017/03/27

Sensortek Technology Corporation

1. OVERVIEW

Description

The STK8BA53 is a ±2g/±4g/±8g, 3-axis linear accelerometer, with digital output (I^2C). It is a low profile capacitive MEMS sensor featuring, compensation for 0g offset and gain errors, and conversion to 12-bit digital values at user configurable samples per second. The device can be arranged for sensor data changes through the interrupt pins. The STK8BA53 is available in a small 2.0mm x 2.0mm x 1.0 mm LGA package and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Feature

- Low Voltage Operation:
  - Supply Internal Domain Voltage: 1.7V~3.6V
  - I/O Voltage Range: 1.62V~3.6V
- ±2g/±4g±/8g dynamically selectable full-scale
- I^2C digital output interface
- Low noise
- 12 bit data output
- 10000 g high shock survivability
- 2.0mm x 2.0mm x 1.0 mm LGA Package
- Configurable Samples from 14 to 2000 samples per second
- Sleep Feature for Low Power Consumption
- On-chip interrupt controller, motion-triggered interrupt-signal generation for
  - New data
  - Any-motion (slope) detection
  - Significant motion
- RoHS Compliant
- Halogen Free
- Environmentally Preferred Product
- Moisture Sensitivity Level 3

Applications

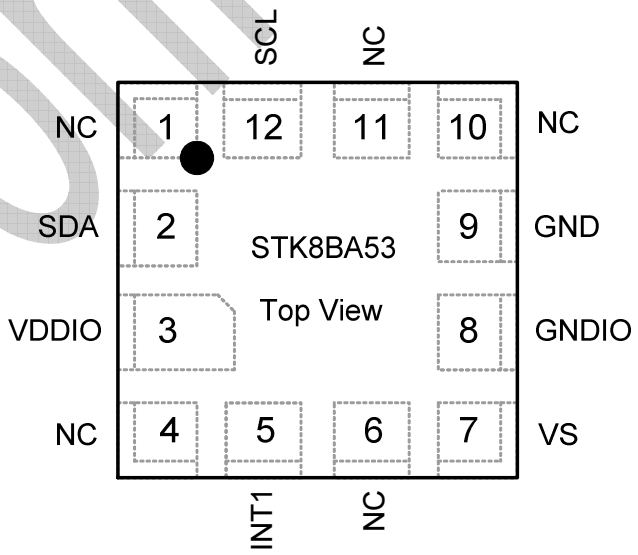
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation
- Pedometer
- Activity trackers for fitness apps
- Smart power management for mobile devices

2. PIN DESCRIPTION

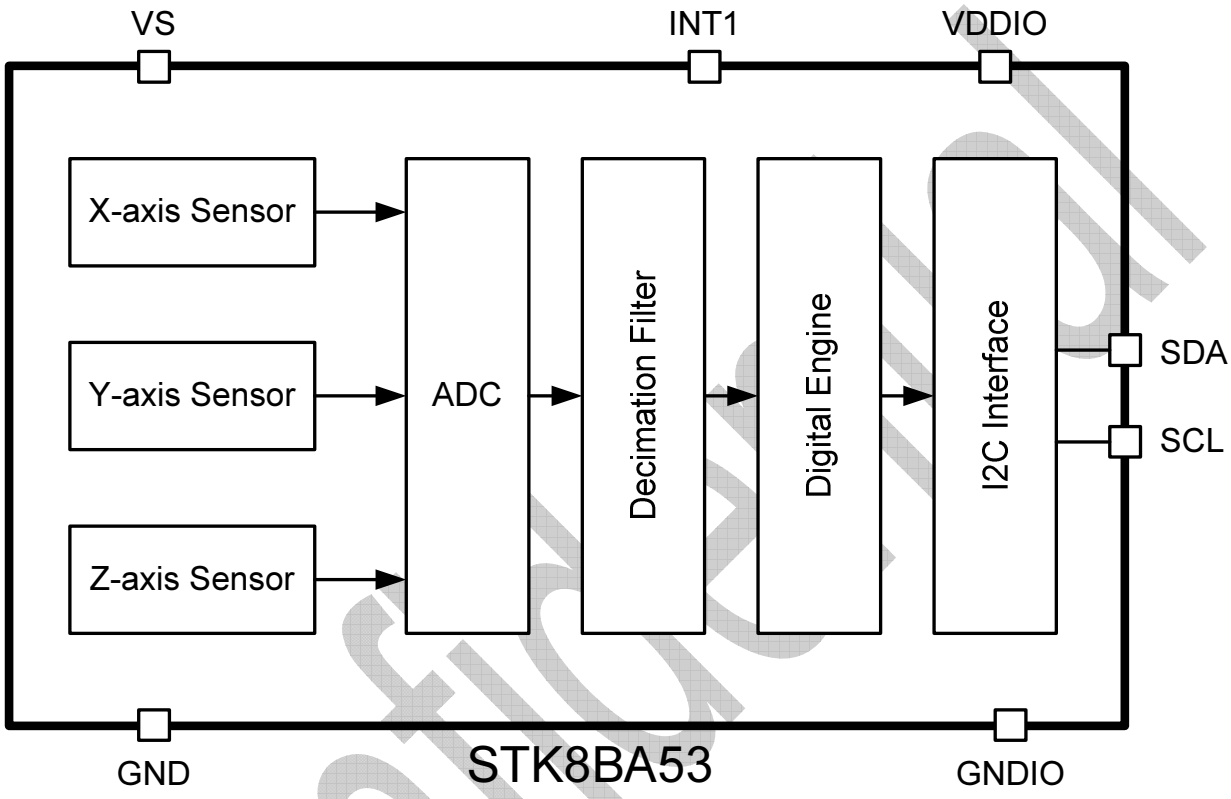
Pin#	Name	Dir.	Function
1	NC	NC	Not Internally Connected.
2	SDA	B	Serial Data (I^2C, Open-Drain)
3	VDDIO	PWR	Digital Interface Supply Voltage.
4	NC	NC	Recommended tie to GND.
5	INT1	O	Interrupt 1 Output.
6	NC	NC	Not Internally Connected.
7	VS	PWR	Supply Voltage.
8	GNDIO	GND	Must be connected to ground.
9	GND	GND	Must be connected to ground.
10	NC	NC	Not Internally Connected.
11	NC	NC	Not Internally Connected.
12	SCL	I	Serial Communications Clock (I^2C, Open-Drain)

Direction denotation:

O	Output	GND	Ground
I	Input	B	Bi-direction
PWR	Power	NC	Not Connected



3. FUNCTION BLOCK



4. ELECTRICAL SPECIFICATIONS

T_A = 25°C, VS = 2.6 V, VDDIO = 2.6 V, acceleration = 0 *g*, C_S = $C_{I/O}$ = 10 µF and 0.1 µF

Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range (VS)		1.7	2.6	3.6	V
Interface Voltage Range (VDDIO)		1.62	2.6	3.6	V
Current consumption in normal mode			110		µA
Current consumption in suspend mode				1	µA
Current consumption in low-power mode	BW=1000Hz Sleep duration=10ms		9.8		uA
Digital high level input voltage (VIH)		0.7 x VDDIO			V
Digital low level input voltage (VIL)				0.3 x VDDIO	V
High level output voltage (VOH)[1]		0.8 x VDDIO			V
Low level output voltage (VOL)[1]				0.2 x VDDIO	V
OUTPUT DATA RATE AND BANDWIDTH	Each axis				
Bandwidth (BW)			7.81		Hz
			15.63		Hz
			31.25		Hz
			62.5		Hz
			125		Hz
			250		Hz
			500		Hz
			1000		Hz
Output data rate (ODR) in normal mode			BW * 2		Hz

1. IOL = 10mA, IOH = -4mA

5. MECHANICAL SPECIFICATIONS

T_A = 25°C, VS = 2.6 V, VDDIO = 2.6 V, acceleration = 0 *g*, C_S = $C_{I/O}$ = 10 µF and 0.1 µF

Parameter	Test Conditions	Min	Typical	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8		g
Non-linearity	Percentage of full scale		±0.5		%FS
Cross-Axis Sensitivity			1		%
OUTPUT RESOLUTION	Each axis				
±2 g Range	Full resolution		12		Bits
±4 g Range	Full resolution		12		Bits
±8 g Range	Full resolution		12		Bits
SENSITIVITY	Each axis				
Sensitivity at XOUT, YOUT, ZOUT	±2g, 12-bit resolution	973	1024	1075	LSB/g
	±4g, 12-bit resolution	486	512	538	LSB/g
	±8g, 12-bit resolution	243	256	269	LSB/g
Sensitivity Change Due to Temperature	X-, Y-, Z-Axes		±0.02		%/°C
0 g OFFSET[1]	Each axis				
0 g Output for XOUT, YOUT, ZOUT			±100		mg
0 g Offset Change Due to Temperature	X-, Y-, Z-Axes		±1		mg/°C
NOISE					
X-, Y-, Z-Axes	±2g, 12-bit resolution BW = 62.5 Hz		200		µg/sqrt(Hz)

1. These parameters are tested in production at final test, and could slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress.

6. ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings	Maximum value	Unit
VS	Supply voltage	-0.3 to 3.6	V
VDDIO	Digital Interface Supply Voltage	-0.3 to 3.6	V
Vin	Input voltage on any control pin	-0.3 to 3.6	V
A_{UNP}	Acceleration (any axis, unpowered)	10000	g
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	4 (HBM)	kV
		500 (CDM)	V
		200 (MM)	V
		100 (Latch Up)	mA

7. DIGITAL INTERFACE

I^2C digital interface are available in STK8BA53. In the cases, the STK8BA53 operates as a slave device.

7.1 I^2C

All registers in STK8BA53 can be accessed via the I^2C bus. All operations can be controlled by the related registers. There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional signal used for sending and receiving the data to/from the interface. Both signals are pull-up to $V_{DD\ I/O}$ through an external resistor.

A watchdog timer (WDT) is used to prevent the I^2C bus lock-up by STK8BA53. The I^2C bus will be reset and return to normal operation state once the WDT is reached. The WDT can be enabled/disabled by I2C_WDT_EN bit and the timer period can be set by I2C_WDT_SEL bit in register INTFCFG (0x34).

The STK8BA53 I^2C command format description for reading and writing operation between the host and STK8BA53 are shown in the following timing chart.

Slave Address

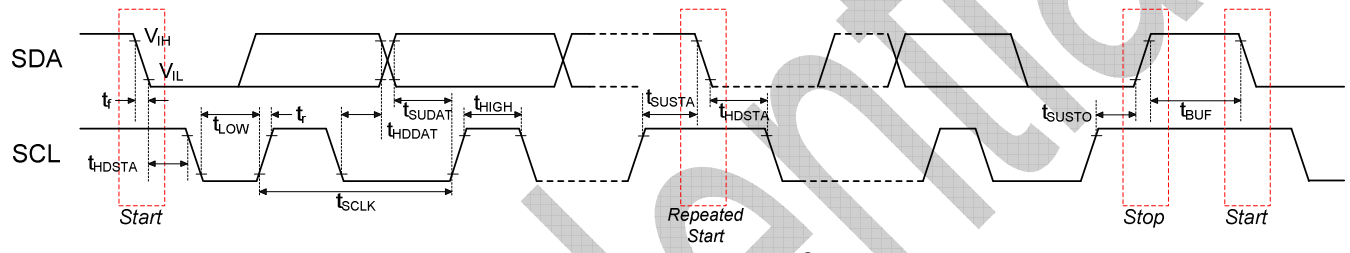
Slave Address (7-bit)	R/W Command Bit	OPERATION
0x18	0	Write Data to STK8BA53
	1	Read Data form STK8BA53

Characteristics of the I^2C Timing

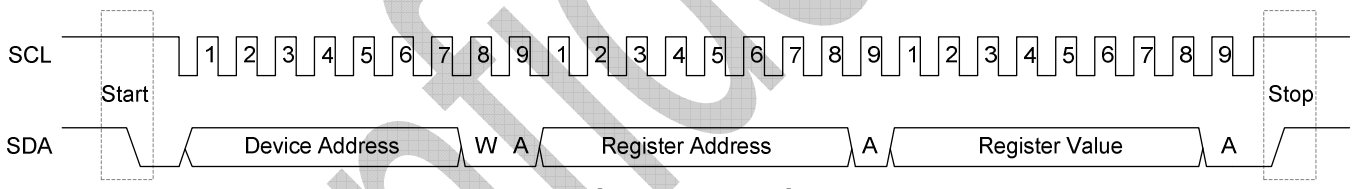
Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCLK}	SCL clock frequency	10	100	10	400	KHz
t_{HDSTA}	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0	—	0.6	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	µs

t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t_{SUSTA}	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t_{HDDAT}	Data hold time	0	—	0	—	ns
t_{SUDAT}	Data set-up time	250	—	100	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	—	300	ns
t_f	Fall time of both SDA and SCL signals	—	300	—	300	ns
t_{SUSTO}	Set-up time for STOP condition	4.0	—	0.6	—	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs

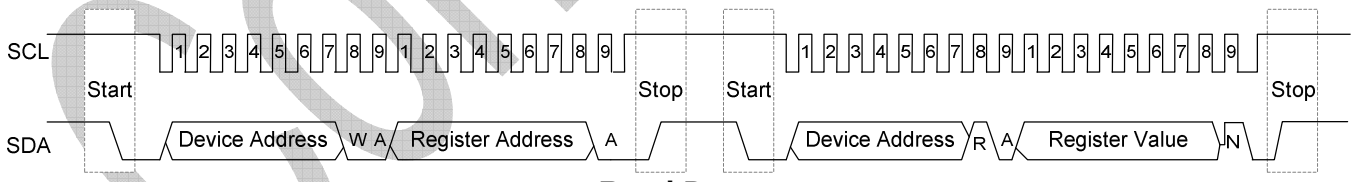
Note: f_{SCLK} is the $(t_{SCLK})^{-1}$.



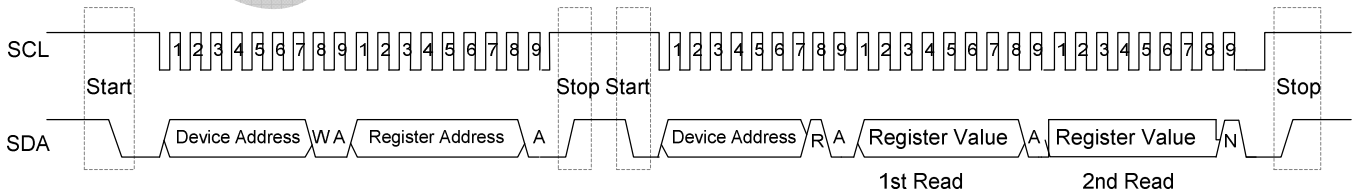
Timing Chart of the I²C



Write Command



Read Data



Sequential Read Data

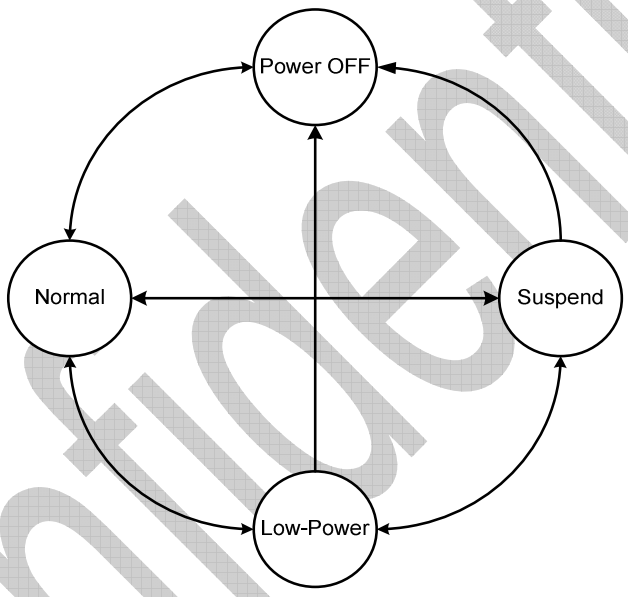
8. PRINPICLE OF OPERATION

8.1 Mode of Operation

STK8BA53 acts as a slave and can communicate with a master (uC or uP). Acceleration data and status information can be accessed with I^2C interface. The interrupt pin are freely configured by user, depends on different requirements.

8.2 Power Management

STK8BA53 has three different power modes, Normal Mode, Low-Power Mode and Suspend Mode. After power-on, it will enter Normal Mode, and user can transfer to Low-Power Mode or Suspend Mode for power-saving purpose.



In **Normal Mode**, all functions are available and data acquisition is performed continuously.

In **Suspend Mode**, whole analog and oscillator are power-down. No data acquisition is performed. Only register reading and writing to SUSPEND bit in register POWMODE (0x11) or register SWRST (0x14) are supported. Suspend mode can be entered by set SUSPEND bit in register POWMODE (0x11) to 1. In the suspend mode, the output data doesn't clear or update, but keeps the last value before entering into suspend mode.

In **Low-Power Mode**, STK8BA53 will switch between wake-up and sleep phase. In wake-up phase, the device is full functional operation, just like in Normal Mode, and in sleep phase, the analog circuit is power-down except oscillator. During the wake-up phase, enabled interrupts are processed normally. If an interrupt is detected, device will stay in wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary interrupt), or until the interrupt is reset (latched interrupt). If no interrupt is detected, the device enters the sleep phase automatically. Average current consumption can be effectively reduced by entering low-power mode. Low-power mode can be entered by setting LOWPOWER bit in register POWMODE (0x11) to 1.

The duration of sleep phase can be set by SLEEP_DUR [3:0] in register POWMODE (0x11).

SLEEP_DUR[3:0]	Duration (ms)
4'b0000 ~ 4'b0101	0.5
4'b0110	1
4'b0111	2
4'b1000	4
4'b1001	6
4'b1010	10
4'b1011	25
4'b1100	50
4'b1101	100
4'b1110	500
4'b1111	1000

8.3 Data, Range and Bandwidth

Acceleration Data

The acceleration data of STK8BA53 is 12 bits and is given in two's complement format. The MSB in each axis will be stored in register XOUT2/YOUT2/ZOUT2 (0x03, 0x05, 0x07) individually, and the LSB will be stored in register XOUT1/YOUT1/ZOUT1 (0x02, 0x04, 0x06) individually. The NEW_X/NEW_Y/NEW_Z bit in register XOUT1/YOUT1/ZOUT1 (0x02, 0x04, 0x06) is used for new data flag, and it will be set to 1 if the data is updated, and reset if either the corresponding MSB or LSB is read. Reading the acceleration data registers shall always start with the LSB part due to the data protection function. When data protection function is enabled, the content of an MSB register will be updated by reading the corresponding LSB register. The data protection function can be disabled (enabled) by writing '1' ('0') to the PROTECT_DIS bit in register DATASETUP (0x13). With disabled data protection, the content of both MSB and LSB registers is updated by a new value immediately.

Range

The STK8BA53 supports four different acceleration measurement ranges. A measurement range can be selected by RANGE[3:0] bits in register RANGESEL (0x0F).

RANGE[3:0]	Sensing Range	Resolution
4'b0011	±2g	0.98 mg/LSB
4'b0101	±4g	1.95 mg/LSB
4'b1000	±8g	3.91 mg/LSB
others	undefined	undefined

Bandwidth

There are two different data stream of STK8BA53, unfiltered data and filtered data. Unfiltered data is sampled as 2 kHz, and the sample rate of filtered data depends on the selected bandwidth; it is twice of the bandwidth. If the DATA_SEL bit in register DATASETUP (0x13) is set to '0' ('1'), the filtered (unfiltered) data will be stored in the XOUT/YOUT/ZOUT data register. Each of the data stream can be separately offset-compensated, and also can be the data source of interrupts controller. The actual bandwidth for the filtered data can be selected by BW [4:0] bits in register BWSEL (0x10).

BW[4:0]	Actual Bandwidth (Hz)
5'b00xxx	7.81
5'b01000	7.81
5'b01001	15.63
5'b01010	31.25
5'b01011	62.5
5'b01100	125
5'b01101	250
5'b01110	500
5'b01111	1000
5'b1xxxx	1000

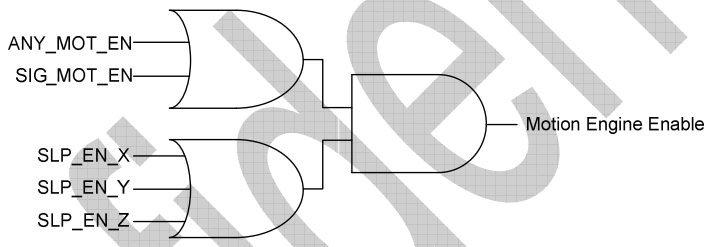
8.4 Motion Algorithm Status and Interrupt Event Detection

The following table shows the interrupt events offered by STK8BA53. Two interrupt engines and one INT pins are integrated for conveniently motion detection. Each interrupt could be enabled independently, and mapped into the INT pin. If the condition of enabled interrupt is fulfilled, the corresponding status is set to '1' and the INT pin is asserted. The INT pin state is logical 'or' combination of all mapped interrupts. The INT pin state is logical 'or' combination of all mapped interrupts. If an interrupt is disabled, all active pins and status are reset immediately.

Two motion algorithms, any-motion and significant motion, used for detecting user movement can flexibly choose three independent axes as the data source via register INTEN1 (0x16), and the event signal is triggered by an "OR" combination of the enabled axes.

Interrupt Event	Control Bit	Status Bit in Register INTSTS1/2 (0x09, 0x0A)
New Data	DATA_EN in INTEN2 (0x17)	DATA_STS
Any-Motion (Slope) Significant Motion	SLP_EN_Z in INTEN1 (0x16) SLP_EN_Y in INTEN1 (0x16) SLP_EN_X in INTEN1 (0x16) ANY_MOT_EN in SIGMOT2 (0x2A) SIG_MOT_EN in SIGMOT2 (0x2A)	ANY_MOT_STS SIG_MOT_STS
		ANY_MOT_STS
		SIG_MOT_STS

Note: Motion algorithm engine follows the logic shown below.



Interrupt Latch Mode

There are two different interrupt latch modes of Any-Motion (Slope) and Significant Motion: temporary, and latched. The modes can be selected by the INT_LATCH [3:0] bits in register INTCFG2 (0x21). The following table shows the different configurations of interrupt modes in INT_LATCH [3:0].

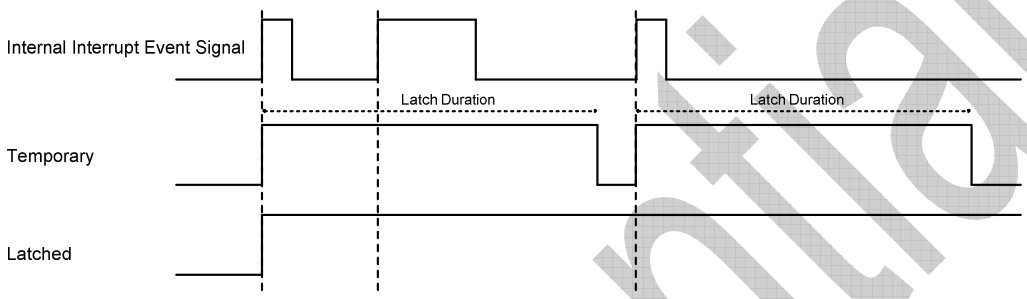
Note: Interrupt latched mode INT_LATCH [3:0] in register INTCFG2 (0x21) can not be default setting after motion algorithms enabled. Interrupt latched mode must be set in the initial configuration.

INT_LATCH[3:0]	Output Mode
4'b0000	reserved
4'b0001	temporary, 250ms
4'b0010	temporary, 500ms
4'b0011	temporary, 1s
4'b0100	temporary, 2s
4'b0101	temporary, 4s
4'b0110	temporary, 8s
4'b0111	latched
4'b1000	reserved
4'b1001	temporary, 250us
4'b1010	temporary, 500us
4'b1011	temporary, 1ms
4'b1100	temporary, 12.5ms
4'b1101	temporary, 25ms
4'b1110	temporary, 50ms
4'b1111	latched

In the **latched mode**, the status and mapped INT pins are cleared only by setting '1' to the INT_RST bit in register INTCFG2 (0x21). If the activation condition still holds when it is cleared, the interrupt pin and status will be both asserted again.

In the **temporary mode**, an asserted interrupt and selected pin are cleared after a defined period of time. The following figure shows the behavior of three interrupt modes.

Both filtered and unfiltered data could be the data source of the interrupt events. Setting the corresponding bit in register DATASETUP (0x13) to '0'('1') will select the filtered(unfiltered) data as the data source for interrupt events.



Interrupt latch mode control bits only apply to Any-Motion (Slope) and Significant Motion. Other interrupt events are fixed to their own latch mode, which are shown in the following table.

Interrupt Event	Type	Latch mode	Clear
New data	Status	Non-latch	Auto clear after 250us
Any-Motion (Slope)	Programmable	Programmable	Based on configuration
Significant Motion	Programmable	Programmable	Based on configuration

Interrupt Pin Mapping

The mapping of interrupts to the INT1 is controlled by registers INTMAP2 (0x1A). Setting the corresponding bit to '1'('0') maps(un-maps) the related interrupt to the INT1 pin.

INT Pin Output Type and Active Level

INT1 could be configured as Push-Pull/Open-Drain output and the active level could also be set as active-high/activelow. The related bits in register INTCFG1 (0x20) are used to select the INT1 output type and active level.

8.5 Offset Compensation

Manual Compensation

STK8BA53 offers the manual digital offset-compensation method. It is done by adding a compensation value to the acceleration data coming from the ADC. The registers OFSTX/Y/Z (0x38, 0x39, 0x3A) are used to for the offset compensation purpose and are given in two's complement format. 1 LSB of OFSTX/Y/Z represents 7.81mg in any sensing range.

By writing '1' to the OFST_RST bit in register OFSTCOMP1 (0x36), all offset compensation registers are reset to zero.

It is recommended to write into these registers immediately after a new data interrupt in order not to disturb running offset computations.

9. REGISTER DEFINATION

9.1 Register Map

ADDR	REG NAME	BIT 7	6	5	4	3	2	1	0	Default
00h	CHIP_ID	CHIP_ID[7:0]								87h
01h	RESERVED	reserved								00h
02h	XOUT1	XOUT[3:0]				reserved			NEW_X	00h
03h	XOUT2	XOUT[11:4]								00h
04h	YOUT1	YOUT[3:0]				reserved			NEW_Y	00h
05h	YOUT2	YOUT[11:4]								00h
06h	ZOUT1	ZOUT[3:0]				reserved			NEW_Z	00h
07h	ZOUT2	ZOUT[11:4]								00h
08h	RESERVED	reserved								00h
09h	INTSTS1	reserved					ANY_MOT_STS	reserved	SIG_MOT_STS	00h
0Ah	INTSTS2	DATA_STS	reserved							00h
0Bh	EVENTINFO1	reserved	SLPSIGN_Z	SLPSIGN_Y	SLPSIGN_X	reserved	SLP_1ST_Z	SLP_1ST_Y	SLP_1ST_X	00h
0Ch-0Eh	RESERVED	reserved								00h
0Fh	RANGESEL	reserved				RANGE[3:0]				03h
10h	BWSEL	reserved			BW[4:0]					1Fh
11h	POWMODE	SUSPEND	LOWPOWER	reserved	SLEEP_DUR[3:0]				reserved	00h
12h	RESERVED	reserved								00h
13h	DATASETUP	DATA_SEL	PROTECT_DIS	reserved						00h
14h	SWRST	SWRST[7:0]								00h
15h	RESERVED	reserved								00h
16h	INTEN1	reserved					SLP_EN_Z	SLP_EN_Y	SLP_EN_X	00h
17h	INTEN2	reserved			DATA_EN	reserved				00h
18h	RESERVED	reserved								00h
19h	INTMAP1	reserved					ANYMOT2INT1	reserved	SIGMOT2INT1	00h
1Ah	INTMAP2	reserved							DATA2INT1	
1Bh-1Fh	RESERVED	reserved								00h
20h	INTCFG1	reserved						INT1_OD	INT1_LV	01h
21h	INTCFG2	INT_RST	reserved			INT_LATCH[3:0]				00h
22h-26h	RESERVED	reserved								00h
27h	SLOPEDLY	reserved						SLP_DUR[1:0]		00h
28h	SLOPETHD	SLP_THD[7:0]								14h
29h	SIGMOT1	SKIP_TIME[7:0]								96h
2Ah	SIGMOT2	reserved					ANY_MOT_EN	SIG_MOT_EN	SKIP_TIME[8]	02h
2Bh	SIGMOT3	reserved	PROOF_TIME[6:0]							32h
2Ch-33h	RESERVED	reserved								00h
34h	INTFCFG	reserved					I2C_WDT_EN	I2C_WDT_SEL	reserved	00h
35h	RESERVED	reserved								00h
36h	OFSTCOMP1	OFST_RST	reserved							00h
37h	RESERVED	reserved								00h

38h	OFSTX	OFST_X[7:0]	**00h**
39h	OFSTY	OFST_Y[7:0]	**00h**
3Ah	OFSTZ	OFST_Z[7:0]	**00h**

9.2 Register Description

CHIP_ID Register (00h)

b7	b6	b5	b4	b3	b2	b1	b0
CHIP_ID[7:0]							
8'b10000111							
RO							

The register contains the chip identification code.

XOUT1 Register (02h)

b7	b6	b5	b4	b3	b2	b1	b0
XOUT[3:0]				reserved			NEW_X
4'b0000				3'b000			0
RO				RO			RO

XOUT1/XOUT2 register contain the x-axis acceleration data and the new data flag for the x-axis.

XOUT2 Register (03h)

b7	b6	b5	b4	b3	b2	b1	b0
XOUT[11:4]							
8'b00000000							
RO							

YOUT1 Register (04h)

b7	b6	b5	b4	b3	b2	b1	b0
YOUT[3:0]				reserved			NEW_Y
4'b0000				3'b000			0
RO				RO			RO

YOUT1/YOUT2 register contain the y-axis acceleration data and the new data flag for the y-axis.

YOUT2 Register (05h)

b7	b6	b5	b4	b3	b2	b1	b0
YOUT[11:4]							
8'b00000000							
RO							

ZOUT1 Register (06h)

b7	b6	b5	b4	b3	b2	b1	b0
ZOUT[3:0]				reserved			NEW_Z
4'b0000				3'b000			0
RO				RO			RO

ZOUT1/ZOUT2 register contain the z-axis acceleration data and the new data flag for the z-axis.

ZOUT2 Register (07h)

b7	b6	b5	b4	b3	b2	b1	b0
ZOUT[11:4]							
8'b00000000							
RO							

INTSTS1 Register (09h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved					ANY_MOT_STS	reserved	SIG_MOT_STS
5'b00000					0	0	0
RO					RO	RO	RO

This register contains the interrupts status in STK8BA53.

BIT	BIT NAME	Description
0	SIG_MOT_STS	Significant motion interrupt status. '1' : event triggered, '0' : no event.
2	ANY_MOT_STS	Any-motion (slope) detection interrupt status. '1' : event triggered, '0' : no event.

INTSTS2 Register (0Ah)

b7	b6	b5	b4	b3	b2	b1	b0
DATA_STS	reserved						
0	7'b00000						
RO	RO						

This register contains the new data interrupt status in STK8BA53.

BIT	BIT NAME	Description
7	DATA_STS	New data interrupt status. '1' : event triggered, '0' : no event.

EVENTINFO1 Register (0Bh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved	SLPSIGN_Z	SLPSIGN_Y	SLPSIGN_X	reserved	SLP_1ST_Z	SLP_1ST_Y	SLP_1ST_X
0	0	0	0	0	0	0	0
RO	RO	RO	RO	RO	RO	RO	RO

This register contains any-motion (slope) detection information.

BIT	BIT NAME	Description
0	SLP_1ST_X	1 : Motion on the X-axis cause SLOPE interrupt asserted.
1	SLP_1ST_Y	1 : Motion on the Y-axis cause SLOPE interrupt asserted.
2	SLP_1ST_Z	1 : Motion on the Z-axis cause SLOPE interrupt asserted.
4	SLPSIGN_X	Sign of acceleration slope on the X-axis that triggered the SLOPE interrupt. 0 : positive. 1 : negative.
5	SLPSIGN_Y	Sign of acceleration slope on the Y-axis that triggered the SLOPE interrupt. 0 : positive. 1 : negative.
6	SLPSIGN_Z	Sign of acceleration slope on the Z-axis that triggered the SLOPE interrupt. 0 : positive. 1 : negative.

RANGESEL Register (0Fh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved				RANGE[3:0]			
4'b0000				4'b0011			
RO				R/W			

This register contains the acceleration sensing range.

RANGE[3:0]	Sensing Range
4'b0011	±2g
4'b0101	±4g
4'b1000	±8g
others	undefined

BWSEL Register (10h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved			BW[4:0]				
3'b000			5'b11111				
RO			R/W				

This register contains the output data bandwidth selection.

BW[4:0]	Actual Bandwidth (Hz)
5'b00xxx	7.81
5'b01000	7.81
5'b01001	15.63
5'b01010	31.25
5'b01011	62.5
5'b01100	125
5'b01101	250
5'b01110	500
5'b01111	1000
5'b1xxxx	1000

POWMODE Register (11h)

b7	b6	b5	b4	b3	b2	b1	b0
SUSPEND	LOWPOWER	SLEEP_TIMER	SLEEP_DUR[3:0]				reserved
0	0	0	4'b0000				0
R/W	R/W	R/W	R/W				RO

This register contains the power mode selection and the sleep time duration setting.

BIT	BIT NAME	Description
[4:1]	SLEEP_DUR[3:0]	Sleep time duration. SLEEP_DUR[3:0] / Duration (ms) 4'b0000 ~ 4'b0101 / 0.5 4'b0110 / 1 4'b0111 / 2 4'b1000 / 4 4'b1001 / 6 4'b1010 / 10 4'b1011 / 25 4'b1100 / 50 4'b1101 / 100 4'b1110 / 500 4'b1111 / 1000
5	SLEEP_TIMER	Sleep timer control bit in low-power mode. 0 : event-driven. 1 : equidistant sampling.
6	LOWPOWER	0 : low-power mode disable. 1 : low-power mode enable.
7	SUSPEND	0 : suspend mode disable. 1 : suspend mode enable.

DATASETUP Register (13h)

b7	b6	b5	b4	b3	b2	b1	b0
DATA_SEL	PROTECT_DIS	reserved					
0	0	6'b000000					
R/W	R/W	RO					

This register is used to select if the output data is filtered or unfiltered and how the output data contained in the register XOUT1/XOUT2, YOUT1/YOUT2, ZOUT1/ZOUT2 are updated.

BIT	BIT NAME	Description
6	PROTECT_DIS	0 : Enable the data protection function. 1 : Disable the data protection function.
7	DATA_SEL	0 : Data output filtered. 1 : Data output unfiltered.

SWRST Register (14h)

b7	b6	b5	b4	b3	b2	b1	b0
SWRST[7:0]							
8'b00000000							
W							

This register is used to software reset. Write 0xB6 into SWRST to reset all the registers to default value.

INTEN1 Register (16h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved					SLP_EN_Z	SLP_EN_Y	SLP_EN_X
5'b00000					0	0	0
RO					R/W	R/W	R/W

This register contains the several interrupt enable bit.

BIT	BIT NAME	Description
0	SLP_EN_X	0 : Disable X-axis any-motion (slope) interrupt. 1 : Enable X-axis any-motion (slope) interrupt.
1	SLP_EN_Y	0 : Disable Y-axis any-motion (slope) interrupt. 1 : Enable Y-axis any-motion (slope) interrupt.
2	SLP_EN_Z	0 : Disable Z-axis any-motion (slope) interrupt. 1 : Enable Z-axis any-motion (slope) interrupt.

INTEN2 Register (17h)

b7	b6	b5	b4	b3	b2	b1	b0
Reserved			DATA_EN	reserved			
3'b000			0	4'b0000			
RO			R/W	RO			

This register contains the several interrupt enable bit.

BIT	BIT NAME	Description
4	DATA_EN	0 : Disable new data interrupt. 1 : Enable new data interrupt.

INTMAP1 Register (19h)

b7	b6	b5	b4	b3	b2	b1	b0
Reserved					ANYMOT2INT1	reserved	SIGMOT2INT1
5'b00000					0	0	0
RO					R/W	RO	R/W

This register is used to map the related interrupt to the desired INT pin.

BIT	BIT NAME	Description
0	SIGMOT2INT1	0 : Do not map significant motion interrupt to INT1. 1 : Map significant motion interrupt to INT1.
2	ANYMOT2INT1	0 : Do not map any-motion (slope) interrupt to INT1. 1 : Map any-motion (slope) interrupt to INT1.

INTMAP2 Register (1Ah)

b7	b6	b5	b4	b3	b2	b1	b0
reserved							DATA2INT1
7'b0000000							0
RO							R/W

This register is used to map the related interrupt to the desired INT pin.

BIT	BIT NAME	Description
0	DATA2INT1	0 : Do not map new data interrupt to INT1. 1 : Map new data interrupt to INT1.

INTCFG1 Register (20h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved						INT1_OD	INT1_LV
6'b000000						0	1
RO						R/W	R/W

This register is used to define the INT1 pin output type and active level. Open-drain or Push-pull output type and active high or active low can be selected.

BIT	BIT NAME	Description
0	INT1_LV	INT1 active level selection. 0 : Active low. 1 : Active high.
1	INT1_OD	INT1 output type selection. 0 : Push-pull output type. 1 : Open-drain output type.

INTCFG2 Register (21h)

b7	b6	b5	b4	b3	b2	b1	b0
INT_RST	reserved			INT_LATCH[3:0]			
0	3'b000			4'b0000			
R/W	RO			R/W			

This register is used to reset latched interrupt pin and select the interrupt mode.

BIT	BIT NAME	Description
[3:0]	INT_LATCH[3:0]	INT pin output mode selection.
7	INT_RST	1 : Reset any latched interrupt pin.

INT_LATCH[3:0]	Output Mode
4'b0000	reserved
4'b0001	temporary, 250ms
4'b0010	temporary, 500ms
4'b0011	temporary, 1s
4'b0100	temporary, 2s
4'b0101	temporary, 4s
4'b0110	temporary, 8s
4'b0111	latched
4'b1000	reserved
4'b1001	temporary, 250us
4'b1010	temporary, 500us
4'b1011	temporary, 1ms
4'b1100	temporary, 12.5ms
4'b1101	temporary, 25ms
4'b1110	temporary, 50ms
4'b1111	latched

SLOPEDLY Register (27h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved						SLP_DUR[1:0]	
6'b000000						2'b00	
RO						R/W	

This register is used to set the number of samples needed in slope detection. The actual number of samples will be equal to SLP_DUR[1:0] + 1.

SLOPETHD Register (28h)

b7	b6	b5	b4	b3	b2	b1	b0
SLP_THD[7:0]							
8'b00010100							
R/W							

This register is used to set the threshold value for the slope detection. The actual slope threshold will depend on sensing range. The default value of SLP_THD[7:0] is 0x14.

RANGE[3:0]	Sensing Range	Actual Slope Threshold (mg)
4'b0011	±2g	SLP_THD[7:0] * 3.91
4'b0101	±4g	SLP_THD[7:0] * 7.81
4'b1000	±8g	SLP_THD[7:0] * 15.63

SIGMOT1 Register (29h)

b7	b6	b5	b4	b3	b2	b1	b0
SKIP_TIME[7:0]							
8'b10010110							
R/W							

This register is used to set the skip time for the significant motion. Holding the duration for skip, for which the motion is checked for re-detection. 1 LSB=20 ms. Range is 0 to 10sec. The default value of SKIP_TIME[8:0] is 0x96 correspond to 3 seconds.

SIGMOT2 Register (2Ah)

b7	b6	b5	b4	b3	b2	b1	b0
reserved					ANY_MOT_EN	SIG_MOT_EN	SKIP_TIME[8]
5'b00000					0	1	0
RO					R/W	R/W	R/W

This register contains MSB of SKIP_TIME[8:0] for the significant motion, and significant motion interrupt enable bit.

BIT	BIT NAME	Description
1	SIG_MOT_EN	0 : Disable significant motion. 1 : Enable significant motion.
2	ANY_MOT_EN	0 : Disable any-motion. 1 : Enable any-motion.

SIGMOT3 Register (2Bh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved	PROOF_TIME[7:0]						
0	7'b0110010						
RO	R/W						

This register is used to set the proof time for the significant motion. Holding the duration for proof, for which the motion is re-checked after. 1 LSB=20 ms. Range is 0 to 2.5sec. The default value of PROOF_TIME[8:0] is 0x32 correspond to 1 seconds.

INTFCFG Register (34h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved					I2C_WDT_EN	I2C_WDT_SEL	reserved
5'b00000					0	0	0
RO					R/W	R/W	RO

This register contains the digital interface parameters for the I²C interface.

BIT	BIT NAME	Description
1	I2C_WDT_SEL	I²C watchdog timer period selection. 0 : Watchdog timer period 1ms. 1 : Watchdog timer period 50ms.
2	I2C_WDT_EN	I²C watchdog timer enable bit. 0 : Disable I2C watchdog timer. 1 : Enable I2C watchdog timer.

OFSTCOMP1 Register (36h)

b7	b6	b5	b4	b3	b2	b1	b0
OFST_RST	reserved						
0	2'b0000000						
W	R						

This register is used to define the setting for the offset compensation.

BIT	BIT NAME	Description
7	OFST_RST	1 : Reset all the offset compensation register (register 0x38 ~ 0x3A) to zero.

OFSTX Register (38h)

B7	b6	b5	b4	b3	b2	b1	b0
OFST_X[7:0]							
8'b00000000							
R/W							

This register contains the offset compensation value for the x-axis data output.

OFSTY Register (39h)

B7	b6	b5	b4	b3	b2	b1	b0
OFST_Y[7:0]							
8'b00000000							
R/W							

This register contains the offset compensation value for the y-axis data output.

OFSTZ Register (3Ah)

b7	b6	b5	b4	b3	b2	b1	b0
OFST_Z[7:0]							
8'b00000000							
R/W							

This register contains the offset compensation value for the z-axis data output.

Register 0x38 to 0x3A can be modified manually set by user. The value in these register will be added to the actual acceleration data sensing by STK8BA53 and store the new value to XOUT/YOUT/ZOUT register.

10. APPLICATION INFORMATION

10.1 New Data Interrupt

This interrupt serves for synchronous reading of acceleration data. It is generated after storing a new value of z-axis acceleration data in the data register. The interrupt is cleared automatically when the next cycle of data acquisition starts. The interrupt status is '0' for at least 50μs. The interrupt mode of the new data interrupt is fixed to non-latched for at least 250 us.

Control Register	Bit Name	Function
INTEN2[4]	DATA_EN	'1': enabled, '0': disabled, and the interrupt mode is fixed to non-latched.
INTSTS[7]	DATA_STS	The interrupt status.
INTMAP2	DATA2INT1	New data interrupt maps to INT1.
DATASETUP[5]	DATA_SEL	'1': unfiltered data, '0': filtered data, as the input of the new data interrupt.

10.2 Any-motion (Slope) Detection

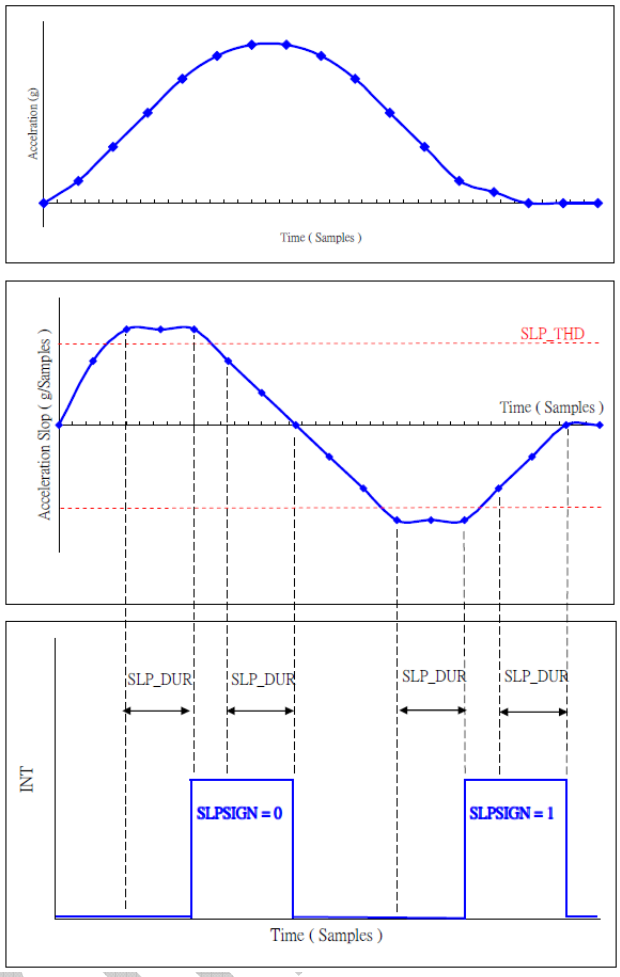
Any-motion (slope) detection is to detect the change of motion. By monitoring the slop of acceleration, user can estimate the variation of acceleration. STK8BA53 use the slop between successive acceleration data to detect it, and would active the interrupt when the slop exceeds a preset threshold. Moreover, a duration setting has to be configured to suppress failure signals. The following figure shows the relationship between acceleration data, acceleration slop, and INT status. If a certain number *N* of consecutive slope data points is larger (smaller) than the slope threshold, the INT would be trigger (clear).

One LSB of SLP_THD [7:0] represents 1 LSB of acceleration data, and it depends on which sensing range is set. For Example, 3.91mg in 2g-range, 7.81 mg in 4g-range, 15.6 mg in 8g-range and 31.3 mg in 16g-range. The consecutive slope data points are set by SLP_DUR [1:0], and is equal to (SLP_DUR [1:0] + 1). The time difference between the successive acceleration signals depends on the selected bandwidth and equates to 1/(2*bandwidth).

Any-motion (slope) detection can be enabled by writing '1' to ANY_MOT_EN bit in the register SIGMOT2 (0x2A). Furthermore, user must select which axes are enabled independently by writing '1' to the bit SLP_EN_X, SLP_EN_Y, and SLP_EN_Z in the register INTEN1 (0x16).

If slope of any axis fulfills the specified condition, INT pin would be triggered, interrupt status would be updated to ANY_MOT_STS, and the sign of slop would be shown in SLPSIGN_X, SLPSIGN_Y, SLPSIGN_Z. Moreover, SLP_1ST_X, SLP_1ST_Y, and SLP_1ST_Z would indicate which axis is the first axis triggering the interrupt of slop detection.

Control Register	Bit Name	Function
INTEN1 [0] INTEN1 [1] INTEN1 [2]	SLP_EN_X SLP_EN_Y SLP_EN_Z	Slope detection enable for X-axis, '1': enabled, '0': disabled for Y-axis, '1': enabled, '0': disabled for Z-axis, '1': enabled, '0': disabled
SIGMOT2[2]	ANY_MOT_EN	Any-motion enable bit. 0: Disabled. 1: Enabled.
SLOPETHD [7:0]	SLP_THD	Slope threshold, 1LSB=1LSB of XOUT/YOUT/ZOUT
SLOPEDLY [1:0]	SLP_DUR	Slope duration, 1LSB=1/(2*bandwidth)
INTMAP1	ANTMOT2INT1	Slope detection interrupt maps to INT1
INTSTS1 [2]	ANT_MOT _STS	Slope detection status which is synchronized with INT1 activity
DATASETUP [7]	DATA_SEL	'1': unfiltered data, '0': filtered data, as the input of the slop detection
EVENTINFO1 [0] EVENTINFO1 [1] EVENTINFO1 [2]	SLP_1ST_X SLP_1ST_Y SLP_1ST_Z	'1': triggered axis, '0': not triggered
EVENTINFO1 [4] EVENTINFO1 [5] EVENTINFO1 [6]	SLPSIGN_X SLPSIGN_Y SLPSIGN_Z	Sign of slope when interrupt is triggered, '0': Positive, '1': Negative



Note: Interrupt latched mode INT_LATCH [3:0] in register INTCFG2 (0x21) can not be default setting after motion algorithms enabled. Interrupt latched mode must be set in the initial configuration.

10.3 Significant Motion

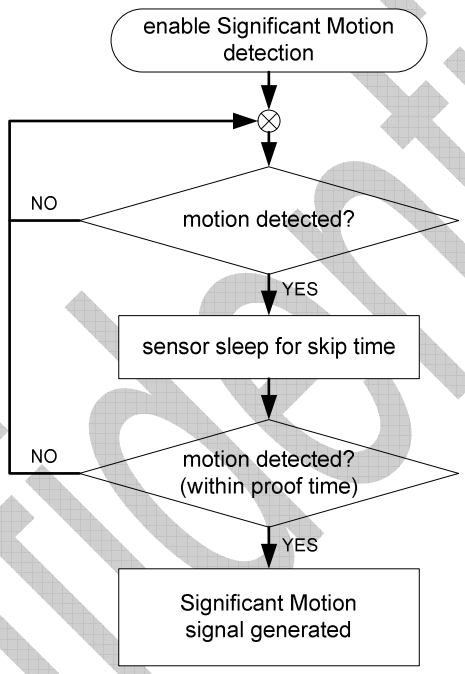
The significant motion is defined as some activities that might lead to a change in a user's location. Examples of significant motions are walking or biking, sitting in a moving car, coach or train, etc. Examples of situations that should not trigger significant motion include phone in pocket and person is not moving, phone is on a table and the table shakes a bit due to nearby traffic or washing machine. For more information, please refer to Android Sensor types: https://source.android.com/devices/sensors/sensor-types.html#significant_motion.

Significant motion function would be triggered by means of monitoring the slope of acceleration over a period of time. The algorithm will be started when a motion is detected, and generates a signal if another motion is detected after the SKIP_TIME[8:0] (0x29-0x2A) and within the PROOF_TIME[7:0] (0x2B). Both 1 LSB of skip time and proof time correspond to 20ms.

The significant motion and slope detection share event-triggered settings including independent XYZ-axes slope enable bit INTEN1 [2:0] (0x16), threshold SLOPETHD [7:0] (0x28), duration SLOPEDLY [1:0] (0x27). User should be noticed that the slope detection has to be enabled before enabling significant motion due to a sharing algorithm engine. Then enable significant motion by writing '1' to SIG_MOT_EN bit in register SIGMOT2 (0x2A).

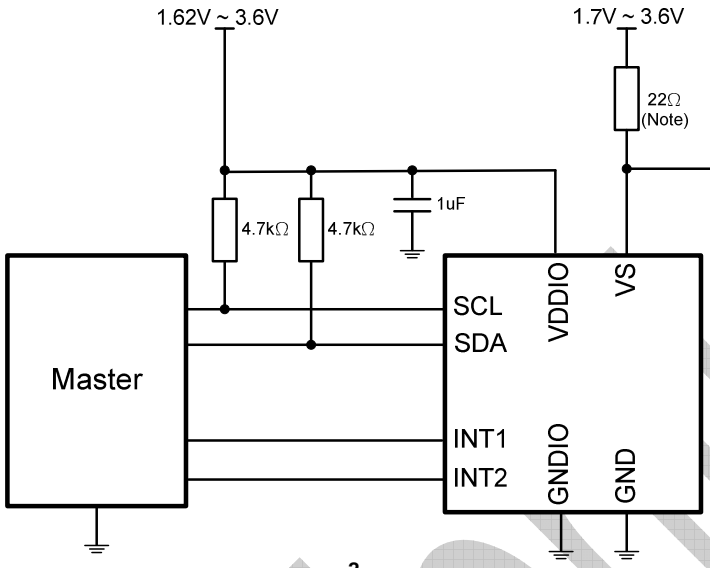
Follow the steps below to enable significant motion:

Step1. (MUST) Set interrupt configurations INTCFG1 (0x20) and INTCFG2 (0x21), especially, interrupt latched mode can not be default setting.
Step2. Set configuration settings include SKIP_TIME[8:0] (0x29-0x2A), PROOF_TIME[7:0] (0x2B), SLOPEDLY[1:0] (0x27) and SLOPETHD[7:0] (0x28).
Step3. Set XYZ-axes slope detection enabled by INTEN1[2:0] (0x16).
Step4. Set significant motion enabled by SIGMOT2[1] (0x2A).
Step5. Mapping significant motion to physical interrupt pin by INTMAP1[0] (0x19).
Step6. Wait for INT triggered or monitor SIG_MOT_STS bit in INTSTS1[0] (0x09)



Significant Motion algorithm flow chart

10.4 Application Circuit

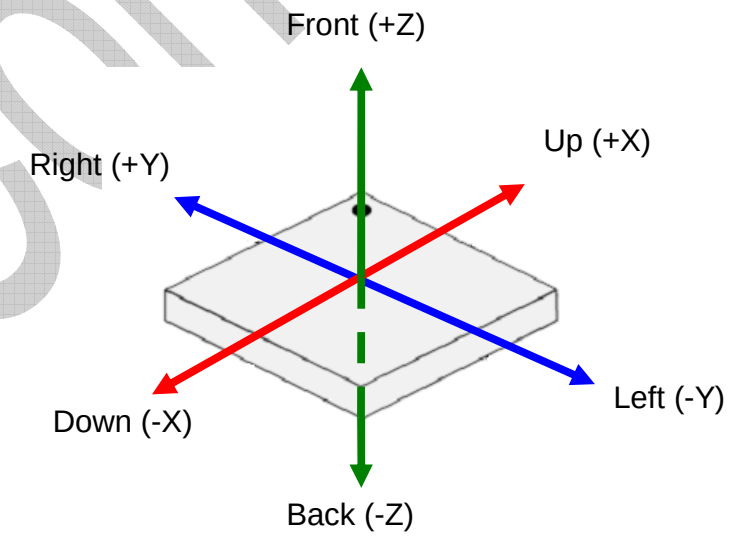


I²C Interface

Note: A 22 ohm resistor is recommended to filter out the system power noise.

10.5 Sensing Axes Orientation

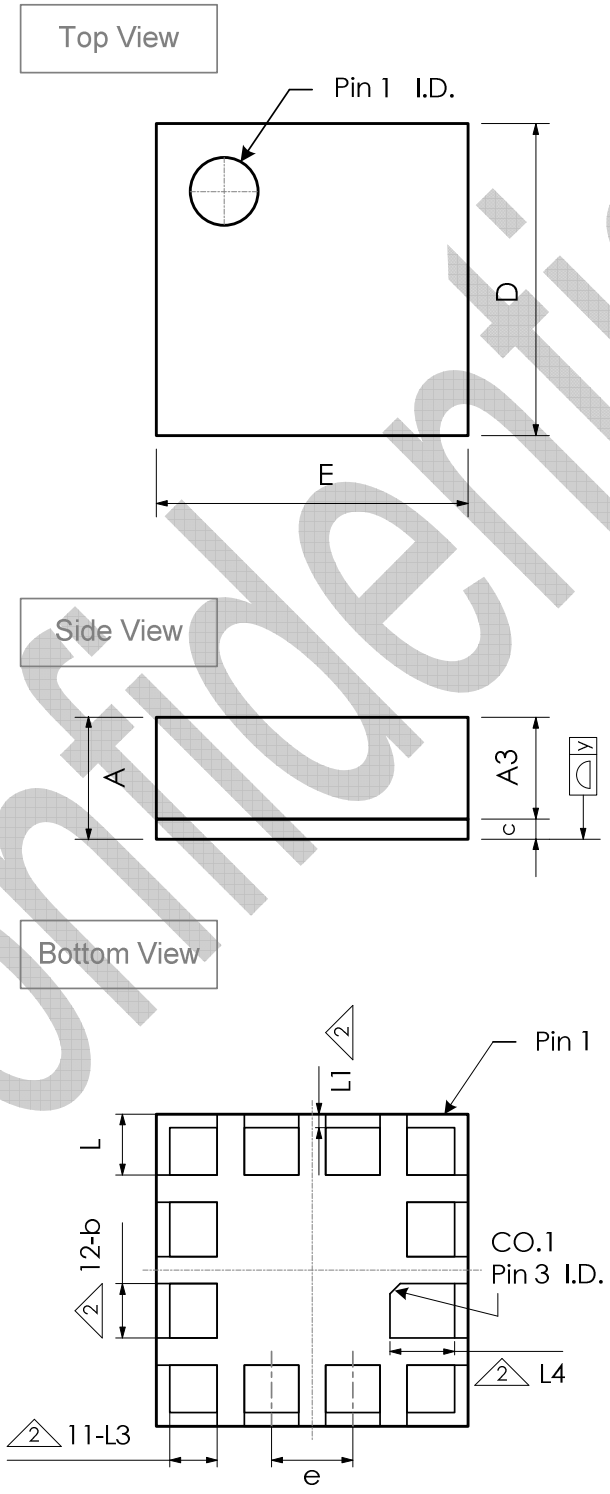
By measuring the acceleration components respect to g field, the position and orientation information could be recognized. It could be used for such applications as Portrait/Landscape in Mobile phone/PDA/PMP. This enables a product to set its display orientation appropriately to either portrait/landscape mode, or to turn off the display if the product is placed upside down. The sensor provides positive or negative directions of X/Y/Z axes. The relationship between directions and six different positions: Left, Right, Up, Down, Back, and Front, is shown in the following figure.



Sensing axes orientation

11. PACKAGE OUTLINE

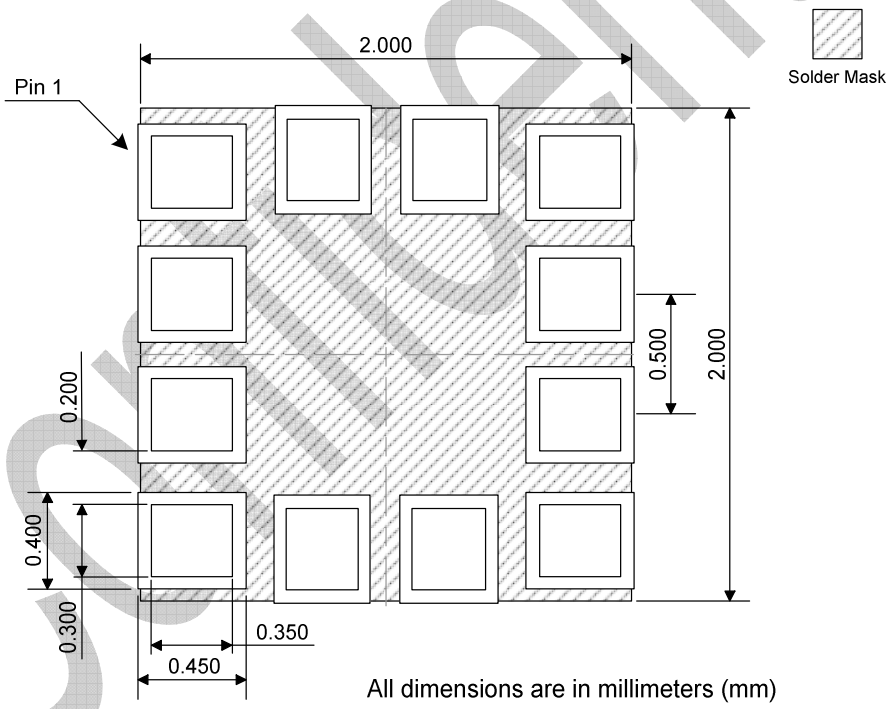
LGA Package Outline Drawing



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX
A	0.95	1.0	1.05
A3	---	0.82 REF.	---
b	0.23	0.28	0.33
c	---	0.18 REF.	---
D	1.90	2.00	2.10
E	1.90	2.00	2.10
e	---	0.50	---
L	0.325	0.375	0.425
L1	---	0.05	---
L3	0.275	0.325	0.375
L4	0.375	0.425	0.475
y	0.00	---	0.10

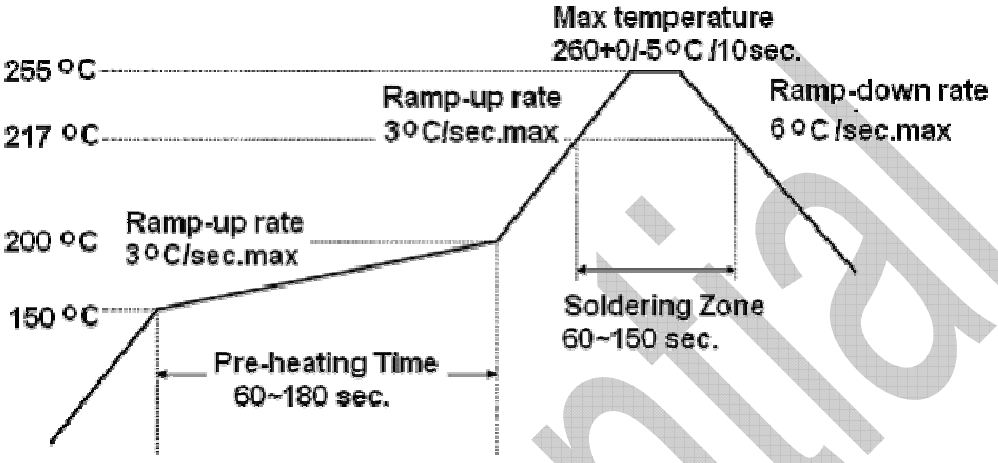
Recommended PCB Layout

The PCB layout should use NSMD (Non Solder mask Defined) pad definitions for all pads. The solder mask opening must be defined at least 0.05 mm larger than the metal pad on all sides.



11.1 Soldering Condition

1. Pb-free solder temperature profile



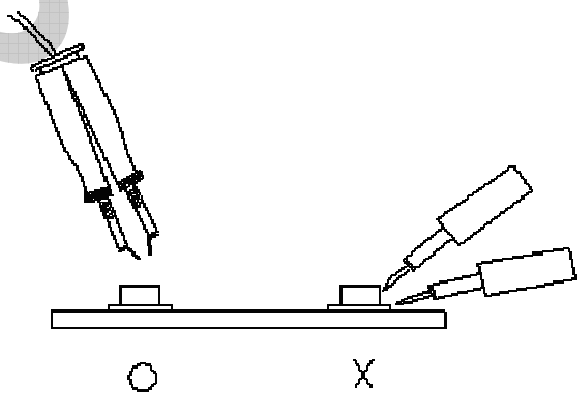
2. Reflow soldering should not be done more than three times.
3. When soldering, do not put stress on the ICs during heating.
4. After soldering, do not warp the circuit board.

11.2 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350℃ for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

11.3 Repairing

Repair should not be done after the ICs have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the ICs will or will not be damaged by repairing.



12. STORAGE INFORMATION

12.1 Storage Condition

1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
2. The delivery product should be stored with the conditions shown below:

Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

12.2 Treatment After Unsealed

1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

Floor Life	168 Hours
Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

2. When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be re-baked before reflow to prevent damage to the devices. The recommended conditions are shown below

Temperature	60℃
Re-Baking Time	12 Hours

Revision History

Date	Version	Modified Items
2015/02/11	0.9	Initial release.
2015/08/07	0.9.1	Fix typo.
2015/09/07	0.9.2	1. Change to bandwidth parameter. 2. Fix typo.
2015/11/24	0.9.3	1. Add the X/Y/Z directions of six orientations. 2. INTMAP naming mismatch Fixed. 3. Add data not updated when suspending.
2016/02/26	0.9.4	1. Add MSL 3 notification. 2. Modify output data rate (ODR). 3. Modify 0 g OFFSET.
2016/08/09	1.0	1. Add CHIP_ID 2. INTCFG1 default value Fixed 3. Update recommended PCB layout 4. Update register table
2016/09/19	1.1	1. Drop +/-16g mode
2017/01/18	1.2	1. Add low power mode, any motion detection, and significant motion detection. 2. Fix typo.
2017/03/27	1.3	1. Modify 8.4 Motion Algorithm description. 2. Add low-power mode control bit. 3. Add ANY_MOT_EN bit. 4. Modify 10.2 any-motion description. 5. Modify 10.3 significant motion description. 6. Fix typo.

单击下面可查看定价，库存，交付和生命周期等信息

>>Sensortek(昇佳電子)