History of Specification

Revsion number	Date	Page	Details	Person in charge	Remark
00	2012.11.01		Creation of Specification Sheet	K.H. Lee	
01	2012.11.15	5	Maximum ratings	K.H. Lee	
		12 - 14	Packing & Labeling		
		14 - 16	Precaution		
02	2013.04.02	9 – 10	Product Name and Sorting Bin	K.H. Lee	
03	2013.05.21	9 – 10	Product Name and Sorting Bin	K.H. Lee	
		8	Visual Inspection(Pinholes, Surface scratch)		
04	2013.11.12	4	Typical Electro-Optical Characteristics at Ta=25℃	K.H. Lee	
		9 - 10	Product Name and Sorting Bin		
05	2014.03.21	12 – 14	Packing & Labeling	H.K. Kim	
		14 – 16	Precaution		
06	2014.11.21	4 – 5	Typical Electro-Optical Characteristics at Ta=25℃	S.H. Lee	
		7 – 8	Visual inspection		
		9 – 10	Product name and Sorting Bins		
		13 -15	Precaution		

History of Specification

Revsion number	Date	Page	Details	Person in charge	Remark
07	2016.01.07	4	Chip Diagram (PAD size 140um->120um)	S.H. Lee	
		7 – 9	Visual inspection		
		issue	Chip structure modified		
			Chip Passivation enhanced		
08	2016.07.11	5 - 6	Typical Electro-Optical Characteristics at Ta=25℃	S.H. Lee	
09	2017.03.03	9~11	Visual inspection addition (1)	J.Y. Park	
	2017.03.08		Visual inspection addition (2)	J.Y. Park	
10	2018.03.06	5	Typical Electro-Optical Characteristics at Ta=25℃ Updates	J.Y. Park	
11	2019.07.01	12 - 13	Added sorting bin	J.H. Lee	

1B-25, 727, Wonsi-dong, Danwon-gu, Ansan-city, Gyeonggi-do, Korea 425-851

Customer:

Part Name: UV1000-39

Contents:

Seoul Viosys Co., Ltd.		
Drawn by	Checked by	Approved by
J.H. Lee		K.H. Lee
2019.07.01		2019.07.01

Customer		
Checked by		Approved by

1. Features and Application

- High Luminous Intensity, Long Operation Life
- Power Package Application
- UV Curing, Printing, Coating

2. Part Name:

- UV1000-39

3. Main Material

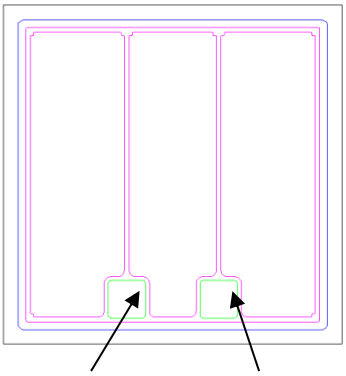
- Epitaxial Layer: GaN Based LED Structure

4. Electrodes

- P-Electrode: Au
- N-Electrode : Au

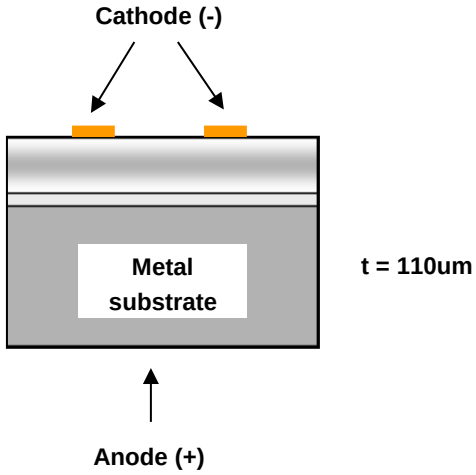
5. Chip Diagram

TOP View



<Fig. 1 >Plane View

Die Cross Section



<Fig. 2> Cross Sectional View

6. Maximum Ratings at Ta=25℃

DC Forward Current	700mA
Junction Temperature[a]	125℃
Operating Temperature Range	-30℃ to + 85℃
Storage Temperature Range (Chip)	-40℃ to +100℃

('Maximum Ratings' mean when it exceeds the chip has the possibility of breaking down when these conditions are exceeded momentarily. 'Maximum ratings', the chip is not guaranteed to endure such conditions. 'Maximum Ratings' concerning your LED device after the chip is built into your package shall be established by yourself since these greatly depend on the design of the device, the conditions of assembly, the environment used, and so forth.)

[a]Measurement condition : AAP63 PKG

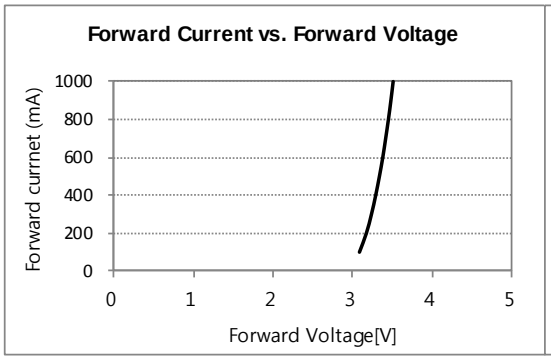
7. Typical Electro-Optical Characteristics at Ta=25℃

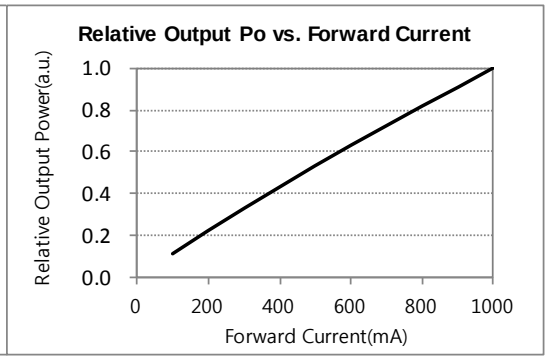
ITEM	Symbol	Condition	Characteristics (Ta=25℃)			Unit
			Min	Typ	Max	
Reverse Current	I_R	V_R =5V	0	-	1.0	uA
Turn-on Voltage	V_{F1}	I_F =10uA	2.3	-	3.0	V
Forward Voltage	V_{F2}	I_F =500mA	3.3	3.50	3.7	V
Peak Wavelength (1)	Wp	I_F =500mA	390	393	400	nm
Full Width Half Maximum	Δλ	I_F =500mA	-	10	-	nm
Luminous Intensity (2)	Po	I_F =500mA	700	1040	1180	mW

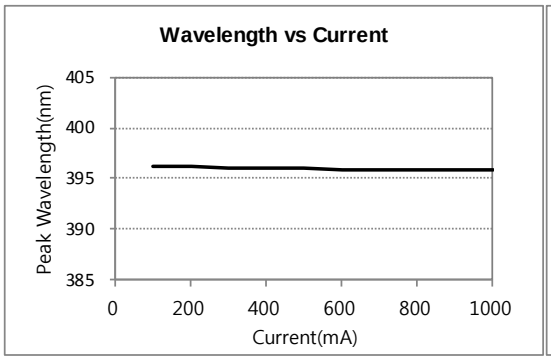
Note: Radiant and Peak wavelength are measured by Seoul Viosys's equipment.

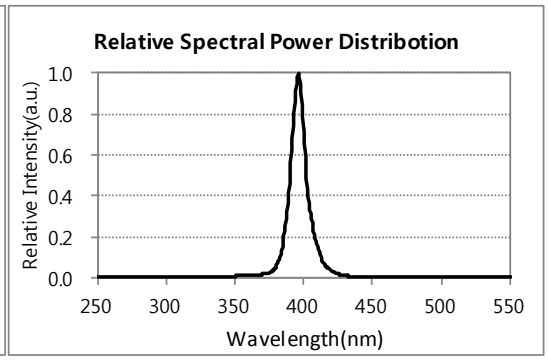
Peak Wavelength: ±1nm. (1), Luminous Intensity : ±10%. (2)

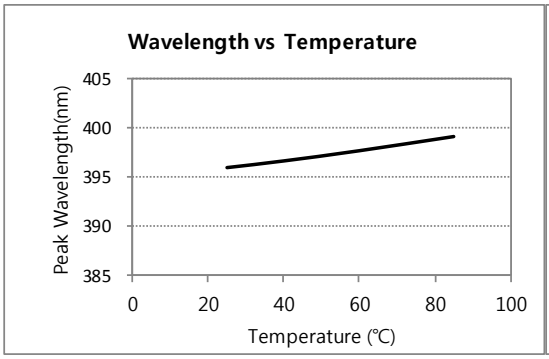
It is recommended to operate the LED at a minimum current 100mA to stabilize the LED characteristics

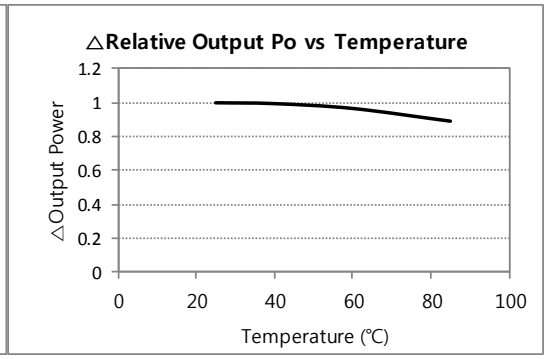


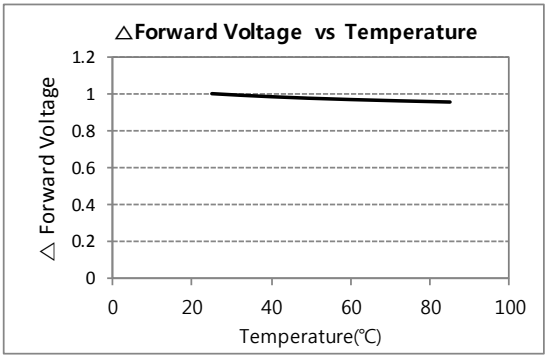












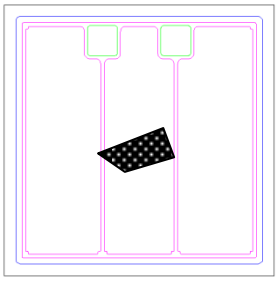
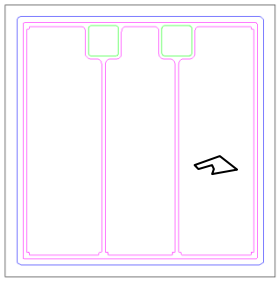
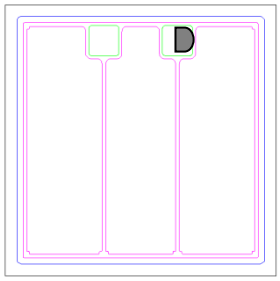
※ These curves represent typical performance of the UV1000-39 LED chip.
Actual performance will vary slightly for different power & peak wavelength bins.

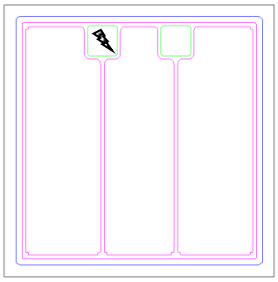
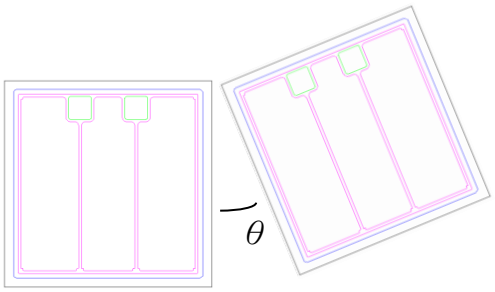
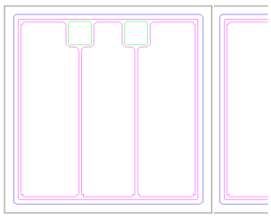
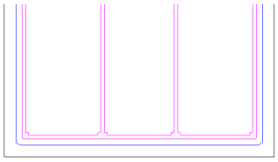
8. Mechanical Specifications

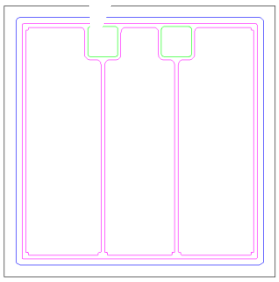
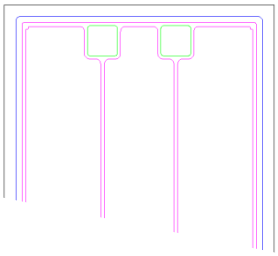
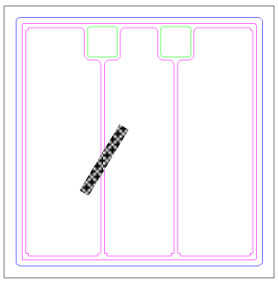
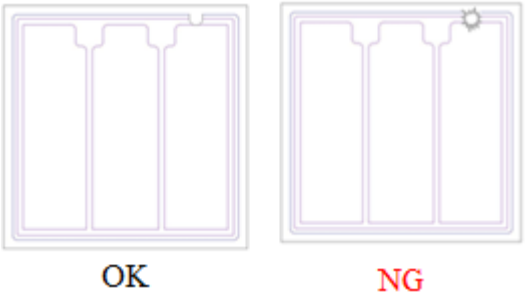
Description	Dimension	Tolerance
P-N junction Area	960 × 960um	±50um
Chip Area	1,050 × 1,050um	±50um
Chip Thickness	110um	±20um
Pad Size	120um	±15um

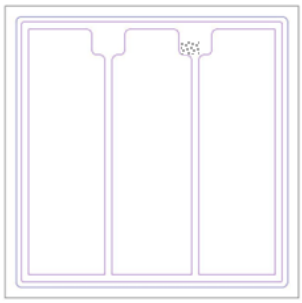
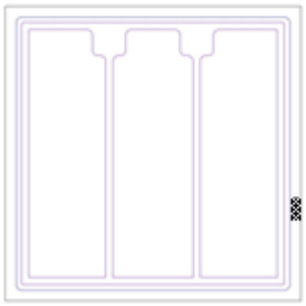
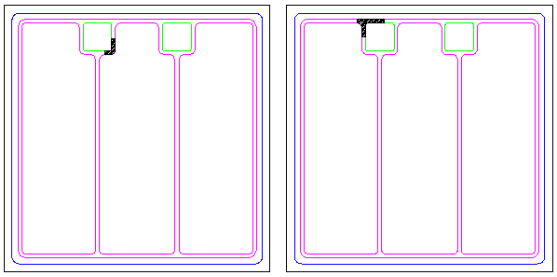
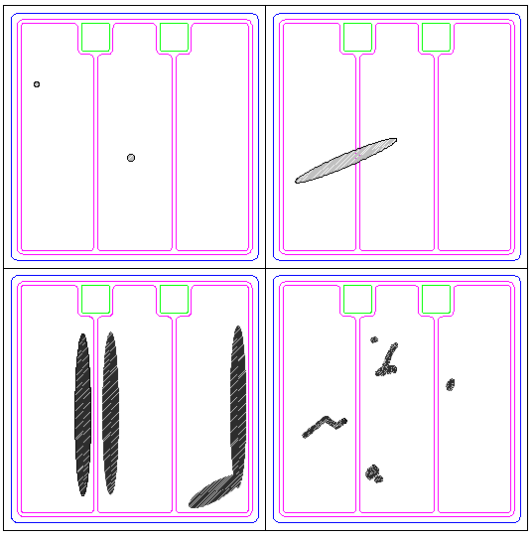
9. Visual inspection

Done by optical microscope (20x).

Item	Accepted (OK)/defective (N.G.)	Example
Surface dirt	accepted：if surface dirt(metal) less than 5% of unit cell.	
Passivation film peeling	accepted：if Passivation film peeling less than 10% of unit cell.	
Partially missing bond pad	accepted：a ＜ b/10 a: missing bond pad b: normal bond pad	

Bond pad scratch	accepted：if bond pad scratch (including probe mark) less than 15 % of bond pad area	
θ shift	accepted：θ < ±5°	
Twins or triples	Inseparable chips are rejected If extra-size is less than 10%, OK.	
Dicing shift	The light-emitting surface, pad can’t be cut-off	

Chipping	Pad electrode not chipped off	
Bad cut	Not accepted : if bad cut is occured	
Surface scratches	accepted : if surface scratch less than 5% of surface emitting area	
Mesa line defect	Accepted : inner metal line (Over etched) Defective : crack or chipping if occurred	

Pad Contamination	Accepted : if contamination less than 10% of bond pad area	
Edge Contamination	Accepted：if contamination less than 5% of chip out line	
Passivation Contamination	Accepted：if SiO2 passivation line is not contact to dark area.	
Surface Color un- uniform (1)	Accepted:Un-uniform area is less than 30% of total area.	
Surface Color un- uniform (2)		

10. Product Name and Sorting Bin

(1) Product Name

Product Name	39	X	YY
UV1000-39XYY	Wp(nm) (390 ~ 400)	L : Low Wp (390~395nm) H : High Wp (395~400nm)	Vf & Power

(2) Sorting Bin

Rank	Bin #	Ir@-5V	Vf1@10uA	Wp@500mA	Vf@500mA	Po@500mA
UV1000-39L01	1	0~1.0uA	2.3~3.0V	390~395nm	3.3~3.4V	700~780mW
UV1000-39L02	2				3.4~3.5V	
UV1000-39L03	3				3.5~3.6V	
UV1000-39L04	4				3.6~3.7V	
UV1000-39L05	5				3.7~3.8V	
UV1000-39L06	6				3.8~3.9V	
UV1000-39L07	7				3.3~3.4V	780~860mW
UV1000-39L08	8				3.4~3.5V	
UV1000-39L09	9				3.5~3.6V	
UV1000-39L10	10				3.6~3.7V	
UV1000-39L11	11				3.7~3.8V	
UV1000-39L11	12				3.8~3.9V	
UV1000-39L13	13				3.3~3.4V	860~940mW
UV1000-39L14	14				3.4~3.5V	
UV1000-39L15	15				3.5~3.6V	
UV1000-39L16	16				3.6~3.7V	
UV1000-39L17	17				3.7~3.8V	
UV1000-39L18	18				3.8~3.9V	
UV1000-39L19	19				3.3~3.4V	940~1020mW
UV1000-39L20	20				3.4~3.5V	
UV1000-39L21	21				3.5~3.6V	
UV1000-39L22	22				3.6~3.7V	
UV1000-39L23	23				3.7~3.8V	
UV1000-39L24	24				3.8~3.9V	
UV1000-39L25	25				3.3~3.4V	1020~1100mW
UV1000-39L26	26				3.4~3.5V	
UV1000-39L27	27				3.5~3.6V	
UV1000-39L28	28				3.6~3.7V	
UV1000-39L29	29				3.7~3.8V	
UV1000-39L30	30				3.8~3.9V	

Rank	Bin #	Ir@-5V	Vf1@10uA	Wp@500mA	Vf@500mA	Po@500mA
UV1000-39H01	31	0~1.0uA	2.3~3.0V	395~400nm	3.3~3.4V	700~780mW
UV1000-39H02	32				3.4~3.5V	
UV1000-39H03	33				3.5~3.6V	
UV1000-39H04	34				3.6~3.7V	
UV1000-39H05	35				3.7~3.8V	
UV1000-39H06	36				3.8~3.9V	
UV1000-39H07	37				3.3~3.4V	780~860mW
UV1000-39H08	38				3.4~3.5V	
UV1000-39H09	39				3.5~3.6V	
UV1000-39H10	40				3.6~3.7V	
UV1000-39H11	41				3.7~3.8V	
UV1000-39H12	42				3.8~3.9V	
UV1000-39H13	43				3.3~3.4V	860~940mW
UV1000-39H14	44				3.4~3.5V	
UV1000-39H15	45				3.5~3.6V	
UV1000-39H16	46				3.6~3.7V	
UV1000-39H17	47				3.7~3.8V	
UV1000-39H18	48				3.8~3.9V	
UV1000-39H19	49				3.3~3.4V	940~1020mW
UV1000-39H20	50				3.4~3.5V	
UV1000-39H21	51				3.5~3.6V	
UV1000-39H22	52				3.6~3.7V	
UV1000-39H23	53				3.7~3.8V	
UV1000-39H24	54				3.8~3.9V	
UV1000-39H25	55				3.3~3.4V	1020~1100mW
UV1000-39H26	56				3.4~3.5V	
UV1000-39H27	57				3.5~3.6V	
UV1000-39H28	58				3.6~3.7V	
UV1000-39H29	59				3.7~3.8V	
UV1000-39H30	60				3.8~3.9V	
UV1000-39L31	61			390~395nm	3.3~3.4V	1100~1180mW
UV1000-39L32	62				3.4~3.5V	
UV1000-39L33	63				3.5~3.6V	
UV1000-39L34	64				3.6~3.7V	
UV1000-39L35	65				3.7~3.8V	
UV1000-39L36	66				3.8~3.9V	
UV1000-39H31	67			395~400nm	3.3~3.4V	1100~1180mW
UV1000-39H32	68				3.4~3.5V	

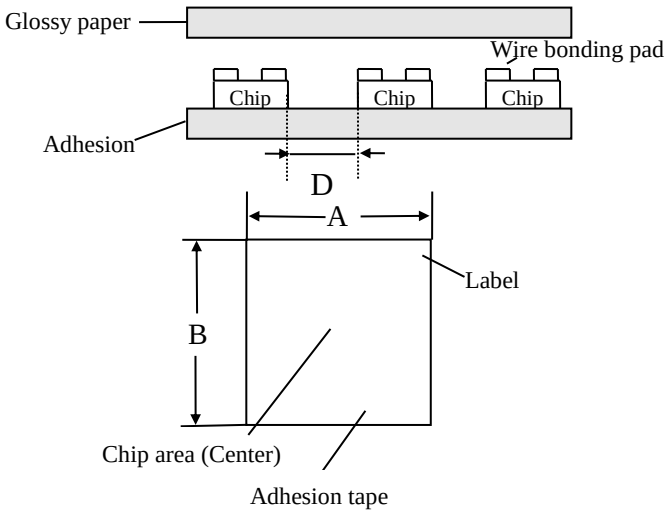
Rank	Bin #	Ir@-5V	Vf1@10uA	Wp@500mA	Vf@500mA	Po@500mA
UV1000-39H33	69	0~1.0uA	2.3~3.0V	395~400nm	3.5~3.6V	1100~1180mW
UV1000-39H34	70				3.6~3.7V	
UV1000-39H35	71				3.7~3.8V	
UV1000-39H36	72				3.8~3.9V	

11. Packing

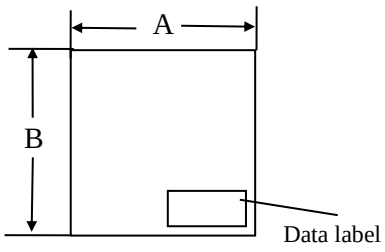
(1) Chips-on-tape

(a) Electro-Optical measurement data should be labeled and tacked on the backside of the glossy paper.

Chip area should be in the center of adhesion tape, and the wire-bonding pad should face toward the covered glossy paper.



(b) Chip type, Lot No. and quantity etc. should be labeled and tacked to the corner of the glossy paper.



(c) Dimensions

Item	Instruction
Adhesion tape	Semi- transparent blue
Glossy paper (A×B)	197mm × 220mm
Chip Qty／tape	Min. 100 EA
Chip separation (D)	Typ. 0.35mm

(2) Packing for shipment

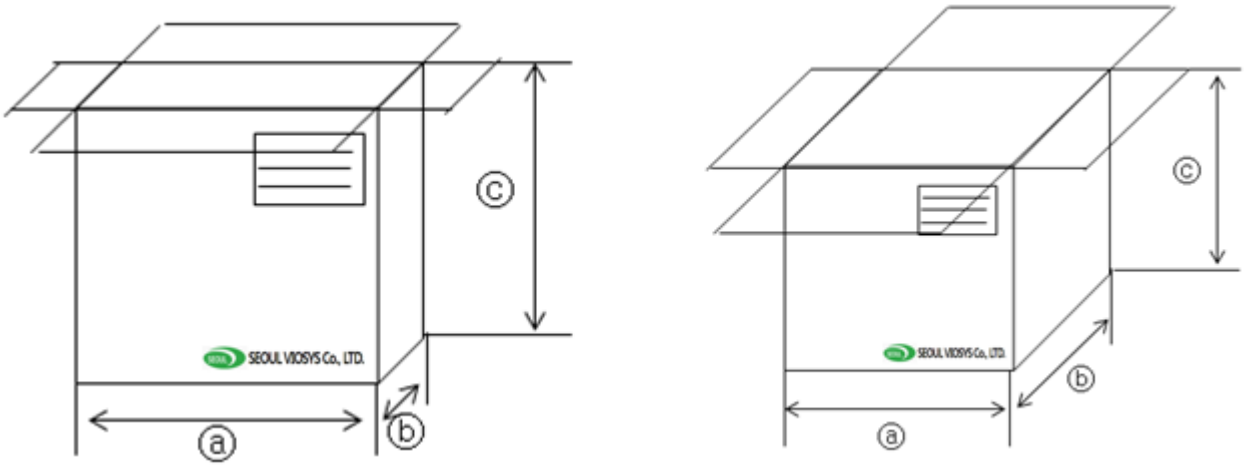
(a) The sheets (adhesion tape + glossy paper) are packed in an anti-static electricity bag. The anti-static electricity bag has two different size; 240mmx270mm and 300mmx300mm. Each anti-static bag can contain up to 80sheets and 150sheets respectively.

(b) The anti-static bags are packed in a box. The size of this box is 250mm×65mm×275mm (ⓐ × ⓑ × ⓒ). Each box can contain up to 5 anti-static electricity bags.

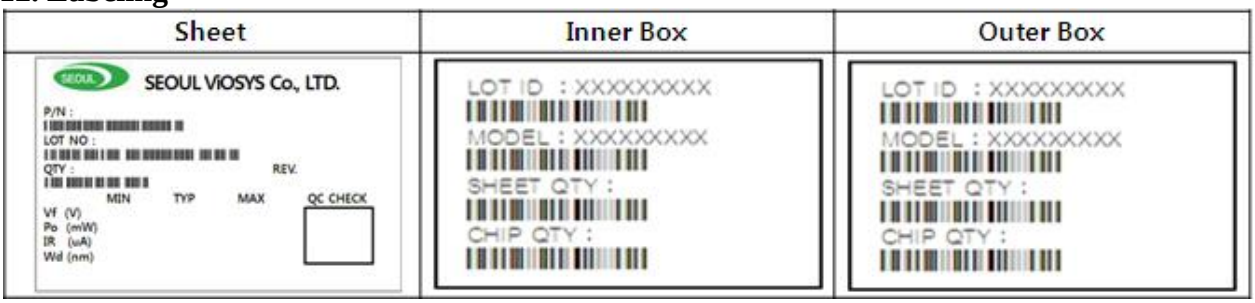
(c) The boxes which contain anti-static electricity bags are packed in the other box. The size of this outer box is 260mm×340mm×290mm (ⓐ × ⓑ × ⓒ). Each outer box can contain up to 5 inner boxes.

(d) Each sheet / box is labeled with information describing its content. (Details please refer to section 12)

TYPE	SIZE(mm)		
	ⓐ	ⓑ	ⓒ
Inner box	250	65	275
Outer box	260	340	290



12. Labeling



(1) Sheet : The measurement data for each lot are also shown on the backside of the sheet.

(2) Inner Box : The information about the products is also shown on the inner box.

(3) Outer Box : The information about the products is also shown on the outer box.

13. Precaution

(1) Quality Guarantee

The chip guarantee period is three months after the delivery under the following preservation conditions. If any defective is found, the customer shall immediately inform of that to Seoul Viosys Co., Ltd. Preservation conditions (when the shipping package is unopened.)

· Temperature and humidity : 0 ~ 45 °C, sealed bag open≤70%RH, sealed bag close ≤90%RH

· Atmosphere: Keep the chips in a desiccator with silica gel or with nitrogen substitution.

(2) Handling of Electrostatic Discharge

· The chips are sensitive to static electricity charge and users are required to handle with care. If the applied current and/or voltage exceed the max rating, the overflow in energy may cause damage to, or possibly result in electrical destruction of the products. Accordingly, Customer should take absolutely secure countermeasure against static electricity and surge when handling products.

· It is highly recommended to utilize the diodes for prevention of ESD damage (Zener diode, TVS, etc) when applications are designed. This measure could keep the applications safe by blocking the excess of maximum ratings for surge current during on/off switching.

· Proper grounding of products (via 1MΩ), use of conductive mat, semiconductive working uniform and shoes, and semiconductive containers are considered to be effective as countermeasures against static electricity and surge. It is recommended to use an ionizer in the facility or environment where static electricity may be generated easily.

· High humidity and extremely low temperature can cause ESD damage to make reliability worse. Users make sure that the chips should not be stored or packaged in this environment and keep an eye on dealing with humidity and temperature.

· Preliminary inspection is first recommended if chips are out of order due to ESD damage in users' applications. ESD damage can be detected by applying low current (≤1mA).
Failure Criteria : V_F <2.0V at 0.5mA

(3) General precaution for use

· Chips should be stored in a clean environment. If the Chips are to be stored for 3 months or more after being shipped from Seoul Viosys, they should be packed by a sealed container with nitrogen gas injected. (Shelf life of sealed bags : 1year)

· Chips should keep away from high humidity environment. The chips surrounded by the environment with high moisture can be damaged, which can cause degradation of optical and electrical performance as well as delamination between the interfaces.

· This chip should not be used directly in any type of fluid such as water, oil, organic solvent, etc. When washing is required, IPA is recommended to use.

· After sealed bag is open, device subjected to soldering, solder flow, or other high temperature processes must be:
Mounted within 168 hours (7days) at an assembly line with a condition of no more than 30°C and 70% RH

· Chips require baking before mounting, if humidity card reading is >70% at, 23±5°C. Chips must be baked for 24Hrs. at 65±5°C, if baking required.

· When the chips are illuminating, the maximum ambient temperature should be first considered before operation. If voltage exceeding the absolute maximum rating is applied to chips, it may cause damage or even destruction to chips. Damaged LEDs will show some abnormal characteristics such as remarkable increase of leak current, lower turn-on voltage and getting unlit at low current.

· Chips are intended to be operating for ordinary electronic devices. It is not guaranteed to be used for the applications (such as aviation, aerospace, heating equipment, life-sustaining equipment) which could require extremely high reliability and safety. In addition to damage to the chips, it could directly threaten human life and safety.

· UV light could have negative effects on raw and subsidiary materials users utilize for applications. If users utilize materials which can be reacted or weakened by UV light, it might be possible to damage the applications. Please keep in mind that it is recommendable to take advantage of durable materials which is not affected by UV light.

· The appearance and specifications of the products may be modified for improvement without further notice.

(4) Chip Handling Precaution

· Adhesives or Tapes : Please keep away from the Adhesives or Tapes to the light emitting surface. Even a small piece of residue can be possible to cause the reduced light extraction efficiency and mechanically damage the surface.

· Wrist bands or Anti-electrostatic gloves : If possible, utilize wrist bands and Anti-electrostatic gloves. This precautionary measure is to ward off ESD damage.

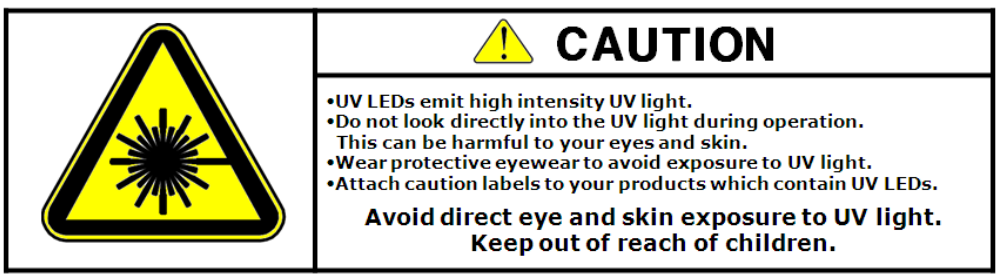
· Do not press the chip even covered with blue sheets.

· Do not fold the blue sheets with the chips.

The above specifications are subject to change with prior notice.

Seoul Viosys Co., Ltd

July 01, 2019



单击下面可查看定价，库存，交付和生命周期等信息

>>Seoul Viosys(首尔伟傲世)