SGM7226
V_{BUS} Directly Powered, High Speed USB 2.0 (480Mbps) DPDT Analog Switch

GENERAL DESCRIPTION

The SGM7226 is a DPDT (double-pole/double-throw) analog switch. It operates from a 1.8V to 5.5V single power supply and can be powered directly by V_{BUS}. Each switch of the SGM7226 is bidirectional, which can ensure that the high speed signals have little or no attenuation at the outputs.

The SGM7226 features high speed, low power and wide bandwidth. The high performances make it very suitable for multiple applications, such as cellular phones and computer peripherals, etc.

The SGM7226 has a power-off protection. It can prevent accidental signal leakage and ensure system reliability under power-down and over-voltage conditions. In addition, the device is capable of withstanding a V_{BUS} short to D+ or D- when the device is either powered on or powered off due to the special circuitry on the D+/D- pins.

The SGM7226 is available in a Green TQFN-2.6×1.8-16L package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Supply Voltage Range: 1.8V to 5.5V**
- **V_{BUS} Directly Power**
- **On-Resistance: 5Ω (TYP)**
- **High Off-Isolation: -35dB (R_L = 50Ω, f = 250MHz)**
- **Low Crosstalk: -30dB (R_L = 50Ω, f = 250MHz)**
- **-3dB Bandwidth: 550MHz**
- **Fast Switching Times at V_{CC} = 5V:**
  t_{ON} = 15ns (TYP)
  t_{OFF} = 20ns (TYP)
- **Break-Before-Make Switching**
- **Power-Off and Power-On Protections**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in a Green TQFN-2.6×1.8-16L Package**

APPLICATIONS

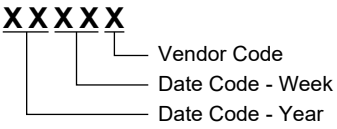
Cellular Phones
Digital Cameras
Portable Equipment
Computer Peripherals
Battery-Powered Systems
Routes Signals for USB 2.0 Full-Speed

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM7226	TQFN-2.6×1.8-16L	-40℃ to +85℃	SGM7226YTQA16G/TR	7226 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... 0V to 6.0V
V_{SET} ..... -0.3V to 5.5V
$\overline{OE}$, S, HSDn+, HSDn-, D+, D- ..... -0.3V to 3.3+0.3V
Continuous Current HSDn or Dn ..... ±50mA
Peak Current HSDn or Dn ..... ±100mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 8000V
MM 400V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 1.8V to 5.5V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

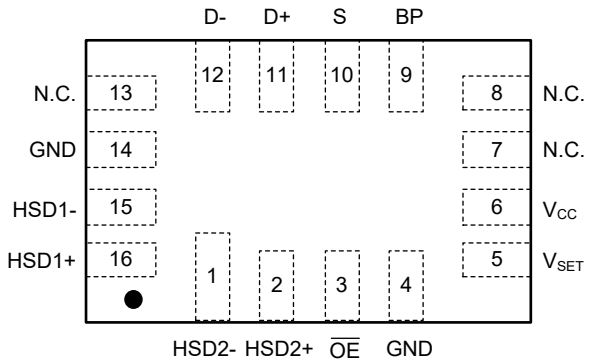
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)

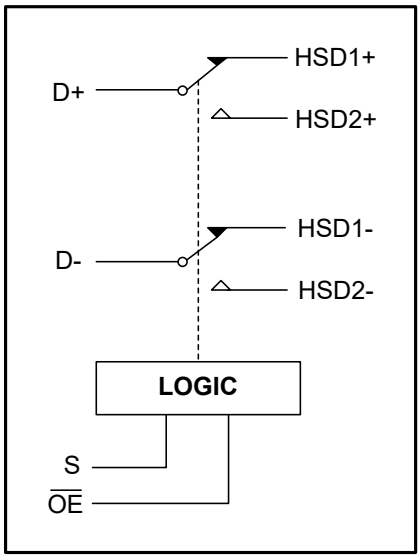


TQFN-2.6×1.8-16L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1,2	HSD2-, HSD2+	Data Ports.
15, 16	HSD1-, HSD1+	
11, 12	D+, D-	
3	$\overline{OE}$	Output Enable Control Pin.
4, 14	GND	Ground.
5	V_{SET}	Internal Used Pin. It is recommended to connect a 10kΩ resistor between V_{SET} pin and V_{CC} pin.
6	V_{CC}	Positive Power Supply Pin.
7, 8, 13	N.C.	No Connect.
9	BP	Internal Voltage Reference Decoupling Pin. A 2.2μF ceramic capacitor must be used to provide enough decoupling. Connect the capacitor between BP pin and GND.
10	S	Select Input Pin.

BLOCK DIAGRAM



FUNCTION TABLE

$\overline{OE}$	S	HSD1+, HSD1-	HSD2+, HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	*X*	OFF	OFF

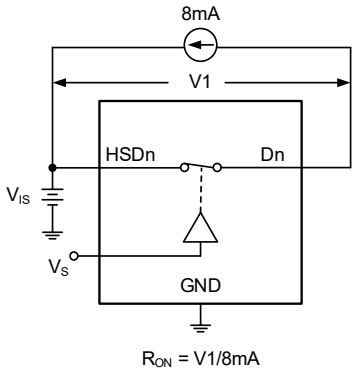
X = Don’t care.

ELECTRICAL CHARACTERISTICS

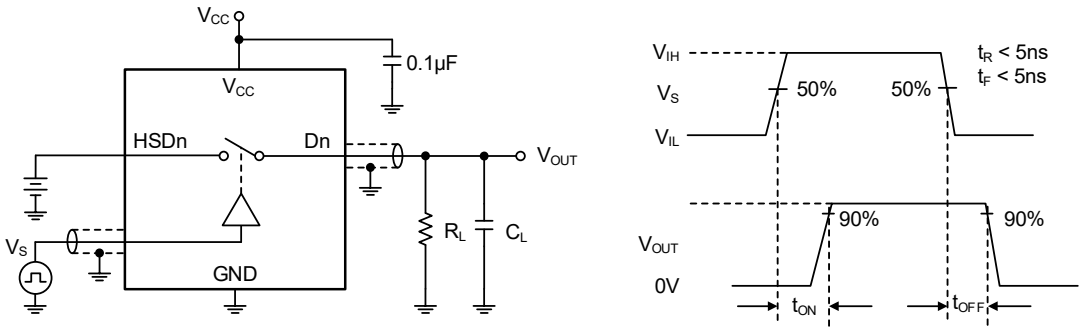
(V_{CC} = +5.0V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Switch						
Analog I/O Voltage (D+, D-, HSD1+, HSD1-, HSD2+, HSD2-)	V_{IS}		0		3.3	V
On-Resistance	R_{ON}	V_{IS} = 0V to 0.4V, I_D = 8mA, Test Circuit 1		5	6.5	Ω
On-Resistance Match between Channels	ΔR_{ON}	V_{IS} = 0V to 0.4V, I_D = 8mA, Test Circuit 1		0.35	0.6	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{IS} = 0V to 1.0V, I_D = 8mA, Test Circuit 1		0.6	1	Ω
Power Off Leakage Current (D+, D-)	I_{OFF}	V_{CC} = 0V, V_D = 0V to 3.6V, V_S , $V_{\overline{OE}}$ = 0V or 3.6 V			1	μA
Source Off Leakage Current	$I_{HSD2(OFF)}$, $I_{HSD1(OFF)}$	V_{IS} = 3.3V/0.3V, V_D = 0.3V/3.3V			1	μA
Channel On Leakage Current	$I_{HSD2(ON)}$, $I_{HSD1(ON)}$	V_{IS} = 3.3V/0.3V, V_D = 3.3V/0.3V or floating			1	μA
Digital Inputs						
Input High Voltage	$V_{IH\ (S,\ \overline{OE})}$		1.5		3.3	V
	$V_{IH\ (VSET)}$		1.5		5.5	
Input Low Voltage	V_{IL}				0.35	V
Input Leakage Current	$I_{IN\ (S,\ \overline{OE})}$				1	μA
	$I_{IN\ ((VSET)}$				1.5	
Dynamic Characteristics						
Turn-On Time	t_{ON}	V_{IS} = 0.8V, R_L = 50Ω, C_L = 10pF, Test Circuit 2		15		ns
Turn-Off Time	t_{OFF}			20		ns
Break-Before-Make Time Delay	t_D	V_{IS} = 0.8V, R_L = 50Ω, C_L = 10pF, Test Circuit 3		3.5		ns
Propagation Delay	t_{PD}	R_L = 50Ω, C_L = 10pF		0.5		ns
Off Isolation	O_{ISO}	Signal = 0dBm, R_L = 50Ω, f = 250MHz, Test Circuit 4		-35		dB
Channel-to-Channel Crosstalk	X_{TALK}	Signal = 0dBm, R_L = 50Ω, f = 250MHz, Test Circuit 5		-30		dB
-3dB Bandwidth	BW	Signal = 0dBm, R_L = 50Ω, C_L = 5pF, Test Circuit 6		550		MHz
Channel-to-Channel Skew	t_{SKEW}	R_L = 50Ω, C_L = 10pF		1.5		ns
Charge Injection Select Input to Common I/O	Q	V_G = GND, C_L = 1.0nF, R_G = 0Ω, Q = C_L × V_{OUT}, Test Circuit 7		10		pC
HSD+, HSD-, D+, D- ON Capacitance	C_{ON}	f = 1MHz		10		pF
		f = 250MHz		15		
Power Requirements						
Power Supply Range	V_{CC}		1.8		5.5	V
Power Supply Current	I_{CC}			20	30	μA

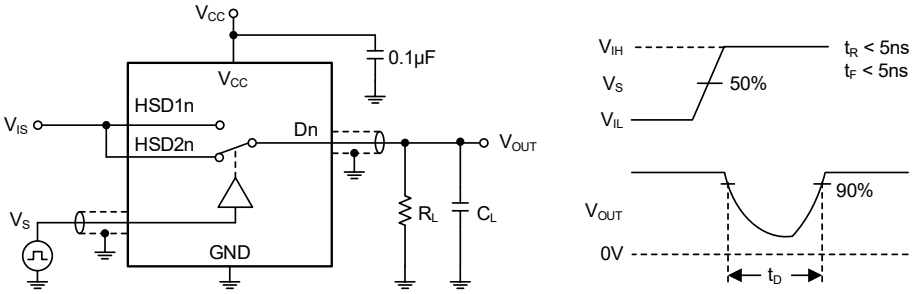
TEST CIRCUITS



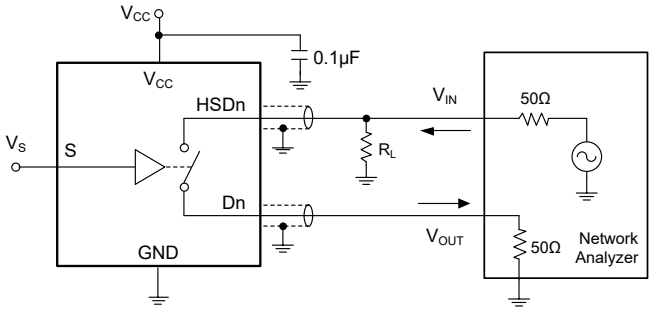
Test Circuit 1. On-Resistance



Test Circuit 2. Switching Times (t_{ON}, t_{OFF})

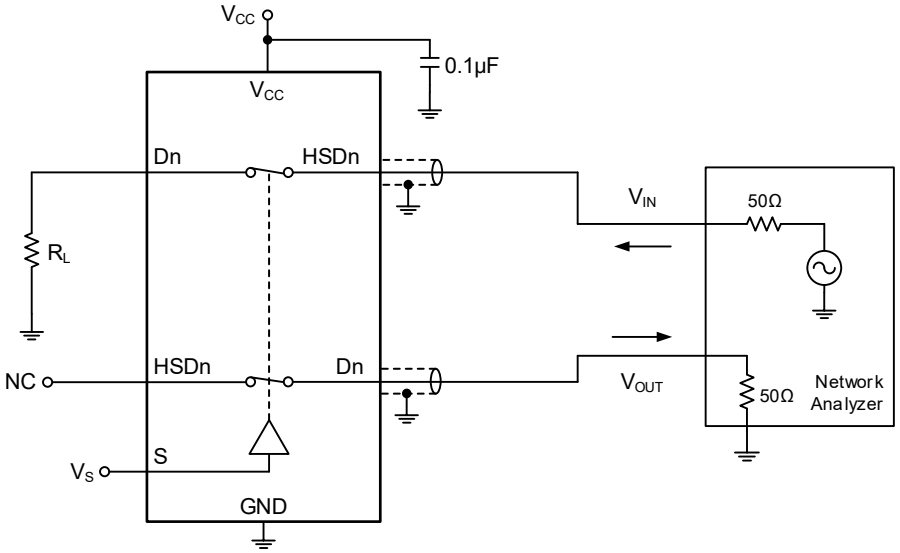


Test Circuit 3. Break-Before-Make Time (t_D)



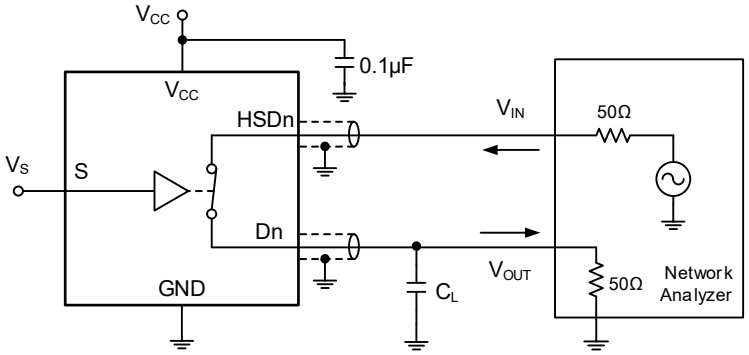
Test Circuit 4. Off Isolation

TEST CIRCUITS (continued)

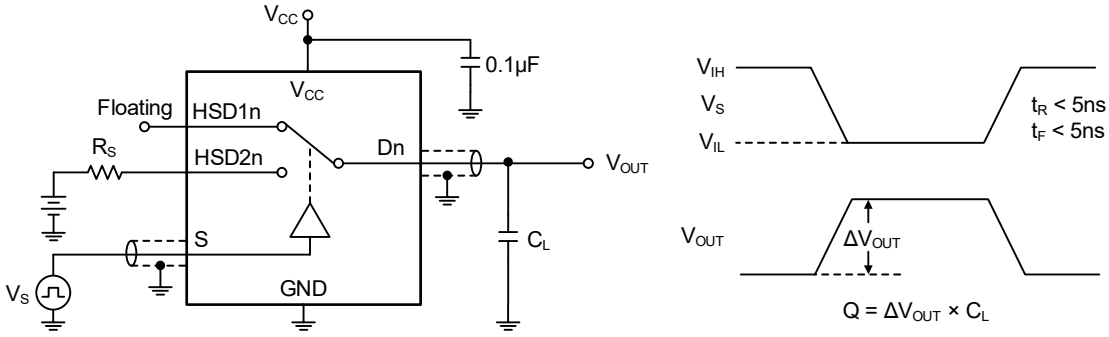


Channel-to-Channel Crosstalk = -20 log (V_{HSDn}/V_{OUT})

Test Circuit 5. Channel-to-Channel Crosstalk



Test Circuit 6. -3dB Bandwidth



Test Circuit 7. Charge Injection (Q)

APPLICATION INFORMATION

Power-Off Protection

When D+ or D- is shorted to V_{BUS}, there is a special protection circuit inside the SGM7226, so that the device will not be damaged within 24 hours. In case of power-down or over-voltage event, the protection circuit can prevent the leakage signal on D+/D- pins to ensure the reliability of the system.

Power-On Protection

The USB 2.0 specification requires USB device to ensure that the device will not be damaged even if V_{BUS} short-circuit occurs during data transmission. Therefore, under over-voltage conditions, the SGM7226 will limit the current flowing back to the V_{CC} track, and the current will not exceed the safe operating range.

Application Circuit

The application circuit is shown in Figure 1. If SGM7226 is powered from V_{BUS}, a 5.1V Zener diode is recommended to be used to suppress the voltage spike in V_{BUS} power line generated by USB interface hot-insertion.

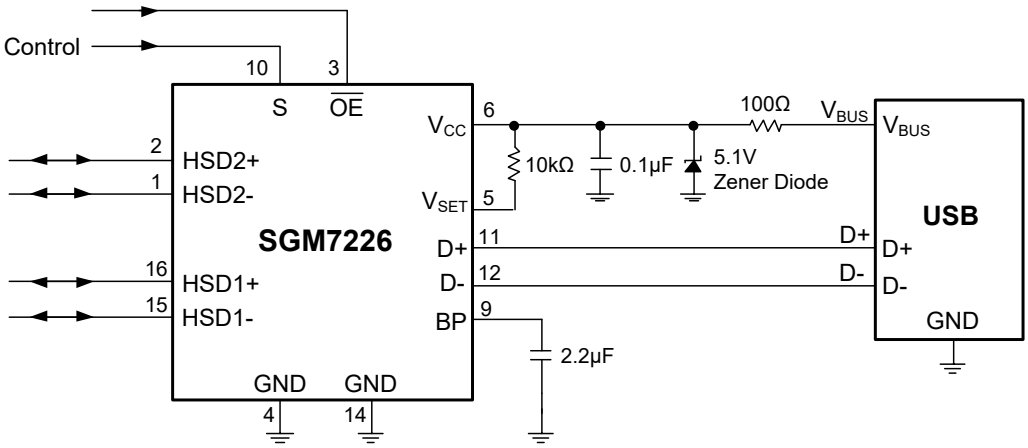


Figure 1. Application Circuit

REVISION HISTORY

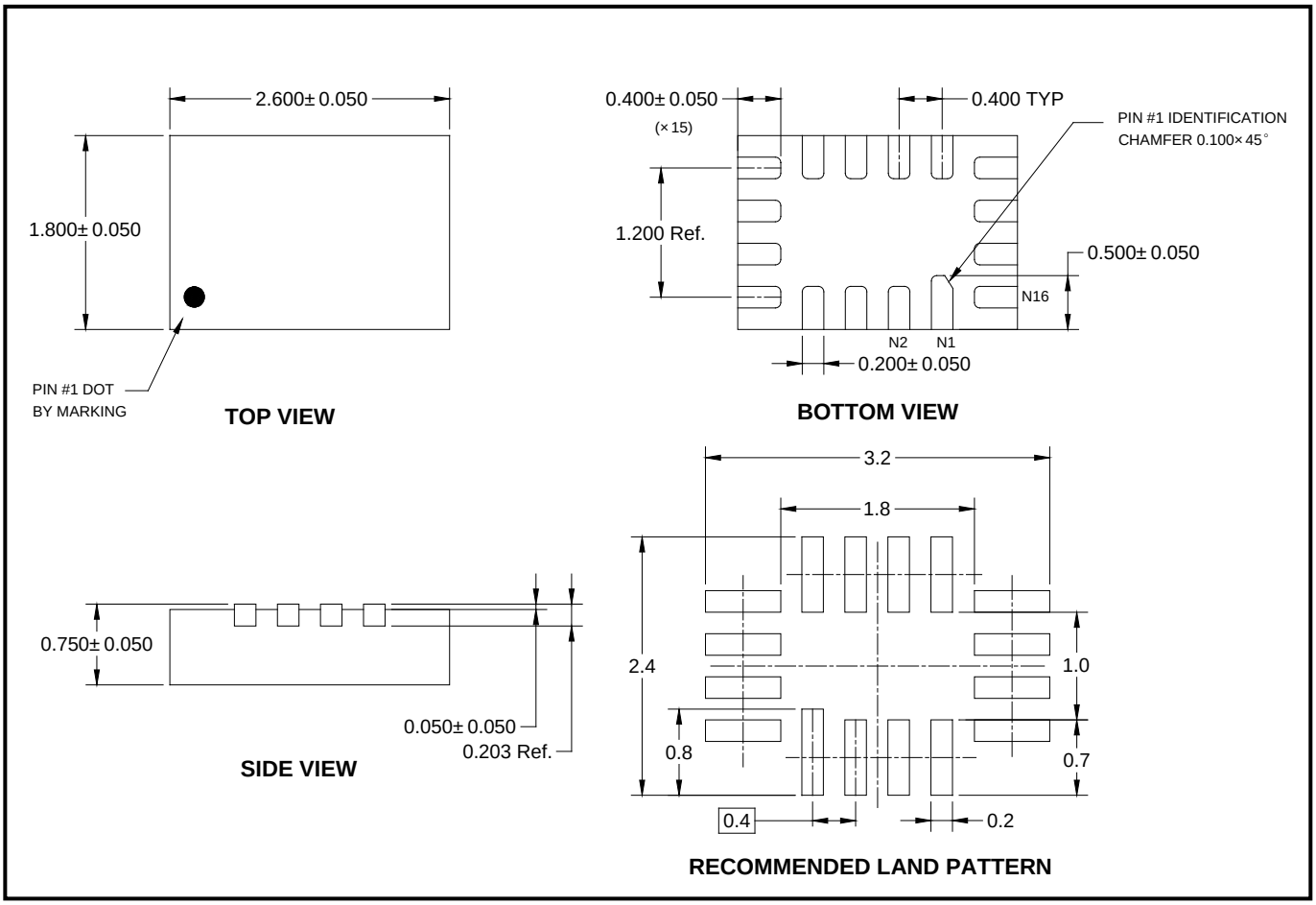
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MAY 2016 – REV.A to REV.A.1	Page
Changed Package Outline Dimensions of TQFN-2.6×1.8-16L to TX00078.001	10
Changed Key Parameter List of Tape and Reel	11

Changes from Original (OCTOBER 2014) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

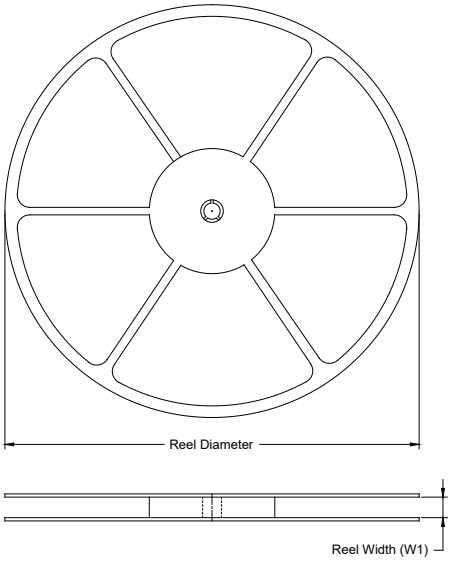
TQFN-2.6×1.8-16L



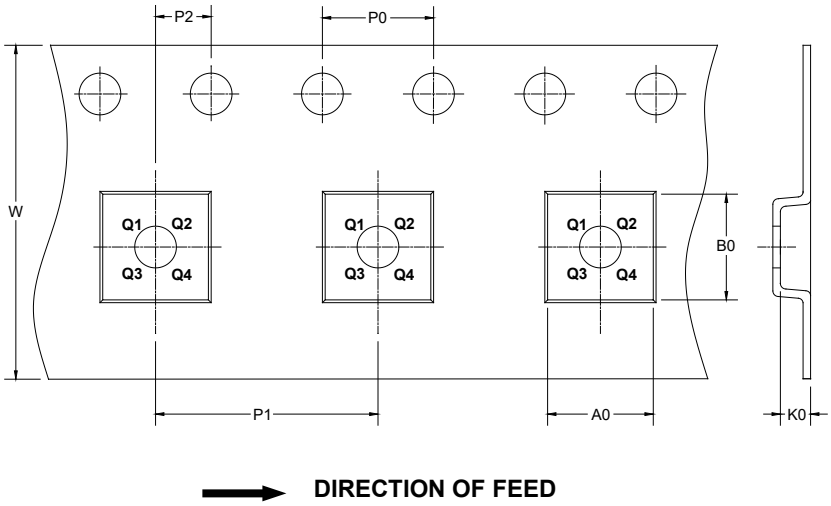
NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

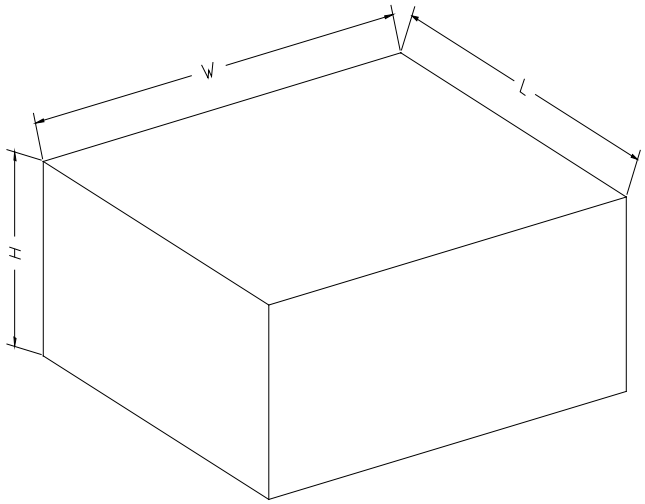
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2.6×1.8-16L	7″	9.0	2.01	2.81	0.93	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002