



### GENERAL DESCRIPTION

The SGM4582 is a high voltage, CMOS analog IC configured as two 4-channel multiplexers. This CMOS device can operate from  $\pm 1.8\text{V}$  to  $\pm 5.5\text{V}$  dual power supplies or from  $+3.6\text{V}$  to  $+11\text{V}$  single supplies. Each switch can handle rail-to-rail analog signals. The off-leakage current is only  $10\text{nA}$  at  $+25^\circ\text{C}$ .

All digital inputs have  $0.8\text{V}$  to  $2.4\text{V}$  logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single  $+5\text{V}$  or dual  $\pm 5\text{V}$  supplies.

SGM4582 is available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3x3-16L packages. It operates over an ambient temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

### FEATURES

- **Guaranteed On-Resistance**
  - $51\Omega$  with  $\pm 5\text{V}$  Supplies
  - $84\Omega$  with Single  $+5\text{V}$  Supply
- **Guaranteed On-Resistance Match Between Channels**
- **Low Off-Leakage Current  $10\text{nA}$  at  $+25^\circ\text{C}$**
- **Low On-Leakage Current  $10\text{nA}$  at  $+25^\circ\text{C}$**
- **$\pm 1.8\text{V}$  to  $\pm 5.5\text{V}$  Dual-Supply Operation**
  - $+3.6\text{V}$  to  $+11\text{V}$  Single-Supply Operation
- **TTL/CMOS-Logic Compatible**
- **Low Distortion:  $0.08\%$  ( $R_L = 600\Omega$ ,  $f = 20\text{Hz}$  to  $20\text{kHz}$ )**
- **High Off-Isolation:  $-66\text{dB}$  ( $R_L = 50\Omega$ ,  $f = 1\text{MHz}$ )**
- **Low Crosstalk:  $-100\text{dB}$  ( $R_L = 50\Omega$ ,  $f = 1\text{MHz}$ )**
- **$-40^\circ\text{C}$  to  $+85^\circ\text{C}$  Operating Temperature Range**
- **Available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3x3-16L Packages**

### APPLICATIONS

Battery-Operated Equipment  
Audio and Video Signal Routing  
Low-Voltage Data-Acquisition Systems  
Communications Circuits  
Automotive

**PACKAGE/ORDERING INFORMATION**

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4582	SOIC-16	-40°C to +85°C	SGM4582YS16G/TR	SGM4582YS16 XXXXX	Tape and Reel, 2500
	SSOP-16	-40°C to +85°C	SGM4582YQS16G/TR	SGM4582 YQS16 XXXXX	Tape and Reel, 3000
	TSSOP-16	-40°C to +85°C	SGM4582YTS16G/TR	SGM4582 YTS16 XXXXX	Tape and Reel, 3000
	TQFN-3x3-16L	-40°C to +85°C	SGM4582YTQ16G/TR	4582TQ XXXXX	Tape and Reel, 3000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to  $V_{EE}$

- $V_{CC}$  ..... -0.3V to 13.2V
- GND ..... -0.3V to 6V
- Voltage into Any Terminal <sup>(1)</sup>  
..... ( $V_{EE} - 0.3V$ ) to ( $V_{CC} + 0.3V$ )
- Continuous Current into Any Terminal..... ±20mA
- Peak Current,  $X_{-}$  (pulsed at 1ms, 10% duty cycle)  
..... ±40mA
- Junction Temperature..... +150°C
- Storage Temperature Range ..... -65°C to +150°C
- Lead Temperature (Soldering, 10s)..... +260°C
- ESD Susceptibility
- HBM..... 3000V
- MM..... 200V

NOTE: 1. Voltages exceeding  $V_{CC}$  or  $V_{EE}$  on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

**RECOMMENDED OPERATING CONDITIONS**

Operating Temperature Range ..... -40°C to +85°C

**OVERSTRESS CAUTION**

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

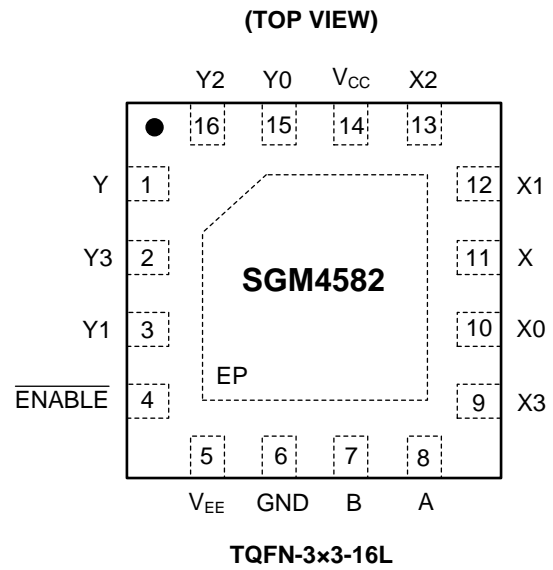
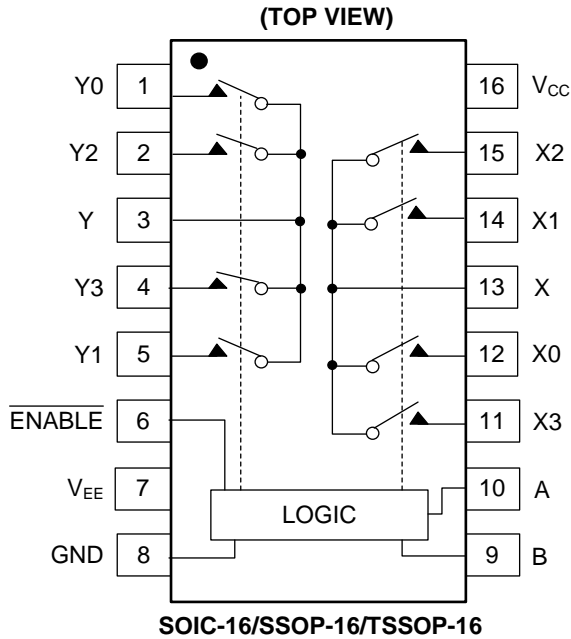
**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

**ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN		NAME	FUNCTION
SOIC-16, SSOP-16, TSSOP-16	TQFN-3x3-16L		
13	11	X	Analog Switch "X" Output.
12, 14, 15, 11	10, 12, 13, 9	X0, X1, X2, X3	Analog Switch "X" Inputs 0-3.
1, 5, 2, 4	15, 3, 16, 2	Y0, Y1, Y2, Y3	Analog Switch "Y" Inputs 0-3.
3	1	Y	Analog Switch "Y" Output.
16	14	V <sub>CC</sub>	Positive Analog and Digital Supply Voltage Input.
10	8	A	Digital Address "A" Input.
9	7	B	Digital Address "B" Input.
8	6	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V <sub>CC</sub> and V <sub>EE</sub> .)
7	5	V <sub>EE</sub>	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation.
6	4	ENABLE	Digital Enable Input. Normally connected to GND.
—	Exposed Pad	EP	Exposed Pad. Connect EP to V <sub>EE</sub> .

NOTE:

Input and output pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.

## FUNCTION TABLE

ENABLE INPUT	SELECT INPUTS		ON SWITCHES
	B	A	
H	X	X	All Switches Open
L	L	L	X-X0, Y-Y0
L	L	H	X-X1, Y-Y1
L	H	L	X-X2, Y-Y2
L	H	H	X-X3, Y-Y3

X = Don't care

## NOTE:

Input and output pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

**ELECTRICAL CHARACTERISTICS (Dual Supplies)**(V<sub>CC</sub> = 4.5V to 5.5V, V<sub>EE</sub> = -4.5V to -5.5V, Full = -40°C to +85°C, typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>X</sub> , V <sub>Y</sub> , V <sub>X</sub> , V <sub>Y</sub>		Full	V <sub>EE</sub>		V <sub>CC</sub>	V
On-Resistance	R <sub>ON</sub>	V <sub>CC</sub> = 4.5V, V <sub>EE</sub> = -4.5V, I <sub>X</sub> , I <sub>Y</sub> = 1mA	+25°C		36	51	Ω
			Full			62	
On-Resistance Match Between Channels	ΔR <sub>ON</sub>	V <sub>CC</sub> = 4.5V, V <sub>EE</sub> = -4.5V, I <sub>X</sub> , I <sub>Y</sub> = 1mA	+25°C		3	11	Ω
			Full			12.7	
On-Resistance Flatness	R <sub>FLAT(ON)</sub>	V <sub>CC</sub> = 4.5V, V <sub>EE</sub> = -4.5V, I <sub>X</sub> , I <sub>Y</sub> = 1mA	+25°C		15	25	Ω
			Full			29	
X <sub>-</sub> , Y <sub>-</sub> Off Leakage Current	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub>	V <sub>CC</sub> = 5.5V, V <sub>EE</sub> = -5.5V, V <sub>X</sub> , V <sub>Y</sub> = ±4.5V, V <sub>X</sub> , V <sub>Y</sub> = ∓4.5V	+25°C		10		nA
X, Y Off Leakage Current	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub>	V <sub>CC</sub> = 5.5V, V <sub>EE</sub> = -5.5V, V <sub>X</sub> , V <sub>Y</sub> = ±4.5V, V <sub>X</sub> , V <sub>Y</sub> = ∓4.5V	+25°C		10		nA
X, Y On Leakage Current	I <sub>X(ON)</sub> , I <sub>Y(ON)</sub>	V <sub>CC</sub> = 5.5V, V <sub>EE</sub> = -5.5V, V <sub>X</sub> , V <sub>Y</sub> = ±4.5V	+25°C		10		nA
<b>DIGITAL I/O</b>							
Logic Input Logic Threshold High	V <sub>AH</sub> , V <sub>BH</sub> , V <sub>ENABLEH</sub>		+25°C	2.4			V
Logic Input Logic Threshold Low	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>ENABLEL</sub>		+25°C			0.8	V
Input-Current High	I <sub>AH</sub> , I <sub>BH</sub> , I <sub>ENABLEH</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub>	+25°C		10		nA
Input-Current Low	I <sub>AL</sub> , I <sub>BL</sub> , I <sub>ENABLEL</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>ENABLE</sub> = 0V	+25°C		10		nA
<b>DYNAMIC CHARACTERISTICS</b>							
Address Transition Time	t <sub>TRANS</sub>	V <sub>X</sub> , V <sub>Y</sub> = ±3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 1	+25°C		70		ns
ENABLE Turn-On Time	t <sub>ON</sub>	V <sub>X</sub> , V <sub>Y</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		60		ns
ENABLE Turn-Off Time	t <sub>OFF</sub>	V <sub>X</sub> , V <sub>Y</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		60		ns
Break-Before-Make Time	t <sub>D</sub>	V <sub>X</sub> , V <sub>Y</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 3	+25°C		20		ns
Charge Injection	Q	R <sub>S</sub> = 0Ω, C = 1nF, V <sub>S</sub> = 0V, Test Circuit 4	+25°C		15		pC
Channel-to-Channel Crosstalk	V <sub>CT</sub>	R <sub>L</sub> = 50Ω, f = 1MHz, Test Circuit 5	+25°C		-100		dB
Off Isolation	V <sub>ISO</sub>	R <sub>L</sub> = 50Ω, f = 1MHz, Test Circuit 5	+25°C		-66		dB
Input Off-Capacitance	C <sub>X(OFF)</sub> , C <sub>Y(OFF)</sub>	f = 1MHz, Test Circuit 6	+25°C		9		pF
Output Off-Capacitance	C <sub>X(OFF)</sub> , C <sub>Y(OFF)</sub>	f = 1MHz, Test Circuit 6	+25°C		20		pF
Output On-Capacitance	C <sub>X(ON)</sub> , C <sub>Y(ON)</sub>	f = 1MHz, Test Circuit 6	+25°C		40		pF
-3dB Bandwidth	BW	R <sub>L</sub> = 50Ω	+25°C		120		MHz
Total Harmonic Distortion	THD	R <sub>L</sub> = 600Ω, 5V <sub>P-P</sub> , f = 20Hz to 20kHz	+25°C		0.08		%
<b>POWER SUPPLY</b>							
Power Supply Range	V <sub>CC</sub> , V <sub>EE</sub>		Full	±1.8		±5.5	V
Power Supply Current	I <sub>CC</sub> , I <sub>EE</sub>	V <sub>CC</sub> = 5.5V, V <sub>EE</sub> = -5.5V, V <sub>A</sub> , V <sub>B</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub> or 0	+25°C		0.01	20	μA

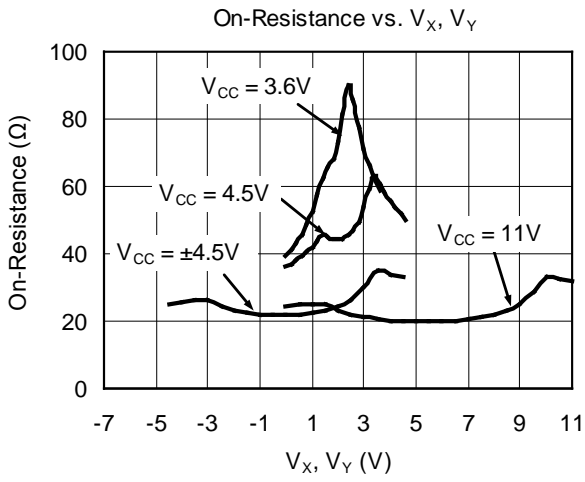
**ELECTRICAL CHARACTERISTICS (Single Supply at +5V)**(V<sub>CC</sub> = 4.5V to 5.5V, V<sub>EE</sub> = 0V, Full = -40°C to +85°C, typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>X</sub> , V <sub>Y</sub>		Full	V <sub>EE</sub>		V <sub>CC</sub>	V
On-Resistance	R <sub>ON</sub>	V <sub>CC</sub> = 4.5V, I <sub>X</sub> , I <sub>Y</sub> = 1mA	+25°C		66	84	Ω
			Full			97	
On-Resistance Match Between Channels	ΔR <sub>ON</sub>	V <sub>CC</sub> = 4.5V, I <sub>X</sub> , I <sub>Y</sub> = 1mA	+25°C		3	11	Ω
			Full			14	
X <sub>-</sub> , Y <sub>-</sub> Off Leakage Current	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub>	V <sub>CC</sub> = 5.5V, V <sub>X-</sub> , V <sub>Y-</sub> = 1V, 4.5V, V <sub>X</sub> , V <sub>Y</sub> = 4.5V, 1V	+25°C		10		nA
X, Y Off Leakage Current	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub>	V <sub>CC</sub> = 5.5V, V <sub>X-</sub> , V <sub>Y-</sub> = 1V, 4.5V, V <sub>X</sub> , V <sub>Y</sub> = 4.5V, 1V	+25°C		10		nA
X, Y On Leakage Current	I <sub>X(ON)</sub> , I <sub>Y(ON)</sub>	V <sub>CC</sub> = 5.5V, V <sub>X</sub> , V <sub>Y</sub> = 4.5V, 1V	+25°C		10		nA
<b>DIGITAL I/O</b>							
Logic Input Logic Threshold High	V <sub>AH</sub> , V <sub>BH</sub> , V <sub>ENABLEH</sub>		+25°C	2.4			V
Logic Input Logic Threshold Low	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>ENABLEL</sub>		+25°C			0.8	V
Input-Current High	I <sub>AH</sub> , I <sub>BH</sub> , I <sub>ENABLEH</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub>	+25°C		10		nA
Input-Current Low	I <sub>AL</sub> , I <sub>BL</sub> , I <sub>ENABLEL</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>ENABLE</sub> = 0V	+25°C		10		nA
<b>DYNAMIC CHARACTERISTICS</b>							
Address Transition Time	t <sub>TRANS</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 3V/0V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 1	+25°C		110		ns
ENABLE Turn-On Time	t <sub>ON</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		85		ns
ENABLE Turn-Off Time	t <sub>OFF</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		65		ns
Break-Before-Make Time	t <sub>D</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 3	+25°C		40		ns
-3dB Bandwidth	BW	R <sub>L</sub> = 50Ω	+25°C		140		MHz
Charge Injection	Q	R <sub>S</sub> = 0Ω, C = 1nF, V <sub>S</sub> = 2.5V, Test Circuit 4	+25°C		2		pC
<b>POWER SUPPLY</b>							
Power Supply Range	V <sub>CC</sub> , V <sub>EE</sub>		Full	3.6		11	V
Power Supply Current	I <sub>CC</sub> , I <sub>EE</sub>	V <sub>CC</sub> = 5.5V, V <sub>A</sub> , V <sub>B</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub> or 0	+25°C		0.01	20	μA

**ELECTRICAL CHARACTERISTICS (Single Supply at +3.6V)**(V<sub>CC</sub> = 3.6V, V<sub>EE</sub> = 0V, Full = -40°C to +85°C, typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

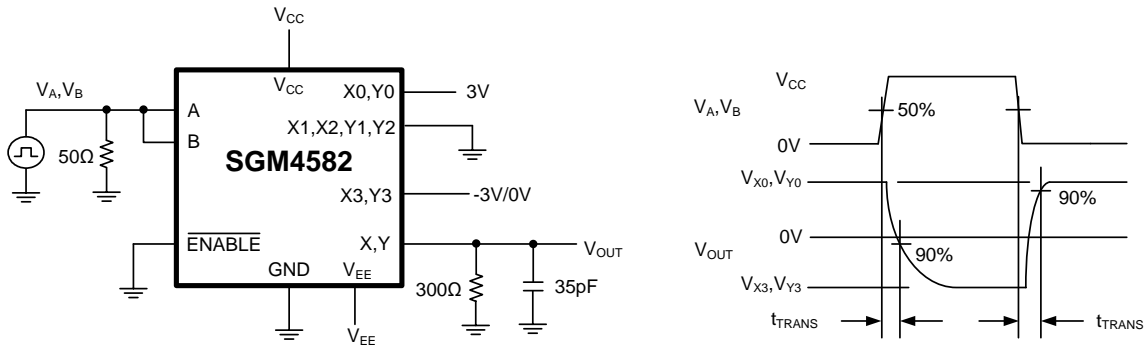
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>X</sub> , V <sub>Y</sub>		Full	V <sub>EE</sub>		V <sub>CC</sub>	V
On-Resistance	R <sub>ON</sub>	I <sub>X</sub> , I <sub>Y</sub> = 1mA	+25°C		100	130	Ω
			Full			140	
X <sub>-</sub> , Y <sub>-</sub> Off Leakage Current	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 1V, 3V, V <sub>X</sub> , V <sub>Y</sub> = 3V, 1V	+25°C		10		nA
X, Y Off Leakage Current	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 1V, 3V, V <sub>X</sub> , V <sub>Y</sub> = 3V, 1V	+25°C		10		nA
X, Y On Leakage Current	I <sub>X(ON)</sub> , I <sub>Y(ON)</sub>	V <sub>X</sub> , V <sub>Y</sub> = 3V, 1V	+25°C		10		nA
<b>DIGITAL I/O</b>							
Logic Input Logic Threshold High	V <sub>AH</sub> , V <sub>BH</sub> , V <sub>ENABLEH</sub>		+25°C	2			V
Logic Input Logic Threshold Low	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>ENABLEL</sub>		+25°C			0.5	V
Input-Current High	I <sub>AH</sub> , I <sub>BH</sub> , I <sub>ENABLEH</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub>	+25°C		10		nA
Input-Current Low	I <sub>AL</sub> , I <sub>BL</sub> , I <sub>ENABLEL</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>ENABLE</sub> = 0V	+25°C		10		nA
<b>DYNAMIC CHARACTERISTICS</b>							
Address Transition Time	t <sub>TRANS</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 3V/0V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 1	+25°C		170		ns
ENABLE Turn-On Time	t <sub>ON</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		140		ns
ENABLE Turn-Off Time	t <sub>OFF</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 2	+25°C		80		ns
Break-Before-Make Time	t <sub>D</sub>	V <sub>X-</sub> , V <sub>Y-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Test Circuit 3	+25°C		70		ns
-3dB Bandwidth	BW	R <sub>L</sub> = 50Ω	+25°C		140		MHz
Charge Injection	Q	R <sub>S</sub> = 0Ω, C = 1nF, V <sub>S</sub> = 2.5V, Test Circuit 4	+25°C		1		pC
<b>POWER SUPPLY</b>							
Power Supply Current	I <sub>CC</sub> , I <sub>EE</sub>	V <sub>CC</sub> = 3.6V, V <sub>A</sub> , V <sub>B</sub> , V <sub>ENABLE</sub> = V <sub>CC</sub> or 0	+25°C		0.01	20	μA

TYPICAL PERFORMANCE CHARACTERISTICS



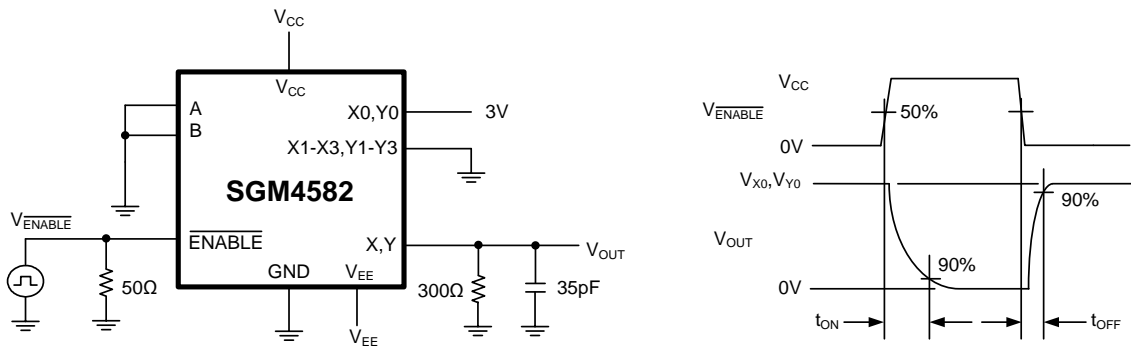


TEST CIRCUITS



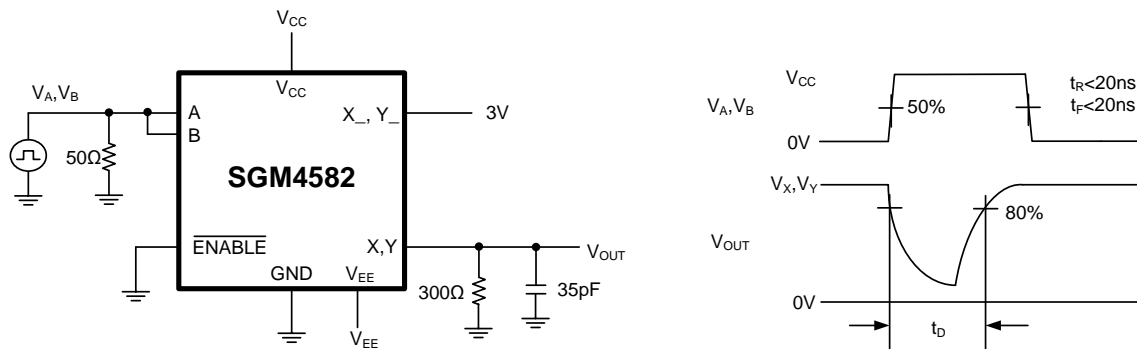
V<sub>EE</sub> = 0V FOR SINGLE-SUPPLY OPERATION.  
TEST EACH SECTION INDIVIDUALLY.

Test Circuit 1. Address Transition Times (t<sub>TRANS</sub>)



V<sub>EE</sub> = 0V FOR SINGLE-SUPPLY OPERATION.  
TEST EACH SECTION INDIVIDUALLY.

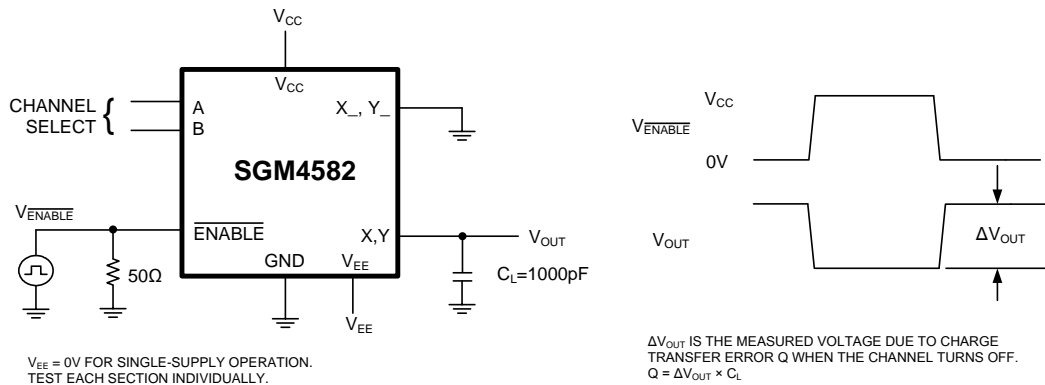
Test Circuit 2. Switching Times (t<sub>ON</sub>, t<sub>OFF</sub>)



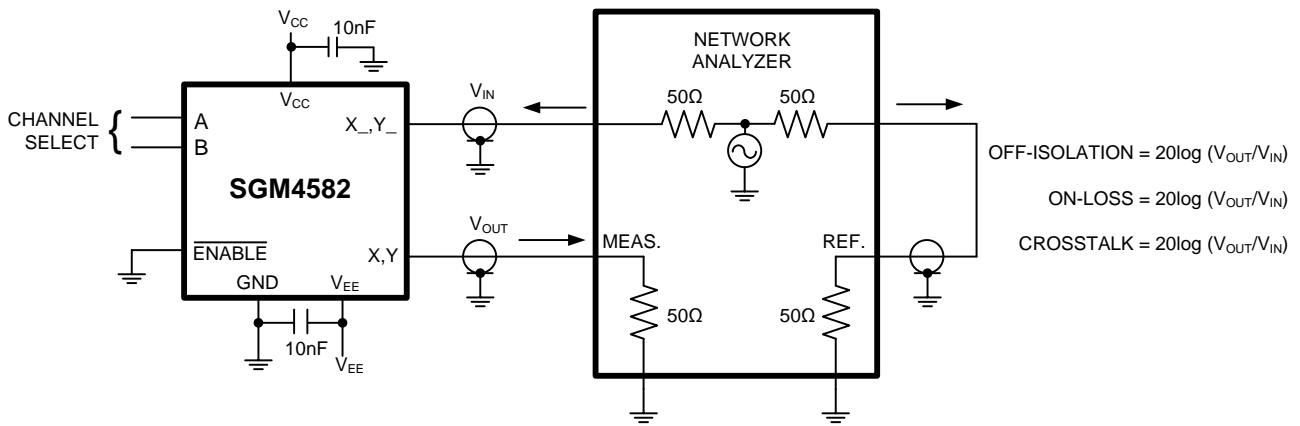
V<sub>EE</sub> = 0V FOR SINGLE-SUPPLY OPERATION.  
TEST EACH SECTION INDIVIDUALLY.

Test Circuit 3. Break-Before-Make Time (t<sub>D</sub>)

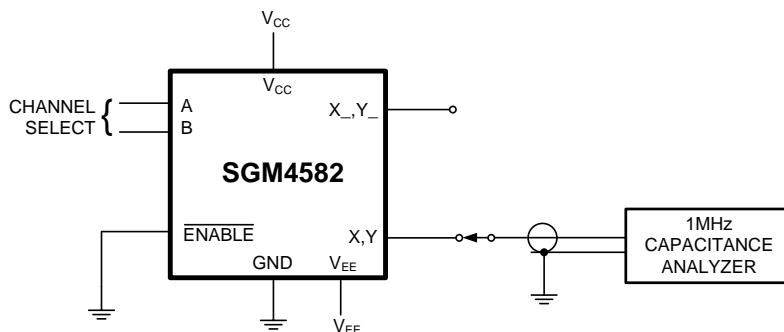
TEST CIRCUITS (continued)



Test Circuit 4. Charge Injection (Q)



Test Circuit 5. Off Isolation, On Loss and Crosstalk



Test Circuit 6. Capacitance

## APPLICATION INFORMATION

### Power-Supply Considerations

#### Overview

The SGM4582 construction is typical of most CMOS analog switch. It has three supply pins:  $V_{CC}$ ,  $V_{EE}$ , and GND.  $V_{CC}$  and  $V_{EE}$  are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog-signal pin and both  $V_{CC}$  and  $V_{EE}$ . If any analog signal exceeds  $V_{CC}$  or  $V_{EE}$ , one of these diodes will conduct. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from  $V_{CC}$  or  $V_{EE}$ .

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either  $V_{CC}$  or  $V_{EE}$  and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the  $V_{CC}$  and  $V_{EE}$  pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND.  $V_{CC}$  and GND power the internal logic and logic-level translators, and set the input logic limits. The logic-level translators convert the logic levels into switched  $V_{CC}$  and  $V_{EE}$  signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies and signals and the analog supplies.  $V_{CC}$  and  $V_{EE}$  have ESD-protection diodes to GND.

#### Bipolar Supplies

This device operates with bipolar supplies between  $\pm 1.8V$  and  $\pm 5.5V$ . The  $V_{CC}$  and  $V_{EE}$  supplies need not be symmetrical, but their sum cannot exceed the  $+13.2V$  absolute maximum rating.

#### Single Supply

This device operates from a single supply between  $+3.6V$  and  $+11V$  when  $V_{EE}$  is connected to GND. All of the bipolar precautions must be observed. At room temperature, it actually "works" with a single supply near or below  $+2.5V$ , although as supply voltage decreases, switch on-resistance and switching times become very high.

### Over-Voltage Protection

Proper power-supply sequencing is recommended for the CMOS device. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence  $V_{CC}$  on first, then  $V_{EE}$ , followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins for over-voltage protection (Figure 1). Adding diodes reduces the analog-signal range to one diode drop below  $V_{CC}$  and one diode drop above  $V_{EE}$ , but does not affect the device's low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between  $V_{CC}$  and  $V_{EE}$  should not exceed  $13.2V$ . These protection diodes are not recommended when using a single supply if signal levels must extend to ground.

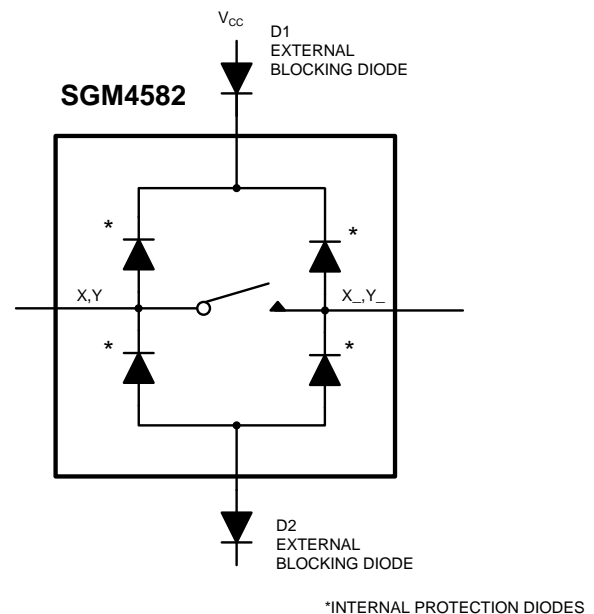
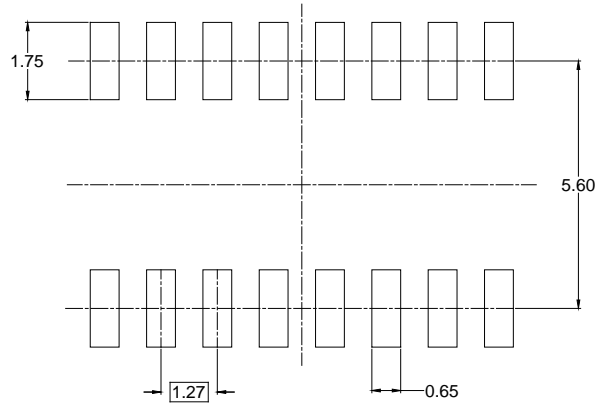
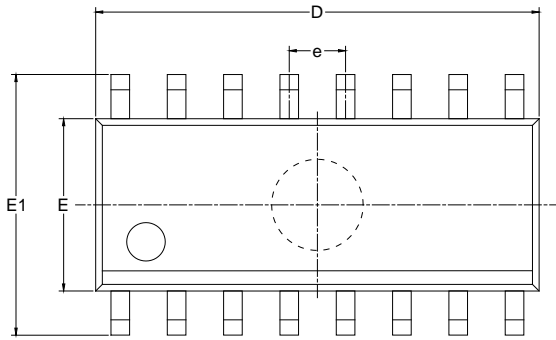


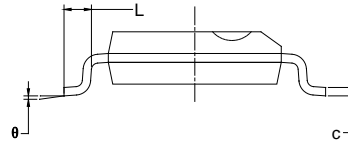
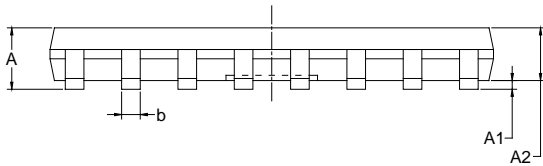
Figure 1. Over-Voltage Protection Using External Blocking Diodes

PACKAGE OUTLINE DIMENSIONS

SOIC-16



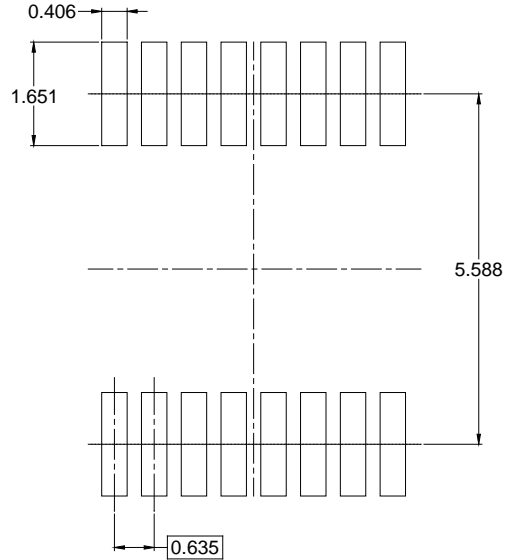
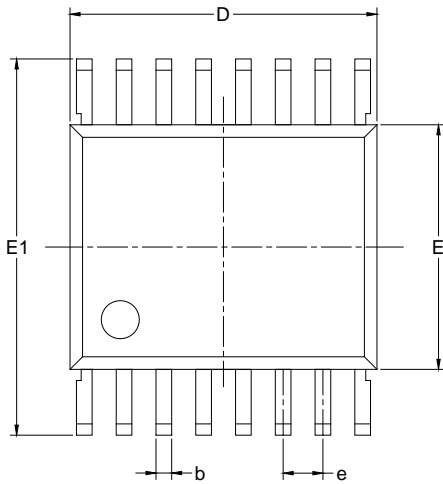
RECOMMENDED LAND PATTERN (Unit: mm)



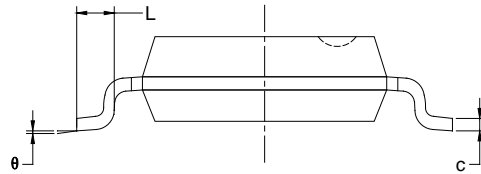
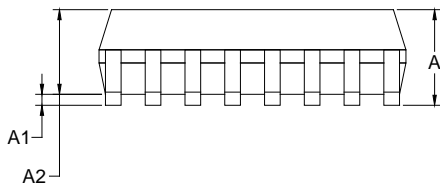
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

SSOP-16



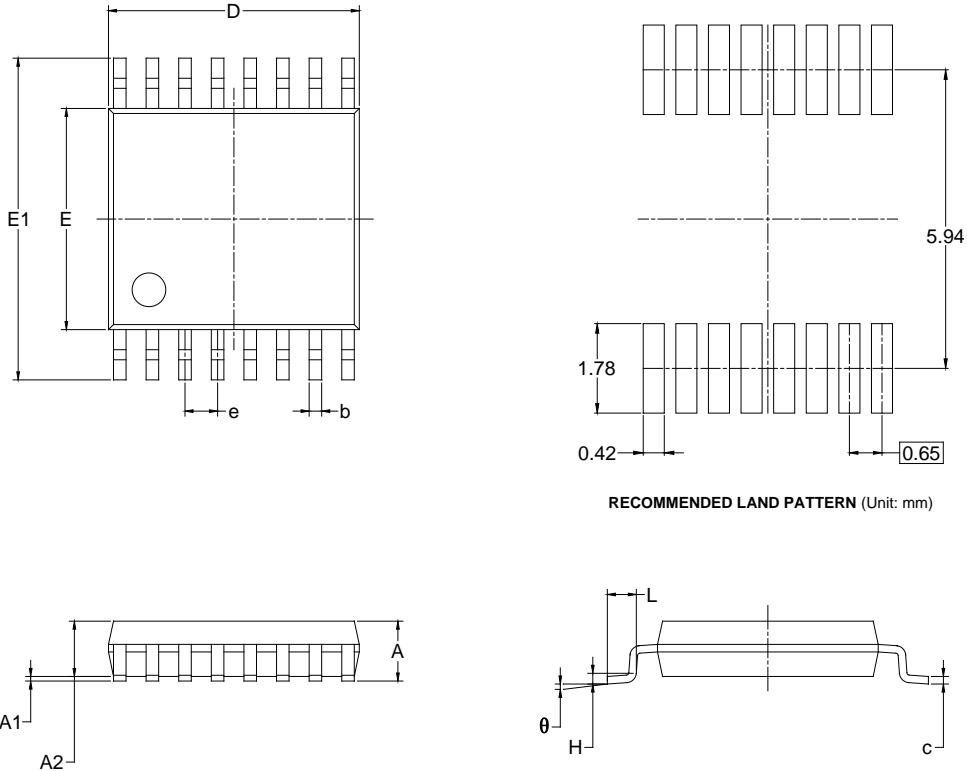
RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635 BSC		0.025 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

TSSOP-16



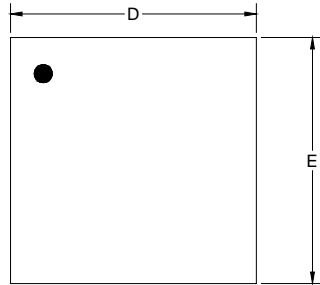
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
$\theta$	1°	7°	1°	7°

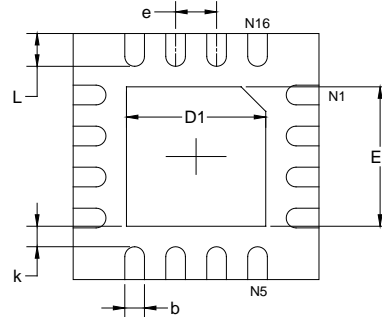
# PACKAGE INFORMATION

## PACKAGE OUTLINE DIMENSIONS

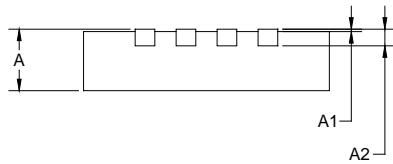
### TQFN-3x3-16L



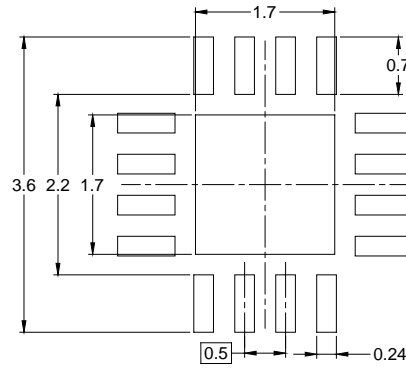
TOP VIEW



BOTTOM VIEW



SIDE VIEW



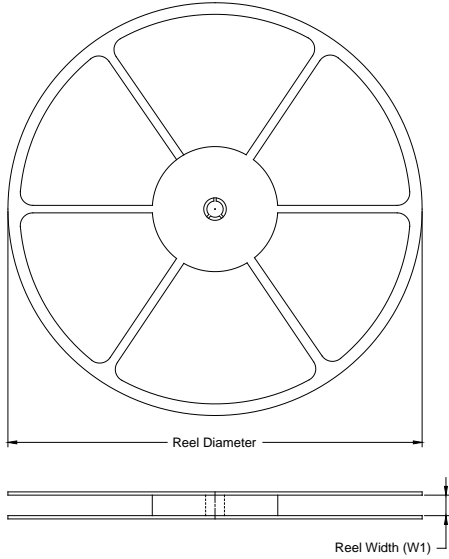
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

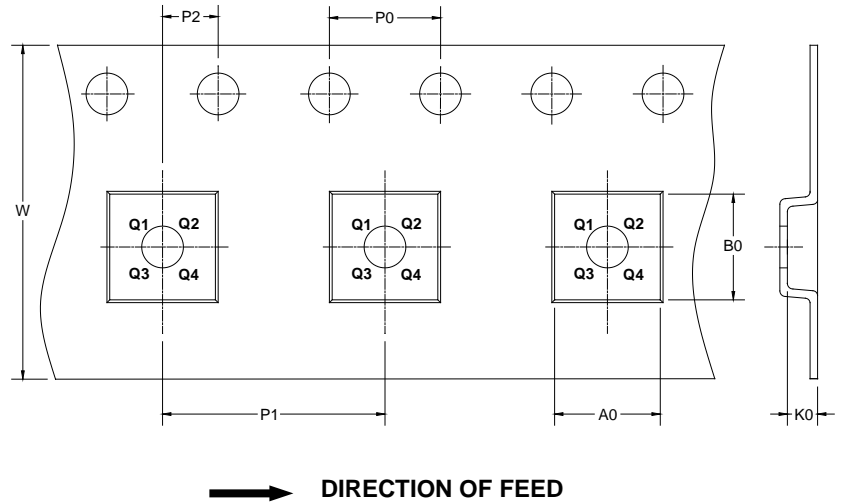
# PACKAGE INFORMATION

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-16	13"	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
SSOP-16	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TSSOP-16	13"	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1
TQFN-3x3-16L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001



# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002

单击下面可查看定价，库存，交付和生命周期等信息

[>>SGMICRO\(圣邦微电子\)](#)