SGM2536
5.5A, 23.7mΩ Electronic Fuse Supporting Bidirectional Current Conduction

GENERAL DESCRIPTION

The SGM2536 family is a compact electronic fuse (eFuse) with a full suite of protection functions. With precision current limit, the device can provide excellent accuracy and be well applied to many system protection applications. The output current limit threshold and the transient over-current blanking timer can be adjusted by the user. Due to the back-to-back FETs packaged inside the chip, the SGM2536 allows bidirectional current to flow through the channel when it is turned on, but prohibits bidirectional current flow when it is turned off, which is very suitable for USB OTG. The V_{OUT} rise time can be programmed by setting an additional capacitor to the SS pin, which can minimize inrush current. Programmable over-voltage protection is used to turn off the device if the IN raises over a threshold value and the downstream circuitry is not damaged by unintended power supply.

The SGM2536 is available in a Green TQFN-2×2-10L package.

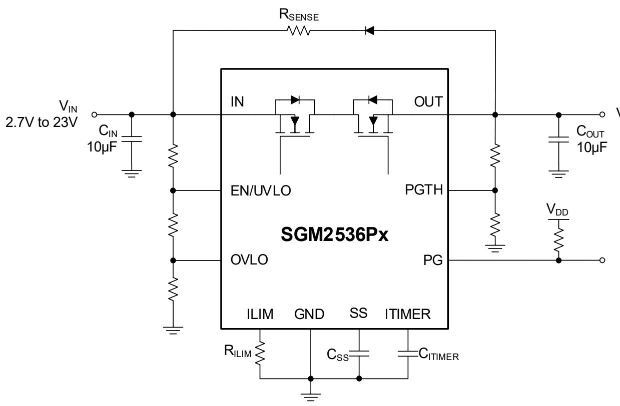
APPLICATIONS

Tablet PC
USB OTG
POS Device
Smartphone
Digital Camera
Wireless Charger

FEATURES

- **Input Voltage: 2.7V to 23V, Surge up to 28V**
- **Back-to-Back FETs Structure**
- **Low On-Resistance: 23.7mΩ (TYP)**
  - **On-State: Bidirectional Current Flow**
  - **Off-State: Reverse Current Blocking**
- **Programmable Output Ramp Time**
- **Programmable Current Limit: 0.5A to 6A (±10% Accuracy for I_{ILIM} > 1A)**
- **Load Current Monitor**
- **Adjustable Transient Blanking Timer (ITIMER) to Allow Peak Current up to 2 × I_{ILIM}**
- **Full Set of Protections**
  - **Programmable Over-Voltage Lockout (OVLO)**
  - **Short-Circuit Protection on OUT Pin**
  - **Under-Voltage Lockout**
  - **Thermal Shutdown**
- **Indication Options**
  - **SGM2536Px: PG and PGTH**
  - **SGM2536Fx: SPGD and nFAULT**
- **Behavior after Fault**
  - **SGM2536xR: Auto-Retry**
  - **SGM2536xL: Latch-Off**

SIMPLIFIED SCHEMATIC

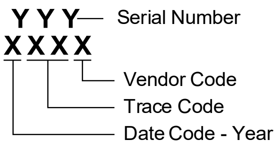


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2536PR	TQFN-2×2-10L	-40℃ to +125℃	SGM2536PRXTSP10G/TR	0EB XXXX	Tape and Reel, 3000
SGM2536PL	TQFN-2×2-10L	-40℃ to +125℃	SGM2536PLXTSP10G/TR	0EC XXXX	Tape and Reel, 3000
SGM2536FR	TQFN-2×2-10L	-40℃ to +125℃	SGM2536FRXTSP10G/TR	0ED XXXX	Tape and Reel, 3000
SGM2536FL	TQFN-2×2-10L	-40℃ to +125℃	SGM2536FLXTSP10G/TR	043 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range, V_{IN} .... -0.3V to 28V
Output Voltage Range, V_{OUT}
T_J = +25℃.. MIN (28V, V_{IN} + 22V)
Output Voltage Pulse (< 1μs), V_{OUT_PLS} .... > -0.8V
Voltage Range
$V_{EN/UVLO}$ .... -0.3V to 6.5V
V_{OVLO} .... -0.3V to 6.5V
V_{PG}, V_{PGTH} (SGM2536Px) .... -0.3V to 6.5V
V_{SPGD}, V_{nFAULT} (SGM2536Fx).......................... -0.3V to 6.5V
V_{SS} .... Internally Limited
V_{ITIMER} .... Internally Limited
V_{ILIM} .... Internally Limited
Maximum Continuous Switch Current, I_{MAX}...........................
.... Internally Limited
Package Thermal Resistance
TQFN-2×2-10L, θ_{JA} .... 69℃/W
Package Thermal Characterization Parameter
TQFN-2×2-10L, ψ_{JT} .... 1.1℃/W
Junction Temperature ....+150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ....+260℃
ESD Susceptibility
HBM (NC Pin 7) 2000V
CDM 1000V
MM 400V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} .... 2.7V to 23V
Output Voltage Range, V_{OUT} .... MIN (23V, V_{IN} + 20V)
Voltage Range
$V_{EN/UVLO}$ .... 5V [(1)]
V_{OVLO} .... 0.5V to 1.5V
V_{PG}, V_{PGTH} (SGM2536Px) 5V
V_{SPGD}, V_{nFAULT} (SGM2536Fx) 5V
ITIMER Capacitor Voltage Rating, V_{ITIMER} .... > 4V
SS Capacitor Voltage Rating, V_{SS} .... > V_{IN} + 5V
Resistance, R_{ILIM} .... 549Ω to 6650Ω
Maximum Continuous Switch Current, I_{MAX} 5.5A
Operating Junction Temperature Range...... -40℃ to +125℃

NOTE: 1. If the supply voltage is less than 5V, EN/UVLO pin can be pulled up to the IN directly. If the supply voltage is larger than 5V, a 350kΩ (MIN) pull-up resistor is recommended for the EN/UVLO pin.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

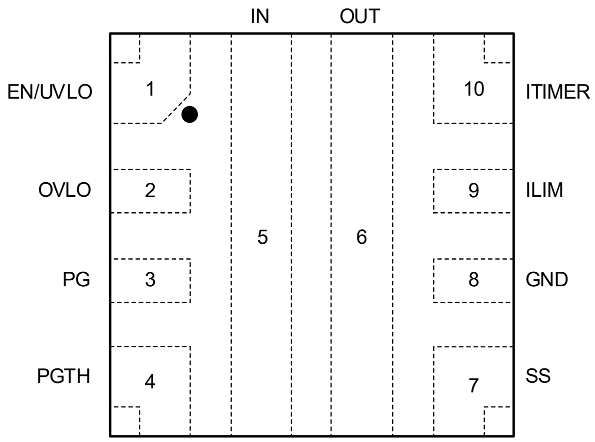
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without notice.

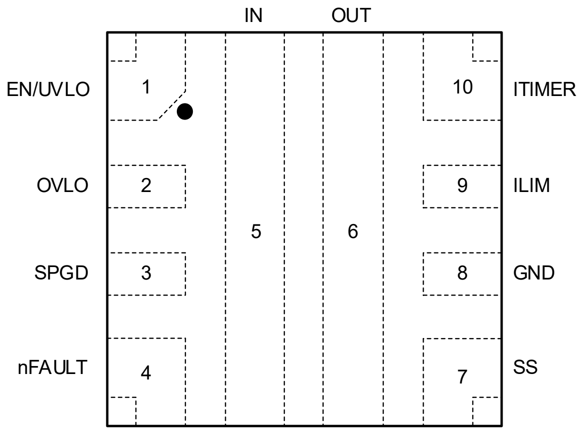
PIN CONFIGURATIONS

SGM2536Px (TOP VIEW)



TQFN-2×2-10L

SGM2536Fx (TOP VIEW)



TQFN-2×2-10L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN/UVLO	Analog Input	Enable and Under-Voltage Lockout Input. Asserting EN/UVLO pin high enables the device. As a UVLO pin, the UVLO threshold is programmed by an external resistor divider. This pin cannot be left floating.
2	OVLO	Analog Input	Over-Voltage Lockout Pin. The over-voltage lockout threshold is programmed by the resistor divider from the power supply to the OVLO terminal to GND. The device is enabled when this pin is tied to low level. This pin cannot be left floating.
3	PG	Digital Output	Power Good Indication (SGM2536Px). This is an open-drain pin, when the internal channels of the chip are all turned on and the PGTH signal value is higher than the set value, the pin is set to high level.
	SPGD		Supply Good Indication (SGM2536Fx). This is an open-drain pin, when the input voltage is within the valid range and the surge has finished, this pin goes high.
4	PGTH	Analog Input	Power Good Threshold (SGM2536Px).
	nFAULT	Digital Output	Fault Event Indicator (SGM2536Fx). This pin is an open-drain output, and when a fault occurs, it will be low.
5	IN	Power	Input Supply Voltage.
6	OUT	Power	Output of the Device.
7	SS	Analog Output	Soft-Start Pin. The capacitor between SS and GND pins will set the slew rate according to the application requirements. When this pin is left floating, the device will start up at the fastest rate.
8	GND	Ground	GND.
9	ILIM	Analog Output	Programming Current Limit Pin. A resistor between this pin and GND sets the overload and short-circuit current limit levels. Do not float this pin.
10	ITIMER	Analog Output	Place a capacitor between this pin and GND can set the over-current blanking time, at this stage, the output current value can temporarily exceed the internally set current limit value (but not exceed the fast-trip threshold). After this time, the device will take action if it is still in over-current state. Leaving this pin open will provide the fastest response to an over-current event.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, $V_{EN/UVLO}$ = 2V, R_{ILIM} = 549Ω, V_{OVLO} = 0V, OUT, SS, ITIMER, PGTH/nFAULT, PG/SPGD pins are open, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply (IN)						
Under-Voltage Protection Threshold	V_{UVP_R}	Rising	2.47	2.54	2.61	V
	V_{UVP_F}	Falling	2.24	2.31	2.37	
Supply Quiescent Current	I_{Q_ON}			132	270	μA
Supply Disabled State Current	I_{Q_OFF}	$V_{SD\_F} < V_{EN/UVLO} < V_{UVLO\_F}$		48	100	μA
Supply Shutdown Current	I_{SD}	$V_{EN/UVLO} < V_{SD\_F}$		3.2	10	μA
On-Resistance (IN - OUT)						
On-Resistance	R_{ON}	V_{IN} = 12V, I_{OUT} = 3A		23.7		mΩ
		2.7V ≤ V_{IN} ≤ 23V, I_{OUT} = 3A			40	
Enable/Under-Voltage Lockout (EN/UVLO)						
EN/UVLO Threshold	V_{UVLO_R}	Rising Threshold	1.184	1.20	1.217	V
	V_{UVLO_F}	Falling Threshold	1.076	1.09	1.108	
EN/UVLO Falling Threshold for Lowest Shutdown Current	V_{SD_F}		0.35	0.71		V
EN/UVLO Leakage Current	I_{ENLKG}		-0.13		0.13	μA
Over-Voltage Lockout (OVLO)						
OVLO Rising Threshold	V_{OVLO_R}		1.184	1.20	1.217	V
OVLO Falling Threshold	V_{OVLO_F}		1.076	1.09	1.108	V
OVLO Pin Leakage Current	I_{OVLKG}	V_{OVLO} = 0.5V	-0.1		0.1	μA
		V_{OVLO} = 1V	-0.1		0.1	
		V_{OVLO} = 1.5V	-0.1		0.1	
Over-Current Protection (OUT)						
Over-Current Threshold	I_{ILIM}	R_{ILIM} = 6.65kΩ, T_J = +25℃	0.475	0.516	0.557	A
		R_{ILIM} = 6.65kΩ, T_J = -40℃ to +125℃	0.467		0.581	
		R_{ILIM} = 3.32kΩ, T_J = +25℃	0.969	1.014	1.061	
		R_{ILIM} = 3.32kΩ, T_J = -40℃ to +125℃	0.954		1.095	
		R_{ILIM} = 1.65kΩ, T_J = +25℃	1.947	2.020	2.094	
		R_{ILIM} = 1.65kΩ, T_J = -40℃ to +125℃	1.924		2.131	
		R_{ILIM} = 750Ω, T_J = +25℃	4.226	4.379	4.534	
		R_{ILIM} = 750Ω, T_J = -40℃ to +125℃	4.187		4.581	
		R_{ILIM} = 549Ω, T_J = +25℃	5.730	5.946	6.163	
		R_{ILIM} = 549Ω, T_J = -40℃ to +125℃	5.674		6.231	
Circuit Breaker Threshold	I_{nFAULT}	ILIM pin open		0.1		A
		ILIM pin shorted to GND		1.1	1.5	
Over-Current Fault Timer (ITIMER)						
ITIMER Internal Pull-Up Voltage	V_{INT}		2.40	2.59	2.80	V
ITIMER Internal Pull-Up Resistance	R_{ITIMER}			17		kΩ
ITIMER Internal Discharge Current	I_{ITIMER}	$I_{OUT} > I_{ILIM}$	1.1	1.8	2.5	μA
ITIMER Discharge Differential Voltage Threshold	ΔV_{ITIMER}		1.40	1.49	1.55	V

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 12V, $V_{EN/UVLO}$ = 2V, R_{ILIM} = 549Ω, V_{OVLO} = 0V, OUT, SS, ITIMER, PGTH/nFAULT, PG/SPGD pins are open, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Load Current Monitor (ILIM)						
Analog Load Current Monitor Gain (I_{MON}: I_{OUT})	G_{IMON}	I_{OUT} = 0.5A, T_J = +25℃	165	176	188	μA/A
		I_{OUT} = 0.5A, T_J = -40℃ to +125℃	154		195	
		I_{OUT} = 0.75A, T_J = +25℃	169	179	187	
		I_{OUT} = 0.75A, T_J = -40℃ to +125℃	162		191	
		I_{OUT} = 1A, T_J = +25℃	172	180	187	
		I_{OUT} = 1A, T_J = -40℃ to +125℃	167		190	
		I_{OUT} = 2A, T_J = +25℃	175	182	187	
		I_{OUT} = 2A, T_J = -40℃ to +125℃	173		191	
		I_{OUT} = 4A, T_J = +25℃	176	183	189	
		I_{OUT} = 4A, T_J = -40℃ to +125℃	175		192	
		I_{OUT} = 5.5A, T_J = +25℃	176	183	190	
		I_{OUT} = 5.5A, T_J = -40℃ to +125℃	175		192	
Power Good (PG) Indication: SGM2536Px or Supply Good (SPGD) Indication: SGM2536Fx						
PG/SPGD Voltage while De-asserted	V_{PGD}	V_{IN} < V_{UVP_F}, V_{EN} > V_{UVLO_R}, weak pull-up (I_{PG} = 26μA)		0.52	1	V
		V_{IN} < V_{UVP_F}, V_{EN} > V_{UVLO_R}, strong pull-up (I_{PG} = 242μA)		0.65	1	
		V_{IN} > V_{UVP_R}, V_{EN} < V_{SD_F}, I_{PG} = 10mA		0.16	0.27	
PG/SPGD Leakage Current, PG/SPGD Asserted	I_{PGLKG}			0.9	3	μA
Power Good Threshold (PGTH): SGM2536Px						
PGTH Threshold	V_{PGTH_R}	Rising	1.183	1.20	1.218	V
	V_{PGTH_F}	Falling	1.076	1.09	1.108	V
PGTH Leakage Current	$I_{PGTHLKG}$		-0.1		0.3	μA
Fault (nFAULT) Indication: SGM2536Fx						
nFAULT Leakage Current	$I_{nFAULTLKG}$		-1		1	μA
nFAULT Pull-Down Resistance	R_{nFAULT}			13	20	Ω
Over-Temperature Protection (OTP)						
Thermal Shutdown Rising Threshold	T_{SD}			155		℃
Thermal Shutdown Hysteresis	T_{HYS}			30		℃
SS						
SS Pin Charging Current	I_{SS}		1.00	2.01	3.00	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Voltage Lockout Response Time	t_{OVLO}	V_{OVLO} > V_{OV_R} to V_{OUT}↓		2.5		μs
Current Limit Response Time	t_{LIM}	I_{ILIM} = 2A, I_{OUT} > 1.2 × I_{ILIM} and I_{ITIMER} expired to I_{OUT} settling to I_{ILIM}		250		μs
Scalable Fast-Trip Response Time	t_{SC}	I_{OUT} > 3 × I_{ILIM} to I_{OUT}↓		500		ns
Auto-Retry Interval after Fault (SGM2536xR)	t_{RST}			110		ms
PG Assertion De-Glitch	t_{PGA}			15		μs
PG De-Assertion De-Glitch	t_{PGD}			15		μs

SWITCHING CHARACTERISTICS

(R_L = 100Ω, C_{OUT} = 10μF, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	V_{IN}	C_{SS} = Open	C_{SS} = 1800pF	C_{SS} = 3300pF	UNITS
Output Rising Slew Rate	SR_{ON}	V_{IN} = 2.7V	7.4	0.86	0.47	V/ms
		V_{IN} = 12V	22	0.96	0.48	
		V_{IN} = 23V	35	0.97	0.46	
Turn-On Time	t_{ON}	V_{IN} = 2.7V	0.58	3.9	6.6	ms
		V_{IN} = 12V	0.79	12.4	24.3	
		V_{IN} = 23V	0.87	22.6	46.2	
Turn-On Delay	t_{D_ON}	V_{IN} = 2.7V	0.29	1.4	2	ms
		V_{IN} = 12V	0.35	2.4	4.4	
		V_{IN} = 23V	0.35	3.6	6.2	
Rise Time	t_R	V_{IN} = 2.7V	0.29	2.5	4.6	ms
		V_{IN} = 12V	0.44	10	19.9	
		V_{IN} = 23V	0.52	19	40	
Turn-Off Delay	t_{D_OFF}	V_{IN} = 2.7V	48	48	50	μs
		V_{IN} = 12V	15	15	15.4	
		V_{IN} = 23V	9	8	10	

In the entire normal voltage range, the output voltage rise rate is set by the internal circuit and remains unchanged to ensure that the load state does not affect the start-up sequence. Adding capacitance between the SS pin and GND can change the OUT rising slope. Increasing capacitor C_{SS} will reduce the rate of rise (SR) of the output voltage. For a detailed description, please refer to the relevant sections on inrush current suppression (SS) and slew rate. However, the time that V_{OUT} falls when the device is turned off is determined by the RC time constants of the load resistor (R_L) and load capacitor (C_{OUT}). The control of the switch only affects the power-on sequence when the chip is turned on.

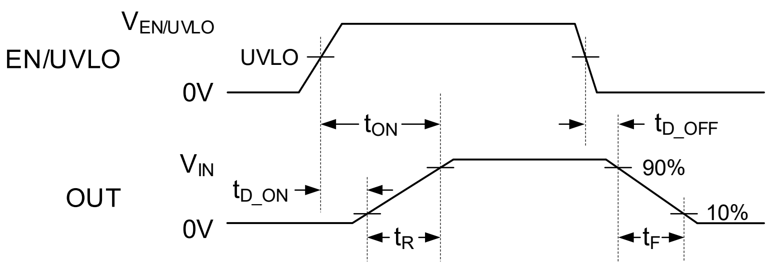
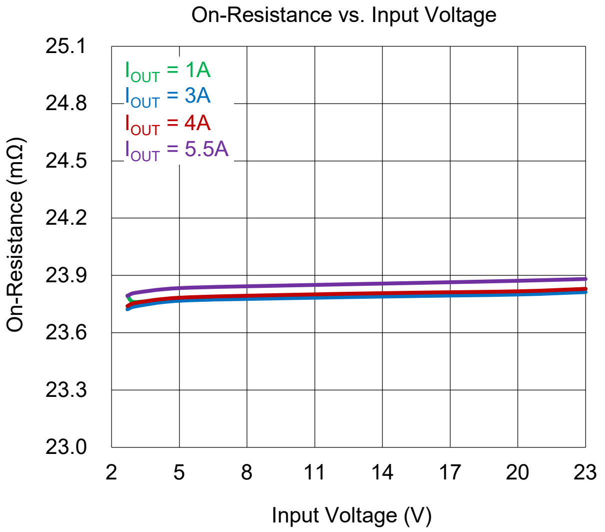
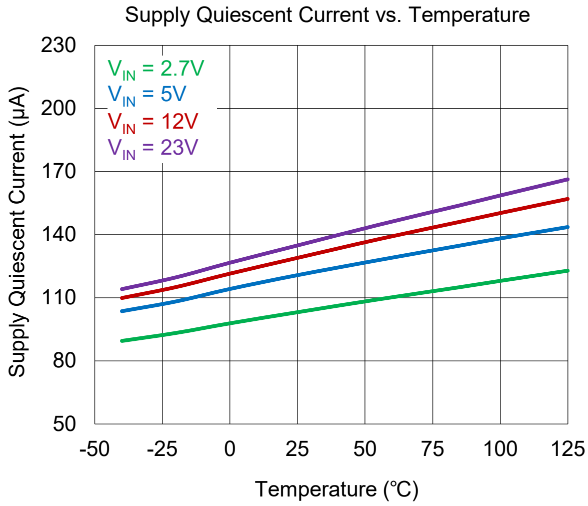
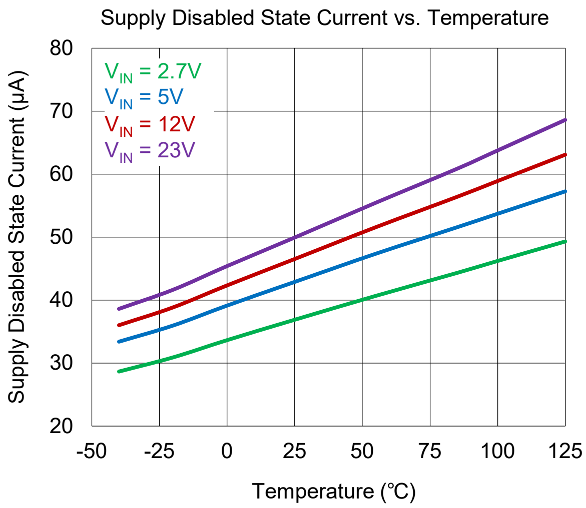


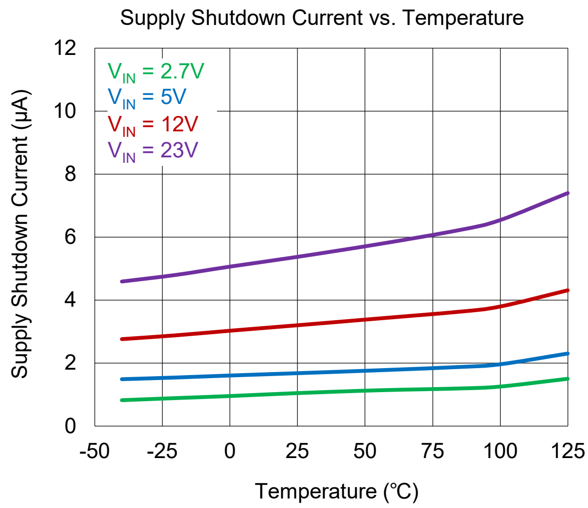
Figure 1. SGM2536 Switching Times

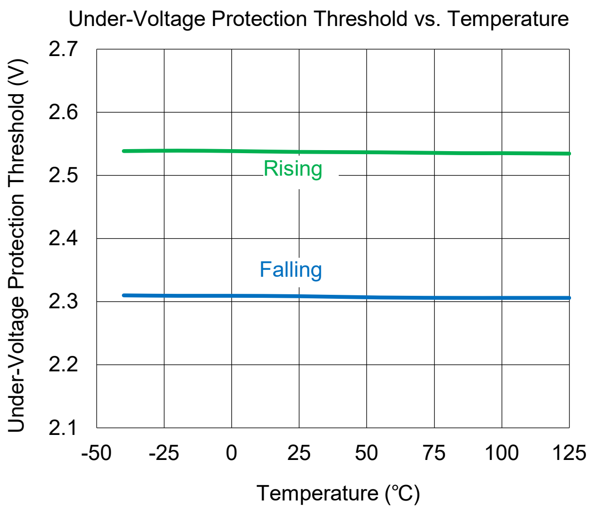
TYPICAL PERFORMANCE CHARACTERISTICS

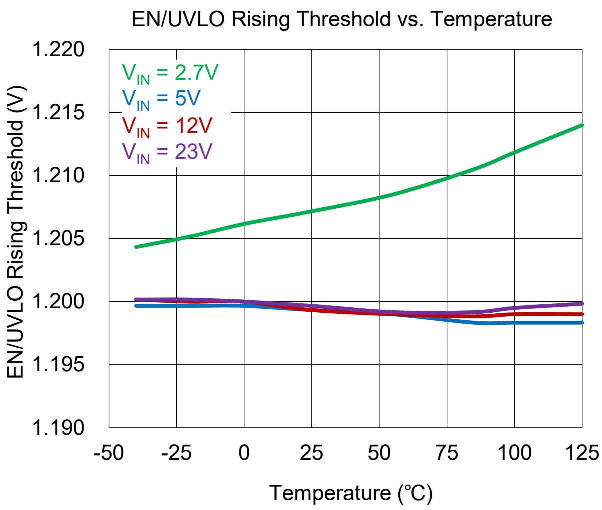






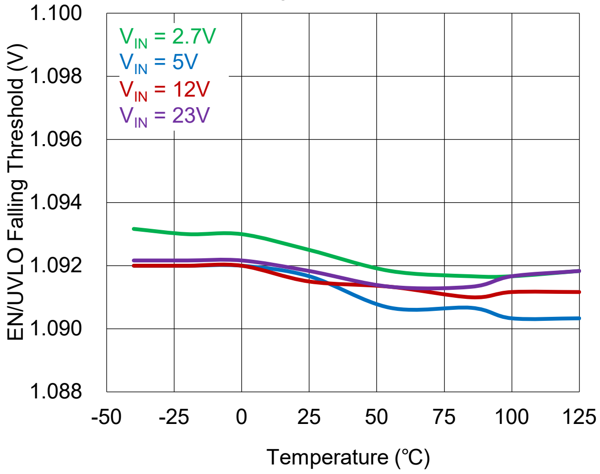




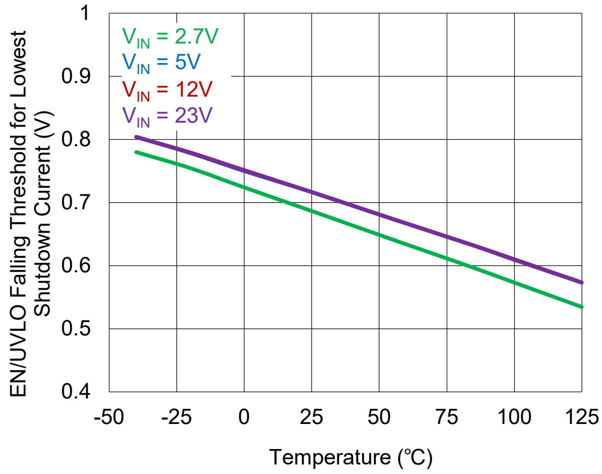


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

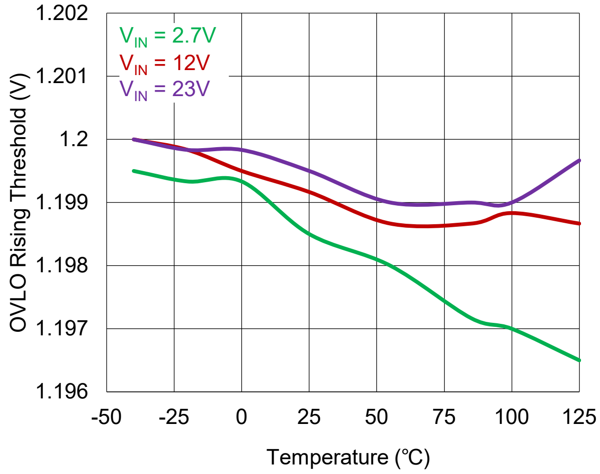
EN/UVLO Falling Threshold vs. Temperature



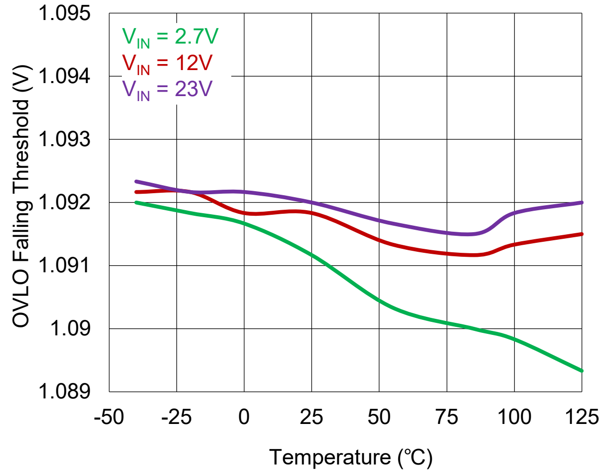
EN/UVLO Falling Threshold for Lowest Shutdown Current vs. Temperature



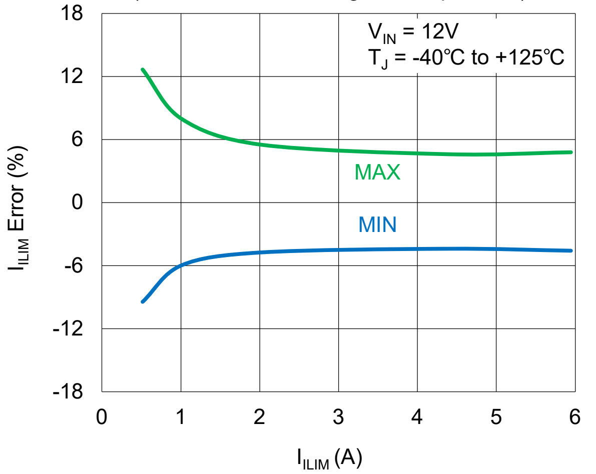
OVLO Rising Threshold vs. Temperature



OVLO Falling Threshold vs. Temperature



Over-Current Threshold Accuracy
(Across Process, Voltage & Temperature)



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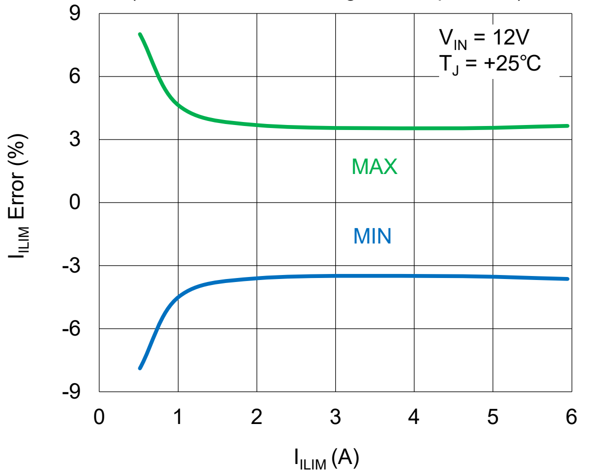
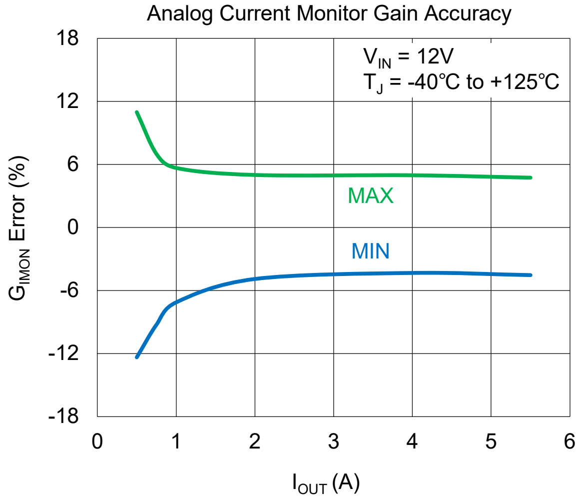
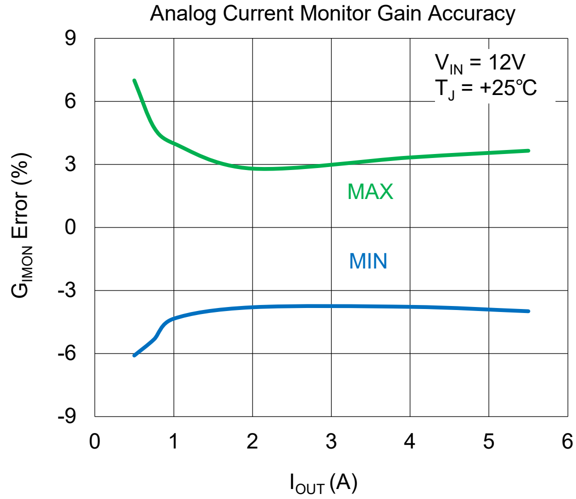


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

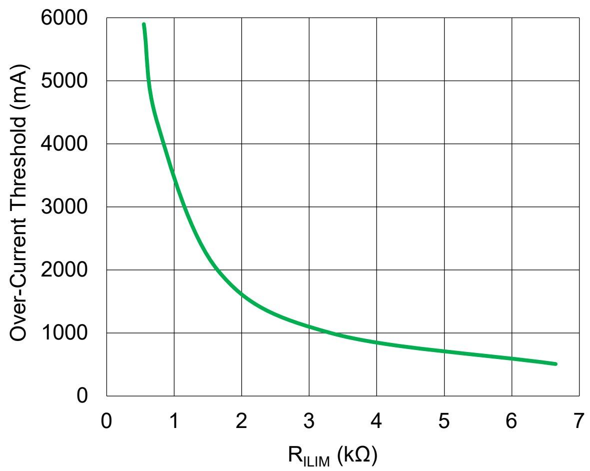
Analog Current Monitor Gain Accuracy



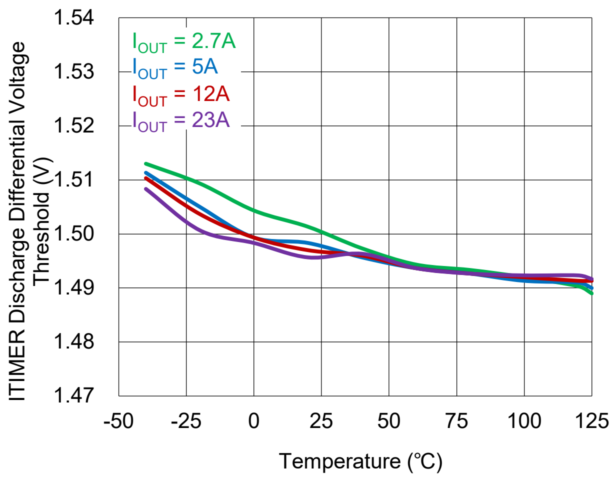
Analog Current Monitor Gain Accuracy



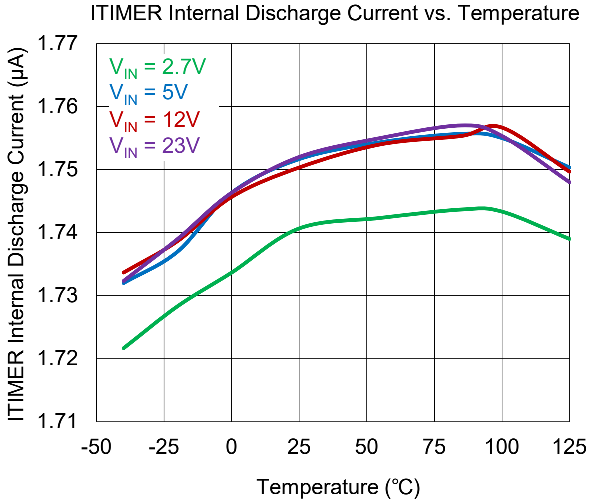
Over-Current Threshold vs. R_{ILIM}



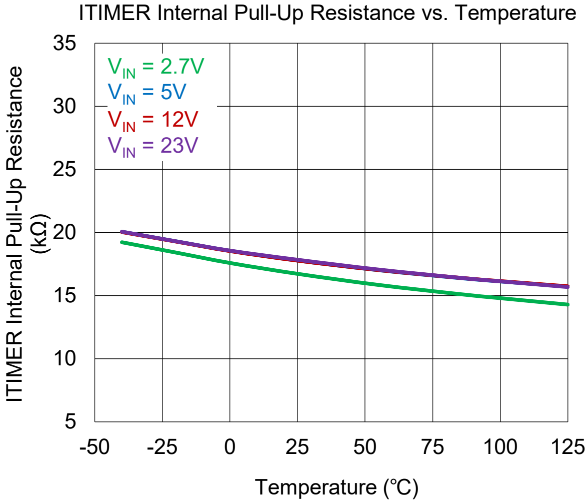
ITIMER Discharge Differential Voltage Threshold vs. Temperature



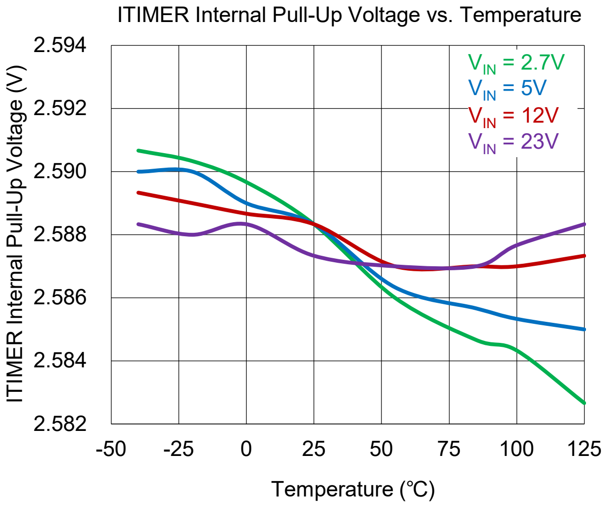
ITIMER Internal Discharge Current vs. Temperature

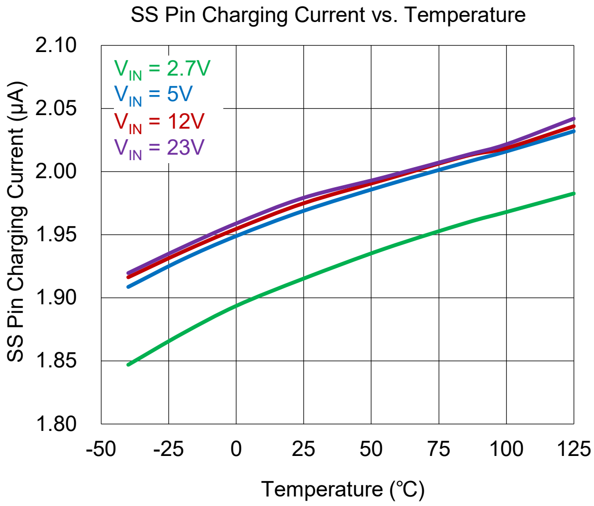


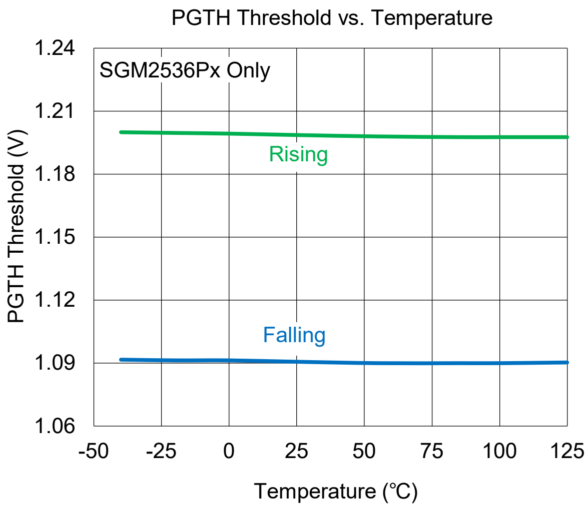
ITIMER Internal Pull-Up Resistance vs. Temperature

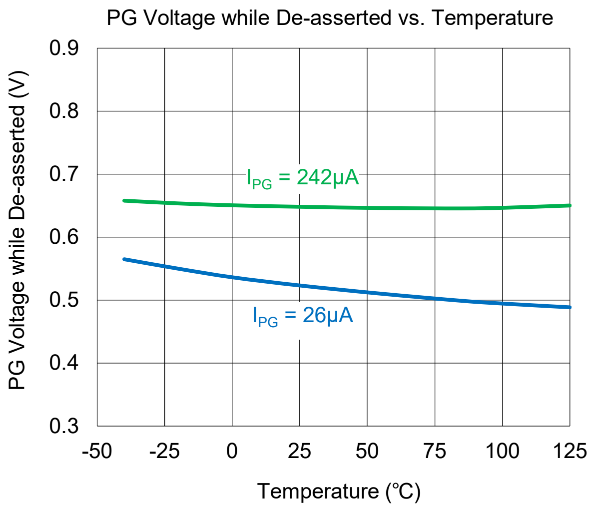


TYPICAL PERFORMANCE CHARACTERISTICS (continued)



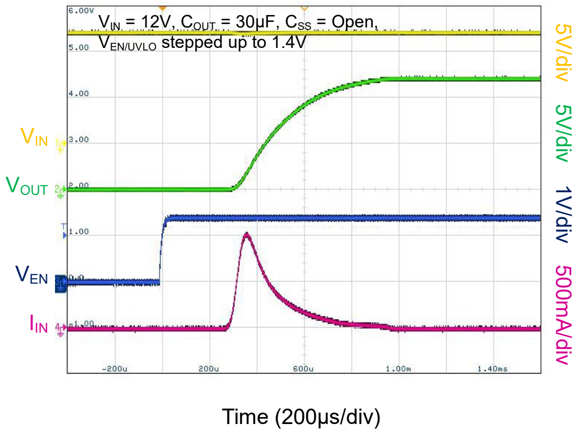




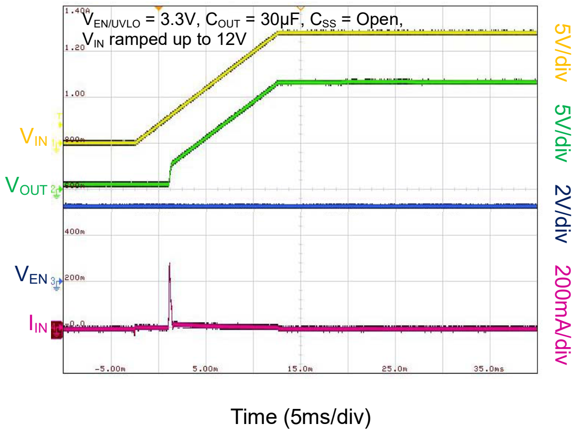


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

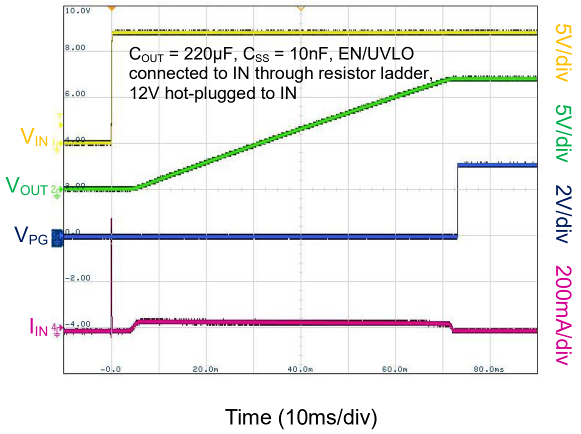
Start-up with Enable



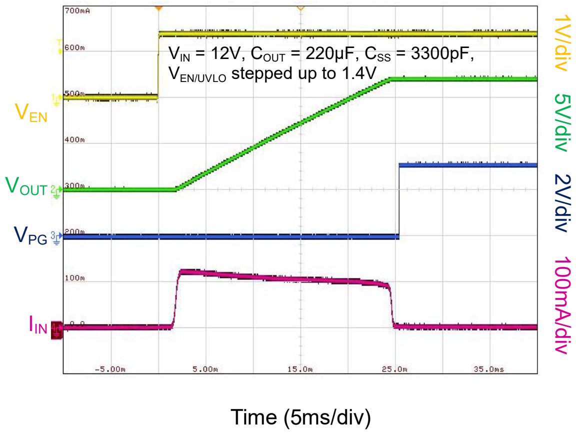
Start-up with IN Supply



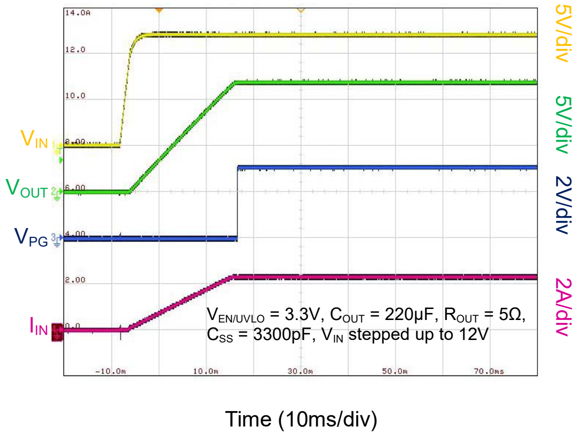
IN Hot-Plug



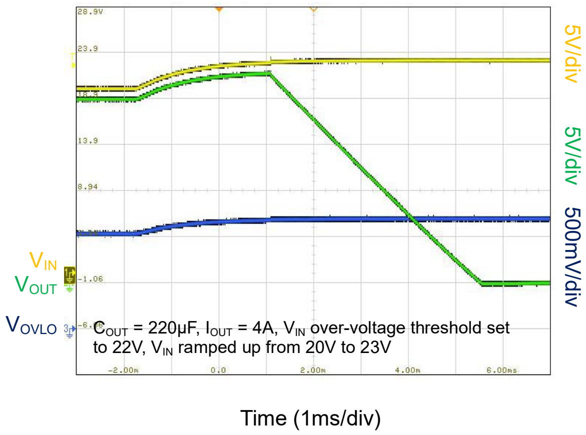
Inrush Current with Capacitive Load



Inrush Current with Resistive and Capacitive Load

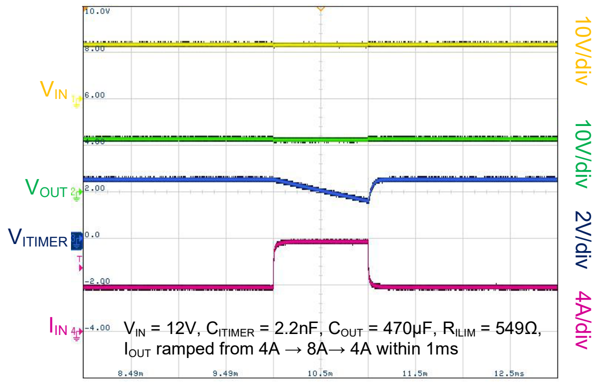


Over-Voltage Lockout Response



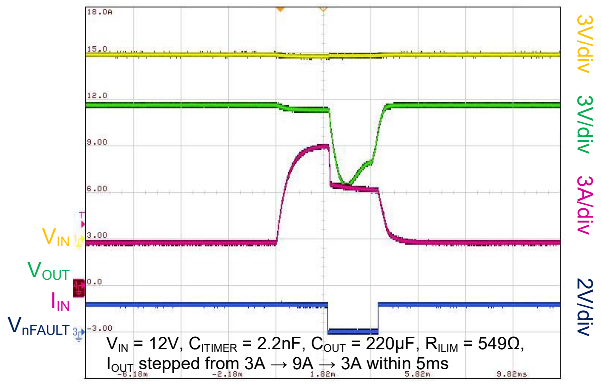
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Transient Over-Current Blanking Timer Response



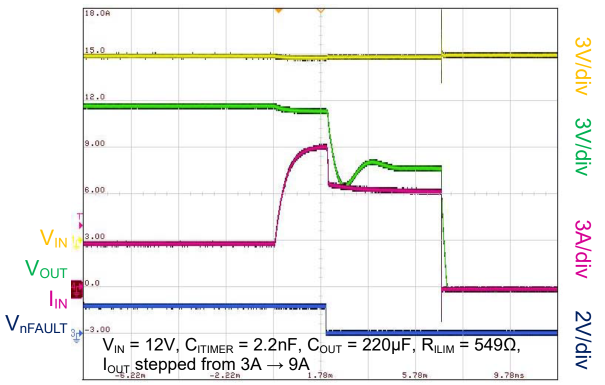
Time (500μs/div)

Active Current Limit Response



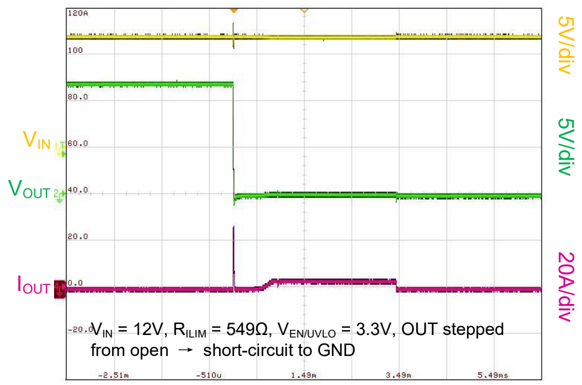
Time (2ms/div)

Active Current Limit Response Followed by T_{SD}



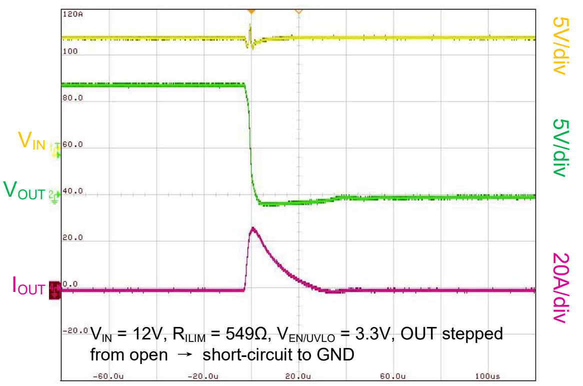
Time (2ms/div)

OUT Pin Short-Circuit during Steady State



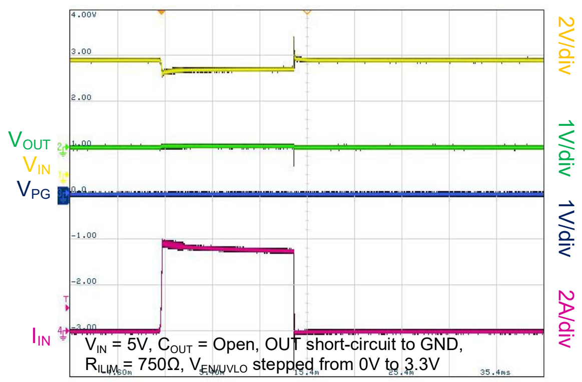
Time (1ms/div)

OUT Pin Short-Circuit during Steady State
(Zoomed In)



Time (20μs/div)

Power-up with OUT Pin Short-Circuit to GND



Time (5ms/div)

FUNCTIONAL BLOCK DIAGRAM

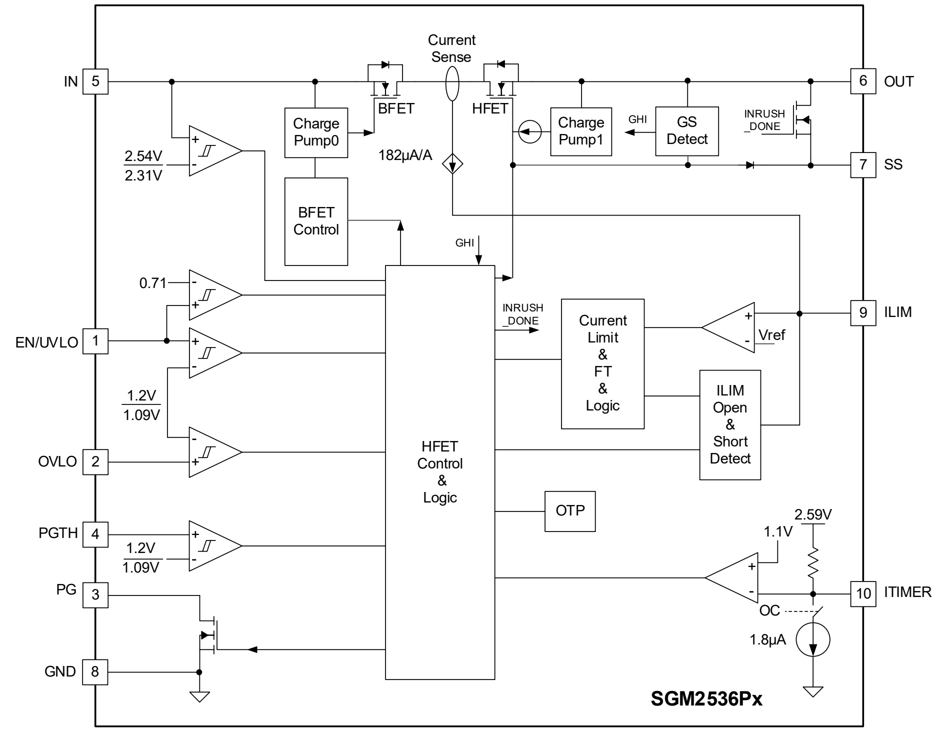


Figure 2. SGM2536Px Block Diagram

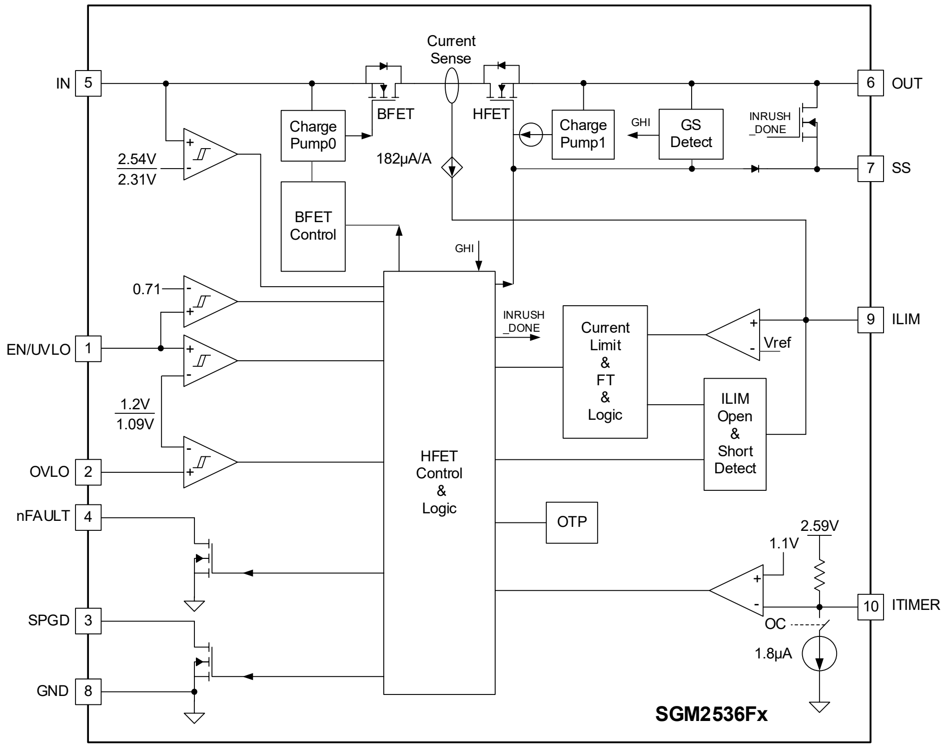


Figure 3. SGM2536Fx Block Diagram

DETAILED DESCRIPTION

Overview

SGM2536 is an eFuse with internal integration of back-to-back FETs (BFET + HFET). It ensures the safety of the power delivery system due to its rich features. When the V_{IN} is greater than V_{UVP_R}, the device starts to sample the voltage of the EN/UVLO pin ($V_{EN/UVLO}$). If $V_{EN/UVLO}$ exceeds V_{UVLO_R}, BFET and HFET start conducting and the current can flow in both directions. When the V_{IN} is less than V_{UVP_F} or $V_{EN/UVLO} < V_{UVLO\_F}$, both BFET and HFET are turned off to realize the reverse current blocking.

After device start-up, the SGM2536 will monitor the V_{IN} and forward current (from IN to OUT). By controlling HFET, the load current cannot exceed the set current limit threshold (I_{ILIM}), and over-voltage spikes are cut-off if they exceed the user-adjustable over-voltage lockout threshold (V_{OVLO}). The fast-trip response of the device can provide rapid protection against serious over-current during short-circuit of OUT pin, so as to prevent the system from being damaged by harmful voltage and current. In addition, the device also provides a user-adjustable over-current blanking timer to allow short-time over-current in the power path without tripping the device frequently. Therefore, SGM2536 not only provides complete protection functions, but also ensures the maximum system uptime during transient events.

There is an integrated thermal sensor to protect itself when the device temperature exceeds the T_{SD}.

Under-Voltage Lockout (UVLO and UVP)

The SGM2536 implements under-voltage protection at IN pin to prevent IN voltage from being too low for normal operation of system and equipment. A fixed locking threshold voltage (V_{UVP}) is provided inside the device for under-voltage protection. In addition, the comparator on the EN/UVLO terminal can be used to set the user-adjustable under-voltage protection threshold through the external resistor divider. Figure 4 and Equation 1 show how to set the specific value of under-voltage protection threshold using an external resistor divider.

$$V_{IN\_UV} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2} \quad (1)$$

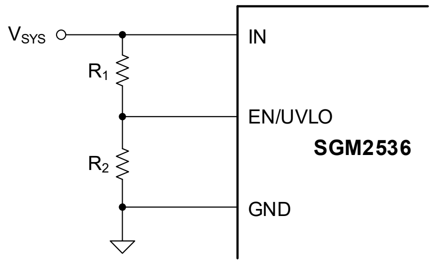


Figure 4. Under-Voltage Lockout

Over-Voltage Lockout (OVLO)

The SGM2536 implements over-voltage lockout at OVLO pin to prevent IN voltage from being too high for normal operation of system and equipment. The comparator on the OVLO pin is used to set the user-adjustable over-voltage protection threshold through the external resistor divider. If the voltage of OVLO pin exceeds the V_{OVLO_R}, the device will shut down the power path. When the voltage of OVLO pin is lower than the V_{OVLO_F}, the power path will be reopened with inrush control. There is a hysteresis between the rising threshold and falling threshold of OVLO. The Equation 2 and Figure 5 show how to set the specific value of over-voltage protection threshold using an external resistor divider.

$$V_{IN\_OV} = \frac{V_{OVLO} \times (R_1 + R_2)}{R_2} \quad (2)$$

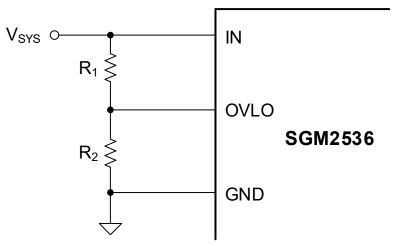


Figure 5. Adjustable Over-Voltage Protection

DETAILED DESCRIPTION (continued)

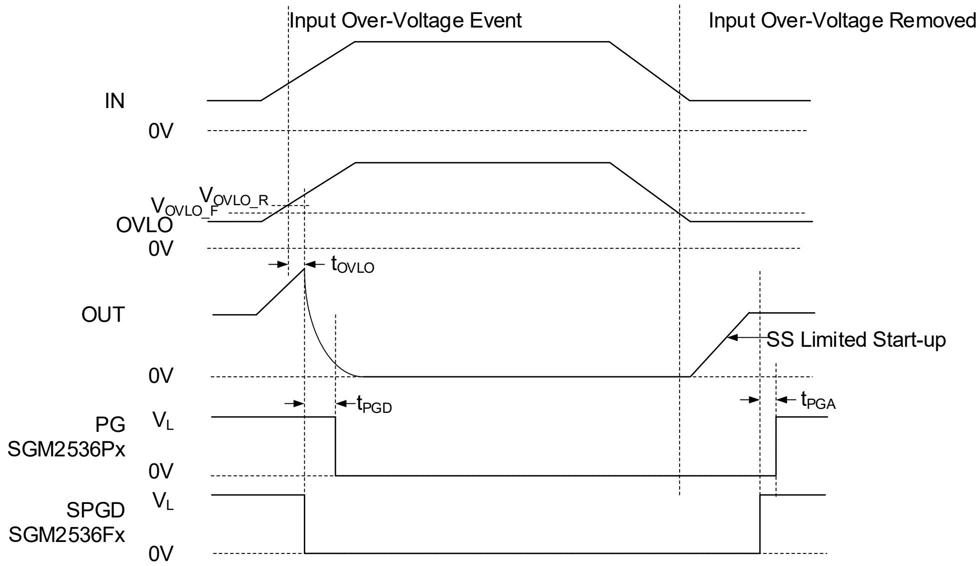


Figure 6. Over-Voltage Lockout and Recovery

Inrush Current, Over-Current, and Short-Circuit Protection

SGM2536 adopts four levels of forward over-current protection function:

- Programmable slew rate (SR) for inrush current protection.
- Programmable current limit threshold (I_{ILIM}) for over-current in steady state or start-up.
- Programmable threshold (I_{SC}) for severe over-current in steady state or start-up.
- Fixed I_{FT} for fast-trip function when short-circuit of OUT occurs.

Slew Rate (SR) and Inrush Current Protection

When hot-plug or system charging large capacitive load occurs, a large inrush current is generated in the equipment power path. The input connector may be damaged or the input power rail voltage may drop, which affects the normal operation and even restarts other equipment in the system.

For a given C_{OUT}, the relationship between the slew rate (SR) and inrush current (I_{INRUSH}) is shown in Equation 3.

$$SR\ (V/ms) = \frac{I_{INRUSH}\ (mA)}{C_{OUT}\ (\mu F)} \quad (3)$$

The slew rate can be controlled by connecting a capacitor at the SS pin to reduce inrush current. For a given slew rate, the corresponding C_{SS} can be calculated by Equation 4. When the SS pin is left floating, the fastest output slew rate can be obtained.

$$C_{SS}\ (pF) = \frac{2000}{SR\ (V/ms)} \quad (4)$$

NOTE: For C_{SS} > 10nF, a 100Ω resistor is recommended to be in series with the C_{SS} on the SS pin.

Current Limit

In case of output over-current, the device actively limits the current after the blanking timer expiring. When the load current exceeds the over-current threshold (I_{ILIM}), but is less than the short-circuit threshold (2 × I_{ILIM}), the device discharges C_{ITIMER} on the ITIMER pin through an internal 1.8μA pull-down current source. Once the load current decreases below the over-current threshold before the C_{ITIMER} is discharged by ΔV_{ITIMER}, the ITIMER pin will be pulled up to V_{INT} internally and the current limit will not be triggered. If the over-current condition still exists after the C_{ITIMER} voltage drops by ΔV_{ITIMER}, the device will limit the current to the over-current threshold by regulating HFET. At the same time, the ITIMER pin is recharged to the V_{INT} to maintain the default state before the next over-current event, which ensures a complete blanking time for each over-current event. In general, the device can provide protection against over-current events and also allow transient current pulses to flow through the power path. For a given over-current threshold, the value of R_{ILIM} can be calculated by Equation 5.

$$R_{ILIM}\ (\Omega) = \frac{3260}{I_{ILIM} - 0.03\ (A)} \quad \text{or} \quad R_{ILIM}\ (\Omega) = \frac{3334}{I_{ILIM}\ (A)} \quad (5)$$

DETAILED DESCRIPTION (continued)

NOTES:
1. The device only provides forward (from IN to OUT) over-current protection function.
2. Leave the ILIM pin floating to set the over-current threshold near zero, and the device can hardly be loaded.
3. The current limit circuit implements the fold-back mechanism. In the fold-back region (0V < V_{OUT} < V_{FB}), the current limit threshold is smaller than the current limit threshold (I_{ILIM}) under steady state.
4. When the ILIM is short to the GND under normal operations, it will be detected as a fault case. There is a minimum I_{nFAULT} which the device allows in this case before the pin short condition is detected.

The blanking time can be adjusted by changing the capacitance connected to the ITIMER pin. Over-current blanking time can be calculated by Equation 6.

$$t_{ITIMER}\ (ms) = \frac{\Delta V_{ITIMER}\ (V) \times C_{ITIMER}\ (nF)}{I_{ITIMER}\ (\mu A)} \quad (6)$$

NOTES:
1. Leaving the ITIMER pin floating or short to GND sets the minimum over-current blanking time. But it is not recommended to leave ITIMER pin short to GND, because it increases the current consumption of the device.
2. The active current limit set by R_{ILIM} is still valid during start-up, which ensures that the load current does not exceed I_{ILIM} during start-up. However, there is no over-current blanking time in the start-up process.
3. Increasing C_{ITIMER} can increase the over-current blanking time, but it also increases the time for C_{ITIMER} to charge to V_{INT}. If the next over-current case occurs before the C_{ITIMER} is fully charged to the V_{INT}, the current blanking time of this event will be shorter than intended.

During the active current limit, there is more power dissipation on the HFET because the output voltage drops. If the internal temperature of the device exceeds the T_{SD}, the HFET will be turned off, and the device will either be latched off (SGM2536xL) or restarted automatically after a certain time interval (SGM2536xR).

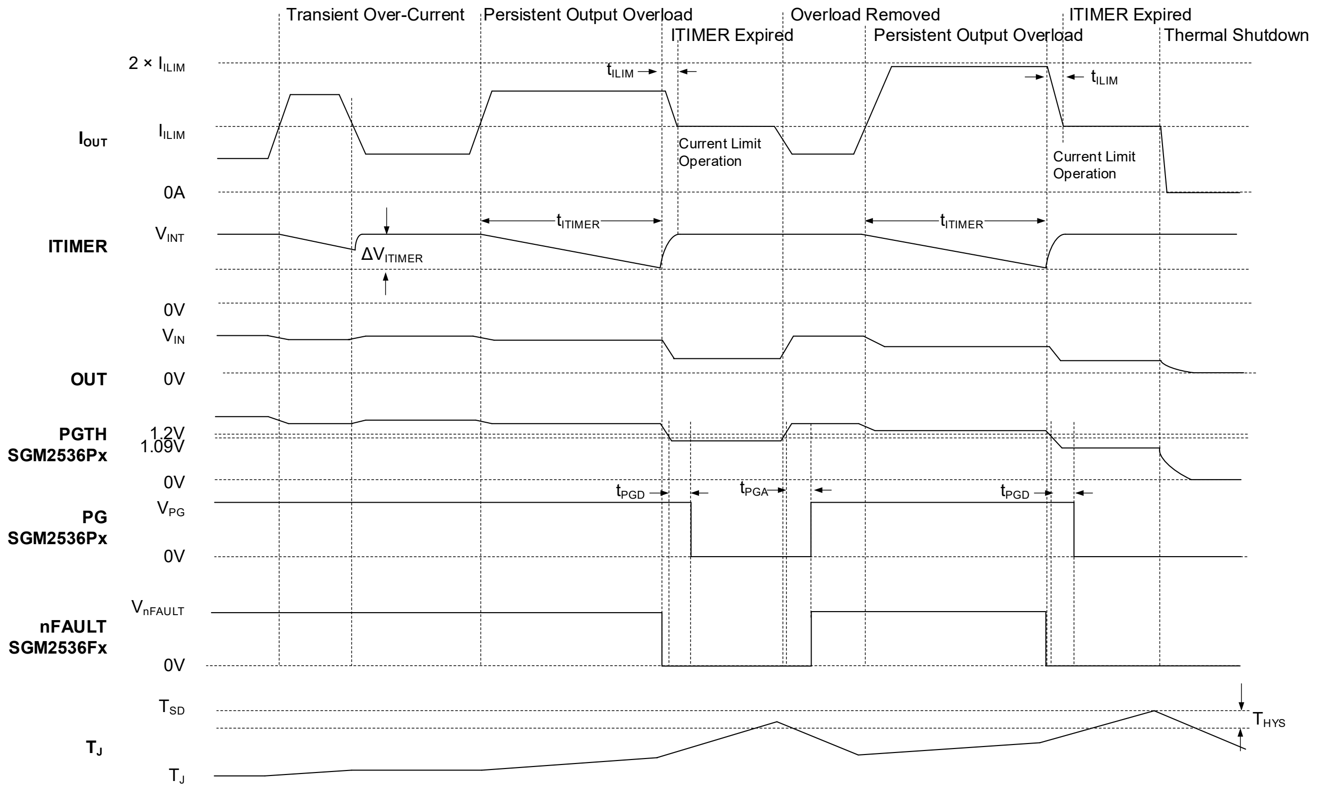
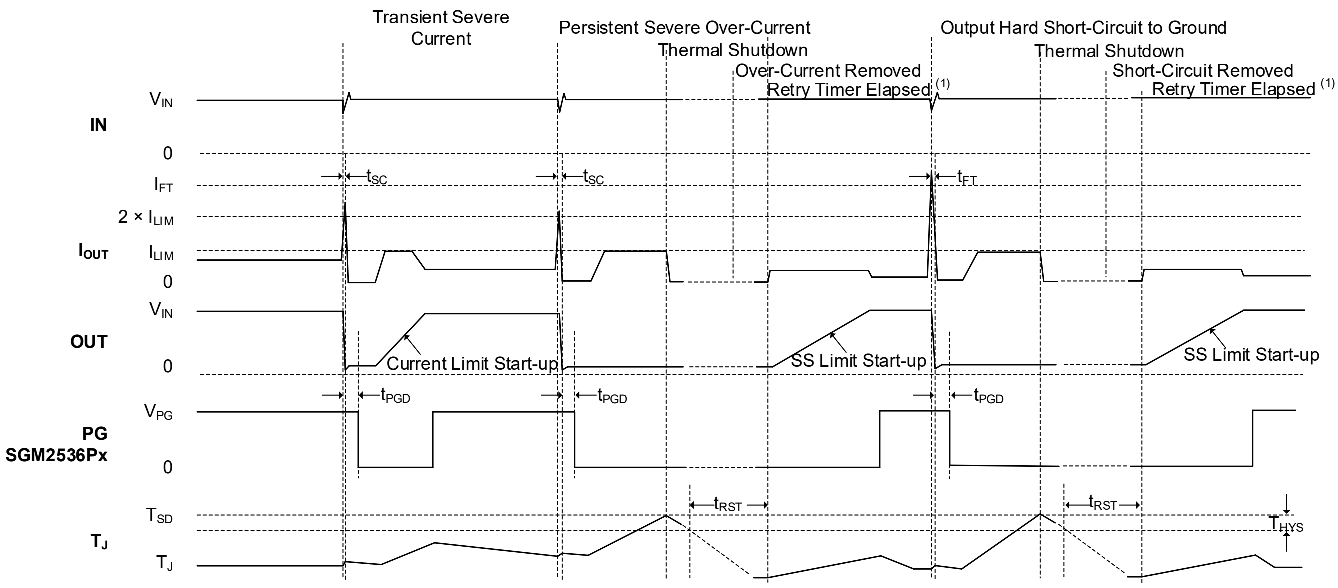


Figure 7. Current Limit Response

DETAILED DESCRIPTION (continued)

Short-Circuit Protection

When a serious over-current event similar to a short-circuit event occurs, the SGM2536 triggers a fast-trip response to prevent the system from being damaged by excessive current flowing through the device. A fast-trip comparator with scalable threshold (I_{SC} = 2 × I_{ILIM}) is adopted inside the device, which allows users to program the fast-trip threshold in low current system. A fixed fast-trip threshold is also set inside the device for fast protection against hard short-circuit events in steady state. It is recommended that the fixed fast-trip threshold be greater than the maximum value of the scalable fast-trip threshold. HFET will be completely turned off within t_{FT} if the current exceeds I_{FT} or I_{SC}. Then the device will turn HFET on again after a short of deglitch time in a current limit mode. In this way, the rapid recovery of HFET can be realized after a transient severe over-current event, and the drop of OUT voltage can be minimized. If the fault persists, the devices continue to operate in the current limit mode, causing the internal temperature of the device to rise until the thermal shutdown.



NOTE: 1. SGM2536xR only.

Figure 8. Short-Circuit Response

DETAILED DESCRIPTION (continued)

Load Current Monitor Output

The device provides an analog current sensing output proportional to the load current at the ILIM pin, which enables the device to monitor the load current (from IN to OUT). The user can calculate the load current through the voltage of the ILIM pin connected to the R_{ILIM}. The relationship between V_{ILIM} and I_{OUT} is shown in Equation 7.

$$I_{OUT}\ (A) = \frac{V_{ILIM}\ (\mu V)}{R_{ILIM}\ (\Omega) \times G_{IMON}\ (\mu A/A)} \qquad (7)$$

NOTES:

1. ILIM pin is sensitive to capacitive loads. In order to ensure the normal operation of the device, the parasitic capacitance of the ILIM pin needs to be less than 50pF.
2. The analog load current monitor is only applicable to the forward current (from IN to OUT).

Reverse Current Protection

The SGM2536 is internally integrated with back-to-back MOSFETs connected in a common drain configuration. When the device is disabled or shutdown, both FETs are turned off, so the current in both directions is blocked.

Over-Temperature Protection (OTP)

The SGM2536 always monitors the temperature (T_J) of the internal die. Once the internal temperature exceeds the T_{SD}, the device shuts down immediately. The SGM2536 will not turn on until the internal temperature is lower than a safe threshold (T_{SD} - T_{HYS}).

When SGM2536xL triggers the thermal shutdown, it still remains in the shutdown state unless the equipment is re-enabled or power cycled. When SGM2536xR triggers the thermal shutdown, it remains in the shutdown state until the internal temperature of the equipment drops by T_{HYS}. After that, it will retry to turn on automatically after a t_{RST} delay time if the device is still enabled.

Fault Response and Indication (nFAULT)

Table 2 shows the protection response of equipment under different fault conditions. The SGM2536Fx provides an active-low external fault flag pin.

A latched fault can be cleared by power cycling (pulling V_{IN} to 0V) or re-enable (pulling EN/UVLO pin below V_{SD}). This will also reset the t_{RST} in SGM2536xR. It is worth mentioning for the whole SGM2536 series, pulling down EN/UVLO below the UVLO threshold cannot clear the latched fault. The SGM2536xR will retry automatically after the t_{RST} timer expiring when a fault has occurred.

Power Good Pin (PG)

The SGM2536Px provides an active-high open-drain output (PG) as the indication pin of power good. It is asserted as high according to the PGTH pin voltage and the equipment working state. PG pin needs to be pulled up to an external power supply.

At the initial stage of power-on, PG is pulled down. Then the device enters the start-up sequence, in which the HFET has been controlled and not fully conductive. When the gate voltage of HFET reaches overdrive, HFET is fully conductive and the start-up sequence is completed, V_{PGTH} is higher than V_{PGTH_R}, and PG is asserted high after a deglitch time (t_{PGA}).

The PG will be de-asserted when the PGTH voltage falls below V_{PGTH_F} or when the system has faults other than over-current during steady state. The deglitch time is t_{PGD}, when PG is de-asserted.

When the device is not powered, the PG pin should be low. However, there is no effective power supply to drive the PG pin down to GND in this case. If the PG is pulled up by an independent power supply and the device is not powered, there may be a small voltage on the PG caused by sink current, which is a function of the pull-up supply and pull-up resistance connected to the PG. In order to avoid the small voltage on the PG pin being detected as logic high by the external related circuit, the sink current of the pin should be minimized.

Table 1. Thermal Shutdown

Device	Enter T_{SD}	Exit T_{SD}
SGM2536xL (Latch-Off)	$T_J \ge T_{SD}$	$T_J < T_{SD} - T_{HYS}$, device power cycled or re-enabled (with EN/UVLO pin)
SGM2536xR (Auto-Retry)	$T_J \ge T_{SD}$	$T_J < T_{SD} - T_{HYS}$, t_{RST} timer expired

DETAILED DESCRIPTION (continued)

Table 2. Fault Summary

Event	Protection Response	Fault Latched Internally	nFAULT Pin Status (1)	nFAULT Assertion Delay (1)
Over-Temperature	Shutdown	Y	L	
Under-Voltage (UVP or UVLO)	Shutdown	N	H	
Over-Voltage	Shutdown	N	H	
Transient Over-Current ($I_{ILIM} < I_{OUT} < 2 \times I_{ILIM}$)	None	N	H	
Persistent Over-Current (from IN to OUT)	Current Limit	N	L	t_{ITIMER}
OUT Short-Circuit to GND	Circuit Breaker Followed by Current Limit	N	H	
Over-Current during ILIM Open	Shutdown	N	L	t_{ITIMER}
Over-Current during ILIM Shorted to GND	Shutdown	Y	L	

NOTE: 1. SGM2536Fx only.

Table 3. SGM2536Px PG Indication

Event	Protection Response	PG Pin Status	PG Delay
Under-Voltage (UVP or UVLO)	Shutdown	L	
Over-Voltage	Shutdown	L	t_{PGD}
Steady State	NA	H (If $V_{PGTH} > V_{PGTH\_R}$)	t_{PGA}
		L (If $V_{PGTH} < V_{PGTH\_F}$)	t_{PGD}
Transient Over-Current	NA	H (If $V_{PGTH} > V_{PGTH\_R}$)	t_{PGA}
		L (If $V_{PGTH} < V_{PGTH\_F}$)	t_{PGD}
Persistent Overload (from IN to OUT)	Current Limit	H (If $V_{PGTH} > V_{PGTH\_R}$)	t_{PGA}
		L (If $V_{PGTH} < V_{PGTH\_F}$)	t_{PGD}
OUT Short-Circuit to GND	Fast-Trip followed by Current Limit	L	t_{PGD}
Over-Current during ILIM Open	Shutdown	L	t_{PGD}
Over-Current during ILIM Shorted to GND	Shutdown	L	t_{PGD}
Over-Temperature	Shutdown	L	t_{PGD}

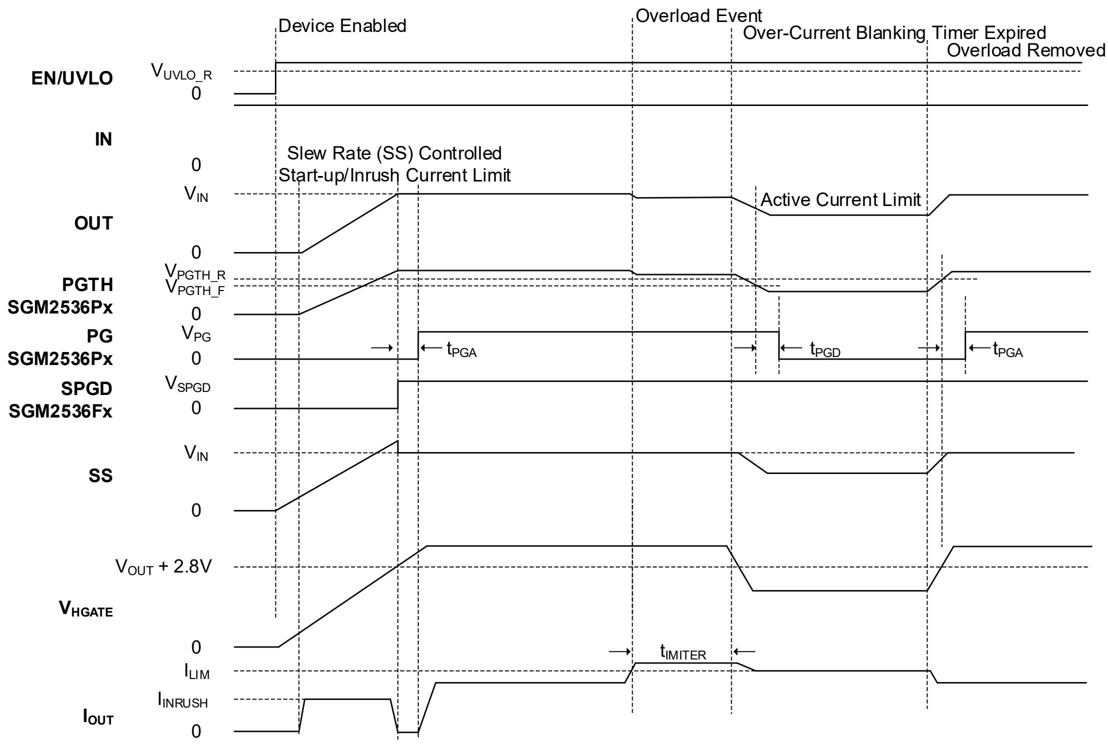


Figure 9. PG Timing

DETAILED DESCRIPTION (continued)

Input Supply Good Indication (SPGD)

The SGM2536Fx provides an active-high open-drain output (SPGD) as a supply valid status indication to the downstream load or system supervisor. SPGD is asserted when the IN voltage is in a proper range (UVP/UVLO < V_{IN} < OVLO) and the inrush sequence of the device is completed. SPGD pin needs to be pulled up to an external power supply.

At the initial stage of power-on, SPGD pin is pulled down. Then the device enters the start-up sequence, in which the HFET has been controlled and not fully conductive. When the gate voltage of HFET reaches overdrive, HFET is fully conductive and the start-up sequence is completed, the SPGD is asserted high.

When the device is not powered, the SPGD pin should be low. However, there is no effective power supply to drive the SPGD pin down to 0V in this case. If the SPGD is pulled up by an independent power supply and the device is not powered, there may be a small voltage on the SPGD caused by sink current, which is a function of the pull-up supply and pull-up resistance connected to the SPGD. In order to avoid the small voltage on the SPGD pin being detected as logic high by the external related circuit, the sink current of the pin should be minimized.

Device Functional Modes

When operating under the recommended operating conditions, the device has one applicable operating mode.

Table 4. SGM2536Fx SPGD Indication

Event	SPGD Pin
Under-Voltage (UVP or UVLO)	L
Over-Voltage (OVLO)	L
Inrush	L
Steady State	H
Over-Current	H
OUT Short-Circuit to GND	L
Over-Current during ILIM Open	L
Over-Current during ILIM Shorted to GND	L
Over-Temperature	L

APPLICATION INFORMATION

Single Device, Self-Controlled

In a system where the MCU is the host, the EN/UVLO or OVLO pin of the device can be driven by the GPIO of the host to realize the control of the device. The ILIM pin can be used as an ADC input to the MCU for current monitoring.

NOTE: ILIM pin is sensitive to capacitive loading. In order to ensure the normal operation of the device, the parasitic capacitance of the ILIM pin needs to be less than 50pF.

For the SGM2536Px, resistor divider of PGTH can be connected to either IN or OUT, depending on which voltage is more suitable as a power good indication.

Typical Application

Many smartphones are equipped with a USB OTG function, which not only allows charging the phone battery, but also allows the phone to be used as a USB host or to charge accessories such as headphones. In addition, some mobile phones are equipped with wireless charging and support wireless charging to charge other devices in reverse. The SGM2536 series can be used as a bidirectional power switch in the above system, as shown in Figure 11.

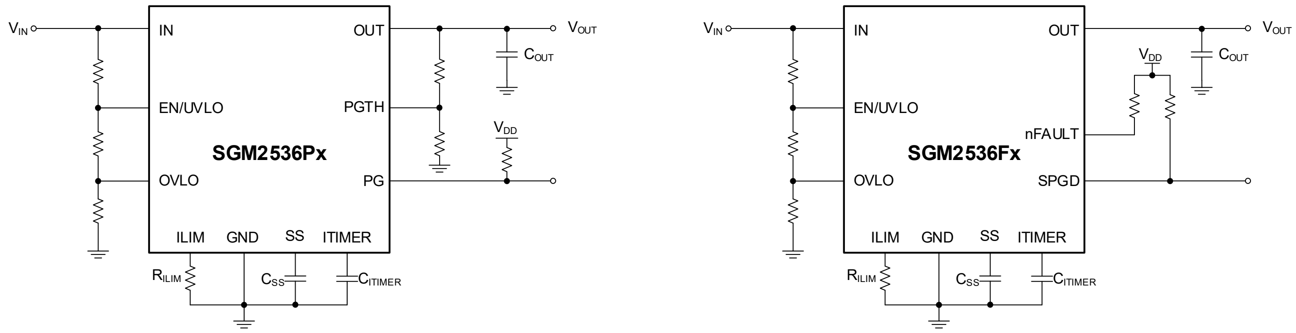


Figure 10. Single Device, Self-Controlled

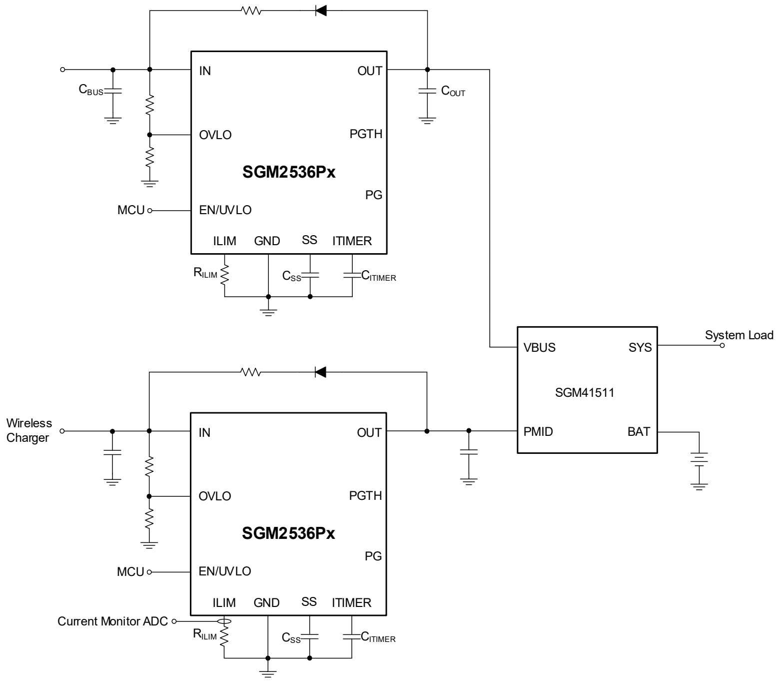
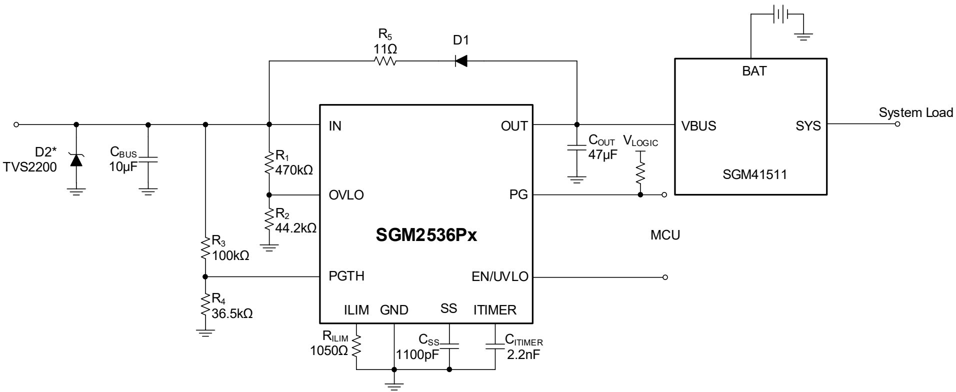


Figure 11. Power Path Example for Smartphone

APPLICATION INFORMATION (continued)

When the USB interface is externally connected to the charger to charge the mobile phone battery, the SGM2536 provides the current path from IN to OUT, and the battery charging IC manages the output control signal to control the charging process of the battery while supplying power to other circuits inside the mobile phone. In this case, the SGM2536 provides over-current and over-voltage protections. Another situation is that when the USB interface is connected to the accessories such as headphones that require the mobile phone battery to provide power, the internal MCU of the mobile phone recognizes the accessories and configures the battery charging IC to BOOST mode and supplies power to the accessories through the USB interface. The SGM2536 needs to provide a current from OUT to IN, and since the IN pin requires a certain voltage (V_{UVP_R}) to turn on the power switch, a diode and resistor in parallel with the device can provide the required bias voltage. The MCU then enables the SGM2536 and establishes a low impedance path to deliver power to the accessories.

Similarly, the device provides a bidirectional power flow path during wireless charging and wireless reverse charging.



* Transient protection requires optional circuit components. See the *Transient Protection* section for details.

Figure 12. USB On-the-Go Port Protection

Design Requirements

Table 5. Design Parameters

Parameter	Value
Bus Voltage during Charging, V_{IN}	9V
Over-Voltage Protection Threshold during Charging, V_{IN_OV}	14V
Bus Power Good Threshold, V_{PG}	4.5V
Max Continuous Charging Current	3A
Load Transient Blanking Interval during Charging, t_{ITIMER}	2ms
Output Capacitance, C_{OUT}	47μF
Output Rise Time, t_R	5ms
Over-Current Threshold (I_{ILIM}) during Charging	3.25A
Start-up Load Current Supported during USB OTG Operation, I_{LOAD}	100mA
Fault Response	Auto-Retry

APPLICATION INFORMATION (continued)

Detailed Design Procedure

SGM2536PR is selected according to the actual application scenario.

Setting Over-Voltage Threshold

The over-voltage threshold is set by a resistor divider connected to the OVLO pin. This threshold can be calculated from Equation 8:

$$V_{IN\_OV} = \frac{V_{OV\_R} \times (R_1 + R_2)}{R_2} \quad (8)$$

where V_{OV_R} is the rising threshold of the OVLO pin and R_1 & R_2 are the resistors of the resistor divider. Since R_1 & R_2 causes additional leakage current to flow out of the input voltage, their values need to be taken into account for the acceptable leakage current of the system. The leakage current flowing through R_1 & R_2 from the supply voltage is $I_{R12} = V_{IN}/(R_1 + R_2)$. Considering that an external active device connected to a resistor divider causes additional leakage current, this increases the calculation error of the supply over-voltage threshold. Therefore, the leakage current flowing through R_1 & R_2 (I_{R12}) should be greater than 20 times the leakage current expected by the OVLO pin.

As can be seen from the EC table, the maximum leakage current of the OVLO pin is 0.1μA, and V_{OV_R} = 1.2V. According to the application scenario requirements, V_{IN_OV} = 14V. Given R_1 = 470kΩ, R_2 = 44.06kΩ can be obtained according to the above equation.

Using the nearest standard 1% resistor values, R_1 = 470kΩ & R_2 = 44.2kΩ are chosen.

Setting Output Voltage Rise Time (t_R)

During the design process, it must be ensured that the junction temperature of the device does not meet the thermal shutdown threshold under either start-up or steady-state conditions. Given that the power stress to which the device is subjected at start-up is typically an order of magnitude larger than under steady-state conditions, the determination of start-up time and inrush current limit is particularly important to avoid thermal shutdown at start-up.

After rise time (t_R) is determined, the slew rate (SR) can be calculated by:

$$SR\ (V/ms) = \frac{V_{IN}\ (V)}{t_R\ (ms)} = \frac{9V}{5ms} = 1.8V/ms \quad (9)$$

The value of the capacitance (C_{SS}) on the SS pin corresponding to this SR can be calculated by the following equation:

$$C_{SS}(pF) = \frac{2000}{SR(V/ms)} = \frac{2000}{1.8} = 1111pF \quad (10)$$

Select the nearest standard capacitor with a capacitance of 1100pF.

The inrush current can be calculated as:

$$I_{INRUSH}\ (mA) = SR\ (V/ms) \times C_{OUT}\ (\mu F) = 1.8 \times 47 = 84.6mA \quad (11)$$

During inrush, the average power dissipation inside the device can be calculated as:

$$PD_{INRUSH}\ (W) = \frac{I_{INRUSH}\ (A) \times V_{IN}\ (V)}{2} = \frac{0.085 \times 9}{2} = 0.38W \quad (12)$$

Based on the calculated power dissipation, the corresponding thermal shutdown time must be higher than the output rise time. Figure 13 shows that for 0.38W, the device thermal shutdown time is greater than 100ms, which is much larger than the output rise time (5ms). Therefore, setting the output rise time to 5ms has no negative impact on device security.

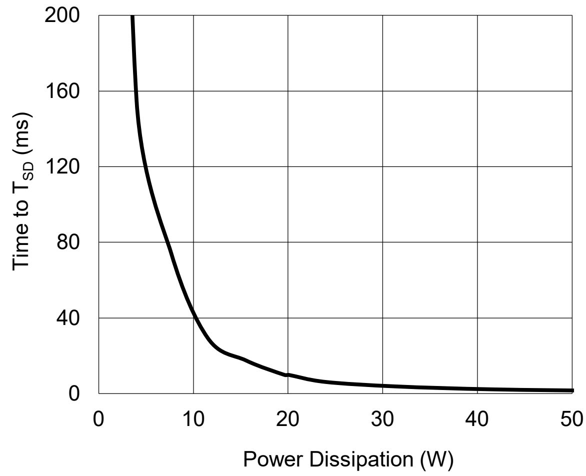


Figure 13. Thermal Shutdown Plot during Inrush

APPLICATION INFORMATION (continued)

Power Good Assertion Threshold

The power good assertion threshold is set by a resistor divider connected to the PGTH pin. This threshold can be calculated from Equation 13:

$$V_{PG} = \frac{V_{PGTH\_R} \times (R_3 + R_4)}{R_4} \quad (13)$$

where V_{PGTH_R} is the rising threshold of the PGTH pin and R_3 & R_4 are the resistors of the resistor divider. Since R_3 & R_4 causes additional leakage current to flow out of the output voltage, their values need to be taken into account for the acceptable leakage current of the system. The leakage current flowing through R_3 & R_4 from the supply is $I_{R34} = V_{IN}/(R_3 + R_4)$. Considering that an external active device connected to a resistor divider causes additional leakage current, this increases the calculation error of the supply over-voltage threshold. Therefore, the leakage current flowing through R_3 & R_4 (I_{R34}) should be greater than 20 times the leakage current expected by the PGTH pin.

As can be seen from the EC table, the maximum leakage current of the PGTH pin is 0.3μA, and V_{PGTH_R} = 1.2V. According to the application scenario requirements, V_{PG} = 4.5V. Given R_3 = 100kΩ, R_4 = 36.4kΩ can be obtained according to the above equation.

Choose the nearest standard 1% resistor values, R_3 = 100kΩ & R_4 = 36.5kΩ are recommended.

Setting Over-Current Threshold (I_{ILIM})

The over-current threshold can be set by the resistor R_{ILIM} connected to the ILIM pin, and its value can be calculated by Equation 14:

$$R_{ILIM}(\Omega) = \frac{3334}{I_{ILIM}\ (A)} = \frac{3334}{3.25A} = 1025.8\Omega \quad (14)$$

Choose the nearest standard 1% resistor values, R_{ILIM} = 1050Ω is recommended.

Setting Over-Current Blanking Interval (t_{ITIMER})

The over-current blanking time can be set by C_{ITIMER}, and it can be calculated as following.

$$C_{ITIMER}\ (nF) = \frac{t_{ITIMER}\ (ms) \times I_{ITIMER}\ (\mu A)}{\Delta V_{ITIMER}\ (V)} = \frac{2 \times 1.8}{1.5} = 2.4nF \quad (15)$$

Select the nearest standard capacitor with a capacitance of 2.2nF.

Selecting External Bias Resistor (R_5)

In OTG mode, the initial state of the SGM2536PR is off. The initial voltage across the USB bus through the diode (D1) and resistor (R_5) can be calculated by:

$$V_{BUS}\ (V) = V_{OUT}\ (V) - V_F\ (V) - I_{LOAD}\ (A) \times R_5\ (\Omega) \quad (16)$$

where:
V_{OUT} is the voltage supplied by the battery charging IC in Boost mode.
V_F is the forward voltage drop across diode D1.
I_{LOAD} is the current drawn by USB powered peripheral initially.

The USB bus voltage must be higher than V_{UVP_R} to ensure that the SGM2536PR can be turned on and can provide sufficient current for USB peripheral devices. Given V_F = 0.4V, V_{OUT_MIN} = 4.5V, V_{UVP_R} = 2.54V, I_{LOAD} = 100mA, the maximum R_5 value of 15.6Ω can be calculated. Select R_5 = 11Ω.

The power dissipation of R_5 under initial conditions can be calculated from Equation 17.

$$P_D\ (W) = I_{LOAD}\ (A) \times I_{LOAD}\ (A) \times R_5\ (\Omega) \quad (17)$$

When the load current is 100mA and R_5 is 11Ω, the power dissipation across R_5 is 0.11W. Therefore, a resistor with a power rate of 0.25W is appropriate.

External Diode (D1) Selection

1. The diode forward voltage drop should be as small as possible to ensure that there is enough headroom for the USB bus voltage to be greater than V_{UVP_R}.
2. The diode can flow more than the maximum current required by the USB peripheral.
3. It must have small footprint.

Power Supply Recommendations

The SGM2536 is designed for a supply voltage from 2.7V to 23V. If the power supply is more than a few inches away from the device, it is recommended to place an input bypass ceramic capacitor greater than 0.1μF. The rated current of the power supply must be greater than the over-current threshold set by the device, otherwise the supply voltage will drop in the event of an over-current or short-circuit.

APPLICATION INFORMATION (continued)

Transient Protection

If the short-circuit or over-current limit case occurs, the device may cut off the current, and due to the parasitic inductance in series at the input and output of the device, a positive voltage spike will occur at the input and output, and a negative voltage spike will occur at the output. The amplitude of the voltage spike is determined by the parasitic inductance. These transients can cause the voltage on the device pins to exceed their maximum absolute rating if the following measures are not taken:

- The length of the wires at the input and output of the device is as small as possible.
- A TVS diode is paralleled at the input port of the device to absorb a positive voltage spike, and a Schottky diode is connected in parallel to the output port to absorb a negative voltage spike.
- Choose a large PCB GND plane.
- Connect a low ESR ceramic capacitor larger than 10μF near the OUT pin.
- A ceramic capacitor greater than 10μF is connected near the input pin to absorb and suppress transient voltage spikes and ringing.

The value of the input capacitance can be calculated from the Equation 18:

$$V_{SPIKE\ (Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (18)$$

where V_{IN} is the rating of the input voltage, I_{LOAD} is the load current, L_{IN} is the effective inductance seen looking into the source, and C_{IN} is the capacitance of the input.

For applications such as USB-C interfaces, the power cord may be plugged into the output of the device. In this case, the voltage stress from OUT to IN may exceed the absolute maximum rating, so it is recommended to add a TVS diode from OUT to IN to clamp the voltage for safety.

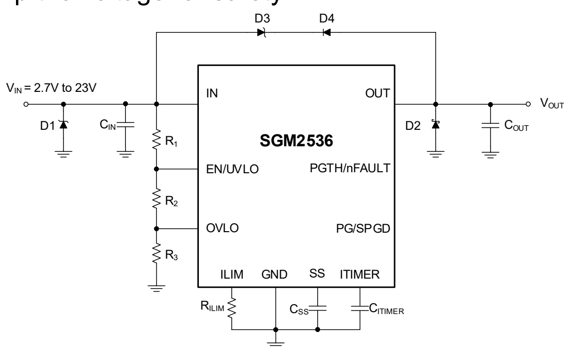


Figure 14. Application with Optional Protection Components

Output Short-Circuit Measurements

The output short-circuit waveform may be affected by factors such as input leads, power supply bypass, layout, device selection, circuit location, and output short-circuit method. It is difficult to obtain repeatable and similar output short-circuit test results. Therefore, the short-circuit results in this datasheet are for informational purposes only. Different short-circuit test results may be achieved because of different test conditions.

Layout Guidelines

In any application, it is recommended to connect a decoupling capacitor of 0.1μF or greater between IN and GND. This decoupling capacitor should be as close as possible to IN and GND pins.

The power path should be as wide and short as possible, with a current carrying capacity of more than twice the device's current limit.

The GND pin of the device must be connected to PCB ground which is a copper plane or island as short as possible.

The IN and OUT pins of the device are used to dissipate heat. Therefore, these two pins should be dissipated as much as possible through the copper plane on the top layer or bottom layer on the PCB. Placing thermal vias on the copper plane improves on-resistance as well as current sensing accuracy.

External components of the device as follows should be placed as close to the corresponding pins as possible:

- R_{ILIM}
- C_{SS}
- C_{ITIMER}
- Resistor dividers of EN/UVLO, OVLO and PGTH

The other end of these components is connected to ground via the shortest possible path. The ILIM pin should have a parasitic capacitance of less than 50pF, and the connection path of this pin should be away from the switching signal.

Protection components such as TVS or Schottky diodes should be connected to the device via a short path to avoid large line inductance. It is important to note that the loop area formed by the protection components should be as small as possible.

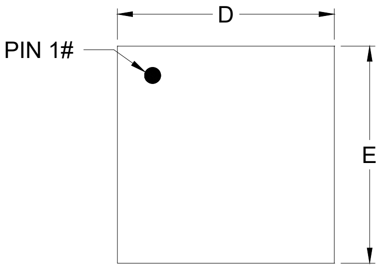
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

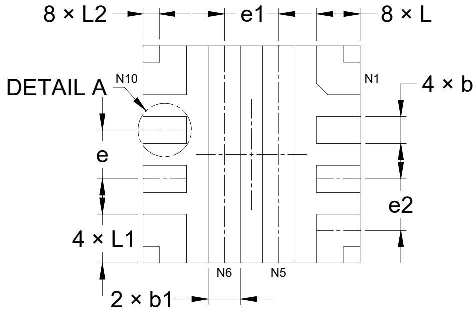
Changes from Original (OCTOBER 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

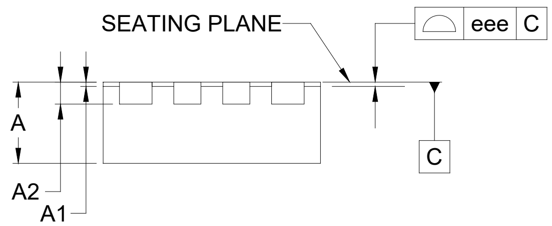
TQFN-2×2-10L



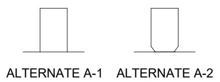
TOP VIEW



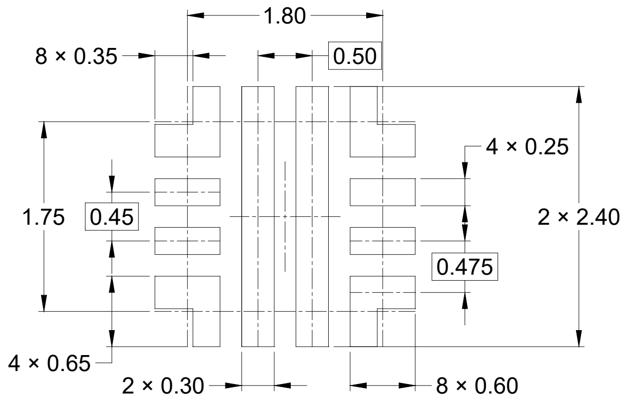
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



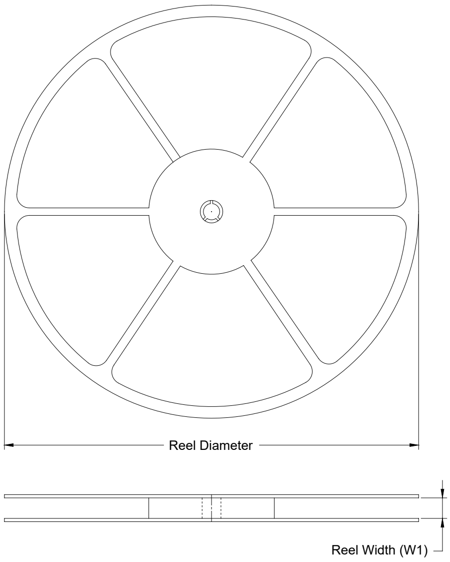
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	**MOD**	**MAX**
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
b1	0.250	-	0.350
D	1.900	-	2.100
E	1.900	-	2.100
e	0.450 BSC		
e1	0.500 BSC		
e2	0.475 BSC		
L	0.300	-	0.500
L1	0.350	-	0.550
L2	0.150 REF		
eee	0.080		

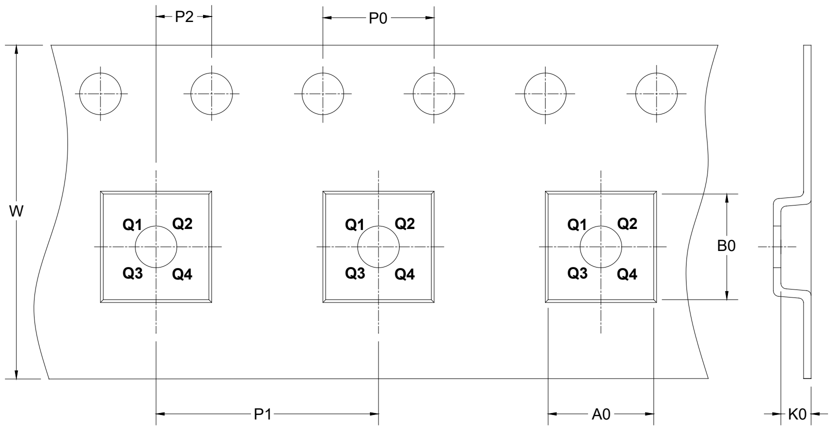
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



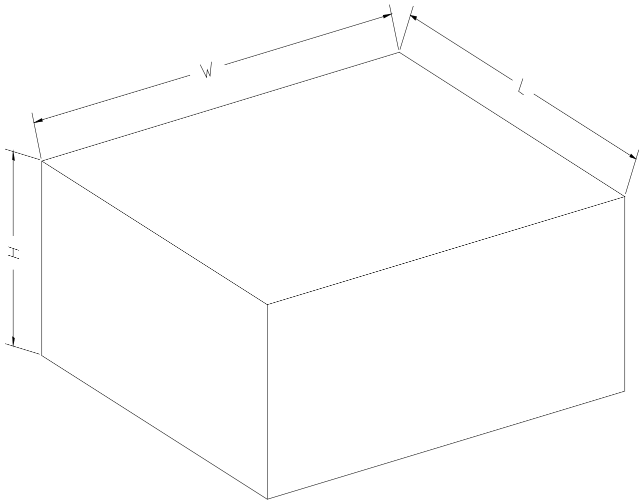
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×2-10L	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002