SGM41282C
70V, 2.5mA Precision Protection APD Bias Dual-Gain Track/Hold Current Mirror

GENERAL DESCRIPTION

The SGM41282C integrates a boost converter for generating up to 70V regulated output, a 1×/8× dual-gain current mirror with a track and hold output buffer, which is unique to simplify the fiber module circuit design due to the use of low resolution ADC.

The SGM41282C is available in a Green TQFN-3×3-16L package.

FEATURES

- **Input Voltage Range: 2.8V to 5.5V**
- **Wide Output Voltage Range from (V_{IN} + 5V) to 70V**
- **850kHz Switching Frequency**
- **1:30 Output Voltage Programming**
- **Adjustable Over-Current Protection**
- **Internal 1×/8× Dual-Gain Current Mirror**
- **2.5V Voltage Buffer for Full-Scale Output Current**
- **Less than 1μA Shutdown Current**
- **Full Chain Circuit: Bias-Mirror-Track/Hold**
- **Replacement of *15059/*3430+*3923**
- **Available in a Green TQFN-3×3-16L Package**

APPLICATIONS

Fiber Modules with APD Photon Sensor
Laser Beam Finders (LIDA)

TYPICAL APPLICATION

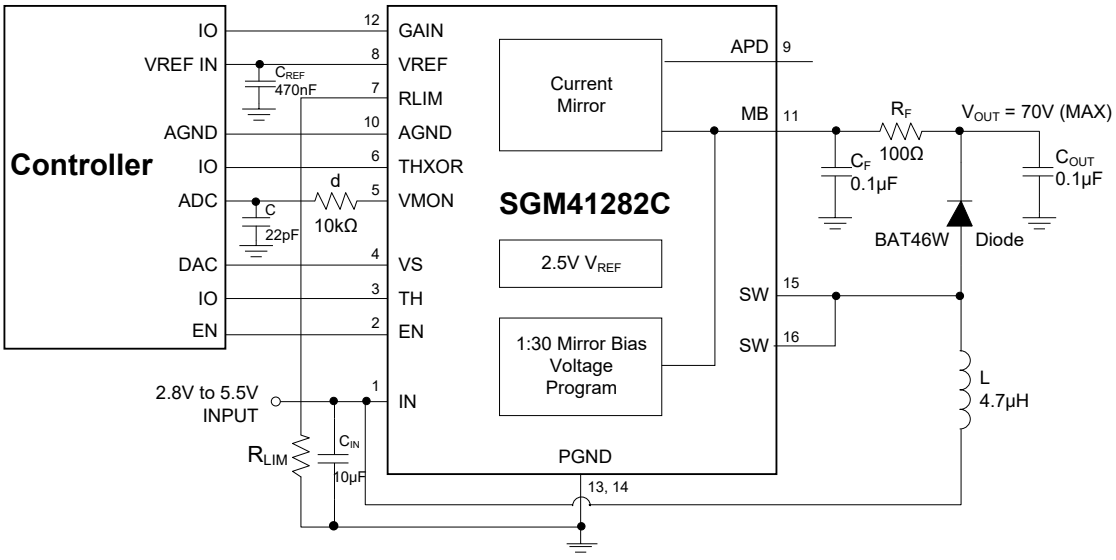


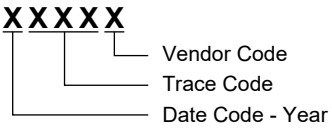
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41282C	TQFN-3×3-16L	-40℃ to +85℃	SGM41282CYTQ16G/TR	MNETQ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, EN, VS, TH, THXOR, VMON, RLIM, VREF, GAIN ..... -0.3V to 6V
SW, MB ..... -0.3V to 76V
APD ..... -0.3V to (V_{MB} + 0.3V)
Package Thermal Resistance
TQFN-3×3-16L, θ_{JA} ..... 45℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.8V to 5.5V
V_{APD} Range ..... 20V to 70V
I_{APD} ..... <2mA
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

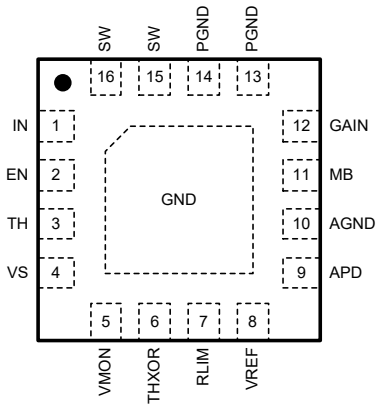
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×3-16L

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1	IN	P	Power Input to all Internal Circuits. Bypass IN to PGND with a ceramic capacitor of 10μF minimum value.
2	EN	I	Enable Input. Input high to enable this chip, and low to shut down the chip.
3	TH	I	Track or Hold Input. Input high for tracking (when THXOR is logic low; check THXOR description for more detail), where the VMON follows the current output of the APD pin simultaneously; low for holding where the VMON outputs a snapshot of APD current captured right after the following edge of the signal applied on the TH pin, in which the APD current snapshot is converted into a voltage and is stored in an internal capacitor.
4	VS	I	Proportional input for programming the MB voltage with an increment gain of 1:30.
5	VMON	O	Current Monitoring Output. Its voltage is proportional to the current of the APD pin.
6	THXOR	I	Logic input; for selecting effective logic level of tracking state at the TH input. The complementary logic level to the logic level of the THXOR at the TH is put for tracking.
7	RLIM	I	Current-Limit Programming. Connect a resistor from RLIM to AGND to program the APD current-limit threshold.
8	VREF	O	Reference Voltage Output.
9	APD	O	Output for Biasing the APD Device. The current out of this pin is sampled with a mirror circuit for current monitoring and over-current protection.
10	AGND	G	Signal Ground. Connect directly to the local ground plane. Connect AGND to PGND at a single point, typically near the return terminal of the output capacitor.
11	MB	I	Mirror Bias Input. Connected to the boost stage output.
12	GAIN	I	1×/8× Gain Selection Input. Input low to select 1× gain and high to select 8× gain; where the 1× gain has an equivalent conversion gain of 1.25kΩ and 10kΩ for 8× gain.
13, 14	PGND	G	Power Ground. Connect the negative terminals of the input and output capacitors to PGND. Connect PGND externally to AGND at a single point, typically at the return terminal of the output capacitor.
15, 16	SW	O	Low End Boost Switch Output. Connect inductor to SW. Minimize the trace area at SW to reduce switching-noise emission.
Exposed Pad	GND	G	Exposed Pad. Connect to a large copper plane at the AGND and PGND potential to improve thermal dissipation. Do not use as the only ground connection.

NOTE：I: input, O: output, G: ground, P: power for the circuit.

ELECTRICAL CHARACTERISTICS

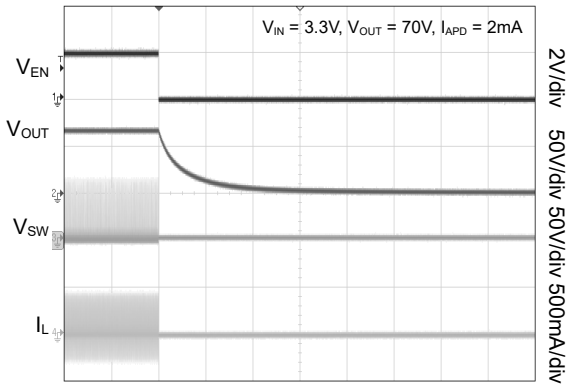
(V_{IN} = 3.3V. Full = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}		Full	2.8		5.5	V
Efficiency	η	70V, 1mA loading	+25℃		26		%
Quiescent Current	I_Q		Full		1.3	2	mA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	Full	2.4	2.5	2.6	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}		+25℃		200		mV
Shutdown Current	I_{SHDN}	V_{SHDN} = 0V	Full		0.01	1	μA
Output Short Circuit Operation Current	I_{SHRT}	V_{OUT} = 40V, R_{LIM} = 28kΩ	+25℃		80		mA
BOOST and APD Biasing							
Switching Frequency	f_{SW}		Full	750	850	950	kHz
Maximum Duty Cycle	D_{MAX}		Full	86.5	90	92	%
V_{VS} to V_{MB} Programming Ratio	VPR		Full	29	30	31	V/V
Boost Start-Up Time	t_{UP}	From EN to 90%, 70V output voltage, 1mA load	+25℃		4		ms
Power Switch On-Resistance	R_{ON}		Full		0.6	1	Ω
Peak Switch Current Limit	I_{LIM_SW}		+25℃	0.9	1.3	1.65	A
Switch Leakage Current		V_{SW} = 72V	+25℃		0.01	1	μA
Mirror Voltage Drop	V_{MD}	I_{APD} = 100μA, V_{OUT} = 50V	Full	2.90	3.05	3.21	V
		I_{APD} = 1mA, V_{OUT} = 50V	Full	3.00	3.15	3.32	V
Current Monitoring							
1× Transfer Resistance	$TR_{1×}$	APD current to VMON transferring ratio, 1× gain	Full	1.16	1.25	1.31	kΩ
8× Transfer Resistance	$TR_{8×}$	APD current to VMON transferring ratio, 8× gain	Full	9.50	10	10.52	kΩ
1× Least End -0.5dB Gain Error Point	$Im_{1×}$	Where the output is -0.5dB off the linear trendline	+25℃		25		μA
1× Most End 0.5dB Gain Error Point	$IM_{1×}$	Where the output is 0.5dB off the linear trendline	+25℃		2.7		mA
Settle Time	t_{ST}	APD to VMON settle time, to 90% for rising and 10% for falling, to 1mA and to 10μA	+25℃		250		ns
TH Effective Delay	t_{DELAY}	TH to track/hold and 1×/8× effective delay	+25℃		50		ns
Effective Hold Aperture Window		The time window for effectively holding	+25℃		3		ns
Holding Droop	V_{DROOP}	Voltage droop measured in 10ms when holding 1V	+25℃		3		V/s
I_{LIM} Programming Accuracy	I_{LIM_APD}	Test with R_{LIM} = 28kΩ for I_{LIM} = 2.4mA	+25℃	2	2.4	2.8	mA
VREF Pin							
Reference Voltage	V_{REF}		Full	2.43	2.48	2.54	V
Load Regulation		From 0 to 1mA	Full		1.5	3	%
Temperature Co-efficiency			+25℃		32		ppm/℃
Logic IO							
Input Low Threshold	V_{IL}		Full			0.4	V
Input High Threshold	V_{IH}		Full	1.6			V
Input Low Souring	I_{LS}	Bias to V_{IL}	Full		0.01	1	μA
Thermal Protection							
Thermal Shutdown Temperature		Temperature rising			160		℃
Thermal Shutdown Hysteresis					15		℃

TYPICAL PERFORMANCE CHARACTERISTICS

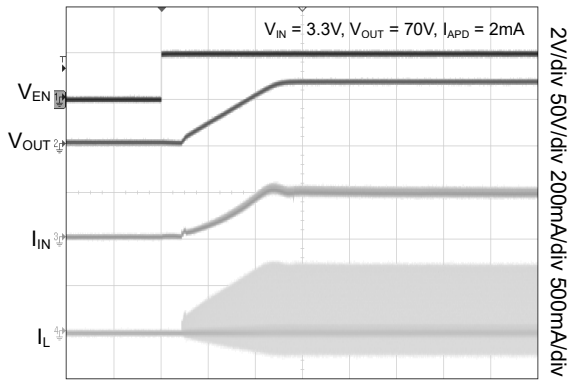
V_{IN} = V_{EN} = 3.3V, V_{OUT} = 70V, T_J = +25℃, unless otherwise noted.

Entering Shutdown



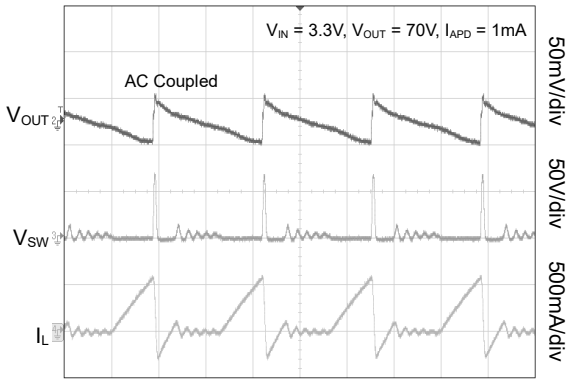
Time (100ms/div)

Exiting Shutdown



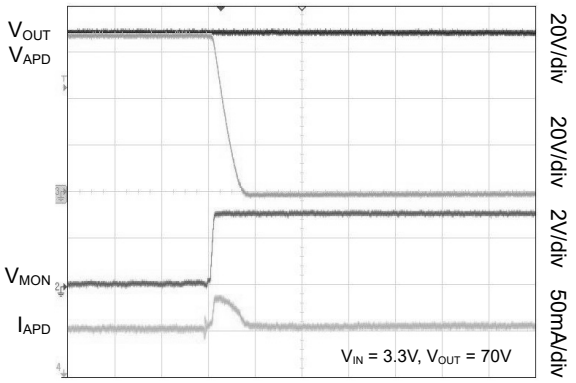
Time (2ms/div)

Steady State



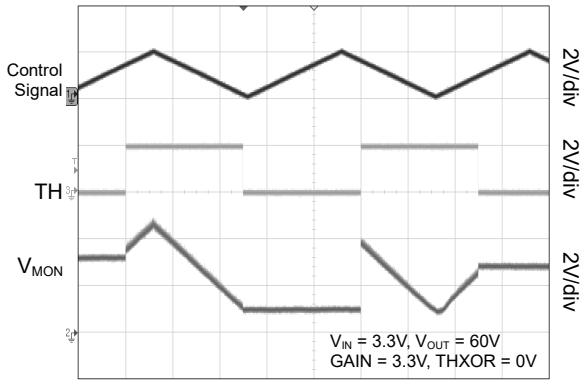
Time (500ns/div)

APD Short-Circuit Response



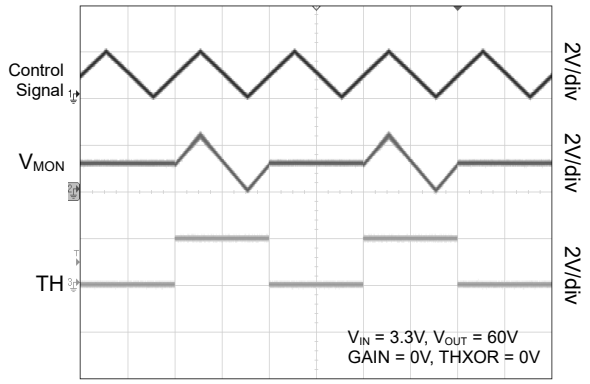
Time (2μs/div)

TH to V_{MON} Timings



Time (2ms/div)

TH to V_{MON} Timings

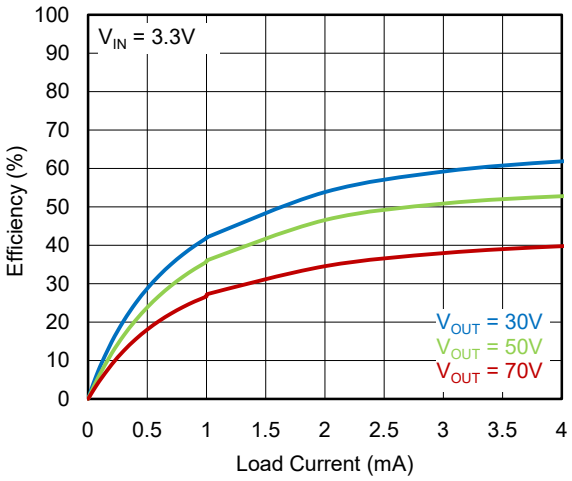


Time (10ms/div)

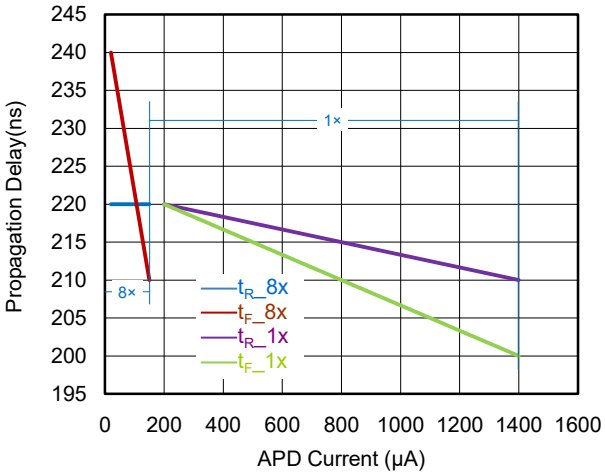
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 70V, T_J = +25℃, unless otherwise noted.

Efficiency vs. Load Current



VMON 0.5V Step Propagation Delay vs. DC Offset Current



FUNCTIONAL BLOCK DIAGRAM

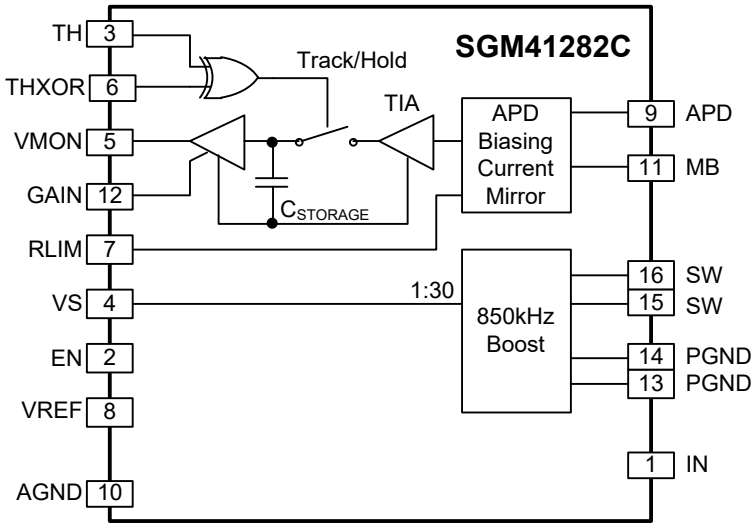


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM41282C is a non-synchronous boost converter using the constant frequency peak current mode control scheme for low voltage systems that require a locally generated high voltage. This device is capable of generating a low noise, high output voltage required for PIN and varactor diode biasing. The supply voltage range is from 2.8V to 5.5V.

The SGM41282C operates in discontinuous mode in order to reduce the switching noise caused by reverse recovery charge of the rectifier diode and eliminates the need for external compensation components. Other continuous-mode boost converters generate large voltage spikes at the output when the SW switch turns on because there is a conduction path between the output, diode, and switch to ground during the time needed for the diode to turn off and reverse its bias voltage. The constant frequency PWM architecture generates an output voltage ripple that is easy to filter. A 72V lateral DMOS device used as the internal power switch is ideal for boost converters with output voltages up to 70V.

Enable and Disable

When the EN pin is pulled to high voltage, the SGM41282C is enabled. When the EN pin is pulled to low voltage, the SGM41282C goes into shutdown mode. Less than 1μA input current is consumed in shutdown mode.

APPLICATION INFORMATION

Extending the Monitoring Range

The GAIN pin input is for selecting 1×/8× gains for proper output levels, that extends the appreciated monitoring range by 8 times. The gain could be changed during tracking or holding, with less interference injection. As the fiber receiver monitors signal in very high dynamic range but less resolution, this circuit brings out a unique tradeoff between the resolution and dynamic range.

Programming the Current Limit Level

Connect a resistor from RLIM pin to AGND to program the current-limit threshold. The R_{LIM} for setting the current limit level is calculated with the following equation, and please refer to the Figure 3 for the typical I_{LIM} to R_{LIM} plot.

$$R_{LIM}(k\Omega) = \frac{70}{I_{APD\_MAX}} \ (mA)$$

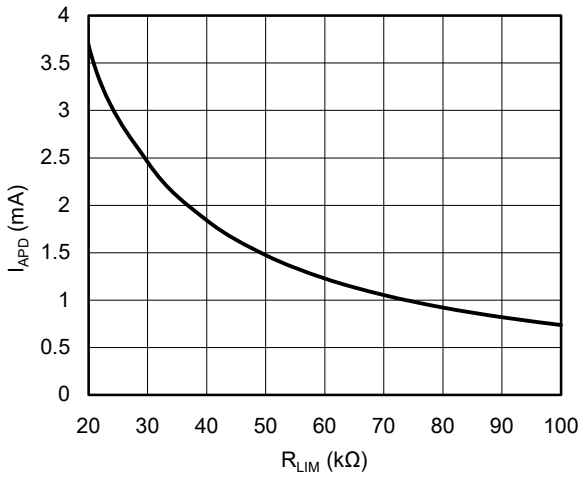


Figure 3. APD Current Limit vs. R_{LIM}

Ripple Filtering

A simple RC filtering circuit could help in suppression of ripple applied at MB input, which then improving the modulation effect to the signal picked-up in the optical channel, which helps in getting better eye diagram opening. Refer to the Figure 4, the resistance of the R inserts drop to be compensated.

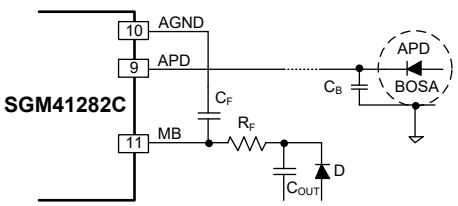


Figure 4. A RC Filtering for Ripple Suppression

Burst Pulse Response

The Figure 5 shows the capture of waveform at the VMON pin in tracking mode, where a train of current pulses with two different peak values is applied to the APD output, representing the case of burst pulse receiving.

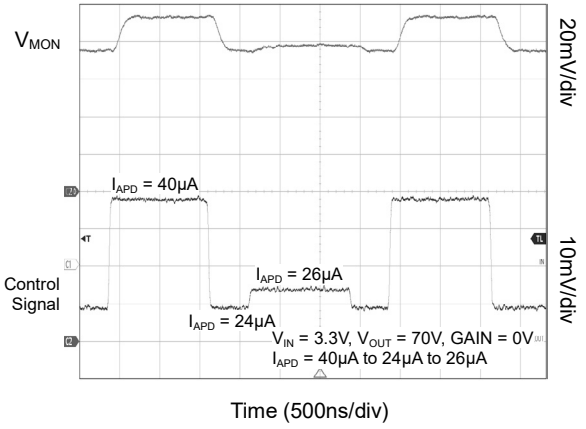


Figure 5. Burst Pulse Receiving Waveform

Backward Scattering

Careful layout of the circuit optimization is desired for assuring fast transient measurement to APD current. Illustrative circuit is showed in the Figure 6, which shows necessary layout considerations. The C_B is low loss capacitor installed in the TO-can in a BOSA, which holds the potential applied on the APD, and the C_B should be evaluated on the final PCB, or , it will slow down the settling time of the monitoring output at the VMON besides the intrinsic propagation and settling of the SGM41282C.

APPLICATION INFORMATION (continued)

The d and the c placed close to the ADC input are for ringing dump, that occurs when the ADC input switch cuts for holding. These two components do not affect the transient, but induce interference to the measurement. Those components should also be evaluated on the final PCB. The recommended values of d and c are 10kΩ and 22pF.

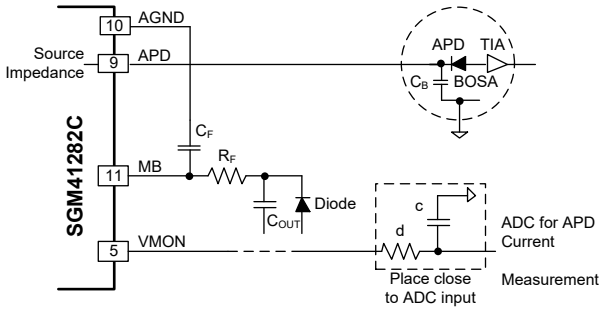


Figure 6. Illustration Circuit

External Components Selection

As the boost circuit works at about 850kHz, capacitors with good high frequency performance are needed for the application circuit. As the storage capacitor (the C_{OUT} in the Figure 1 or the Figure 2) works under high bias voltage, please refer to the capacitor's datasheet to assure its effective capacitance is more than 0.1μF at the output voltage.

Table 1. Key Components Selection Reference

L (μH)	Diode (Schottky Small Signal)	C_{OUT} (μF 100V)	C_{IN} (μF)	R_F (Ω)	C_F (μF 100V)	C_{REF} (nF)
4.7	BAT46W	0.1	10	100	0.1	470

REVISION HISTORY

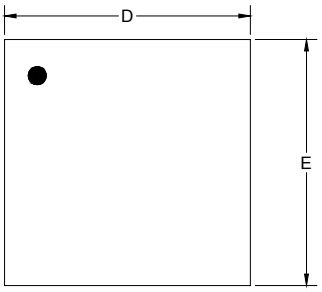
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

NOVEMBER 2020 – REV.A to REV.A.1	Page
Updated Marking Information section	2

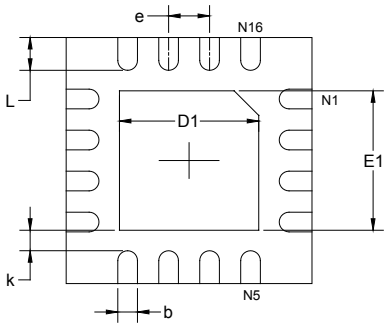
Changes from Original (DECEMBER 2019) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

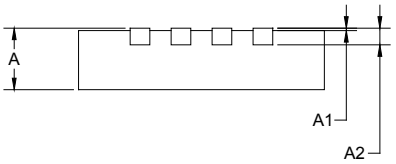
TQFN-3×3-16L



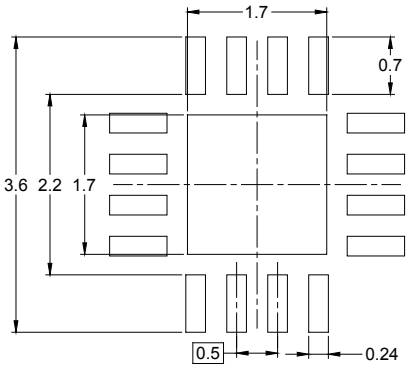
TOP VIEW



BOTTOM VIEW



SIDE VIEW

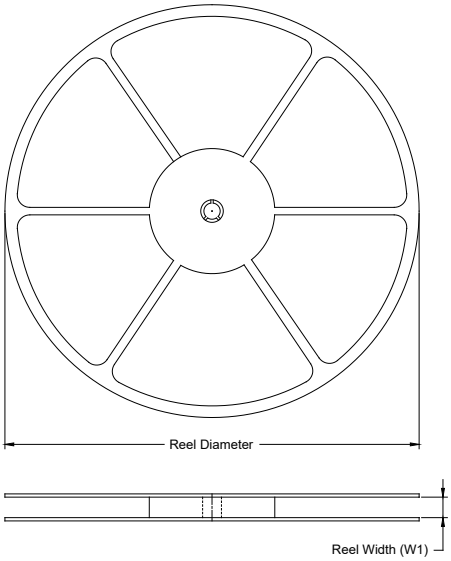


RECOMMENDED LAND PATTERN (Unit: mm)

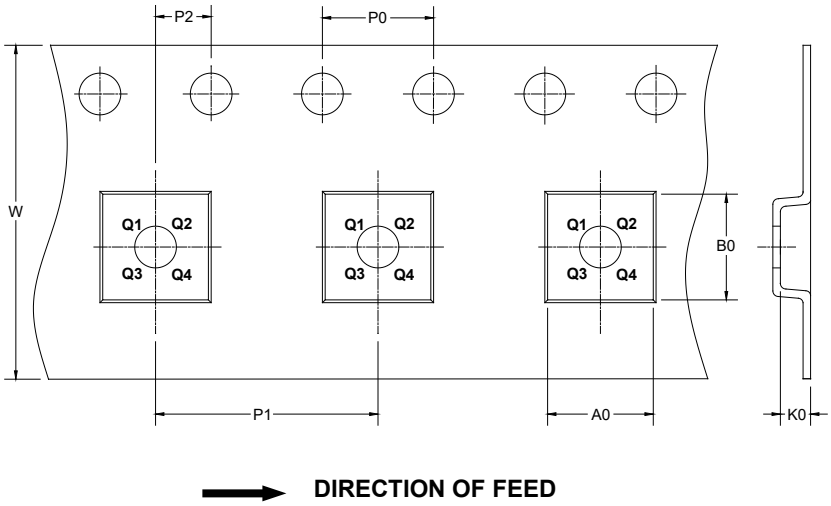
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



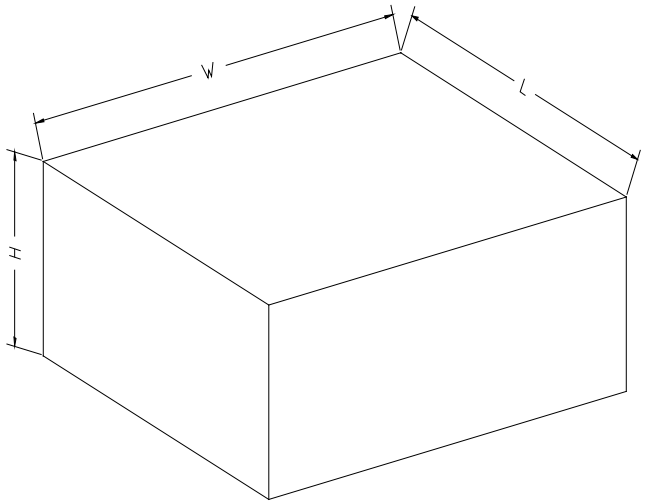
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002