SGM2049

2A, High Accuracy, Low Noise, Low Dropout Linear Regulator

GENERAL DESCRIPTION

The SGM2049 is a high accuracy, low noise, very low dropout linear regulator. It is capable of supplying 2A output current with typical dropout voltage of only 75mV. The operating input voltage range is from 1.1V to 7V with BIAS and 1.4V to 7V without BIAS. The output voltage of the SGM2049 can be set from 0.8V to 3.95V in pin-selectable operation and adjusted from 0.8V to 5.2V by using an external resistor divider.

Other features include logic-controlled shutdown mode, short-circuit current limit and thermal shutdown protection. The SGM2049 has automatic discharge function to quickly discharge V_{OUT} in the disabled status.

The SGM2049 is suitable for application which needs high accuracy, low noise and high current power supply, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs) and RF components.

With very high accuracy, remote sensing, and soft-start capabilities to reduce inrush current, the SGM2049 ensures the optimal system performance for powering digital loads such as FPGAs, DSPs and ASICs.

The SGM2049 is available in Green TQFN-3.5×3.5-20L and TQFN-5×5-20L packages. It operates over an operating temperature range of -40℃ to +125℃.

APPLICATIONS

Wireless Equipment
Industrial, Instrumentation and Medical
ADC and DAC
ATE

FEATURES

- **Operating Input Voltage Range:**
  - **With BIAS: 1.1V to 7V**
  - **Without BIAS: 1.4V to 7V**
- **Output Voltage Range:**
  - **Adjustable Operation: 0.8V to 5.2V**
  - **Pin-Selectable Operation: 0.8V to 3.95V**
- **Output Voltage Accuracy: ±1% at +25℃**
- **Low Dropout Voltage: 75mV (TYP) at 2A**
- **Low Noise: 5μV_{RMS} (TYP) with BIAS**
- **Excellent Load and Line Transient Responses**
- **With Output Automatic Discharge**
- **Adjustable Soft-Start Inrush Control**
- **Support Power-Good Indicator Function**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TQFN-3.5×3.5-20L and TQFN-5×5-20L Packages**

TYPICAL APPLICATION

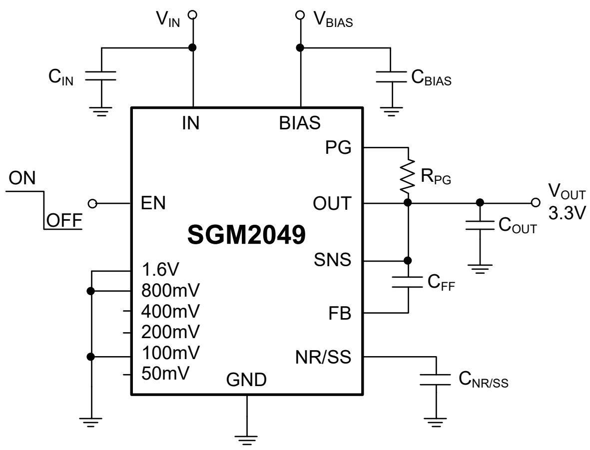


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2049	TQFN-3.5×3.5-20L	-40℃ to +125℃	SGM2049XTRL20G/TR	SGM2049 XTRL20 XXXXX	Tape and Reel, 4000
	TQFN-5×5-20L	-40℃ to +125℃	SGM2049XTRM20G/TR	SGM2049 XTRM20 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX
- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, BIAS, PG, EN to GND .... -0.3V to 8V
SNS, OUT to GND .... -0.3V to Min(V_{IN} + 0.3V, 8V)
NR/SS, FB to GND .... -0.3V to 3.6V
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V to GND
....-0.3V to (V_{OUT} + 0.3V)
PG Current (Sink Current into Device)............................5mA
Package Thermal Resistance
TQFN-3.5×3.5-20L, θ_{JA}... 40℃/W
TQFN-3.5×3.5-20L, θ_{JB}... 14℃/W
TQFN-3.5×3.5-20L, θ_{JC}... 29℃/W
TQFN-5×5-20L, θ_{JA}.. 37℃/W
TQFN-5×5-20L, θ_{JB}.. 13℃/W
TQFN-5×5-20L, θ_{JC}.. 19℃/W
Junction Temperature ....+150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ....+260℃
ESD Susceptibility
HBM...6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range ....1.1V to 7V
Bias Supply Voltage Range (1) ....3V to 7V
Output Voltage Range ....0.8V to 5.2V
Enable Voltage Range .... 0V to V_{IN}
Output Current ....0A to 2A
Input Effective Capacitance, C_{IN} .... 5μF (MIN)
Output Effective Capacitance, C_{OUT} .... 10μF to 1000μF
Bias Effective Capacitance, C_{BIAS} .... 5μF (MIN)
Power-Good Pull-Up Resistance .... 10kΩ to 100kΩ
Operating Junction Temperature Range ...... -40℃ to +125℃

NOTE:
1. Bias supply voltage is required when V_{IN} < 1.4V and not required when V_{IN} ≥ 1.4V.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

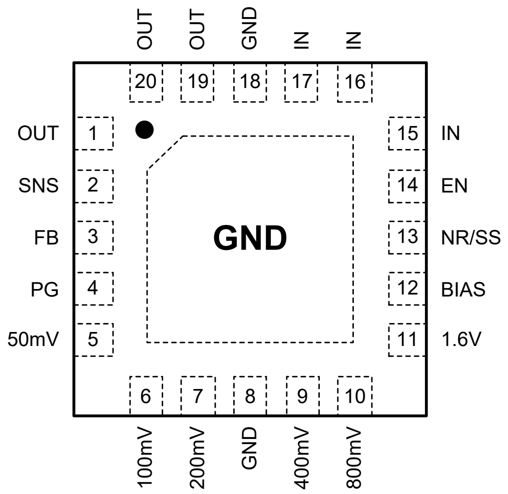
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)



TQFN-3.5×3.5-20L/TQFN-5×5-20L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 19, 20	OUT	Regulator Output Pin. It is recommended to use an output capacitor with effective capacitance in the range of 10μF to 1000μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
2	SNS	Output Voltage Sense Input Pin. The SNS pin is connected to the load side of the output trace only when the pin-selectable programming mode is used. Keep SNS pin floating if the V_{OUT} voltage is set by external resistor.
3	FB	Feedback Voltage Input Pin. Connect this pin to the midpoint of an external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.
4	PG	Power-Good Indicator Output Pin. An open-drain, active-high output that indicates the status of V_{OUT}. When the output voltage reaches $V_{IT(PG)}$ of the target, the PG pin goes into a high-impedance state.
5	50mV	Output Voltage Setting Pins. Select the desired output voltage by connecting these pins to the ground. Connecting these pins to the ground increases the output voltage value corresponding to the pin name. Multiple pins can be connected to GND at the same time. When V_{OUT} is set by an external resistor, leave these pins floating (open).
6	100mV	
7	200mV	
9	400mV	
10	800mV	
11	1.6V	
12	BIAS	Bias Supply Voltage Pin for Internal Control Circuits. This pin is monitored by internal under-voltage lockout circuit and enables the use of low-input voltage, low-output voltage conditions (V_{IN} < 1.4V).
13	NR/SS	Noise-Reduction and Soft-Start Pin. Using an external capacitor $C_{NR/SS}$ to decouple this pin to GND can not only reduce output noise to very low level but also slow down the V_{OUT} rise like a soft-start behavior.
14	EN	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. This pin must be connected to IN or BIAS pin if enable functionality is not used.
15, 16, 17	IN	Input Supply Voltage Pin. It is recommended to use a 10μF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to IN pin.
8, 18	GND	Ground.
Exposed Pad	GND	Exposed Pad. Connect it to GND internally. Connect it to a large ground plane to maximize thermal performance; this pad is not an electrical connection point.

ELECTRICAL CHARACTERISTICS

(V_{IN} = ($V_{OUT(NOM)}$ + 0.4V) or 1.4V (whichever is greater), V_{BIAS} = Open, $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1.1V, C_{IN} = 10μF, C_{OUT} = 22μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF and PG pin pulled up to V_{IN} with 100kΩ, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage Range	V_{IN}		1.1		7	V
Bias Supply Voltage Range	V_{BIAS}	V_{IN} = 1.1V	3		7	V
Output Voltage Range	V_{OUT}	Pin-selectable operation	0.8		3.95	V
		Adjustable operation, using external resistors	0.8		5.2	
Feedback Voltage	V_{FB}	T_J = +25℃	0.792	0.8	0.808	V
			0.784		0.816	
NR/SS Pin Voltage	$V_{NR/SS}$			0.8		V
Input Supply UVLO with Bias	$V_{UVLO1(IN)}$	V_{IN} rising with V_{BIAS} = 3V		0.78	0.95	V
$V_{UVLO1(IN)}$ Hysteresis	$V_{HYS1(IN)}$	V_{BIAS} = 3V		100		mV
Input Supply UVLO without Bias	$V_{UVLO2(IN)}$	V_{IN} rising		1.14	1.4	V
$V_{UVLO2(IN)}$ Hysteresis	$V_{HYS2(IN)}$			40		mV
Bias Supply UVLO	$V_{UVLO(BIAS)}$	V_{BIAS} rising, V_{IN} = 1.1V		2.5	2.8	V
$V_{UVLO(BIAS)}$ Hysteresis	$V_{HYS(BIAS)}$	V_{IN} = 1.1V		260		mV
Output Voltage Accuracy	V_{OUT}	V_{IN} = 1.4V to 7V without BIAS, or V_{IN} = 1.1V, V_{BIAS} = 3V to 7V, I_{OUT} = 5mA to 2A; T_J = +25℃	-1		1	%
		V_{IN} = 1.4V to 7V without BIAS, or V_{IN} = 1.1V, V_{BIAS} = 3V to 7V, I_{OUT} = 5mA to 2A; T_J = -40℃ to +125℃	-1.7		1.3	
		Pin-selectable operation, I_{OUT} = 5mA; T_J = +25℃	-1.4		1.4	
		Pin-selectable operation, I_{OUT} = 5mA; T_J = -40℃ to +125℃	-2		2	
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 1.4V to 7V, I_{OUT} = 5mA		0.04	1.5	mV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{BIAS} = 3V to 7V, V_{IN} = 1.1V, I_{OUT} = 5mA to 2A		0.1	1.8	mV/A
		I_{OUT} = 5mA to 2A		0.1	2.2	
		I_{OUT} = 5mA to 2A, V_{OUT} = 5.2V		0.7	4.5	
Dropout Voltage	V_{DROP}	V_{IN} = 1.4V, I_{OUT} = 2A, V_{FB} = 0.776V		75	120	mV
		V_{IN} = 5.2V, I_{OUT} = 2A, V_{FB} = 0.776V		75	120	
		V_{IN} = 1.1V, V_{BIAS} = 5V, I_{OUT} = 2A, V_{FB} = 0.776V		75	120	
Output Current Limit	I_{LIMIT}	V_{OUT} forced at 90% × $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.4V	2.2	3.2	4	A
Short-Circuit Current Limit	I_{SC}	R_{LOAD} = 20mΩ, under foldback operation		1.7		A
GND Pin Current	I_{GND}	V_{IN} = 7V, I_{OUT} = 5mA		3.3	4.1	mA
		V_{IN} = 1.4V, I_{OUT} = 2A		2.3	3	mA
Shutdown Current	I_{SHDN}	PG = Open, V_{IN} = 7V, V_{EN} = 0.5V, T_J = +25℃		1.4	3	μA
		PG = Open, V_{IN} = 7V, V_{EN} = 0.5V			15	
BIAS Pin Current	I_{BIAS}	V_{IN} = 1.1V, V_{BIAS} = 7V, $V_{OUT(NOM)}$ = 0.8V, I_{OUT} = 2A		2.9	3.6	mA
EN Pin Low-Level Input Voltage	$V_{IL(EN)}$	EN input voltage "L"	0		0.5	V
EN Pin High-Level Input Voltage	$V_{IH(EN)}$	EN input voltage "H"	1.1		7	V
EN Pin Current	I_{EN}	V_{IN} = 7V, V_{EN} = 0V and 7V	-0.3		0.3	μA
Turn-On Time	t_{ON}	From assertion of V_{EN} to V_{OUT} = 90% × $V_{OUT(NOM)}$		300		μs
Output Discharge Resistance	R_{DIS}	V_{IN} = 1.4V, V_{EN} = 0V, V_{OUT} = 0.5V	190	260	330	Ω

ELECTRICAL CHARACTERISTICS (continued)

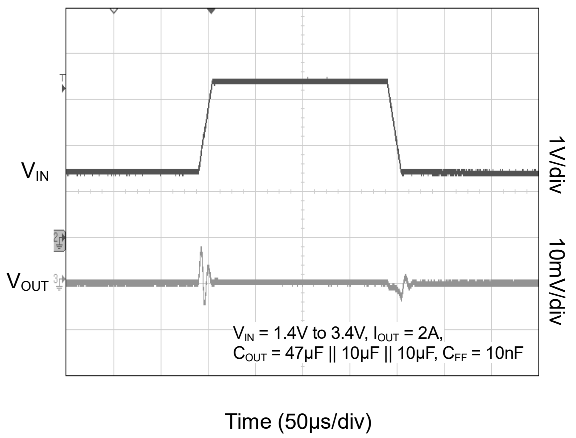
(V_{IN} = ($V_{OUT(NOM)}$ + 0.4V) or 1.4V (whichever is greater), V_{BIAS} = Open, $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1.1V, C_{IN} = 10μF, C_{OUT} = 22μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF and PG pin pulled up to V_{IN} with 100kΩ, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PG Pin Threshold	$V_{IT(PG)}$	For falling V_{OUT}		84% × V_{OUT}	89% × V_{OUT}	93% × V_{OUT}	V
PG Pin Hysteresis	$V_{HYS(PG)}$	For rising V_{OUT}			1.7% × V_{OUT}		V
PG Pin Low-Level Output Voltage	$V_{OL(PG)}$	V_{OUT} < $V_{IT(PG)}$, I_{PG} = -1mA (current into device)			0.17	0.3	V
PG Pin Leakage Current	$I_{lkg(PG)}$	V_{OUT} > $V_{IT(PG)}$, V_{PG} = 7V, V_{IN} = 7V			0.01	0.5	μA
NR/SS Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 7V		3.5	5.8	8.5	μA
FB Pin Leakage Current	I_{FB}	V_{IN} = 7V		-120		120	nA
Power Supply Rejection Ratio	PSRR	V_{IN} to V_{OUT}, V_{OUT} = 0.8V, (V_{IN} - V_{OUT}) = 0.4V, V_{BIAS} = 5V, I_{OUT} = 2A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 22μF	f = 10kHz		51		dB
			f = 500kHz		23		
		V_{IN} to V_{OUT}, V_{OUT} = 5V, (V_{IN} - V_{OUT}) = 0.4V, I_{OUT} = 2A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 22μF	f = 10kHz		47		
			f = 500kHz		20		
Output Voltage Noise	e_n	f = 10Hz to 100kHz, I_{OUT} = 2A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF	V_{OUT} = 0.8V, V_{IN} = 1.1V, V_{BIAS} = 5V		5		$μV_{RMS}$
			V_{OUT} = 5V, V_{IN} = 5.4V, V_{BIAS} = 0V		11		
Thermal Shutdown Temperature	T_{SHDN}				165		℃
Thermal Shutdown Hysteresis	$ΔT_{SHDN}$				25		℃

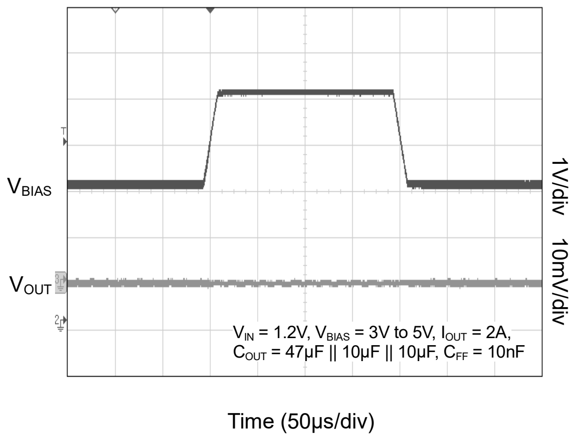
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.4V) or 1.4V (whichever is greater), V_{BIAS} = Open, $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1.1V, C_{IN} =10μF, C_{OUT} = 22μF, $C_{NR/SS}$ = 0nF, no C_{FF}, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

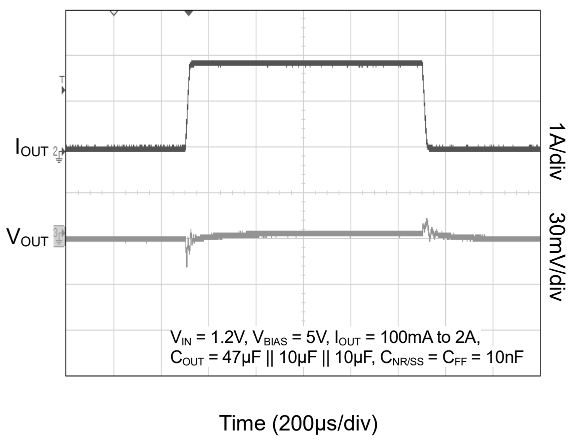
V_{IN} Line Transient Response without BIAS



V_{BIAS} Line Transient Response



Load Transient Response with BIAS



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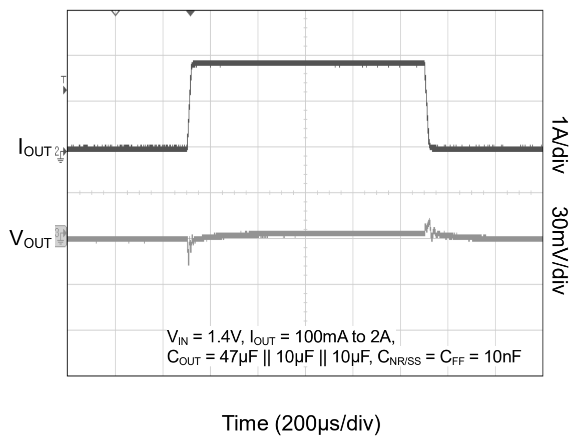
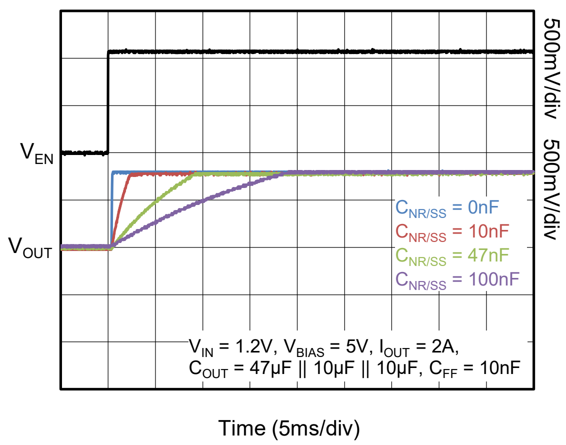
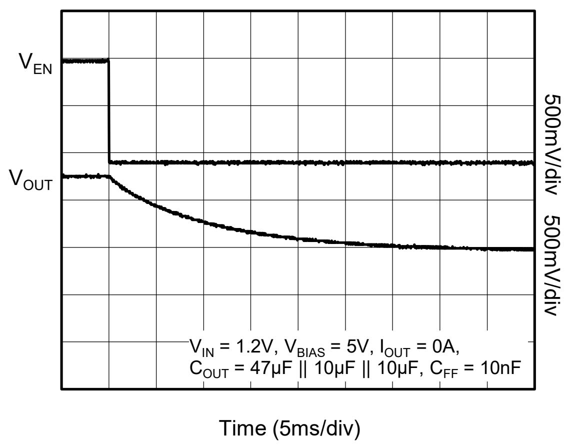


Enable Turn-On Response



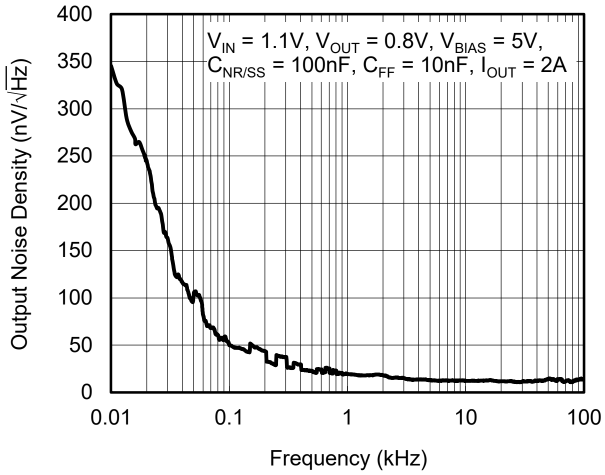
Enable Turn-Off Response



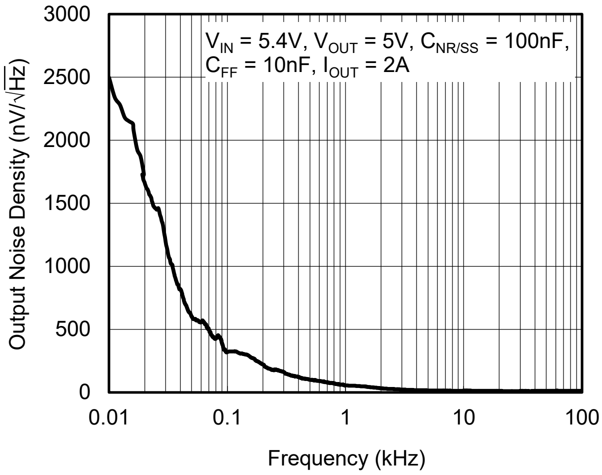
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.4V) or 1.4V (whichever is greater), V_{BIAS} = Open, $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1.1V, C_{IN} =10μF, C_{OUT} = 22μF, $C_{NR/SS}$ = 0nF, no C_{FF}, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

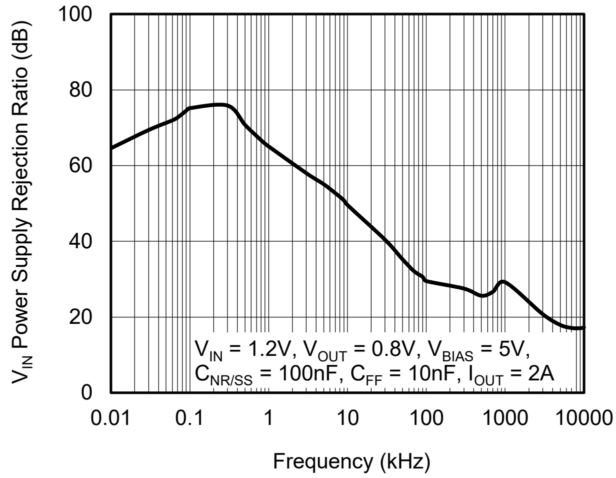
Output Noise Density vs. Frequency



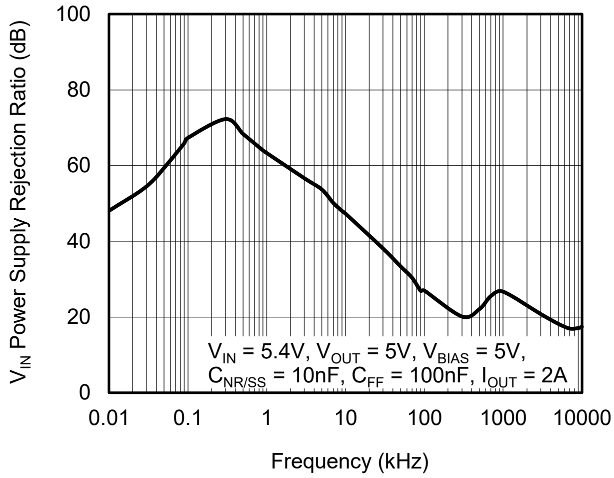
Output Noise Density vs. Frequency



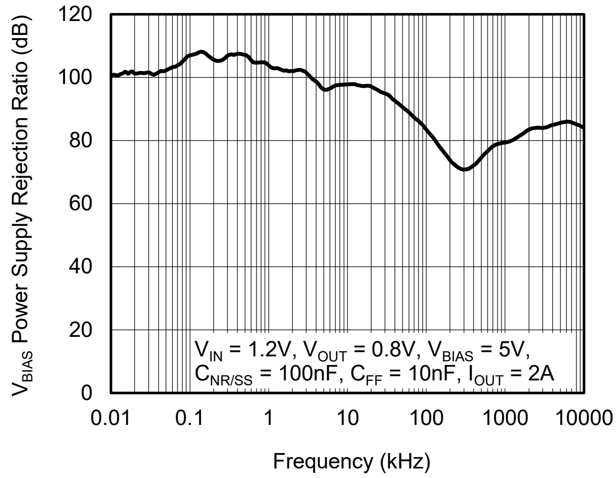
V_{IN} Power Supply Rejection Ratio vs. Frequency



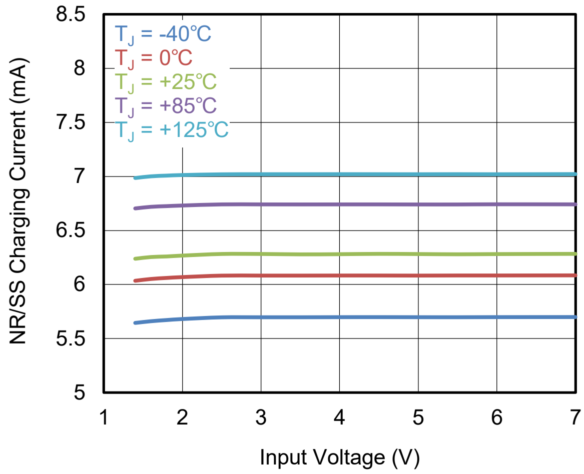
V_{IN} Power Supply Rejection Ratio vs. Frequency



V_{BIAS} Power Supply Rejection Ratio vs. Frequency



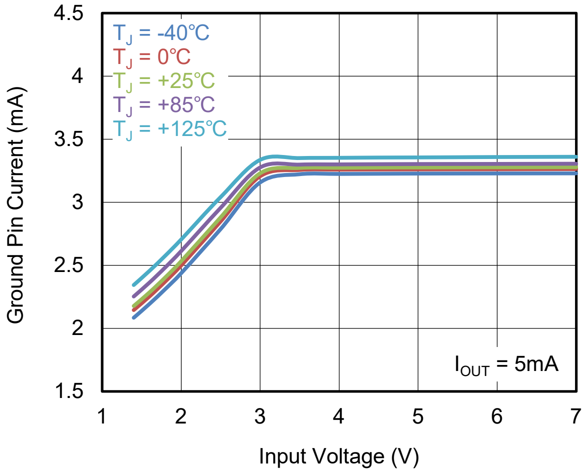
NR/SS Charging Current vs. Input Voltage



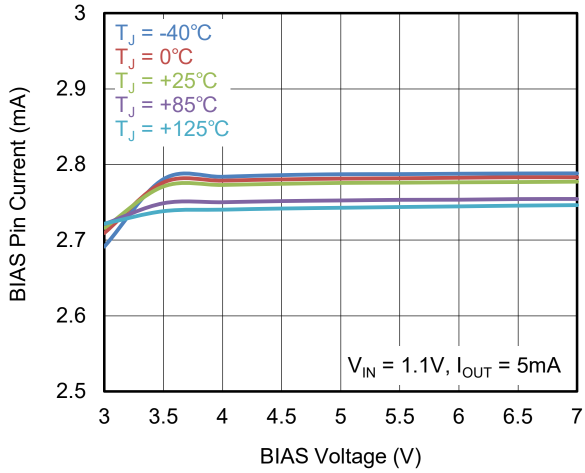
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.4V) or 1.4V (whichever is greater), V_{BIAS} = Open, $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1.1V, C_{IN} =10μF, C_{OUT} = 22μF, $C_{NR/SS}$ = 0nF, no C_{FF}, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

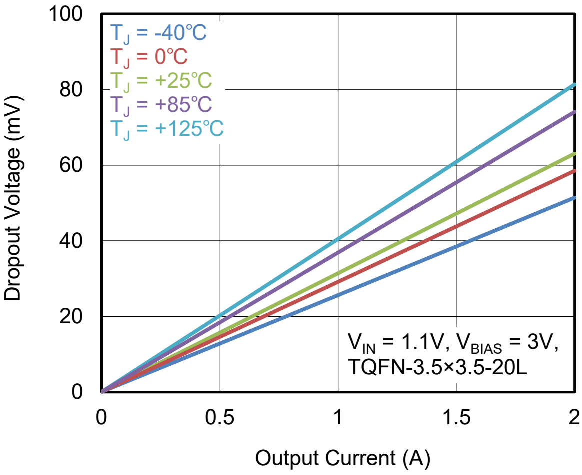
Ground Pin Current vs. Input Voltage



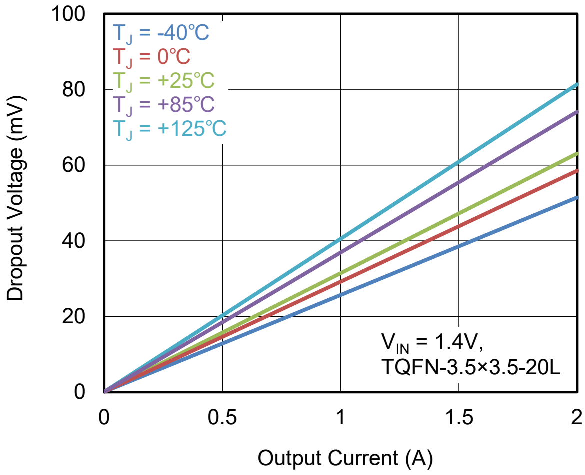
BIAS Pin Current vs. BIAS Voltage



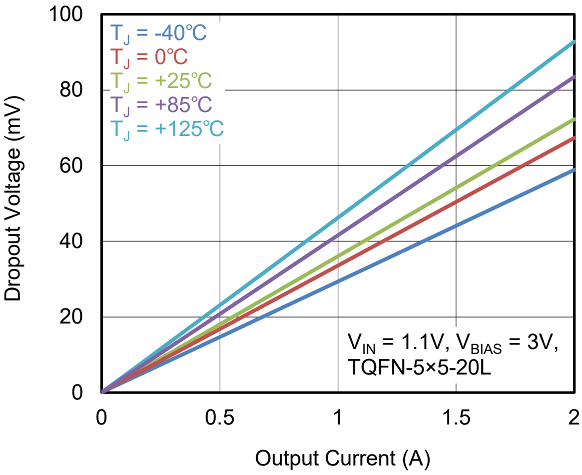
Dropout Voltage vs. Output Current with BIAS



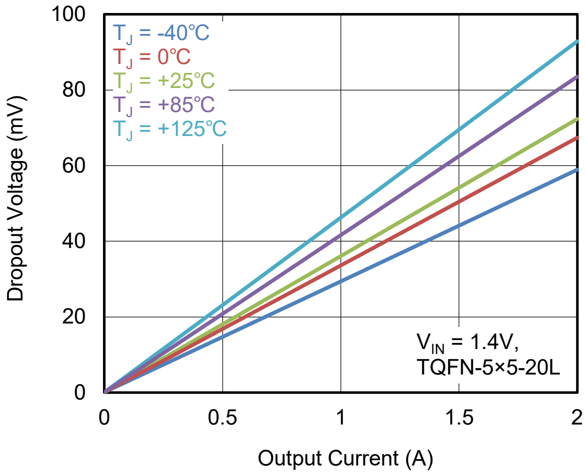
Dropout Voltage vs. Output Current without BIAS



Dropout Voltage vs. Output Current with BIAS



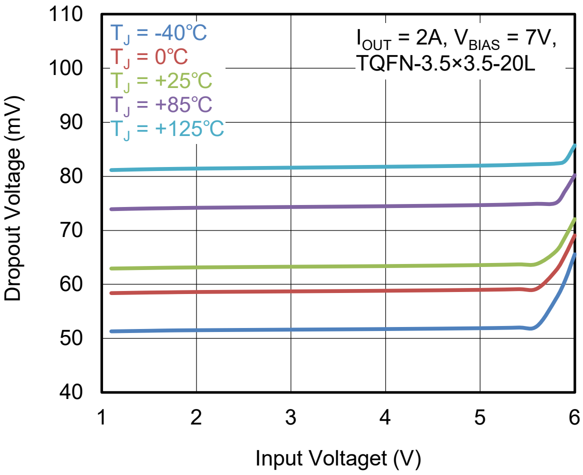
Dropout Voltage vs. Output Current without BIAS



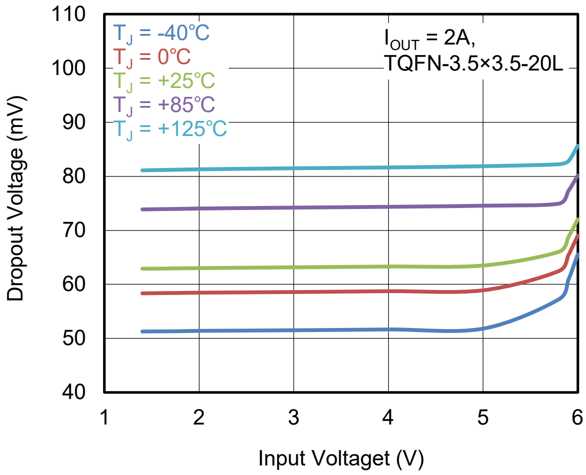
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.4V) or 1.4V (whichever is greater), V_{BIAS} = Open, $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1.1V, C_{IN} =10μF, C_{OUT} = 22μF, $C_{NR/SS}$ = 0nF, no C_{FF}, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

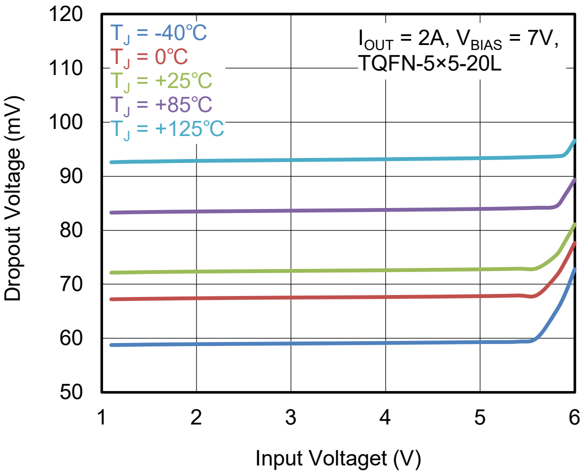
Dropout Voltage vs. Input Voltage with BIAS



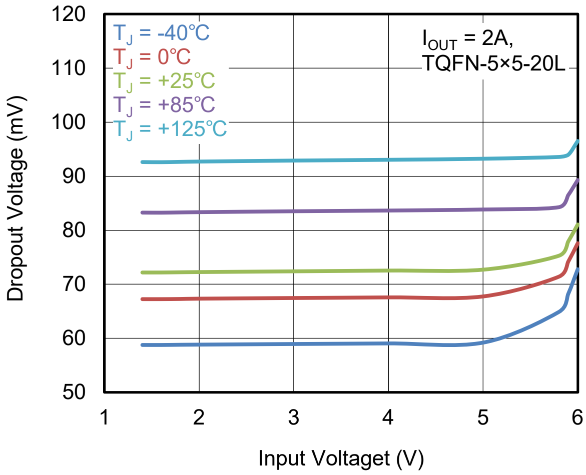
Dropout Voltage vs. Input Voltage without BIAS



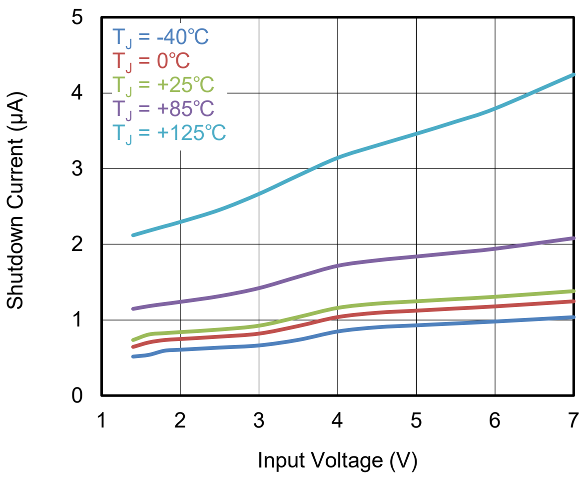
Dropout Voltage vs. Input Voltage with BIAS



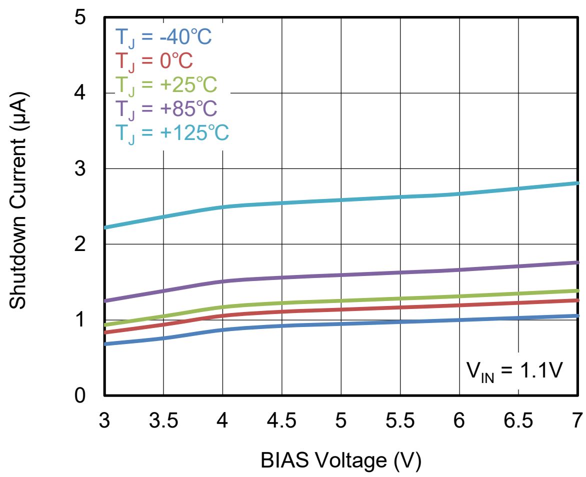
Dropout Voltage vs. Input Voltage without BIAS



Shutdown Current vs. Input Voltage

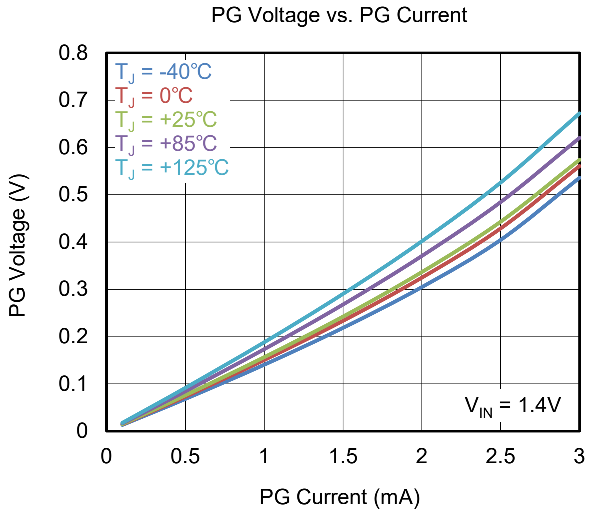


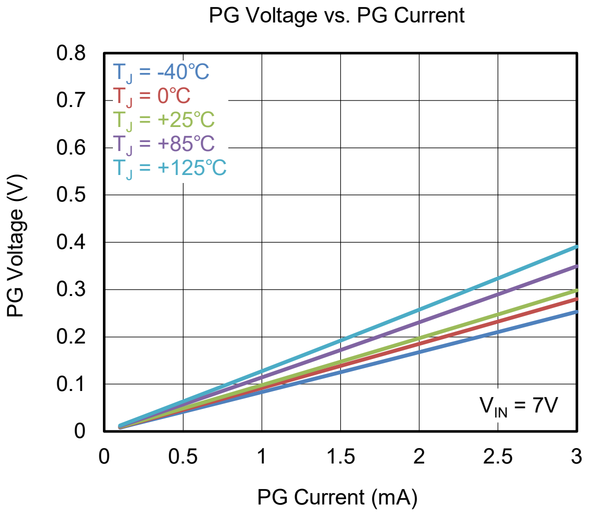
Shutdown Current vs. BIAS Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.4V) or 1.4V (whichever is greater), V_{BIAS} = Open, $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1.1V, C_{IN} =10μF, C_{OUT} = 22μF, $C_{NR/SS}$ = 0nF, no C_{FF}, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.





FUNCTIONAL BLOCK DIAGRAM

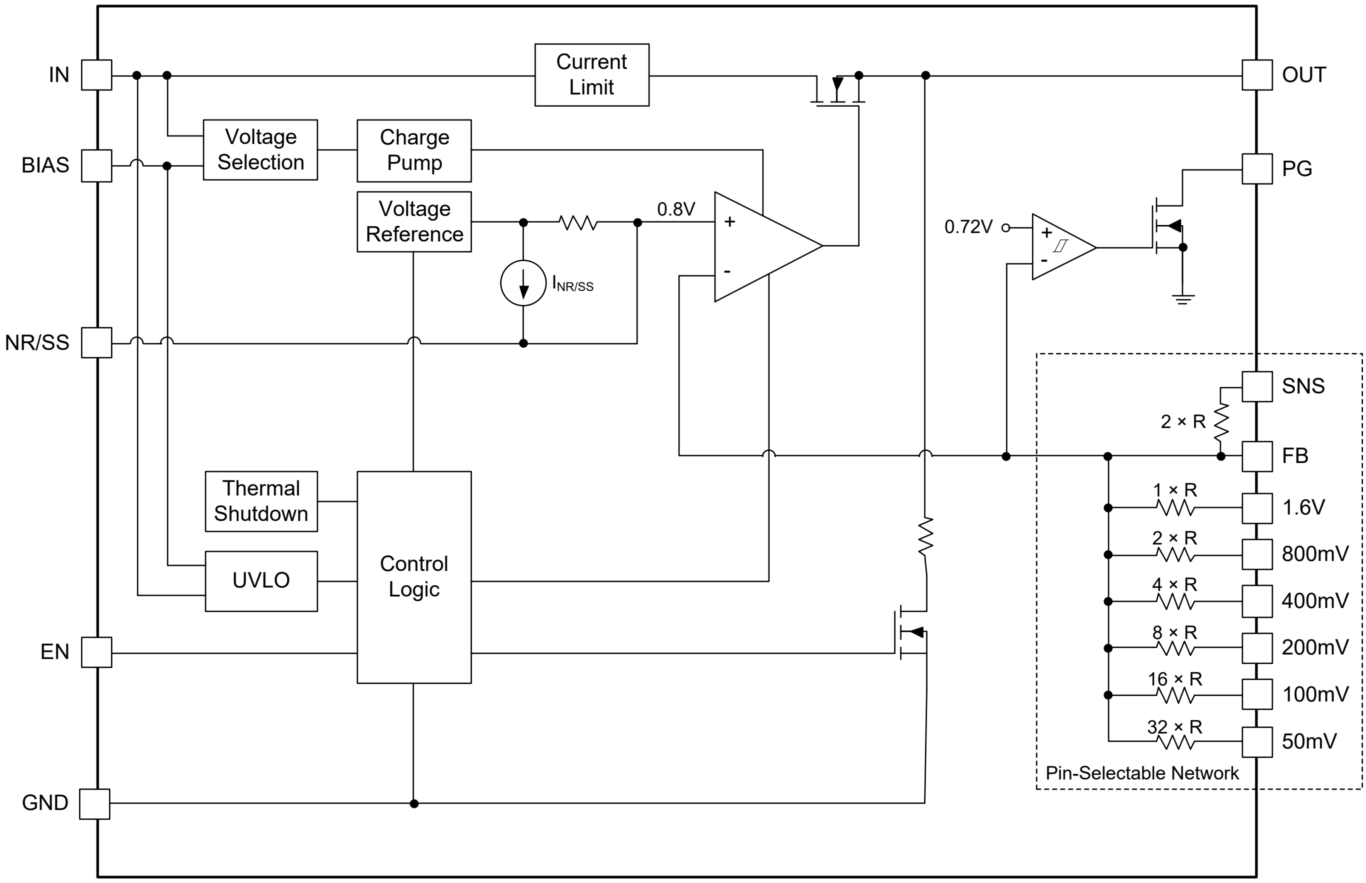


Figure 2. Block Diagram

APPLICATION INFORMATION

The SGM2049 is a high accuracy, low noise, fast transient response high performance LDO, it provides 2A output current. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply. The high performance also makes the SGM2049 useful in a variety of applications. The SGM2049 provides the protection functions for output overload, output short -circuit condition and overheating.

The SGM2049 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown current consumes as low as 1.4μA (TYP).

Input Capacitor Selection (C_{IN}, C_{BIAS})

The input decoupling capacitor should be placed as close as possible to the IN pin and BIAS pin for ensuring the device stability. C_{IN} = 10μF/C_{BIAS} = 5μF or larger X7R or X5R ceramic capacitors are selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

Output Capacitor Selection (C_{OUT})

The output capacitor should be placed as close as possible to the OUT pin. 10μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of C_{OUT} that SGM2049 can remain stable is 10μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of C_{OUT} must be considered in design. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Noise-Reduction and Soft-Start Capacitor Selection ($C_{NR/SS}$)

The SGM2049 is designed for a programmable, monotonic soft-start time of output rising, and it can be achieved via an external capacitor ($C_{NR/SS}$) on the NR/SS pin. Using an external $C_{NR/SS}$ is recommended for general application. It not only minimizes the inrush current but also helps reduce the noise component from internal reference.

Adjustable Output Voltage

The SGM2049 can be set either with the internal pin-selectable network or by connecting with external resistors to achieve different output voltages. When the output voltage range is from 0.8V to 3.95V, the SGM2049 can be programmed by using the pin-selectable network. When the output voltage range is greater than 3.95V and up to 5.2V, external resistors must be used as shown in Figure 3. The output voltage is determined by the following equation:

$$V_{OUT} = 0.8V \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

One parallel capacitor (C_{FF} = 10nF) with R_1 can be used to improve the feedback loop stability and PSRR, increase the transient response and reduce the output noise. Use an R_1 approximately 12kΩ to maintain a 5μA minimum load.

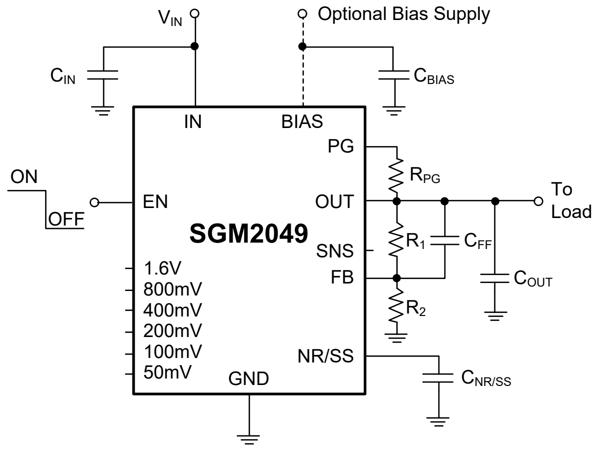


Figure 3. Adjustable Output Voltage Application

APPLICATION INFORMATION (continued)

Pin-Selectable Programmable Output Voltage

Pin-selectable programmable output voltage is achieved with the pin-selectable resistors via pin 2 and pins 5 to 11. Each pin can be grounded (active) or floating (open) or connected to the SNS pin. Pin-selectable programming is set as the internal reference voltage by Equation 2 plus the accumulated sum of the respective voltages assigned to each active pin. Table 1 shows these voltage values related to each active pin setting for reference.

$$V_{OUT} = 0.8V + (\Sigma \text{ Pin-Selectable Pins to Ground}) \quad (2)$$

Table 1. Pin-Selectable Programmable Output Voltage

Pin-Selectable Program Pins (Active Low)	Additive Output Voltage Level
Pin 5 (50mV)	50mV
Pin 6 (100mV)	100mV
Pin 7 (200mV)	200mV
Pin 9 (400mV)	400mV
Pin 10 (800mV)	800mV
Pin 11 (1.6V)	1.6V

The output voltage is set according to Equation 1 as for the adjustable operation, but R_1 and R_2 are internally integrated and matched for higher accuracy. By reducing the value of R_1 and connecting any of the pin-selectable pins to the SNS pin, the resolution of the internal feedback network can be improved.

Enable Control

The EN pin of the SGM2049 is used to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than $V_{IL(EN)}$, the device is in shutdown state, there is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 260Ω (TYP) resistor.

When the EN pin voltage is higher than $V_{IH(EN)}$, the device is in active state, the input voltage is regulated to the output voltage and the automatic discharge transistor is turned off.

Reverse Current Protection

The pass transistor has an inherent body diode which will be forward biased in the case when $V_{OUT} > (V_{IN} + 0.3V)$. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

Negatively Biased Output

When the output voltage is negative, the chip may not start up due to parasitic effects. Ensure that the output is greater than -0.3V under all conditions. If negatively biased output is excessive and expected in the application, a Schottky diode can be added between the OUT pin and GND pin.

Output Current Limit and Short-Circuit Protection

When overload events happen, the output current is internally limited to 3.2A (TYP). When the OUT pin is shorted to ground, the short-circuit protection will limit the output current to 1.7A (TYP).

Thermal Shutdown

The SGM2049 can detect the temperature of die. When the die temperature exceeds the threshold value of thermal shutdown, the SGM2049 will be in shutdown state and it will remain in this state until the die temperature decreases to +140℃.

Power Dissipation (P_D)

Thermal protection limits power dissipation in the SGM2049. When power dissipation on pass element ($P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$) is too much and the operating junction temperature exceeds +165℃, the OTP circuit starts the thermal shutdown function and turns the pass element off.

Therefore, thermal analysis for the chosen application is important to guarantee reliable performance over all conditions. To guarantee reliable operation, the junction temperature of the SGM2049 must not exceed +125℃.

The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction temperature and ambient temperature. The maximum power dissipation can be approximated using the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (3)$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

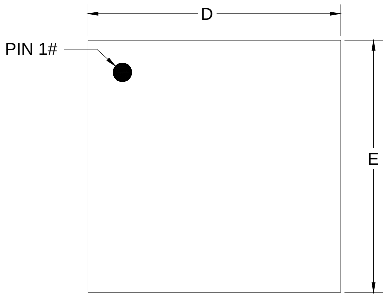
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

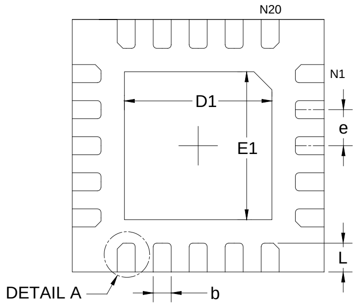
Changes from Original (DECEMBER 2021) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

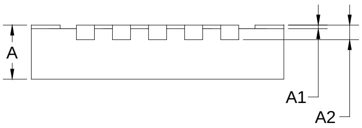
TQFN-3.5×3.5-20L



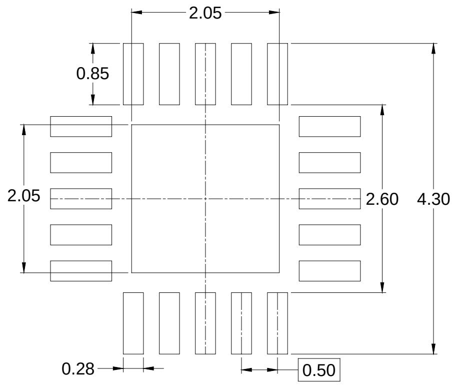
TOP VIEW



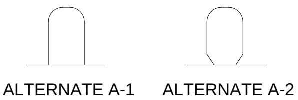
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



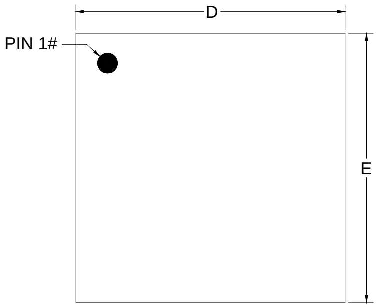
DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	-	-	0.050
A2	0.203 REF		
D	3.450	3.500	3.550
D1	2.000	2.050	2.100
E	3.450	3.500	3.550
E1	2.000	2.050	2.100
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.350	0.400	0.450

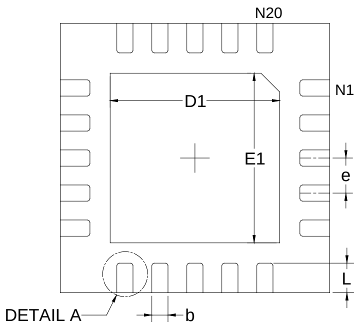
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

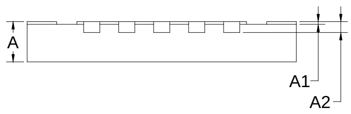
TQFN-5×5-20L



TOP VIEW

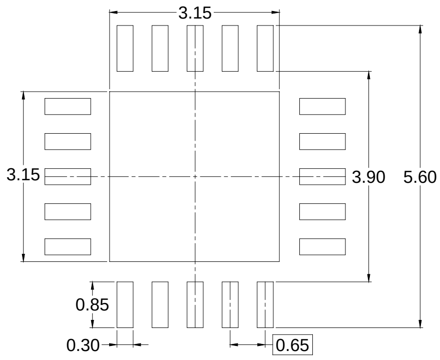


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL
CONSTRUCTION



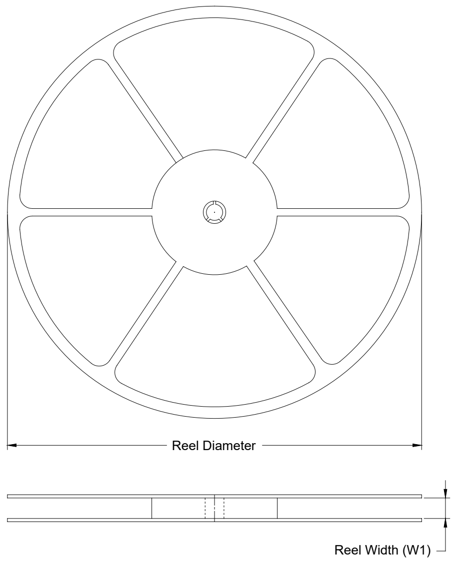
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	**MOD**	**MAX**
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
D	4.950	5.000	5.050
D1	3.100	3.150	3.200
E	4.950	5.000	5.050
E1	3.100	3.150	3.200
b	0.250	0.300	0.350
e	0.650 BSC		
L	0.500	0.550	0.600

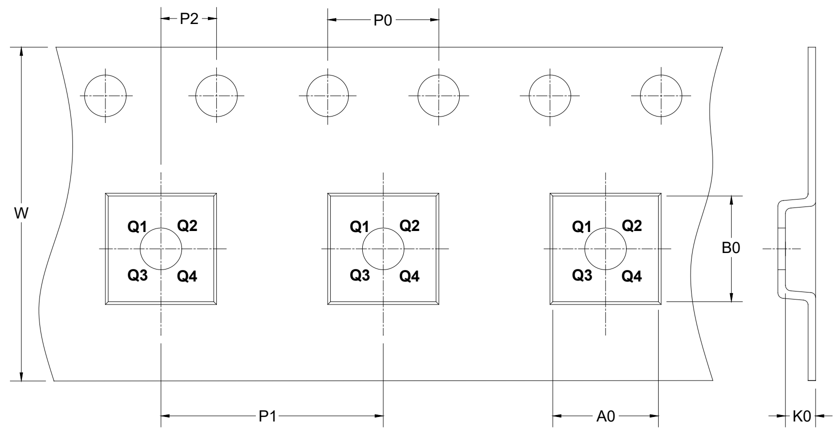
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

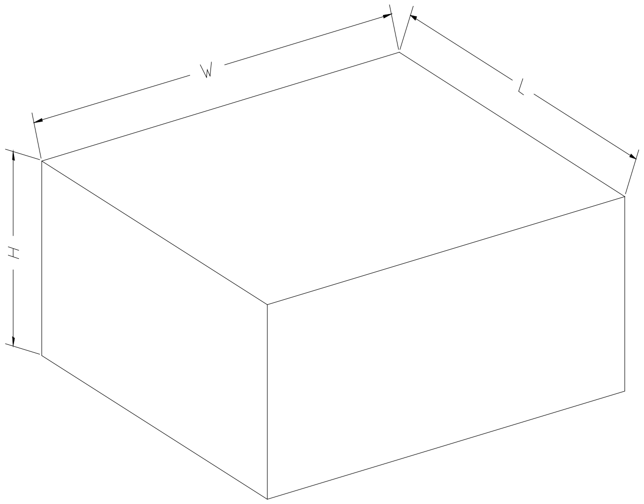
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×3.5-20L	13″	12.4	3.80	3.80	0.95	4.0	8.0	2.0	12.0	Q2
TQFN-5×5-20L	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002