SGM61024
2.4V to 5.5V, 2A Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61024 is a high frequency synchronous Buck converter with an input voltage range from 2.4V to 5.5V and a wide output current range, optimized for compact solutions. For SGM61024A, to keep the high efficiency in the whole load range, the device operates in pulse width modulation (PWM) mode at normal load and automatically enters the power-save mode (PSM) at light loads. The minimum static current is only 5.7μA to maintain its high efficiency. For SGM61024B, the device operates in force PWM mode at light and heavy loads.

With its adaptive hysteresis and pseudo-constant on-time control (AHP-COT) architecture, the load transient performance is excellent and the output voltage regulation accuracy is achieved.

The device is available in a Green UTDFN-1.5×1.5-6L package.

FEATURES

- **AHP-COT Architecture for Fast Transient Regulation**
- **2.4V to 5.5V Input Voltage Range**
- **2A Output Current**
- **0.6V to 4V Wide Output Voltage Range**
- **Low Quiescent Current: 5.7μA (SGM61024A)**
- **100% Duty Cycle for the Lowest Dropout**
- **Output Discharge Function**
- **Power Good Output**
- **Thermal Shutdown**
- **Power-Save Mode at Light Loads: SGM61024A**
- **Force PWM Mode: SGM61024B**
- **Hiccup Short-Circuit Protection**
- **Available in a Green UTDFN-1.5×1.5-6L Package**

APPLICATIONS

Battery-Powered Applications
Point-of-Load
Processor Power Supplies
Hard Disk Drives (HDD)/Solid State Drives (SSD)

TYPICAL APPLICATION

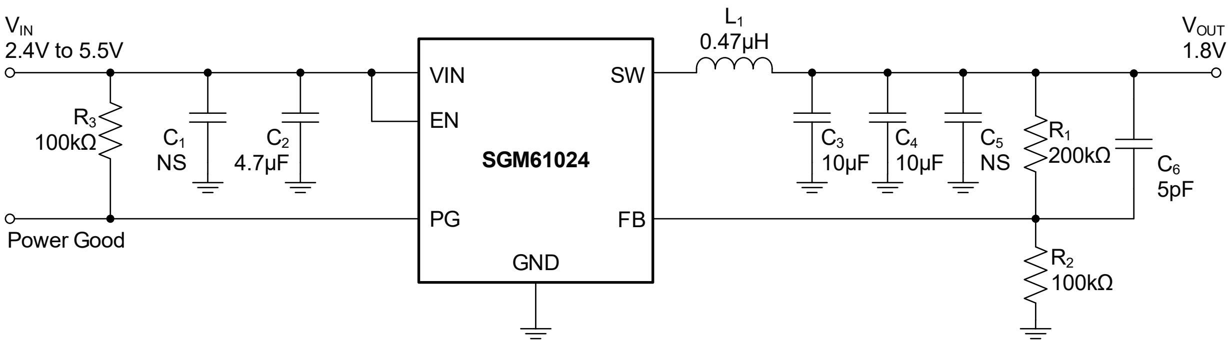


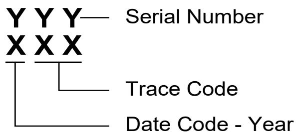
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61024A	UTDFN-1.5×1.5-6L	-40℃ to +125℃	SGM61024AXUGJ6G/TR	04W XXX	Tape and Reel, 4000
SGM61024B	UTDFN-1.5×1.5-6L	-40℃ to +125℃	SGM61024BXUGJ6G/TR	04X XXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltages Referred to GND
- VIN, FB, EN, PG .... -0.3V to 6V
- SW (DC) .... -0.3V to V_{IN} + 0.3V
- SW (AC, Less than 10ns) .... -2.5V to 10V

Package Thermal Resistance
- UTDFN-1.5×1.5-6L, θ_{JA} .... 117.4℃/W
- UTDFN-1.5×1.5-6L, θ_{JB} .... 21.5℃/W
- UTDFN-1.5×1.5-6L, θ_{JC} .... 73.2℃/W

Junction Temperature .... +150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) .... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} .... 2.4V to 5.5V
Output Voltage Range, V_{OUT} .... 0.6V to 4.0V
Output Current Range, I_{OUT} .... 0A to 2A
Sink Current at PG Pin, I_{SINK_PG} 1mA
Pull-up Resistor Voltage, V_{PG} 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

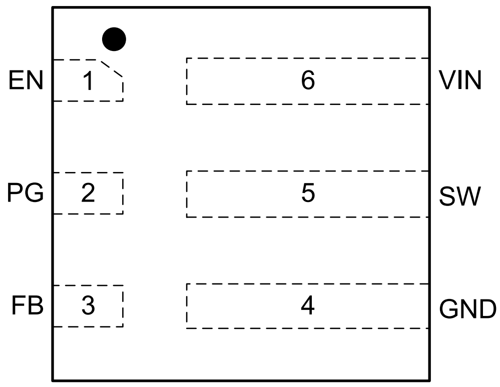
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



UTDFN-1.5×1.5-6L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN	I	Active High Enable Input. Logic high sets the device active. Logic low disables it and turns it into shutdown mode. Do not leave this pin floating.
2	PG	O	Power Good Open-Drain Output. If the output voltage is less than the regulation limit, this pin is pulled low. Leave this pin floating when not in use.
3	FB	I	Feedback Input. An external feedback divider is needed for setting the output voltage.
4	GND	G	Power and Signal Ground.
5	SW	P	Switching Node.
6	VIN	P	Power Supply Voltage Input.

NOTE: I = input, O = output, G = ground, P = power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃ and V_{IN} = 2.4V to 5.5V. Typical values are measured at T_J = +25℃ and V_{IN} = 5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Quiescent Current	I_Q	EN = high, no load, device not switching, SGM61024A		5.7	12	μA
		EN = high, no load, device not switching, SGM61024B		400	500	
Shutdown Current	I_{SD}	EN = low, T_J = -40℃ to +85℃		0.05	1.8	μA
		EN = low, T_J = -40℃ to +125℃			6.5	
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling	2.1	2.2	2.3	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}	V_{IN} rising		160		mV
Thermal Shutdown Threshold	T_{SD}	T_J rising		150		℃
Thermal Shutdown Hysteresis	T_{HYS}	T_J falling		18		℃
Logic Interface EN						
High-Level Threshold Voltage	V_{IH}		1.02			V
Low-Level Threshold Voltage	V_{IL}				0.35	V
Input Leakage Current into EN Pin	I_{EN_LKG}	EN = High		0.01	0.1	μA
Soft-Start, Power Good						
Soft-Start Time	t_{SS}	Time from EN high to 95% of V_{OUT} nominal		1.4		ms
Power Good Lower Threshold	V_{PG}	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	94	96	98.5	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	89	92	94	%
Power Good Upper Threshold		V_{PG} rising, V_{FB} referenced to V_{FB} nominal	102	105	107	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	107	110	112	%
Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA			0.4	V
Input Leakage Current into PG Pin	I_{PG_LKG}	V_{PG} = 5.0V		0.01	0.15	μA
Power Good Deglitch Delay	t_{PG_DLY}	PG rising edge		100		μs
		PG falling edge		18		
Output						
Feedback Regulation Voltage	V_{FB}	PWM mode, V_{IN} = 5V, T_J = +25℃	594	600	606	mV
		PWM mode, V_{IN} = 5V, T_J = -20℃ to +85℃	591		609	
		PWM mode	588		612	
Feedback Input Leakage Current	$I_{FB,LKG}$	V_{FB} = 0.6V		0.01	0.05	μA
Output Discharge Current	I_{DIS}	V_{SW} = 0.4V, EN = Low	33	77		mA
Power Switch						
High-side FET On-Resistance	R_{DSON}			34	82	mΩ
Low-side FET On-Resistance				24	54	
High-side FET Switch Current Limit, DC	I_{LIM}		2.8	4.4	5.6	A
Low-side FET Current Limit, DC			2.4	3.5	4.9	
Low-side FET Negative Current Limit, DC	I_{LIM}			-1.6		A
PWM Switching Frequency	f_{SW}	I_{OUT} = 1A, V_{OUT} = 1.8V		2.2		MHz

SYSTEM CHARACTERISTICS

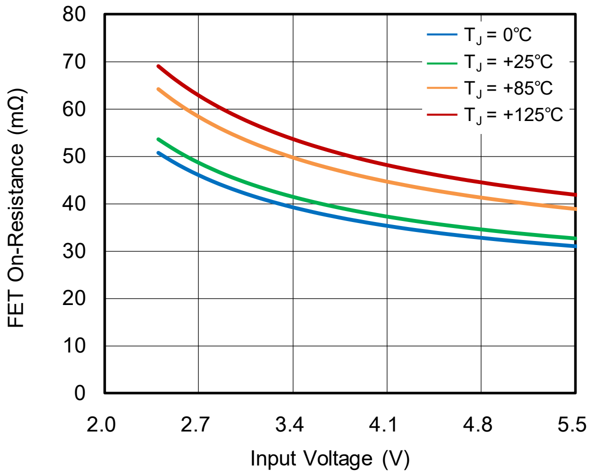
(T_J = 0℃ to +85℃ and V_{IN} = 3.3V. All typical values are measured at T_J = +25℃ and V_{IN} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN (1)	TYP	MAX (1)	UNITS
EN Delay Time	t_{DELAY_EN}	V_{IN} = 3.3V, time from EN high to the first SW pulse	85	270	465	μs
Startup Time	$t_{STARTUP}$	V_{IN} = 3.3V, time from the first SW pulse to 95% of VOUT nominal	500	1050	1550	μs
Switching Frequency	f_{SW}	V_{IN} =3.3V, V_{OUT} = 1.2V, CCM	1.6	2.2	2.7	MHz
		V_{IN} =3.3V, V_{OUT} = 0.85V, CCM	1.5	2	2.6	MHz

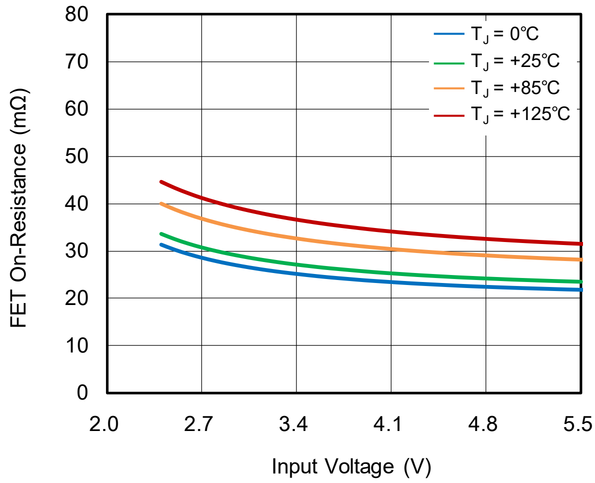
NOTE: 1. These parameters are specified by design and characterization, not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

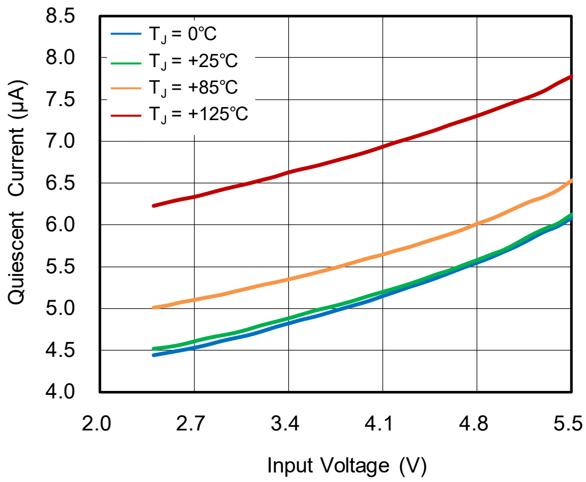
High-side FET R_{DSON} vs. Input Voltage



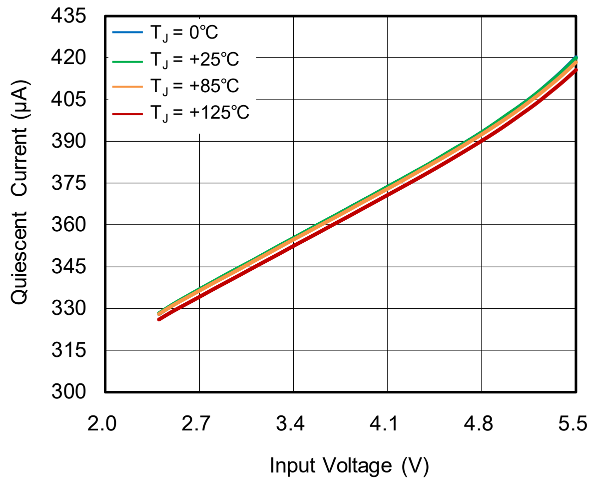
Low-side FET R_{DSON} vs. Input Voltage



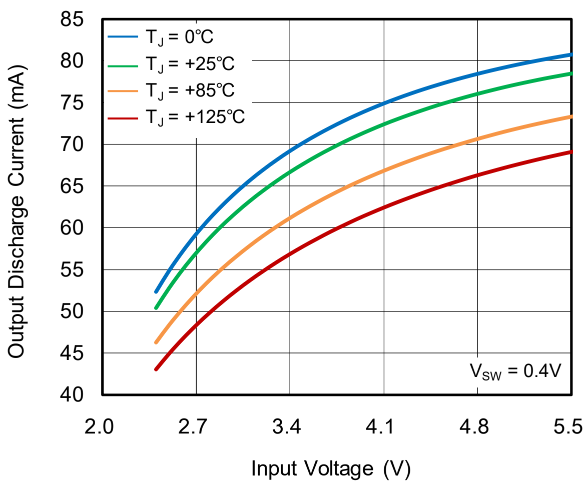
Quiescent Current vs. Input Voltage (SGM61024A)



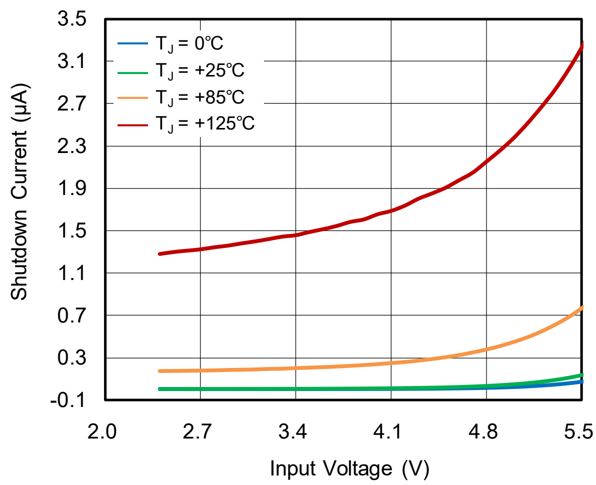
Quiescent Current vs. Input Voltage (SGM61024B)



Output Discharge Current vs. Input Voltage



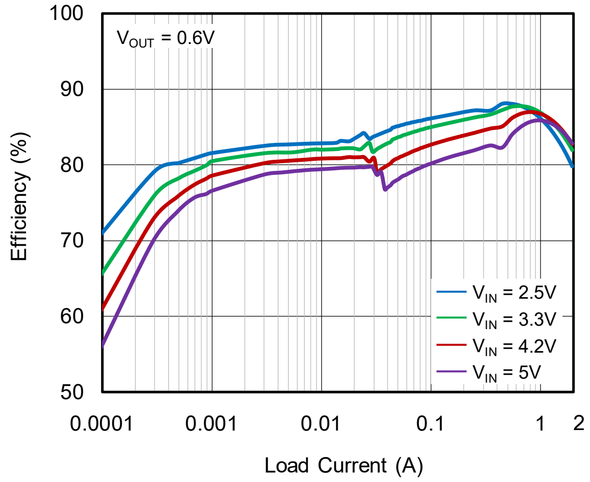
Shutdown Current vs. Input Voltage



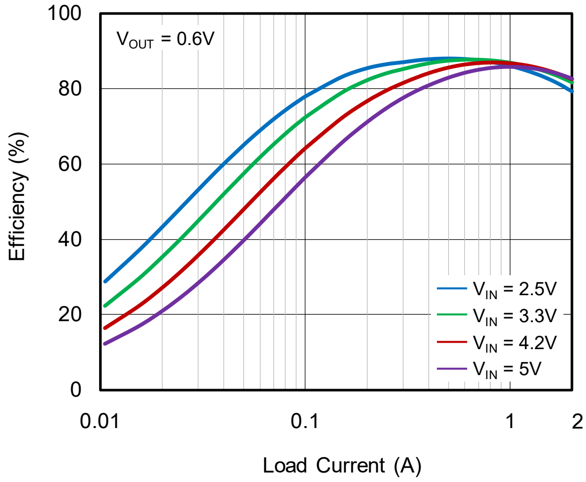
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.47μH, and C_{OUT} = 2 × 10μF, unless otherwise noted.

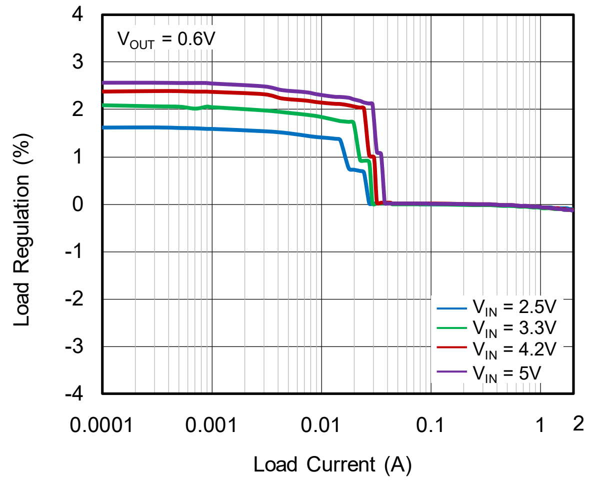
Efficiency vs. Load Current (SGM61024A)



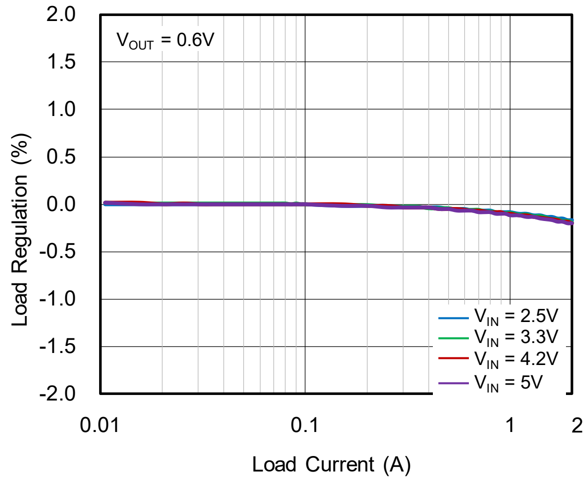
Efficiency vs. Load Current (SGM61024B)



Load Regulation (SGM61024A)



Load Regulation (SGM61024B)



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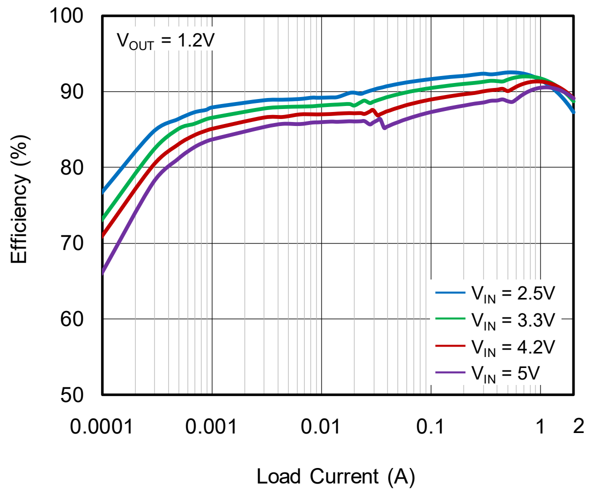

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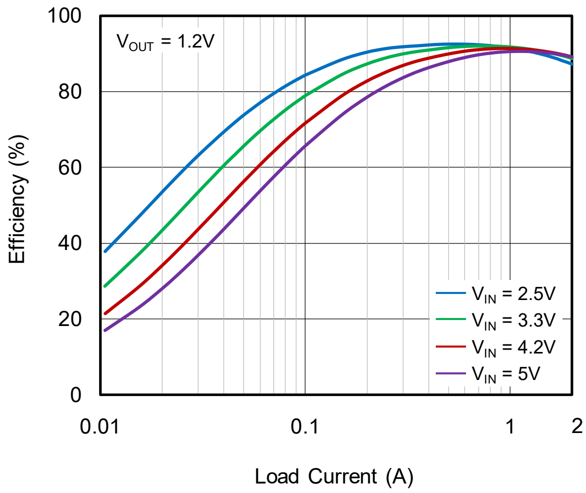

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V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.47μH, and C_{OUT} = 2 × 10μF, unless otherwise noted.

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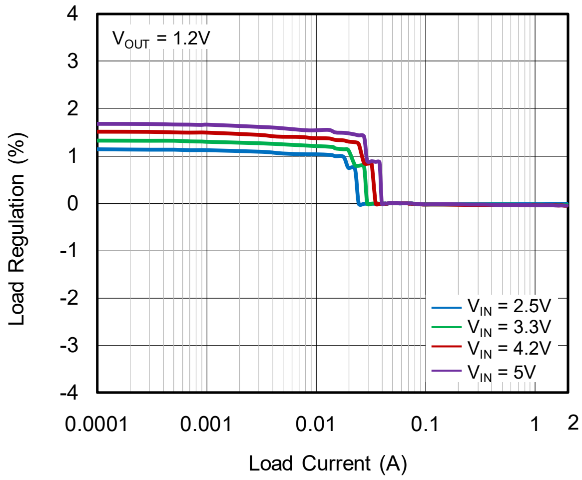

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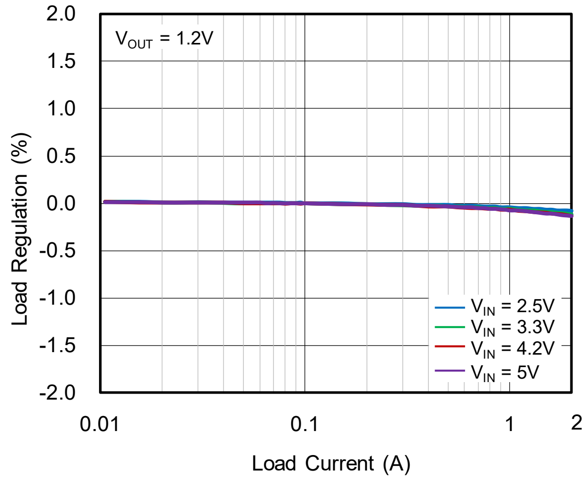

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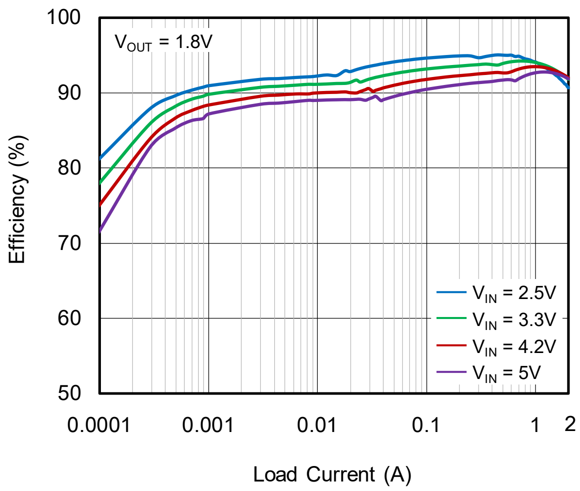

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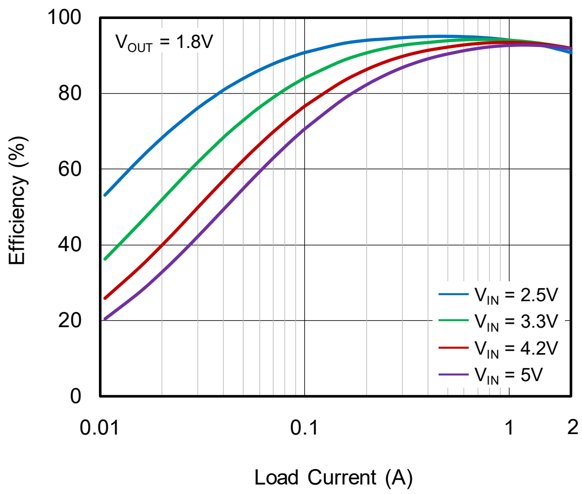

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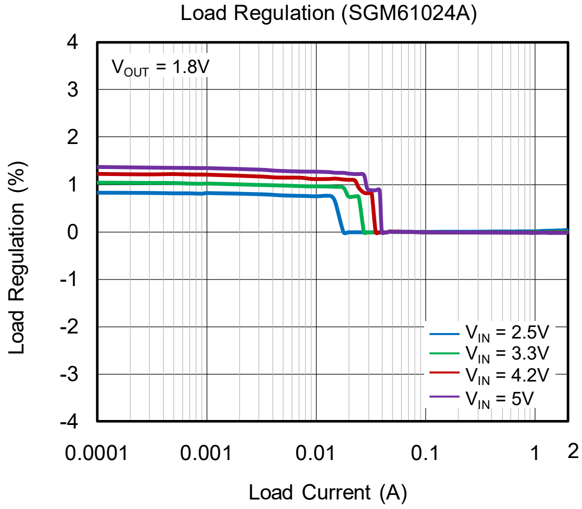

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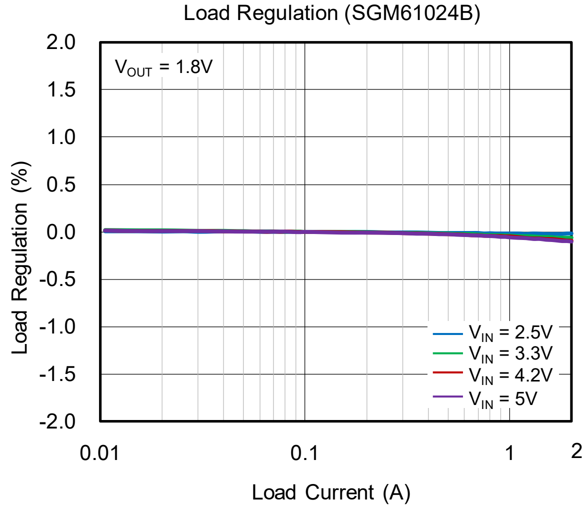
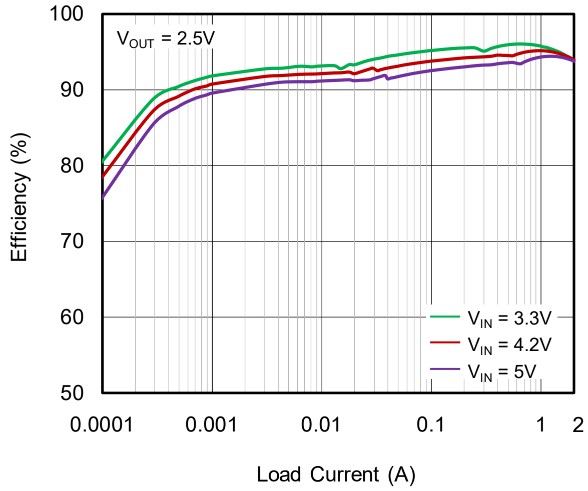


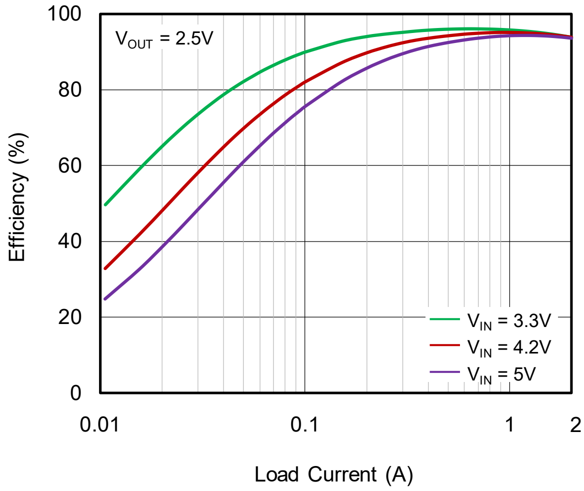
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.47μH, and C_{OUT} = 2 × 10μF, unless otherwise noted.

Efficiency vs. Load Current (SGM61024A)



Efficiency vs. Load Current (SGM61024B)



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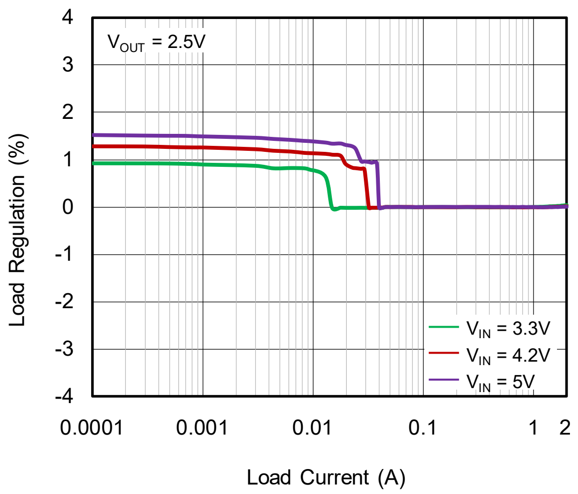

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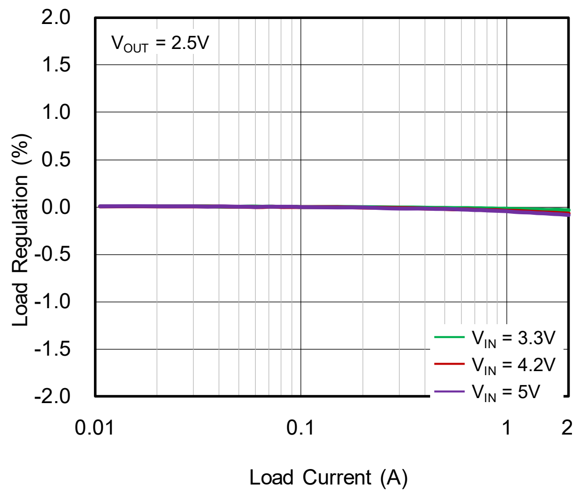
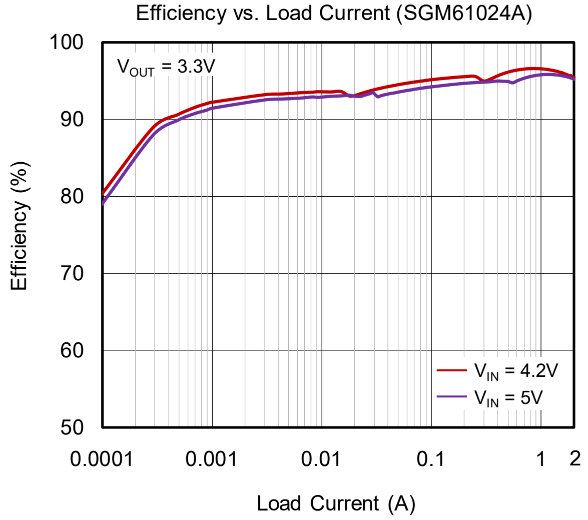
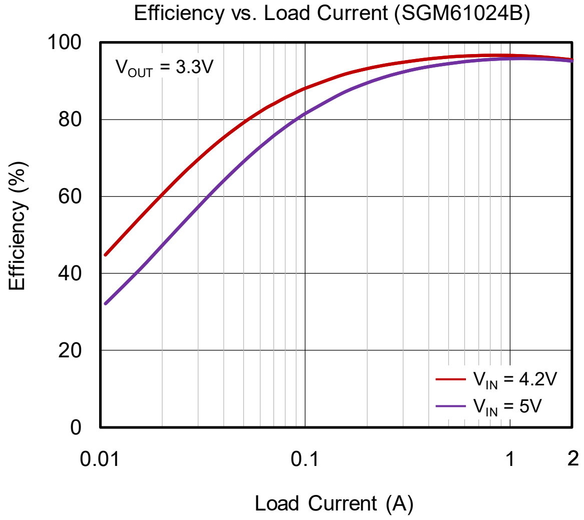


Efficiency vs. Load Current (SGM61024A)



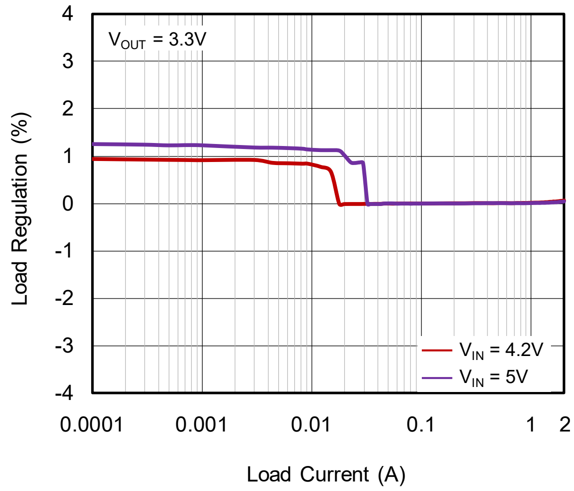
Efficiency vs. Load Current (SGM61024B)



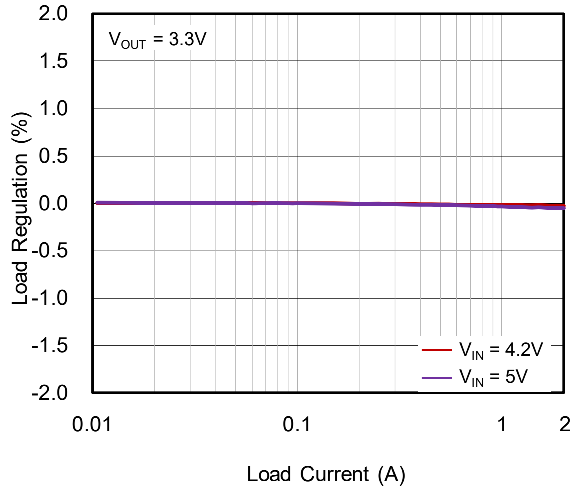
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.47μH, and C_{OUT} = 2 × 10μF, unless otherwise noted.

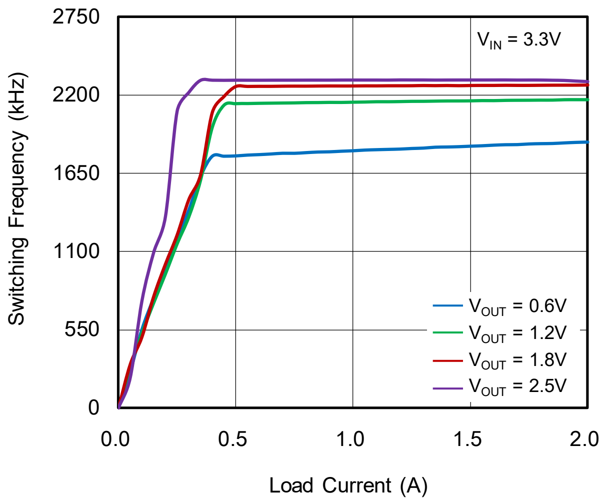
Load Regulation (SGM61024A)



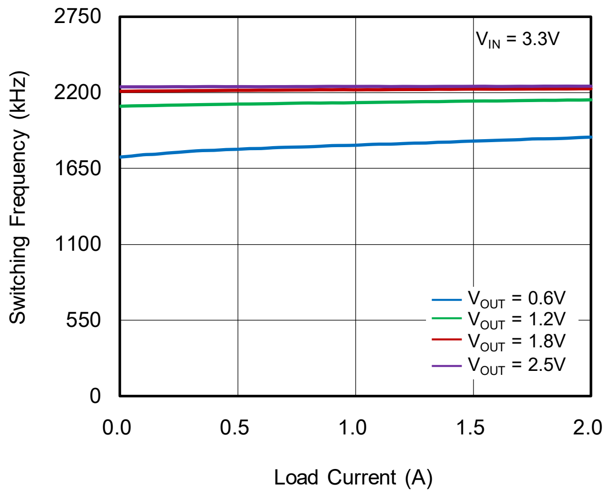
Load Regulation (SGM61024B)



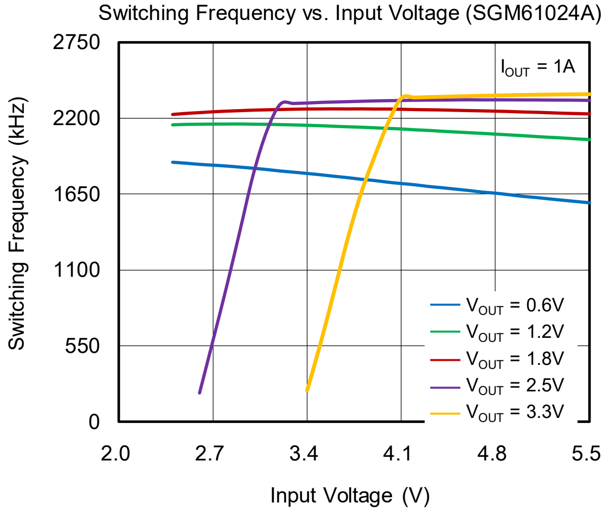
Switching Frequency vs. Load Current (SGM61024A)



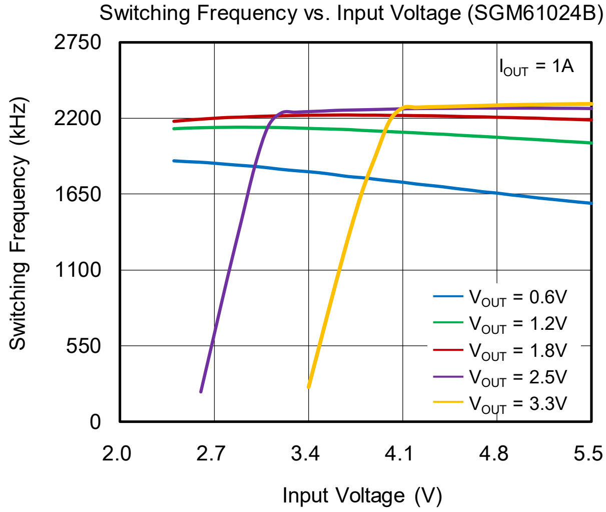
Switching Frequency vs. Load Current (SGM61024B)



Switching Frequency vs. Input Voltage (SGM61024A)



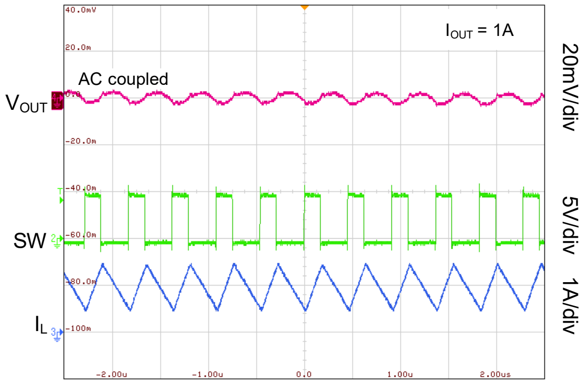
Switching Frequency vs. Input Voltage (SGM61024B)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

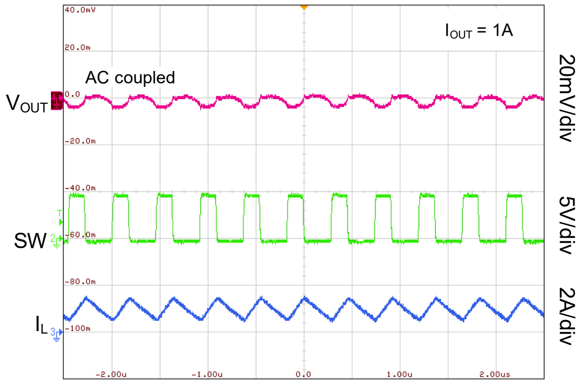
V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.47μH, and C_{OUT} = 2 × 10μF, unless otherwise noted.

PWM Operation (SGM61024A)



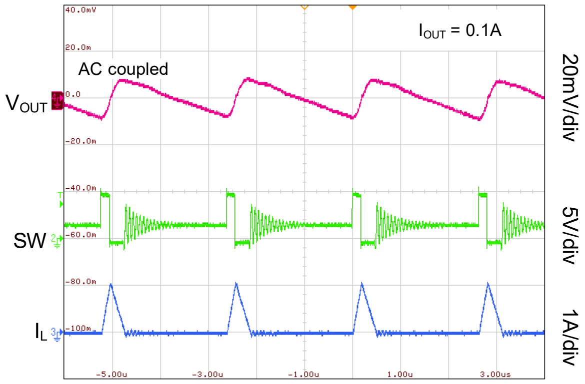
Time (500ns/div)

PWM Operation (SGM61024B)



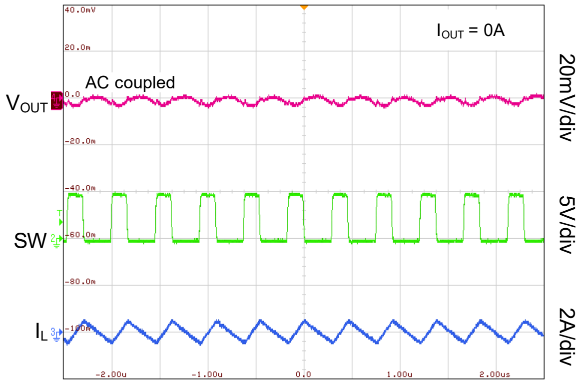
Time (500ns/div)

PSM Operation (SGM61024A)



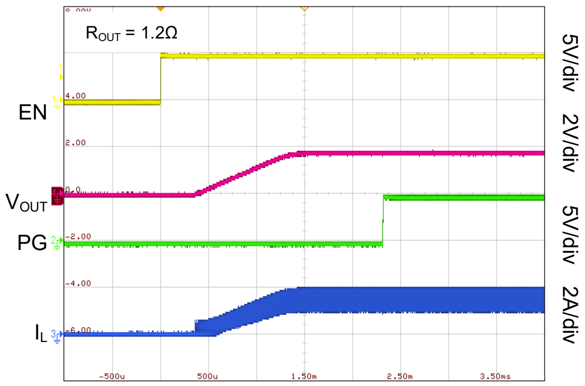
Time (1μs/div)

PWM Operation (SGM61024B)



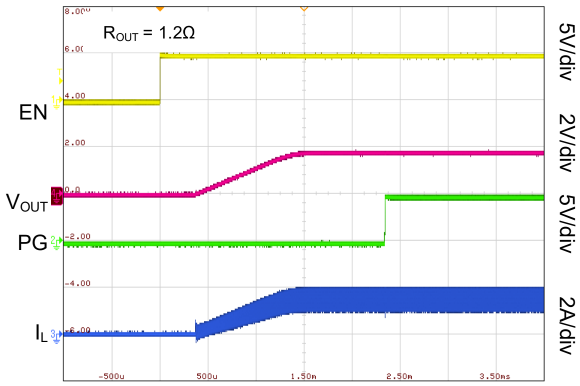
Time (500ns/div)

Startup with Load (SGM61024A)



Time (500μs/div)

Startup with Load (SGM61024B)

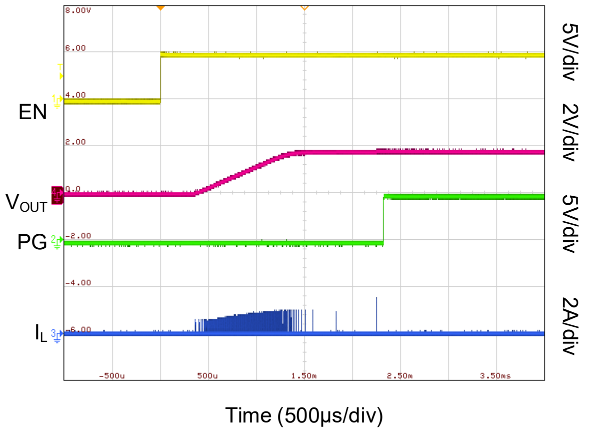


Time (500μs/div)

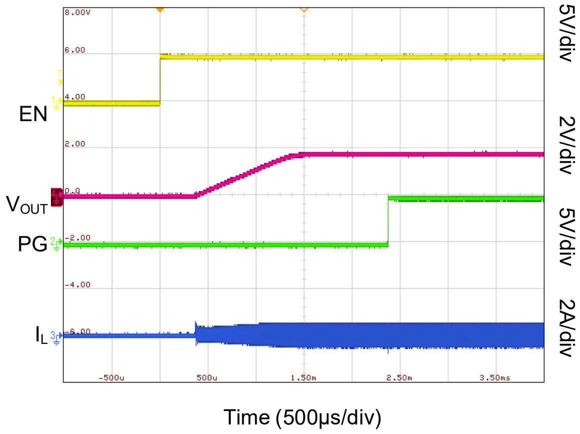
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.47μH, and C_{OUT} = 2 × 10μF, unless otherwise noted.

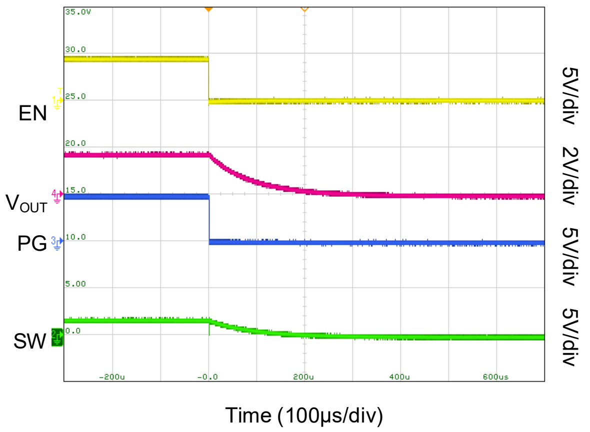
Startup with No Load (SGM61024A)



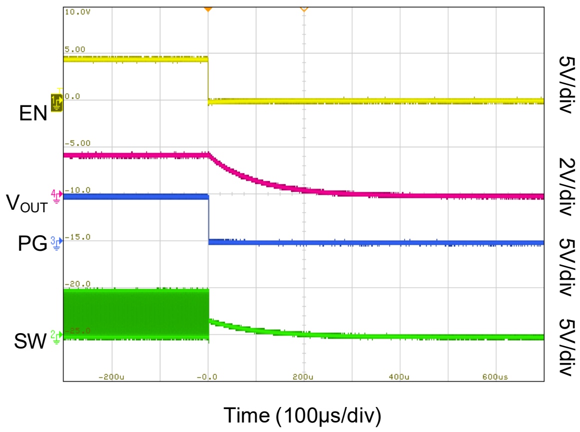
Startup with No Load (SGM61024B)



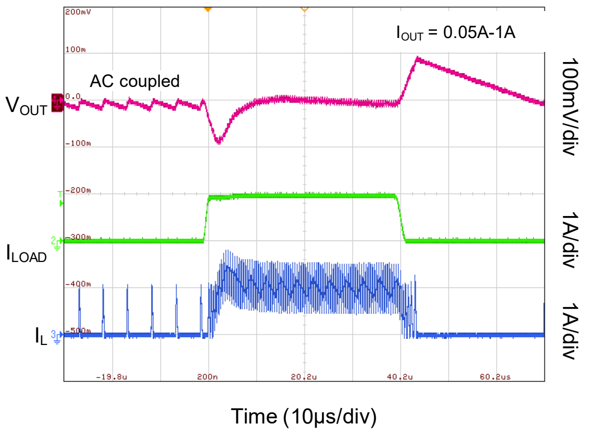
Disable with No Load (SGM61024A)



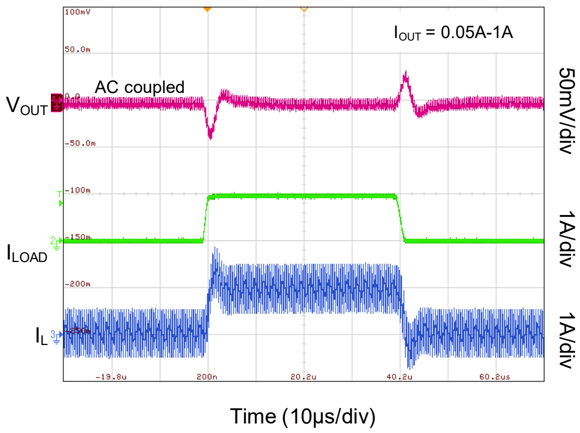
Disable with No Load (SGM61024B)



Load Transient (SGM61024A)



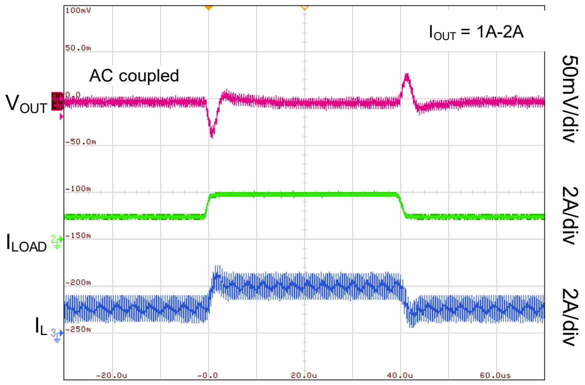
Load Transient (SGM61024B)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

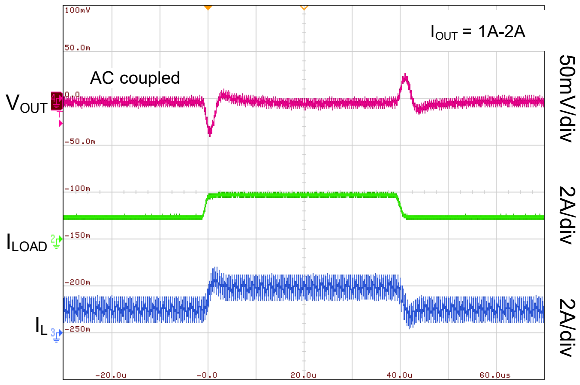
V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.47μH, and C_{OUT} = 2 × 10μF, unless otherwise noted.

Load Transient (SGM61024A)



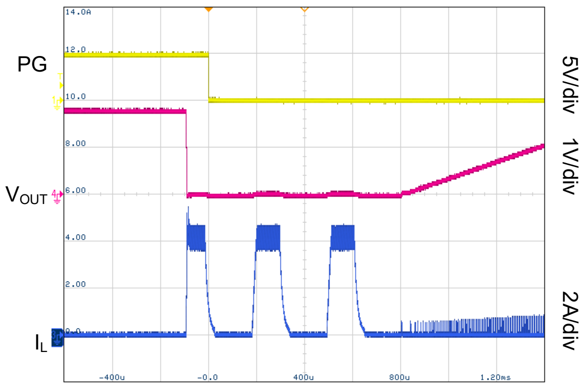
Time (10μs/div)

Load Transient (SGM61024B)



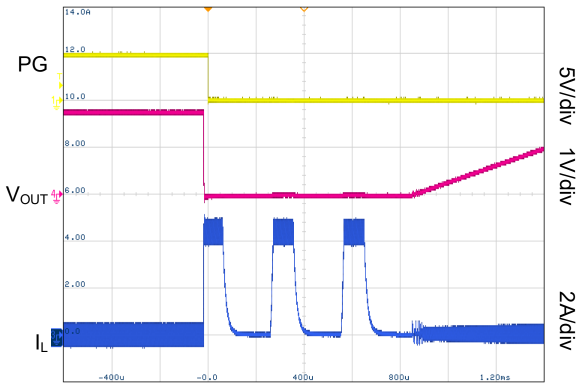
Time (10μs/div)

Hiccup (SGM61024A)



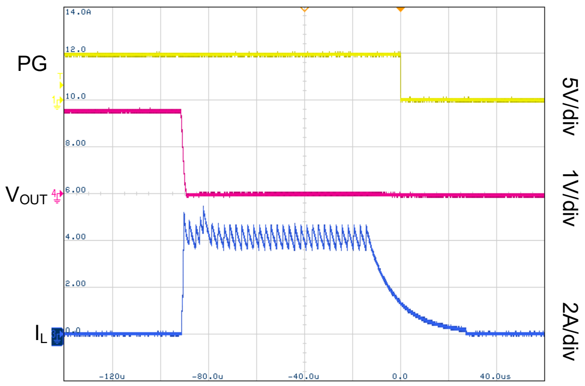
Time (200μs/div)

Hiccup (SGM61024B)



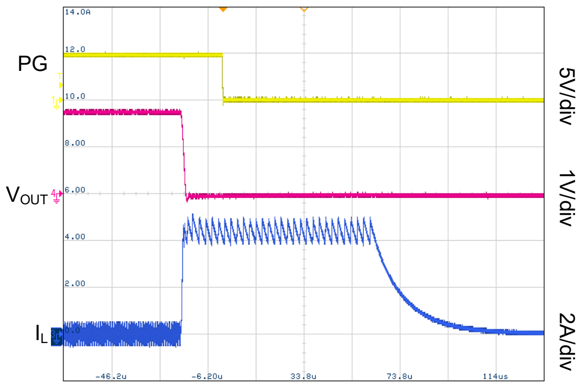
Time (200μs/div)

Hiccup Zoom In (SGM61024A)



Time (20μs/div)

Hiccup Zoom In (SGM61024B)



Time (20μs/div)

FUNCTIONAL BLOCK DIAGRAM

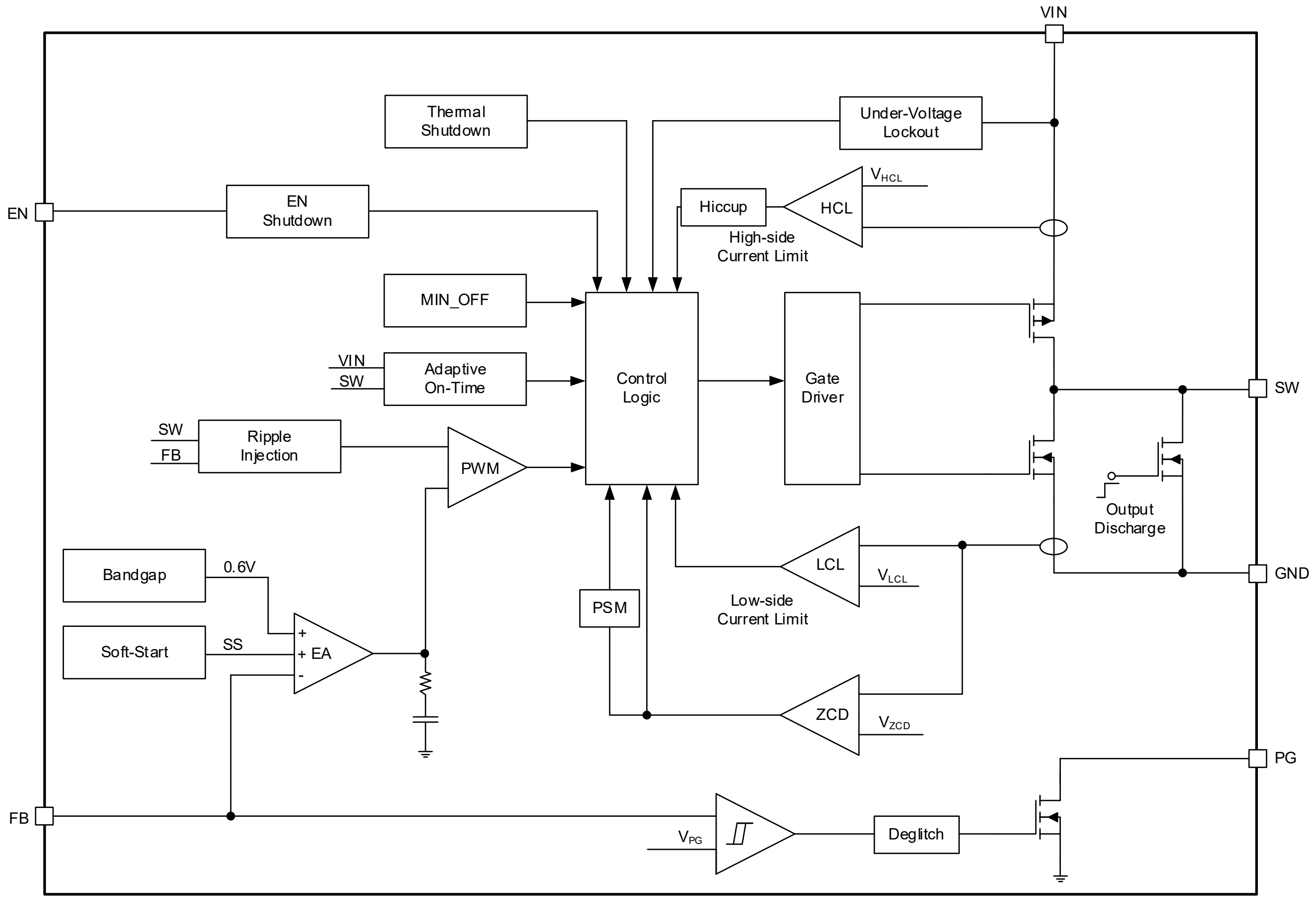


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

SGM61024 is a high frequency synchronous Buck converter with AHP-COT architecture and advanced regulation topology.

For SGM61024A, the device works in pulse width modulation (PWM) mode at medium to heavy loads. When the load current falls, it transitions seamlessly from PWM mode to pulse frequency modulation (PFM) once the inductor current becomes discontinuous. At lighter load conditions, it shifts to the power-save mode (PSM) to minimize the losses. It also shuts down most of the internal circuits in power-save mode. In this mode, one or few PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal value again and the switches will be turned off. In power-save mode, the output voltage is slightly higher than nominal output voltage. For SGM61024B, the device works in force PWM mode at full load range. In PWM mode, the device works with a nominal switching frequency of 2.2MHz.

Under-Voltage Lockout (UVLO)

The device implements the under-voltage lockout (UVLO) with a 160mV hysteresis. When the input voltage falls below the V_{UVLO}, it shuts down the device.

Device Enable and the Output Discharge FET

When the input voltage is valid, pulling the EN input to logic high to enable the device and pulling it low to shut it down. In the shutdown mode, the switches and all control circuits are turned off to reduce the device current to 0.05μA. During shutdown, an internal FET is turned on and connects the SW pin to the GND for smooth discharge of the output.

Soft-Start and Pre-biased Startup

When EN is set to logic high and after internal delay, the device starts switching and V_{OUT} increases with 1.4ms internal soft-start circuit. The soft-start is critical to prevent excessive inrush currents and to avoid triggering of the output over-current protection to provide a smooth output rise. It also prevents extreme input voltage drops due to large inrush current over the high-impedance batteries and input sources that can interrupt the power-up. The device is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turned on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off period and the device must restart under pre-biased output condition. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value. Without the pre-biased capability, the device may not be able to start up properly.

Power Good (PG)

There is the PG function inside the device. PG is an open-drain output with 1mA sinking capability. This pin should be pulled up with an external resistor to a logic high rail which is no more than 5.5V unless it is not used. The PG signal is in high-impedance state when the output voltage is in regulation range. Table 1 shows how the PG state is changed in different conditions. PG remains low until V_{OUT} comes up to 96% to 105% of its nominal (set) value. PG function has hysteresis effect. When PG is high, it will go low if V_{OUT} changes down to 92% or up to 110% of its nominal (set) value. When the device is disabled, under-voltage lockout or in thermal shutdown, the PG pin is driven to low.

The PG output is useful for power supply sequencing as well. Usually, the multiple power rails of a system need to be powered in a specific sequence for proper startup. The PG output of the leading power supply is connected to the EN input of the subsequent power supply to implement such sequencing. If not used, the PG pin needs to keep floating. The PG signal has a rise delay of 100μs and a fall delay of 18μs.

Table 1. PG Output State in Different Conditions

Device Information		PG State	
		Hi-Z	Low
Enable (EN = High)	$V_{FB} \ge 0.576V$	√	
	$V_{FB} \le 0.552V$		√
	$V_{FB} \le 0.63V$	√	
	$V_{FB} \ge 0.66V$		√
Shutdown by EN	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$1.4V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 1.4V$	Uncertain	

DETAILED DESCRIPTION (continued)

Pulse Width Modulation (PWM) Operation

In the condition of continuous conduction mode (CCM), which occurs at medium to heavy load or the force PWM mode, the device works in pulse width modulation (PWM) operation. The switching frequency is slightly affected by VIN, VOUT and load condition. Then a fixed on-time architecture is activated and for SGM61024B, the typical on-time is t_{ON} = 455ns × (V_{OUT}/V_{IN}). For SGM61024A, it automatically exits PWM mode when the inductor current is discontinuous.

Power-Save Mode (PSM) at Light Loads: SGM61024A

Once the load current decreases, the SGM61024A will enter power-save mode. Then, the device has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency. In power-save mode, the inductor current is discontinuous and the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

Minimum Duty Cycle and 100% Duty Cycle

Due to the reduction of the switching frequency for regulation, the device has no minimum duty cycle set. When the input voltage gradually drops to the regulation output voltage, the device can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

- V_{IN_MIN} is the minimum input voltage to maintain output voltage in regulation.
- I_{OUT_MAX} is the maximum output current.
- R_{DSON} is high-side MOSFET on-resistance.
- R_L is inductor DC resistance (DCR).

Switch Current Limits and Short-Circuit Protection (Hiccup)

Limiting the switch current protects the switch itself and also prevents over-current of the source and the inductor. If the high-side (HS) switch current exceeds the ILIM threshold, HS switch is turned off and the low-side (LS) switch is turned on to reduce the inductor current and limit the peak current. If 32 cycles consecutive repetition of this event occur, the device stops switching. A new startup is initiated automatically (hiccup) after 200μs. The hiccup repeats until the overload or short-circuit fault is cleared.

LS switch current limit is also integrated in the device. Each cycle, the HS switch is not allowed to turn on until the LS current is below the low-side FET current limit.

Thermal Protection and Shutdown

Thermal protection is included to protect the die against overheating damage. If the junction temperature exceeds T_{SD} threshold, the switching is stopped and the device is shut down. An automatic recovery with a soft-start begins when the junction cools down for 18℃ below the T_{SD} limit.

APPLICATION INFORMATION

In this section, power supply design with the SGM61024 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

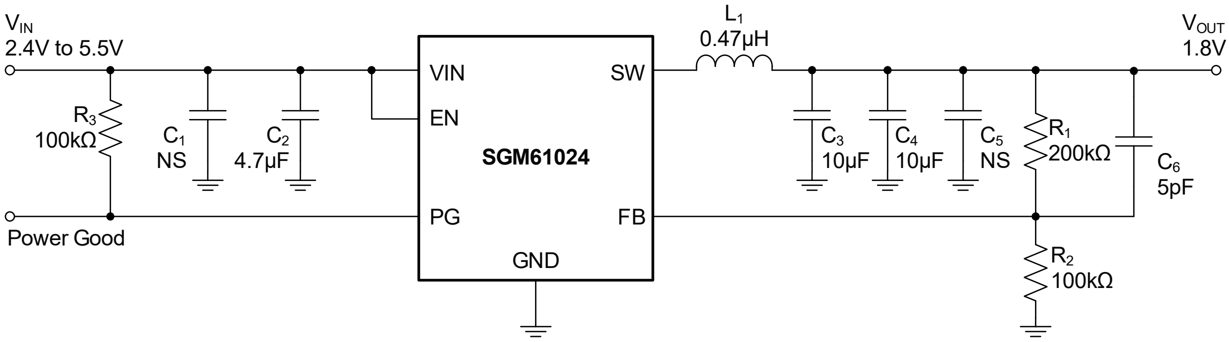


Figure 3. 1.8V Output Voltage Application of SGM61024

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	2.4V to 5.5V
Output Voltage	1.8V
Output Ripple Voltage (CCM)	< 20mV
Maximum Output Current	2A

Table 3. Selected Components for the Design Example

Ref	Description
C_1	Optional
C_2	4.7μF, 10V, X7R, 0603, Ceramic Capacitor
C_3	10μF, 10V, X5R, 0603, Ceramic Capacitor
C_4	10μF, 10V, X5R, 0603, Ceramic Capacitor
C_5	NS
C_6	5pF, 50V, C0G, 0603, Ceramic
L_1	0.47μH, DCR_{TYP} = 6.4mΩ
R_1	200kΩ, 1%, 0603, 1/16W Chip Resistor
R_2	100kΩ, 1%, 0603, 1/16W Chip Resistor
R_3	100kΩ, 1%, 0603, 1/16W Chip Resistor

Input Capacitor Selection

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. The high frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. In most cases, a 4.7μF low ESR multilayer ceramic input capacitor with X5R or better dielectric is recommended, a larger value reduces input voltage ripple and improves system. If the input cable or PCB copper is too long, it is suggested to add another input capacitor as C_1 in the schematic diagram and place it as indicated by the recommended layout later.

Inductor Selection

The inductor current ripple is determined by the inductance value (L). A lower inductance results in higher peak-to-peak current that increases the converter conduction losses. On the other hand, a large inductance results in slower transient response and larger size. I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Generally, the saturation current above high-side current limit is enough. The inductor initial tolerance can be as high as -20% to +20% of the nominal value and proper current derating is usually required.

Equation 2 can be used to choose the inductance value based on ΔI_L.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (2)$$

where:
- I_{OUT_MAX} is the maximum output DC current.
- ΔI_L is the inductor current ripple (peak-to-peak).
- f_{SW} is switching frequency (MHz).
- L is the inductance value (μH).

APPLICATION INFORMATION (continued)

Output Voltage Adjustment

Use Equation 3 for selecting the feedback resistors (R_1 and R_2) in Figure 3 to set the desired output voltage. First choose R_2 value below 100kΩ to avoid high noise sensitivity on the FB pin. Do not choose a very small value for R_2 otherwise the loss will be increased on this resistor that reduces the light load efficiency.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R_2 \times \left(\frac{V_{OUT}}{0.6V} - 1\right) \quad (3)$$

A feed-forward capacitor improves transient response to the load steps and reduces the output ripple in PSM.

Output Capacitor Selection

For output capacitor design, output ripple, transient response and loop stability should be considered. Choosing ceramic capacitor with X5R or better dielectric is very important for temperature characteristics. Bias voltage can cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value. For this example, the output capacitance is recommended to use 2 × 10μF.

Thermal Considerations

Especial care must be taken for power dissipation and thermal relief in high power density designs. The SGM61024 is a low-profile and fine-pitch surface-mount package that is typically used in a small area or volume. Thermal coupling, airflow and heat sinking must be considered in the system level and the space between heat generating elements must be managed properly.

To enhance the thermal performance, the PCB itself has a significant role and to help transfer the heat away by using large copper traces/planes that are connected to the device pins (and thermal pads if present). Considering a proper airflow in the system can complete the thermal relief for reliable operation of the power supply.

LAYOUT GUIDELINES

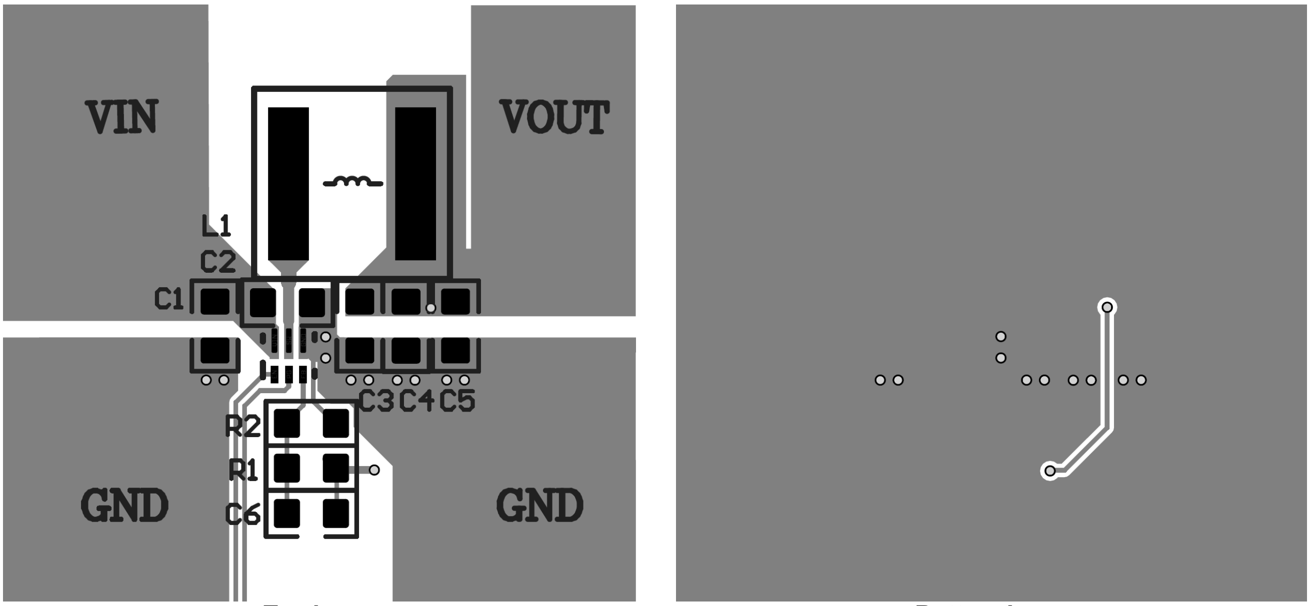
A critical component of a high frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the device.

• Place the input/output capacitors and the inductor as close as possible to the IC pins and keep the power traces short. Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.

• Connect the ground returns of the input and output capacitors close to the GND pin and at the same point to avoid a ground potential shift and to minimize high frequency current path.

• Keep the output voltage sense trace and FB pin connections away from the high frequency and noisy conductors such as power traces and SW node to avoid magnetic and electric noise coupling.

• Use GND planes in mid-layers for shielding and minimizing the ground potential drifts.



Top Layer **Bottom Layer**

Figure 4. PCB Layout

ADDITIONAL TYPICAL APPLICATION CIRCUITS

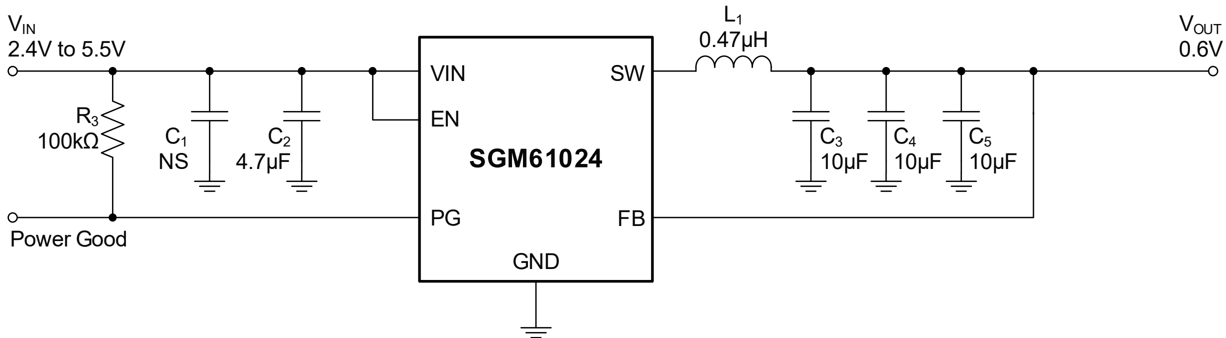


Figure 5. 0.6V Output Voltage Application of SGM61024

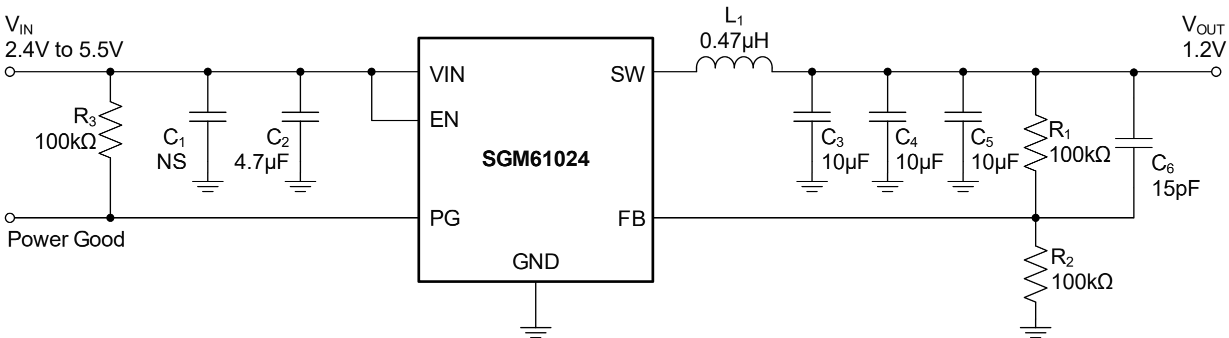


Figure 6. 1.2V Output Voltage Application of SGM61024

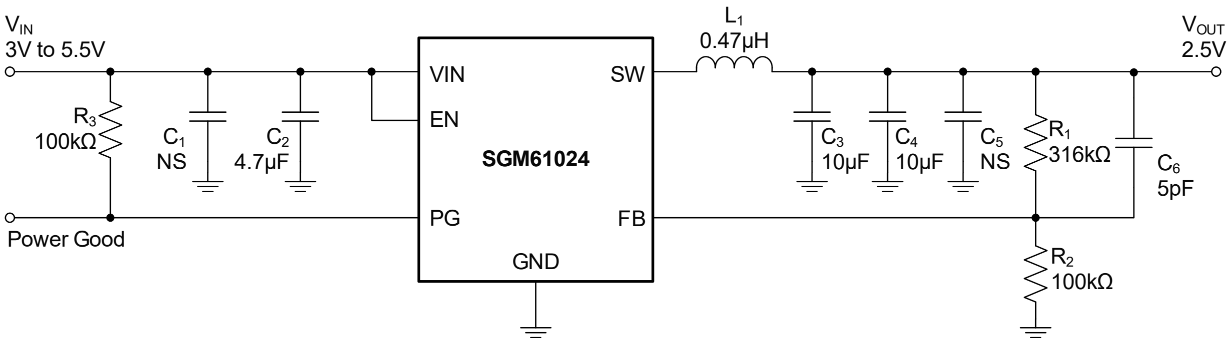


Figure 7. 2.5V Output Voltage Application of SGM61024

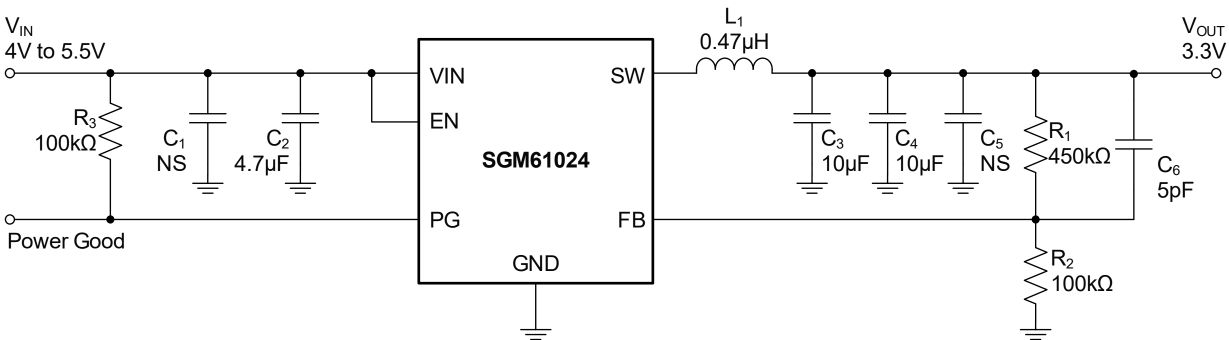


Figure 8. 3.3V Output Voltage Application of SGM61024

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

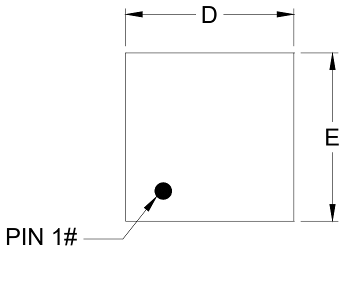
MAY 2024 – REV.A.1 to REV.A.2	Page
Added system characteristics	5

APRIL 2024 – REV.A to REV.A.1	Page
Updated typical performance characteristics	5, 6, 7, 8, 9

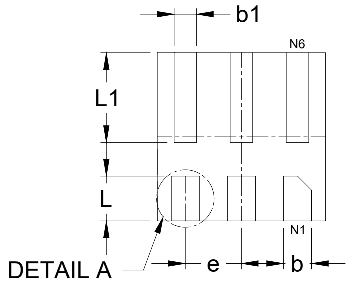
Changes from Original (MARCH 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

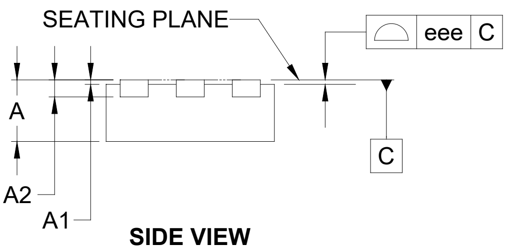
UTDFN-1.5×1.5-6L



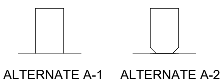
TOP VIEW



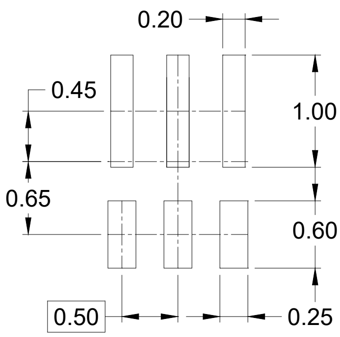
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



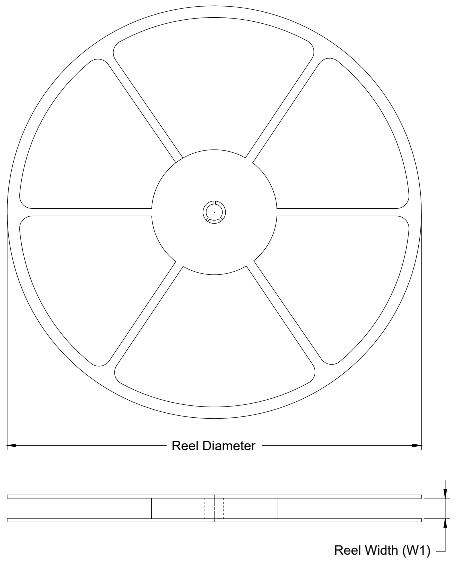
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	**MOD**	**MAX**
A	0.500	-	0.600
A1	0.000	-	0.050
A2	0.152 REF		
b	0.200	-	0.300
b1	0.150	-	0.250
D	1.400	-	1.600
E	1.400	-	1.600
e	0.500 BSC		
L	0.300	-	0.500
L1	0.700	-	0.900
eee	0.080		

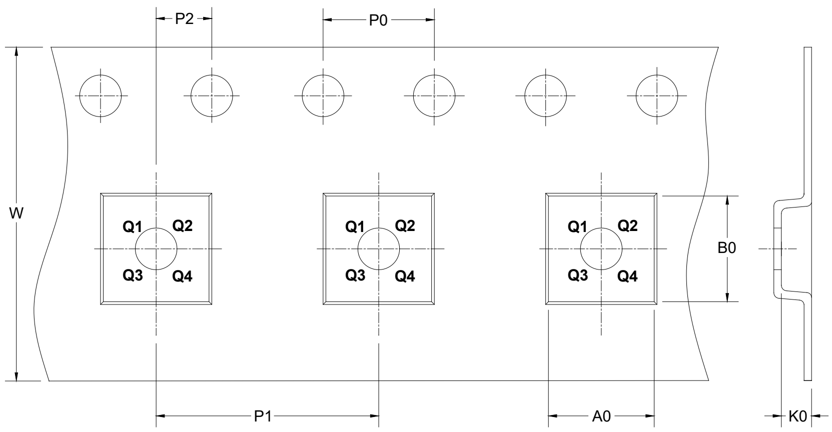
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

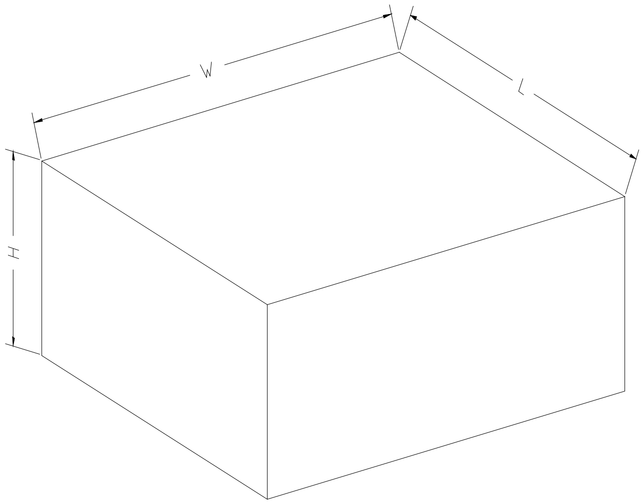
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.5×1.5-6L	7"	9.5	1.70	1.70	0.75	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002